DESIGN AND SIMULATION OF CMOS-BASED BANDGAP REFERENCE VOLTAGE WITH COMPENSATION CIRCUIT USING 0.18 µm PROCESS TECHNOLOGY

By

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TABLE OF CONTENTS

Acknowledgement ii
Table of Contents iii
List of Tables v
List of Figures and Illustrations vi
List of Abbreviations and Nomenclature viii
Abstrak ix
Abstract x

CHAPTER 1 1
1.0 Introduction 1
1.1 Problem Statement 2
1.2 Research Objective 3
1.3 Scope of Limitation 4
1.4 Thesis Structure 4

CHAPTER 2 6
LITERATURE REVIEW 6
2.0 Introduction 6
2.1 Review of Operational Amplifier 7
2.2 Review of Bandgap Reference Circuits 8
2.2.1 Principle Operation of Bandgap Reference Circuit 8
2.2.2 Current Trend in Topology of Bandgap Reference Circuitry 12
2.2.3 Summary of Characteritics of Different Design of BGR Circuits 29
2.3 Summary 31

CHAPTER 3 32
METHODOLOGY 32
3.0 Introduction 32
3.1 Overall Design Flow 32
3.2 Proposed Bandgap Voltage Reference Circuitry Topology 35
3.3 Layout Design 48
3.4 Experimental Setup 50
3.5 Experimental Parameters 51
3.6 Summary 52

CHAPTER 4 53
RESULTS AND DISCUSSION 53
4.0 Introduction 53
4.1 Pre Layout Simulation 53
4.1.1 Simulation Result of Vref Versus Temperature 55
4.1.2 Simulation Result of Vref Versus VDD 56
4.1.3 PSRR Simulation Result 58
4.1.4 Multi Supply Voltage Versus Temperature Simulation Result 59
4.1.5 Monte Carlo Analysis 61
4.1.6 Simulation Result of Different Process Corner 63
4.2 Post Layout Simulation 66
4.4 Performance Comparison 68
4.5 Summary 70

CHAPTER 5 71
CONCLUSION AND RECOMENDATIONS 71
5.1 Conclusions 71
5.2 Future Works 72

REFERENCES 73

LIST OF TABLES

Table 2-1 Summary of Characteristics of Different Design of BGR Circuits 30

Table 3-1 Final Component Dimension of Schematic 47

Table 3-2 Final Component Dimension of Layout.....48

Table 4-1 Performance of Proposed BGR Circuit at Different Voltage Supply 60

Table 4-2 Voltage Variation and TC at 1.8V for All Corners.....65

Table 4-3 Performance Comparison.....69

LIST OF FIGURES

Figure 2-1 Classical Two-Stage Op-Amp[19] 7

Figure 2-2 CTAT Graph (Voltage versus temperature)[18] 9

Figure 2-3 PTAT Graph (Voltage versus temperature)[18] 9

Figure 2-4 Combination of PTAT And CTAT Graph 10

Figure 2-5 Classis Structure of BGR Circuit [23] 10

Figure 2-6 First Order BGR Circuit With Proposed Curvature Compensation [23] 13

Figure 2-7 BGR Circuit with Temperature Dependent Resistor [22] 15

Figure 2-8 Operation of BGR Circuit With Piecewise Nonlinear Curvature-Corrected Circuit [25] 17

Figure 2-9 BGR Circuit With Piecewise Nonlinear Curvature-Corrected Circuit [25] 17

Figure 2-10 BGR Circuit with enhancement piecewise nonlinear curvature-corrected circuit [25] 19

Figure 2-11 Current Flow Through M9 and Nonlinear Curvature-Corrected Current [25] 20

Figure 2-12 Proposed MOSFET Based Bandgap Circuit [10] 21

Figure 2-13 core of the proposed subthreshold MOSFET reference circuit [11] 23

Figure 2-14 Schematic of Bandgap Circuit [27] 25

Figure 2-15 Schematic of Proposed Piecewise-Curvature Corrected Bandgap Reference Circuit [11] 27

Figure 2-16 Schematic of Proposed Piecewise-Curvature Circuit [13] 28

Figure 3-1 Design Flow for Schematic 33

Figure 3-2 Design Flow for Layour 34

Figure 3-3 Schematic of Proposed BGR Circuit With Compensation Circuit 35

Figure 3-4 Schematic of Op Amp Circuit In The Proposed BGR Circuitry 36

Figure 3-5 Proposed Method of TC Reduction 37

Figure 3-6 Operation of Compensation Circuit A 38

Figure 3-7 Graph of Vref versus Temperature by Proposed Circuit [11] 39

Figure 3-8 Graph of Vref Versus Temperature 40

Figure 3-9 Operation of Circuit B 41

Figure 3-10 Graph of Vctat And Vptat Versus Temperature 42

Figure 3-11 Schematic of Compensation Circuit C 43

Figure 3-12 Operation of Compensation Circuit C 44

Figure 3-13 Graph of Iptat Versus Temperature 45

Figure 3-14 Graph of Icc Versus Temperature 45

Figure 3-15 Overall Operation of Compensation Circuits 46

Figure 3-16 Testbench of The Proposed BGR Circuit 50

Figure 4-1 Schematic of The Proposed BGR Circuit 54

Figure 4-2 Schematic of The Op-Amp Circuit 54

Figure 4-3 Graph of Vref versus Temperature 55

Figure 4-4 Measure Supply Voltage Dependency of Proposed BGR Circuit at -25, 27, 100, 150°C 57

Figure 4-5 Measured Voltage Supply Dependency at 27°C 58

Figure 4-6 Measured PSSR of the Proposed BGR 59

Figure 4-7 Simulated Temperature Behavior of Vref at Different Supply Voltage 60

Figure 4-8 Distribution of Output Reference Voltage Obtained From Monte Carlo Simulations of 1000 Runs With Supply Voltage of 1.8V at 27°C 61

Figure 4-9 Distribution of Output Reference Voltage Obtained From Monte Carlo Simulations of 1000 Runs With Supply Voltage of 3.3 V at 27°C 62

Figure 4-10 Graph of Vref Versus Temperature of Different Process Corner 64

Figure 4-11 Graph of Vref Versus Supply Voltage of Different Process Corner at 27°C 65

Figure 4-12 Layout Design of The Proposed Circuit 66

Figure 4-13 LVS Result 67

Figure 4-14 DRC Result 67

Figure 4-15 Graph of Vref Versus Temperature of Post Layout Simulation 68

LIST OF ABBREVIATIONS

Abbreviation	Meaning
IOT	Internet Of Things
BGR	Bandgap Reference
CMOS	Complementary Metal-Oxide-Semiconductor
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Op-amp	Operational Amplifier
CTAT	Complementary Proportional to Absolute Temperature
PTAT	Proportional to Absolute Temperature
PSSR	Power Supply Rejection Ratio
TC	Temperature Coefficient

REKA BENTUK DAN SIMULASI LITAR BANDGAP VOLTAN RUJUKAN DENGAN LITAR PEMBAIKAN BERASASKAN TEKNOLOGI PROSES CMOS 0.18 µm

ABSTRAK

Litar voltan rujukan merupakan komponen yang penting dalam dunia elecktronik pada masa kini. Litar bandgap voltan rujukan (BGR) berasaskan CMOS lebih popular kerana saiznya lebih kecil dan kuasa digunakan lebih rendah. Tetapi, variasi voltannya adalah besar dalam julat suhu yang lebar dan menyebabkan pekali suhu tinggi. Jadi, pembetulan kelengkungan sesecebis telah direka dan diubahsuai untuk mengatasi masalah disebutkan di atas. Litar BGR direka dengan menggunakan proses yang serasi dengan CMOS 0.18µm teknologi proses dan disimulasi dengan mengunakan Cadence. Litar BGR dicadangkan dalam projek ini mampu beroperasi baik dengan voltan rujukan daripada 558.6mV ke 558.3mV dengan mengubahkan voltan bekalan 1.4 V ke 3.3 V dalam suhu 27°C dan ia mempamerkan pengaturan talian sebanyak 0.016%. Selain itu, pekali suhu yang terbaik ialah 9.2 ppm/°C dalam julat suhu -25°C sampai 150°C pada 1.8 V bekal voltan. PSSR bagi litar yang dicadang adalah -69.91 dB dalam kekerapan yang kurang daripada 10 kHz. Selain itu, reka bentuk bentangan bagi litar yang dicadang telah dilaksanakan dengan mengunakan Silterra 0.18 µm process CMOS yang biasa dan luas bentangan adalah hanya 0.0175 mm^2 dan pekali suhu yang diperolehi dalam simulasi reka bentuk bentangan ialah 11.66ppm/°C. Kesimpulan, keputusan simulasi menunjukan litar yang dicadangkan boleh beroperasi dalam julat suhu yang lebar dengan variasi voltan yang rendah secara bandingan.

DESIGN AND SIMULATION CMOS-BASED BANDGAP REFERENCE VOLTAGE CIRCUITRY WITH COMPENSATION CIRCUIT USING 0.18 µm PROCESS TECHNOLODY

ABSTRACT

Voltage reference circuit is important in electronic world nowadays. A CMOS based bandgap reference (BGR) circuit is preferred due to its size is smaller and consume less power. However, the drawback is the reference voltage variation of CMOS based BGR circuit is big in wide range of temperature, thus the temperature coefficient of it is high. Hence, an improved version of piecewise curvature-corrected Bandgap voltage reference circuit which has low voltage variation in wide range of temperature is introduced in this project to overcome the problem mentioned above. The BGR circuit is designed using CMOS compatible process in 0.18µm CMOS process technology and simulated by using Cadence tool. The proposed piecewise curvature-corrected BGR operate properly with output voltage of 558.6 mV to 558.3 mV by varying the voltage supply 1.4 V to 3.3 V at 27°C and the line regulation is 0.016% . Besides that, the best temperature coefficient obtained is 9.2 ppm/°C in the temperature range of -25°C to 150°C at 1.8 V. The PSSR of the proposed circuit is -69.91 dB at frequency less 10 kHz. The layout design of the proposed circuit is done by using Silterra 0.18 µm standard CMOS process and total die area is 0.0175 mm^2 and temperature coefficient obtained in post layout simulation is 11.66ppm/°C. In short, it is found that the proposed design of BGR circuit is able to achieve high temperature range and relatively low voltage variation.

CHAPTER 1

INTRODUCTION

1.0 Introduction

A reliable constant voltage reference is important in electronic world. It is an essential component for many applications ranging from purely analog, mixed-signal to purely digital circuit system. Power converters, flash memory controllers and A/D converters are some of the example that need a good voltage reference [1].

Voltage reference is used to provide biasing voltage and at the same time compensate variation of output caused by the change of voltage, process and temperature [2]. Nowadays, as the emerging of IOT device in the market, requirement for a constant voltage reference is even higher. Low power, less area consumption and high accuracy of a voltage reference design is essential for design of robust IOT application [2, 3].

In some of the application like electronic circuit system in oil and gas industry, a voltage reference is needed to provide a stable biasing voltage to the electronic system [4] under the extreme high temperature in the harsh environment of oil and gas industry. In this circumstances, bandgap reference circuit is needed because it able to provide a stable voltage with small voltage variation if the temperature

changed. On top of that, bandgap reference circuit (BGR) is one of the circuit topology that can generate a temperature independent voltage reference.

The research carried out in this thesis is to design a bandgap reference circuit that can provide a stable voltage with small voltage variation that independent in a wide range of temperature.

1.1 Problem Statement

Nowadays, bandgap voltage reference (BGR) circuitry topology is one of the core element in power supply management circuitry especially for portable electronic device and Internet of things (IOT) based sensor. As moving forward to IOT electronic, low power and capable operating in wide temperature range are demand as robustness and reliability issue.

Conventionally, parasitic vertical bipolar junction transistors (BJTs) have been used in bandgap reference circuit in current CMOS technology [5]. The base-emitter voltage or the pn junction of the bipolar transistor is characterized and act as the basic of voltage reference generation [6]. This type of BGR output voltage is about 1.2 V hence it cannot work with a sub 1 V supply voltage that modern deep-submicron technology prefer to [7].

Therefore, MOS transistor based voltage reference is alternative topology especially in IOT devices. This topology capable work in low voltage and consume less power [8] and its size is much more smaller [9] compared to BJT based BGR voltage

reference. It utilize the subthreshold MOSFET's temperature characteristics to achieve temperature compensation [10]. In order word, it use V_{TH} of the MOSFET transistor as the basic of reference generation [8] . However, the drawback of this type of Bandgap reference voltage is variation of the threshold voltage (V_{TH}) is big and degrading the performance [11]. In this instances, MOS based BGR [12] is having a high temperature coefficient (> 100ppm/℃) in wide temperature (-10℃ to 100℃) due to the characteristics of the MOS transistor.

To solve this problem, MOS based BGR proposed by [13] is adopting a compensation circuit to reduce the voltage variation of [12] . However, the temperature coefficient is still high (127.26 ppm/℃) if operate in wide range of temperature such as form -25℃ to 150℃. This is because the CTAT characteristics of MOS transistor is become weaker and become less impactful at high temperature. In consequence, PTAT element of the MOS based BGR become dominant and causing the reference voltage increased a lot in high temperature. In short, the characteristics of the MOS transistor change at high temperature causing the PTAT voltage become dominant and the temperature coefficient is high in wide range of temperature.

To conclude, an improved version of compensation circuit is needed to enhance the MOS transistor based band gap reference circuit performance in a wide range of temperature.

1.2 Research Objectives

The main objectives of this research are:

- To design and simulate a CMOS transistor based bandgap reference circuit that can operate in temperature range of -25℃ to 150℃.
- To integrate with compensation circuitry topology to achieve temperature coefficient that is less than 20 ppm/℃.

1.3 Scope of Limitation

The objective of this research is to study and design a CMOS based BGR circuit which having low voltage variation. The scope of study is confined as below:

I. Only Complementary Metal Oxide Semiconductor (CMOS) compatible process is used in the designed circuit.
II. Supply voltage VDD is 1.8V

1.4 Thesis Structure

This thesis consists of five chapters. Chapter 1 is including the simple introduction of the dissertation, follow by background of the research and problem statement. Then, research objective and scope of study and thesis structure is described in chapter 1 as well.

Next, Chapter 2 will discuss about the basic principle operation of BGR circuit, compensation technique used by BGR circuit to improved performance and type of existing BGR circuit.

Chapter 3 is about the method or technique used to design the proposed BGR circuit starting from designing phase until the simulation setup is explained in this chapter.

Chapter 4 presents the simulation data, analysis, observation and detail of the simulated data.

Chapter 5 is the final chapter and it summarized the finding of the research and area of improvement in the future.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

There are different types of constant voltage reference other than BGR circuit such as Zener diode circuitry. Zener diode based voltage reference having a better accuracy compared to BGR. However the drawback of this voltage reference is the minimum power supply required for it to operate is 6V or above. Hence, Zener based voltage reference is not popular compared to BGR especially power consumption is critical in today technology [14]. Furthermore, Zener diode based voltage reference require tight process control to maintain a given tolerance and it is relatively noisy [15].

Bandgap reference was first proposed by Wilder in 1971 [15] and it has been popular since there until now. It used Conventional junction isolated bipolar-integrated circuit technology to produce a stable voltage reference which is around 1.220V [16]. On top of that, pn junction of the bipolar transistor is used in BGR as basic of reference voltage generation.

There are a lot of work has been done to enhance the performance of BGR circuit over the years such as quadratic temperature, exponential temperature compensation, piecewise-nonlinear curvature correction and etc. Different goal like reduce the

voltage variation, improve the temperature coefficient and increasing the temperature range of the BGR circuit are intended to be achieved by using the technique above. In this chapter, basic operation of the BGR circuit is explained and different types of BGR circuits are reviewed.

2.1 Review of Operational Amplifier

Operational amplifier also known as Op-amp. It is a components that widely used in a vast array of consumer, industrial, and scientific devices [17]. Meanwhile, it is also widely used as a building block in BGR circuit. On top of that, the advantages of using Op-amp is forcing the same current to CTAT and PTAT reference so that the VDD of the circuit can move lower before it affects the output voltage reference of the BGR circuit [18].

Figure 2-1 below shows the classical two-stage op-amp with compensation capacitors which commonly used nowadays [19].

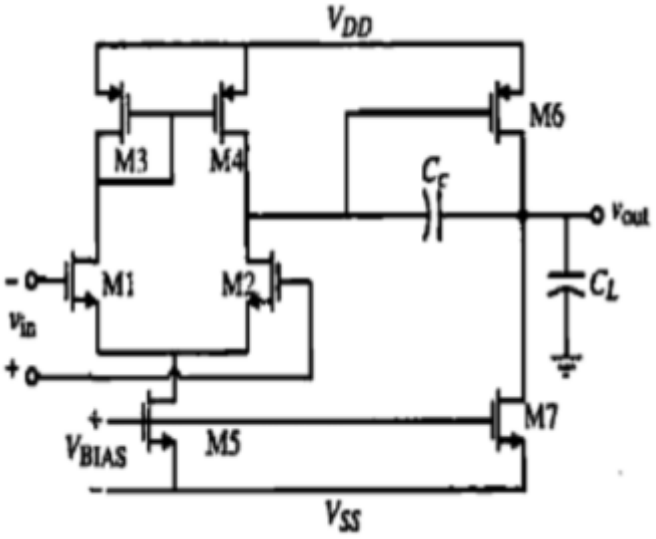

Figure 2-1 Classical Two-stage Op-Amp [19]

The whole amplifier is biased by transistor M5 and transistor M3 and M4 forms a current mirror. Meanwhile, transistor M1 and M2 is the differential pair of the input to the amplifier. On top of that, M5 and M7 supply the differential pair with bias current. Apart from that, transistor M6 loaded with transistor M7 form the 2nd stage of the amplifier [19]. The total gain of the amplifier is summation gain of first and second stage of amplifier. In addition, gain frequency characteristics with dominant pole is achieved by adding in the compensation capacitor C_C [20].

2.2 Review of Bandgap Reference Circuits

Basic Operation of Bandgap reference circuit is described in the session below. Besides that, previous of works to improve the performance the Bandgap reference circuit are discussed and tabulated in the session below.

2.2.1 Principle Operation of Bandgap Reference Circuit

BGR provide a reference voltage without affected by the temperature. Temperature independence can be achieved by combining two phenomena that have opposite temperature coefficients [21]. Thus, reference voltage of BGR is a summation of negative TC (temperature coefficient) voltage and positive TC [22]. In order word, BGR consists of CTAT and PTAT circuit that can compensate each other to give a constant voltage ideally regardless how the temperature changed.

On top of that, CTAT is known as complementary to absolute temperature. Figure 2-2 below shows how CTAT graph where voltage is inversely proportional to temperature.

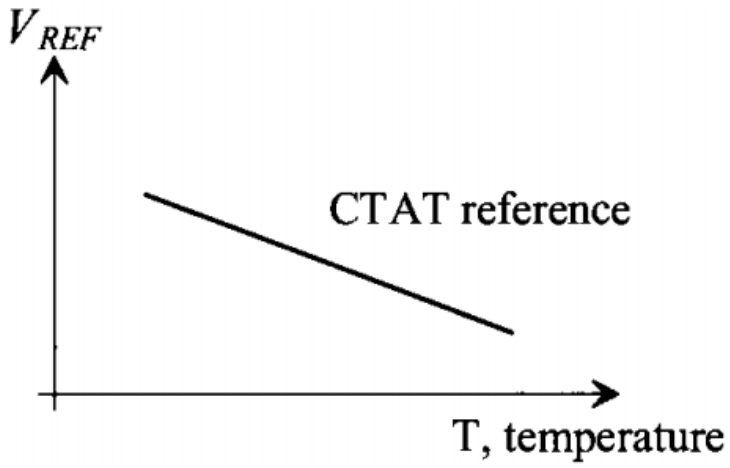

Figure 2-2 CTAT Graph (Voltage Versus Temperature) [18]

Meanwhile, PTAT is known as proportional to absolute temperature. Figure 2-3 below show PTAT graph is where voltage is directly proportional to temperature.

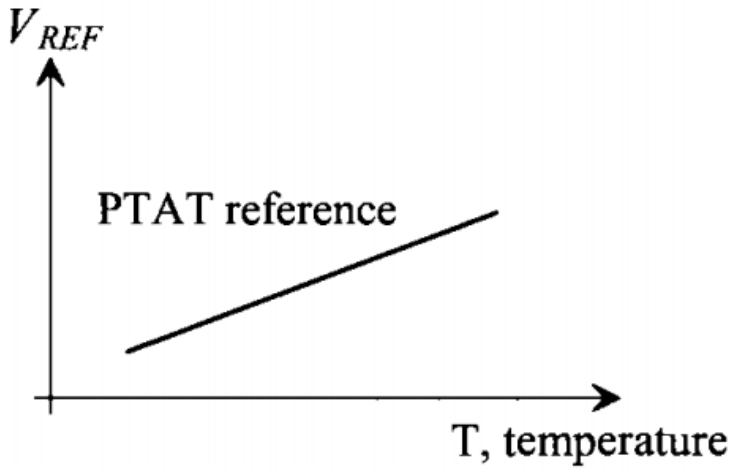

Figure 2-3 PTAT Graph (Voltage Versus Temperature)[18]

In short, summation of PTAT and CTAT voltage will get a constant voltage across a range of temperature as shown in Figure 2-4[18].

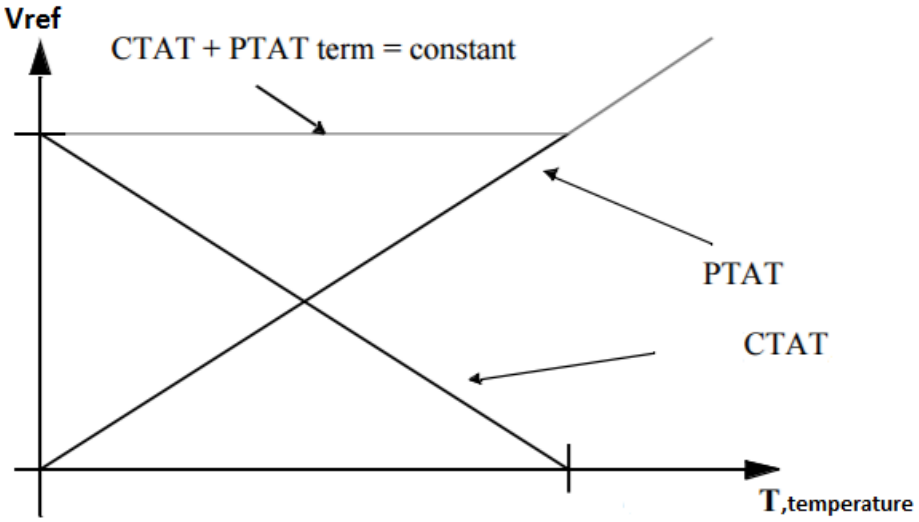

Figure 2-4 Combination of PTAT and CTAT Graph

Next, the classic design of bandgap is shown in the figure 2.5 below. It consists of one amplifier, three resistors and two BJT transistors.

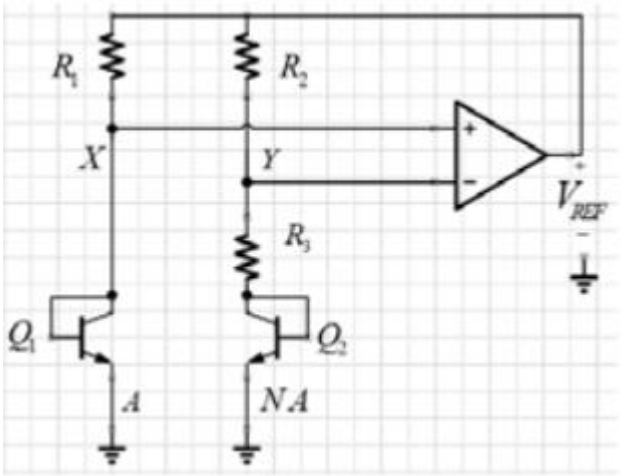

Figure 2-5 Classis Structure of BGR Circuit [23]

Based on the Figure 2-5, PTAT element of the BGR circuit is made up by Q_3 and R_3 while CTAT element is made up by Q_1 transistor. In addition, and the output voltage of the BGR circuit is as below

$$Vref = V_{BE2} + \Delta(R_3 + R_2) = V_{BE2} + \Delta V_{BE}\left(1 + \frac{R_2}{R_3}\right) \quad (2.1)$$

While V_{BE} is represented by the equation below. V_{BE} is a complex function of T which has a higher order such as Tln T and it is a nonlinear. In addition, it has negative TC of about =1.8mV/°C and it is CTAT element in BGR circuit.

$$V_{BE}(T) = V_{g0}(T_0) + \left(\frac{T}{T_0}\right) \times \left[V_{BE}(T_0) - V_{g0}(T_0)\right] - (n - m)\left(\frac{kT}{q}\right)\ln(\frac{T}{T_0}) \quad (2.2)$$

V_g - The bandgap voltage of silicon at 0 K

K – Boltzman's constant

n – Temperature constant depend on technology

m – Order of the temperature dependence of the collector current

q – Charge of an electron

T_0 – Reference of temperature

Apart from that, PTAT element is the difference between two BJT base emitter when both BJT work at different current density [23]. Hence

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln n \quad (2.3)$$

Thermal voltage $V_T(\frac{kT}{q})$ is a directly proportional to the absolute temperature (PTAT) and it is linear function of T [23].

By differentiation of equation 2. 3 , $\frac{\partial V_{BE}}{\partial T} = \frac{k}{q}\ln n$ where it will exhibits a positive TC. As shown in equation of BGR voltage, ΔV_{BE} is multiply by $\left(1 + \frac{R_2}{R_3}\right)$ in order to large positive TC and help to get a nominally zero TC of the BGR.

However, only the 1st order of T term is being canceled out in the classic Bandgap design. This is because ΔV_{BE} is linear function of T and it only cancel out the first order of nonlinear function of ΔV_{BE} .

The BGR voltage is as below if the best case of 1st order function of T is totally cancel out.

$$V_{ref} = V_{g0} - (n - m)\frac{kT}{q}\ln\frac{T}{T_0} \quad (2.4)$$

Vref will decrease with temperature and it is hard to improve the temperature stability in large scale [24] and this is the common problem faced by the traditional BGR circuit.

The next section will describe different type of BGR circuit that can overcome the weakness of the conventional BGR circuit.

2.2.2 Current Trend In Topology of Bandgap Reference Circuitry

The paper "A 3.2 ppm/°C Curvature-Compensated Bandgap Reference with Wide Supply Voltage Range" described how higher order curvature compensation can done by using exponential curvature compensation (ECC) and translinear loop circuit

(TLC). Function of ECC is to reduce the temperature to some degree first and follow by TLC which used to further lower down the temperature drift at higher temperature [23].

The proposed circuit in this paper is shown in Figure 2-6 below. It consists of conventional first order bandgap core circuit and curvature compensation circuit.

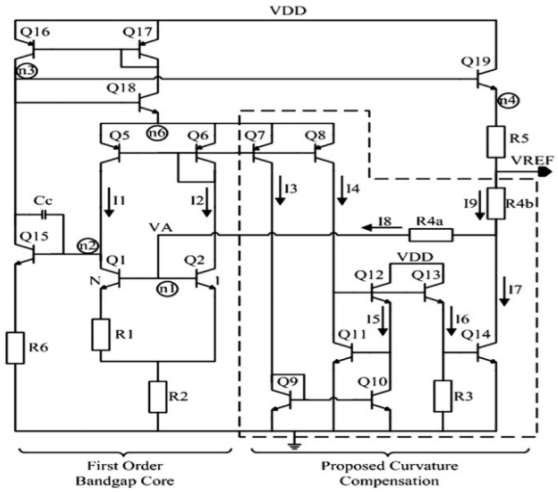

Figure 2-6 First Order BGR Circuit with Proposed Curvature Compensation [23]

The first order temperature compensated voltage is at node 1 and can be expressed in

$$V_A = V_{BE2} + 2R_2V_T \ln {}^{N}/_{R} \quad (2.5)$$

and current I1 and I2 can expressed as

$$V_T \ln N/R_1 \quad (2.6)$$

N is the emitter-area ratio of Q1 and Q2.

Meanwhile, I_8 the compensation current from the proposed compensation circuit can be represented as $I_8 = 2V_T \ln N/[R_1\beta(T)]$ where $\beta(T)$ is the common emitter current gain.

Apart from that, TLC is formed by transistor Q11, Q12, Q13, Q14 and resistor R3. In addition, I_7 is generated by TLC circuit as compensation current besides I_8.
By the help form compensation circuit proposed by this paper, the output reference voltage can be represented as

$$V_{REF} = V_{BE2} + 2\frac{R_2}{R_1}V_T \ln N + 2\frac{(R_{4a}+R_{4b})\ln N}{R_1}\frac{V_T}{\beta(T)} + E\frac{R_3R_{4b}}{{R_1}^2}\frac{T^2}{V_{BE14}} \qquad (2.7)$$

From the simulations results, the BGR circuit is having a line regulation of less than 0.088mV/V when the supply voltage changed from 3.5V to 30V in the range of temperature range of -55^0C to 125^0C. Besides that, the minimum temperature coefficient is 3.2 ppm/^{o}C and the maximum temperature coefficient is 5.4 ppm/^{o}C.

Next, Paper "A Bandgap Reference Circuit with 2nd Order Curvature Correction" published by Wei Kui and Jianyang Zhou in 2012 proposed a 2nd order compensated band gap reference (BGR) circuit based on a temperature dependent resistor ratio [22].

The proposed BGR with the compensation circuit is shown as Figure 2-7 below.

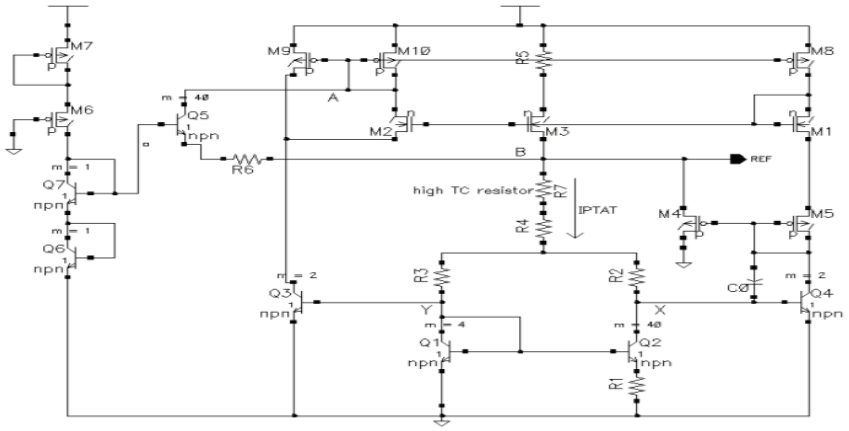

Figure 2.7 BGR Circuit With Temperature Dependent Resistor [22]

Based on the figure above, VBE is obtained from the base of Q1 and Q2. On top of that, emitter area ratio between Q1 and Q2 is 10. Hence, PTAT current is produced and flowing through R2, R3 (R2=R3), R4 and R7. In addition, R2, R3 and R4 are thin film resistor and nearly temperature independent. Meanwhile, R7 is a well diffuse resistor and having a high TC up to 6500ppm/^{0}C. In short, Vref can be represented by the equation below:

$$V_{ref} = V_{BE1} + \frac{V_T \ln 10}{R_1}[2(R_4 + R_7) + R_3] \qquad (2.8)$$

On Top of that, R7 is a temperature dependent resistor and its resistance is expressed as

$$R_7 = [1 + \alpha.(T - T_0)].R_0 \qquad (2.9)$$

α – 1st order of TC of R7

T0 – 25^{0}C

R0 – value of R7 at 25^{0}C.

The polynomial expansion of $V_{BE}(Tln\,T)$ is approximately with T2 term. Therefore, this paper proposed to use a temperature dependent PTAT resistor R7 to get a T2 term of PTAT element by multiply it to existing PTAT element VT. Hence, cancelation of T2 term of $Tln\,T$ in V_{BE} can be achieved and V_{ref} can be represented as

$$V_{ref} = \frac{V_T \ln 10}{R_1}[2(R_4 + R_7) + R_3] \quad (2.10)$$

Based on the simulation result, the effective temperature coefficient obtained is about 7.14 ppm/^{o}C in the range of temperature -50^{0}C to130^{o}C with V_{DD} = 5V. Besides that, the disadvantages is that the cost of high resistive poly resistor used in compensation is high [22].

Apart from that, Piecewise curvature-corrected CMOS is one of the technique to improve the performance of the band gap reference circuit by compensating the nonlinear voltage of conventional first order bandgap reference circuit. On top of that, BGR circuit using this technique proposed in paper "An Improvement of a Piecewise Curvature-Corrected CMOS Bandgap Reference" [25] managed to compensate the nonlinear voltage. In this paper, PNCCC generator is used in [25] to compensate the nonlinear term of first order BGR in the higher temperature. Figure 2-8 below illustrated the operation proposed circuit by [25] and the proposed circuit is shown in Figure 2-9 below.

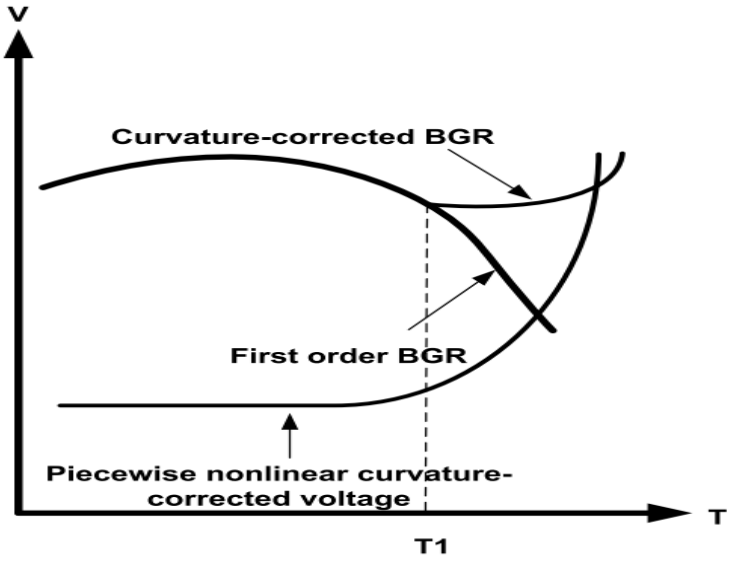

Figure 2-8 Operation of BGR Circuit with Piecewise Nonlinear Curvature-Corrected Circuit [25]

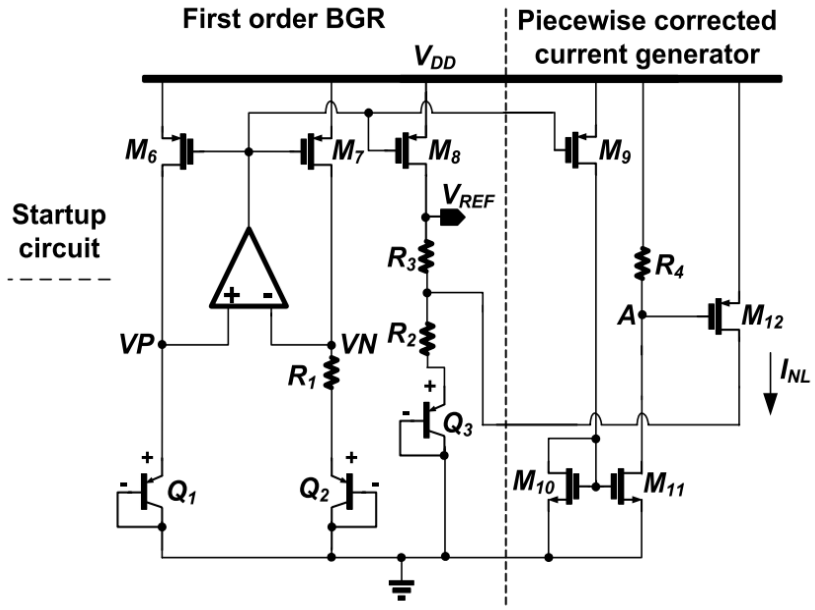

Figure 2-9 BGR Circuit with Piecewise Nonlinear Curvature-Corrected Circuit [25]

Based on figure 2-8, the nonlinear voltage in the first order BGR circuit is being compensated significantly by Piecewise nonlinear curvature-corrected voltage when the temperature is higher than T_1.

Meanwhile, based on figure, PTAT current will flow through resistor R4 thereby PTAT V_{GM12} voltage is produced. V_{GM12} voltage can be represented by

$$V_{GM12} = R_4 I_{PTAT} \quad (2.11)$$

And

$$I_{PTAT} = \frac{V_T \ln n}{R_1} \quad (2.12)$$

In short, V_{GM12} will varied by temperature and thus control the operation of transistor M12 as well as I_{NL}, the nonlinear drain source current of M12. To conclude, I_{NL} current help to increase the BGR voltage at higher temperature based on the reference voltage equation.

$$V_{REF} = V_{EBQ3} + \frac{V_T \ln n(R_2+R_3)}{R_1} + I_{NL}R_2 \quad (2.13)$$

The proposed circuit able to compensate the nonlinear voltage by using the method above. However, the drawback of the proposed PNCCC generator of the circuit is power consumption at low temperature even the circuit remains inactive.

Hence, an improvement of piecewise curvature-corrected CMOS bandgap reference (BGR) circuit, current control circuit (CCC) is proposed in this paper [25] as well. Figure 2-10 illustrated the proposed circuit.

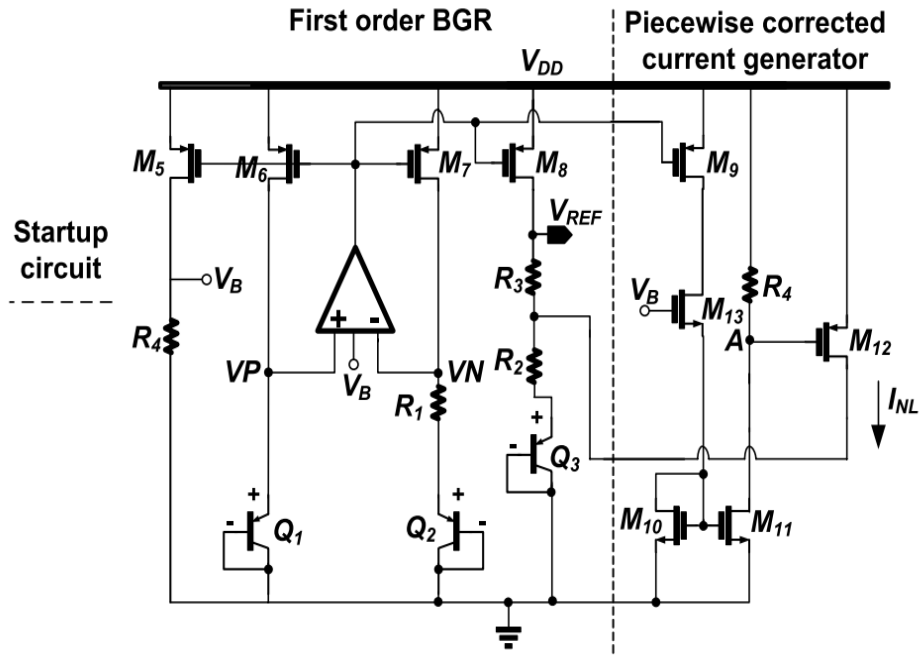

Figure 2-10 BGR Circuit with Enhancement Piecewise Nonlinear Curvature-Corrected Circuit [25]

The only difference between figure 2-8 and figure 2-9 is the additional M13 transistor. M13 is bias by PTAT voltage VB and can be expressed

$$V_B = \frac{V_T \ln nR_4}{R_1} \qquad (2.14)$$

In addition, the current flowing through M9 is now control by M13 unlike the proposed circuit. This help to reduce the power consumption as illustrated by Figure 2-11 below compared with the circuit proposed by [26].

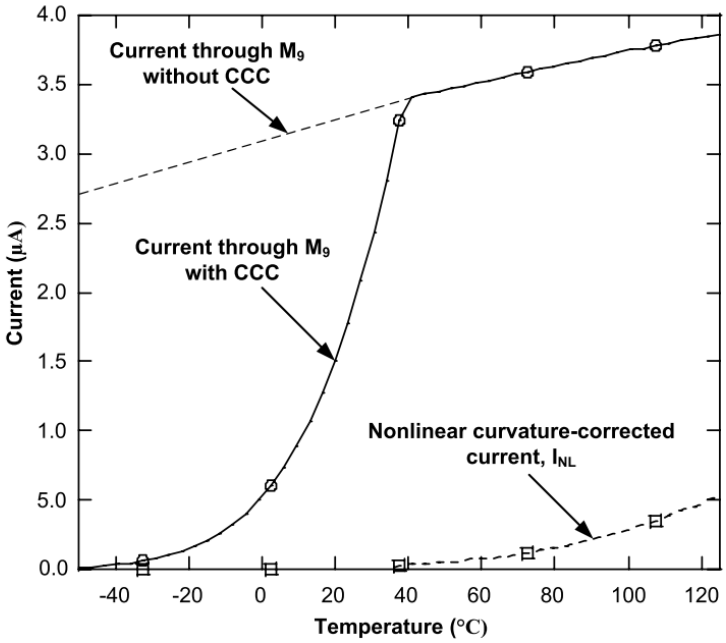

Figure 2-11 Current Flow Through M_9 And Nonlinear Curvature-Corrected Current [25]

The simulation is performed in CMOS 0.13μm process. According to simulation result, the proposed circuit able to save power consumption by 18.6% compared with a circuit without control current circuit. The supply voltage for this paper is 2.5V and it able to achieve 3.1ppm/^{0}C of temperature coefficient in the range of temperature from -50^{0}C till 125^{0}C [25].

A BGR circuit based on subthreshold MOSFET is introduced in the paper "A Subthreshold MOSFET Bandgap Reference with Ultra-Low Power Supply Voltage". Characteristics of subthreshold MOSFET is adapted to achieve temperature compensation is presented. Moreover, the proposed BGR can work under very low supply voltage [10].

Next, the gate-source voltage of subthreshold MOSFET can be represented as

$$V_{gs} = V_{th} = nV_T(\ln C - ln\frac{W}{L} + (\gamma - 2)\,)\ln T \quad (2.15)$$

n and γ are constants related to process of MOSFET and C is related to the current of MOSFET in subthreshold. V_{gs} of MOSFET in subthreshold region has negative temperature coefficient due to the first order derivative of the equation is negative. Next, different between V_{gs} of two MOSFET can be expressed as

$$\Delta V_{gs} = V_{gs1} - V_{gs2} = nV_T \ln \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} \quad (2.16)$$

Assuming n and γ of two MOSFET are the same. Based on the expression above, ΔV_{gs} will has positive temperature if $\left(\frac{W_2}{L_2}\right) > \left(\frac{W_1}{L_1}\right)$. The proposed circuit [10] is shown in Figure 2.11 below.

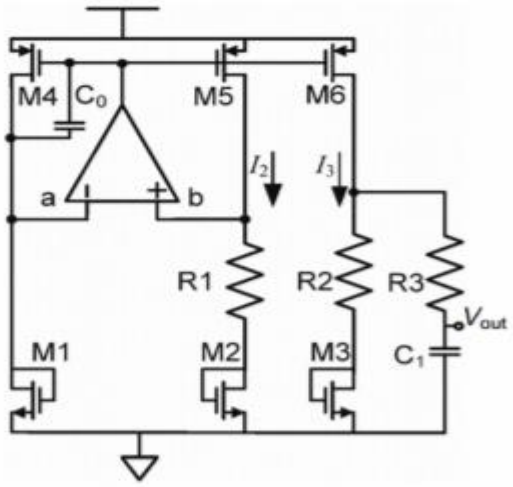

Figure 2-12 Proposed MOSFET Based Band Gap Circuit [10]

In Figure 2-12 above, node a and b will have the same voltage since the feedback loop gain of the operational transconductance amplifier is large. Capacitor C_0 is used stabilize the circuit. Meanwhile, the size of transistor M4 and M5 are the same to make sure the drain current to M1 and M2 is the same. Besides that, the current flowing to M1 and M2 transistor will be the same due to the input impedance of OTA is very large. Hence, I_2 can be expressed

$$I_2 = \frac{\Delta V_{gs}}{R1} = \frac{nV_T}{R1} \ln \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} \qquad (2.17)$$

Apart from that, I_2 is equal $I_3$to since M6 is mirror to M5 and M4. Hence, the output voltage of bandgap can be presented as

$$V_{out} = V_{gs3} + I_3 R2 = V_{gs3} + \frac{nV_T R2}{R1} \ln \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} \qquad (2.18)$$

Based on the equation above, M3 is having the negative temperature coefficient while the voltage drop on R2 has the positive temperature coefficient. Thus, zero temperature coefficient can be achieved if the expression below is fulfilled.

$$\frac{R1}{R2} = -\frac{nk}{q} \ln \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} \cdot \frac{1}{\frac{\partial V_{gs3}}{\partial T}} \qquad (2.19)$$

The forward voltage drop on BJT is about 700 mV while the saturate voltage of MOSFET is around 100mV. On top of that, the proposed bandgap has more potential

to work in low supply voltage in advanced technology while the forward voltage of BJT does scale significantly with advanced of technology [10].

The proposed circuit [10] is implemented in SMIC 0.13 µm RF technology. Supply voltage of this circuit can be as low as 0.6V and provide output reference of 0.43V in the range of temperature from -20^{0}C till 80^{0}C. Temperature coefficient of the proposed circuit is 25.6ppm/^{0}C.

The paper "A 0.45-V, 14.6-nW CMOS Subthreshold Voltage Reference with No Resistors and No BJTs" is suggesting a technique that can dynamically control the V_{TH} of MOSFET by using different body-bias voltage through current trimming [11]. This method is aim to overcome the problem of big threshold voltage variation of MOSFETS in the subthreshold. Figure 2.13 illustrated the proposed subthreshold CMOS reference circuit.

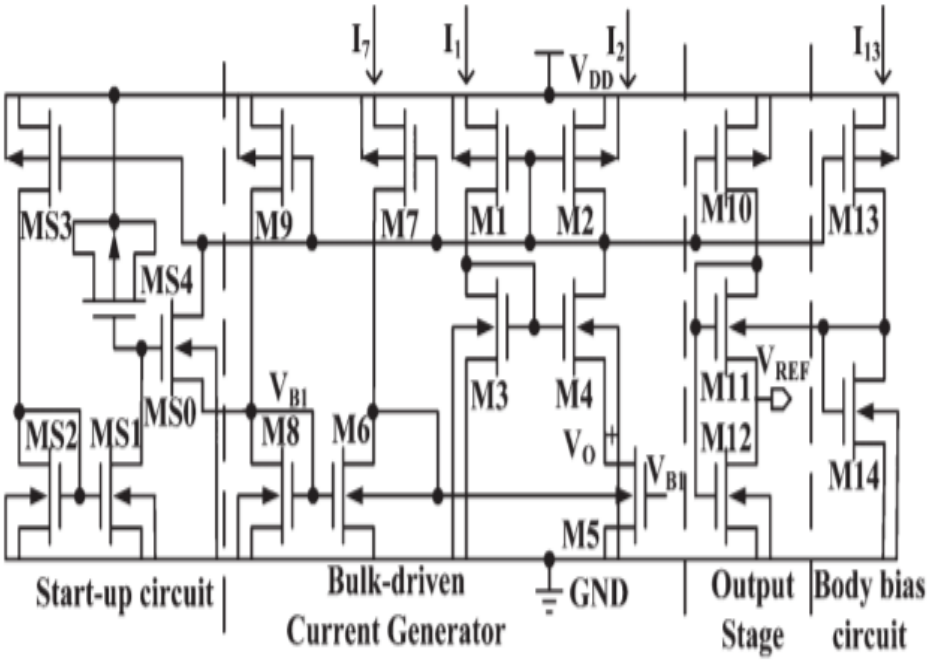

Figure 2-13 Core Of The Proposed Subthreshold MOSFET Reference Circuit [11]

Based on the Figure 2-13 above, it consists of start-up circuit, bulk-driven current generator, a body bias circuit and as well as output stage. On top of that, only m5 and M6 are not operate in sub threshold region. Bias voltage of, V_{gs} of M14 is provided by the body bias circuit to achieve temperature compensation. Moreover, the summation of positive TC voltage from the different between gate source voltage of M12 and M11 (ΔV_{gs}) and negative TC voltage from V_{gs} of M14 generate the temperature-independent V_{REF} [11].

The function of the bulk driven current generator is used to provide a stable current that will not affected by supply variation as much as possible. This is aim to compensate the temperature effect of $V_{REF.}$ The generated current I_2 from the current generator can be expressed by

$$I_2 = \frac{V_0}{R_{M5}} = \mu \cos k_5 (V_{GS,M5} - V^*_{TH,M5}) V_T ln \frac{K_1 K_4}{K_2 K_3} \qquad (2.20)$$

Where

$$V^*_{TH} \approx V_{TH0} + (n-1)V_{SB} \qquad (2.21)$$

R_{M5} – resistance of M5

K_1, K_2, K_3, K_4 are the aspect ratio of M1, M2, M3 and M4 respectively.

The current is mirror to the output stage and the V_{REF} can be expressed by

$$V_{REF} = \Delta V'_{gs} + f(V_{GS,M14}) \qquad (2.22)$$

Where $\Delta V'_{gs}$ is gate source voltage difference between M12 and M11.