

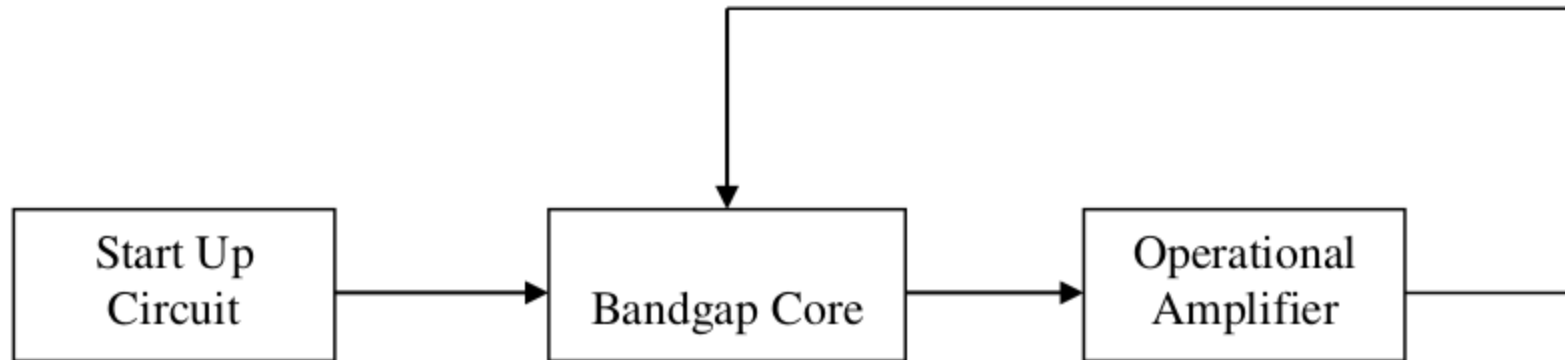
# Bandgap Design

---

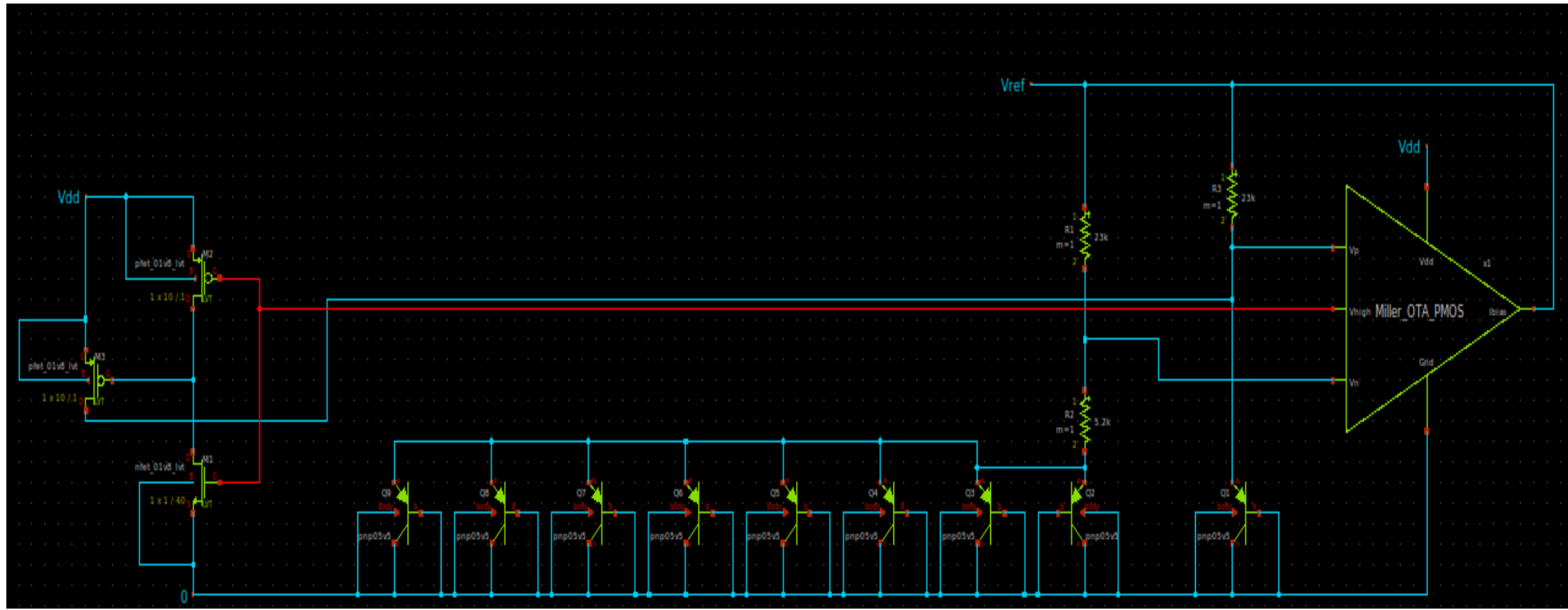
# Proposed Band-gap Design

---

The block diagram of the circuit is given below:



# Design of BGR using 1.8v supply



# Proposed Band-gap Design

## 1- Band-gap core analysis

---

-  $VR2 = I2 \times R2$

$$= ((V_{BE2} - V_{BE1}) / R3) \times R2$$

$$= V_T \ln(n) \times (R2 / R3)$$

$$= V_T \ln(8) \times (R2/R3)$$

Where: [n = 8 for our circuit] and  $V_T = KT/q$ .

-  $VR2$  is a positive TC which is  $1.94 \text{ mV}/^\circ\text{C}$  for the BJT's used in this circuit.

-  $V_{out} = V_{ref} = VR2 + V_{BE2}$ , thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).

## 2- Band-gap core analysis

---

$$V_{ref} = a_1 V_{R2} + a_2 V_{BE} = \text{const.} \Rightarrow dV_{ref}/dT = a_1 dV_{R2}/dT + a_2 dV_{BE}/dT = 0$$

$$\text{So } a_1(85\mu\text{V/K}) - a_2(1.6\text{mV/K}) = 0$$

Since CTAT slope is greater than PTAT slope we will make  $a_2=1$  and vary  $a_1$  to make PTAT slope increasing to reach CTAT slope:

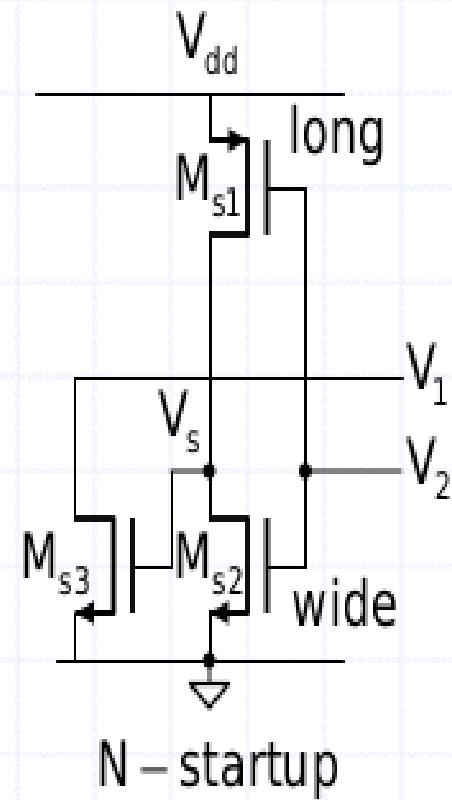
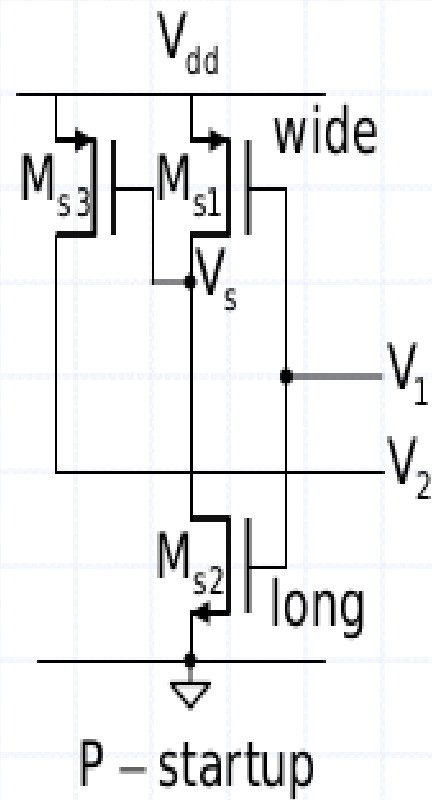
$$\text{So } a_1 = 1.6\text{m}/85\mu \Rightarrow a_1 = 19 = (R_2/R_1) \cdot \ln(8)$$

$$\text{Let } I = 30\mu\text{A} \text{ then } R_1 = V_T \ln(8)/I = 2\text{k ohm} \text{ and } R_2 = a_1 R_1 / \ln(8) = 18\text{k}$$

# Proposed Band-gap Design

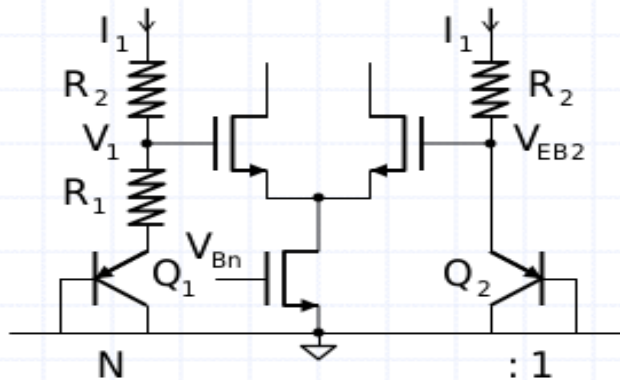
## 2- Start-up Circuit schemes

---



### 3- Choosing input stage of OTA

Let the gate overdrive voltage be  $V_{gsn} - V_{tn} = |V_{gsp}| - |V_{tp}| = V_{ov}$ .



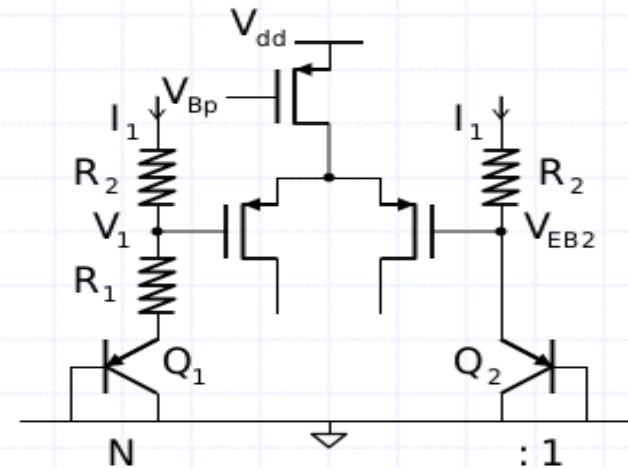
For NMOS input, we need

$$V_{EB2} > V_{tn} + 2V_{ov}$$

$V_{EB2}$  ranges from 0.5V to 0.7V

$$\Rightarrow V_{tn} < 0.2V$$

$\Rightarrow$  too tough to be satisfied



For PMOS input, we need

$$V_{dd} > V_{EB2} + |V_{tp}| + 2V_{ov}$$

For  $V_{EB} = 0.64V$ ,  $|V_{tp}| = 0.44V$ ,

$$V_{ov} = 0.15V$$

$$\Rightarrow V_{dd}(\min) = 1.38V.$$

## 4- Stability of Bandgap

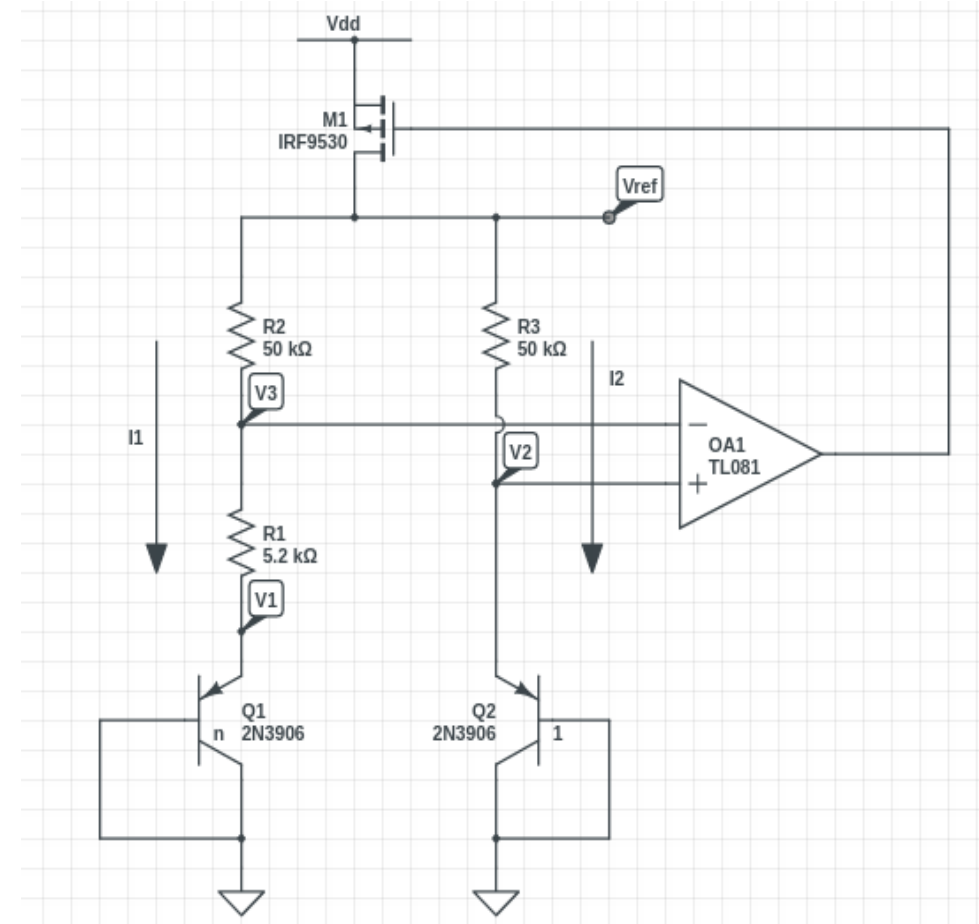
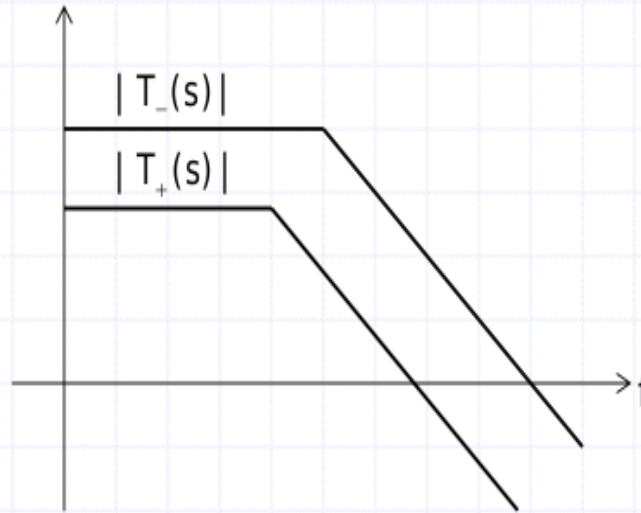
## Negative feedback loop:

$$T_- = \frac{1 + g_{m1}R_1}{1 + g_{m1}(R_1 + R_2)} \times A(s)$$

### Positive feedback loop:

$$T_+ = \frac{-1}{1 + g_{m1}R_2} \times A(s)$$

For stability, we need  $|T_-| > |T_+|$ , and this criterion is satisfied by the above two relations.





# Analysis of BGR circuit

$$I_2 = I_0 \exp(v_2/v_t) , I_1 = n * I_0 \exp(v_1/v_t)$$

$$\text{So } v_1 - v_2 = v_t \ln(I_1/nI_2)$$

$$I_1 = I_2$$

$$v_3 = I_1 * R_2 + v_1 = v_2$$

$$V_{ref} = I_1 * R_1 + v_3 \text{ and } V_{ref} = I_2 * R_3 + v_2$$

$$I_1 = I_2 = (v_2 - v_1)/R_2 \text{ so } I_1 = v_t/r_2 \ln(n)$$

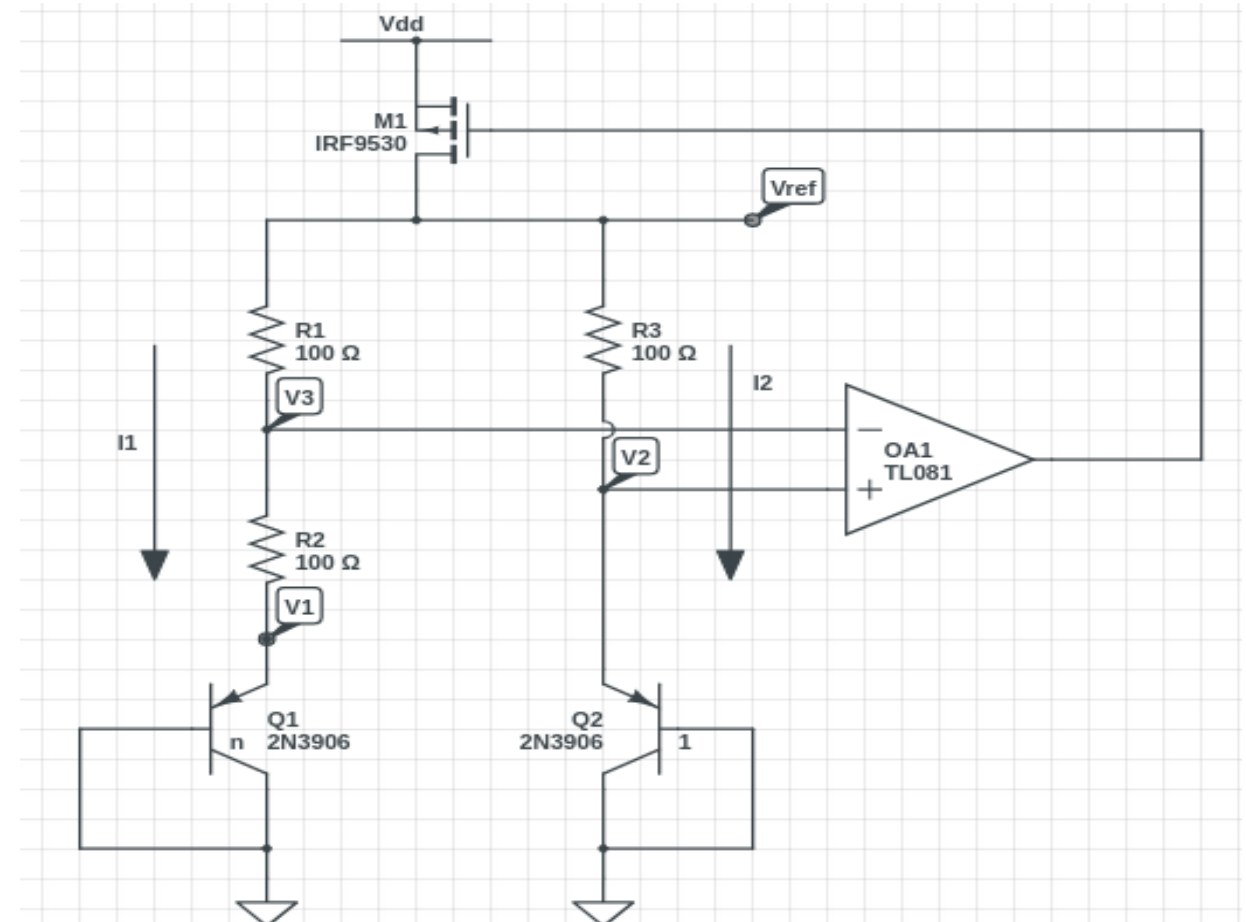
$$V_{ref} = v_t * (R_3/R_2) * \ln(n) + v_2 = 1.2v$$

$$V_{ref} = \text{-----PTAT-----} + \text{CTAT} = 1.2v$$

$$\text{Using } I_1 = I_2 = 10 \mu A , n = 8$$

$$\text{From above equation } R_2 = 5.2k\Omega$$

$$R_3 = R_1 = 50k\Omega$$



The circuit schematic shows a differential amplifier with a current mirror load. The circuit includes the following components and connections:

- PMOS Transistors:**
  - M1, M2, M5, M6, and M7 are PMOS transistors.
  - M1 and M2 are the main differential pair, with  $W/L = 1 \times 30 / 1$ .
  - M5 and M6 are part of the current mirror load, with  $W/L = 1 \times 10 / 1$ .
  - M7 is a PMOS transistor with  $W/L = 1 \times 54 / 1$ .
- NMOS Transistors:**
  - M3, M4, and M8 are NMOS transistors.
  - M3 and M4 are the tail current source, with  $W/L = 1 \times 7.4 / 0.5$ .
  - M8 is a PMOS transistor with  $W/L = 1 \times 75 / 0.5$ .
- Current Source:**
  - A current source M8 is connected to the output node, with  $W/L = 1 \times 75 / 0.5$ .
- Capacitor:**
  - A capacitor C1 with value 900f and  $m=1$  is connected to the output node.
- Inputs and Outputs:**
  - Vdd is the positive supply voltage.
  - Gnd is the ground.
  - Vp and Vn are the differential inputs.
  - Vhigh is a high voltage input.
  - Ibias is the bias current input.

# Analysis of OTA

---

- Two stage miller OTA used with the following specs:-

DC gain = 60 dB , GBW = 30 MHz , Phase margin  $\geq 60$  deg , ICMR = 0.8v : 1.6v

Slew rate = 20v / microsec , C load = 2pf , Vdd = 1.8v

- Miller cap  $C_c \geq 0.22$  to achieve PM  $\geq 60$  deg so  $C_c = 800$ fF

- from Slew rate equation :  $SR = I_5 / C_c$  we get  $I_5 = 20$  microAmp

- from GBW equation:  $GBW = gm_1 / 2\pi C_c$  we get  $gm_1$  then (W/L) of m1,m2

- from ICMR+ equation : we get (W/L) of m3,m4

- from ICMR- equation : we get (W/L) of m5,m6

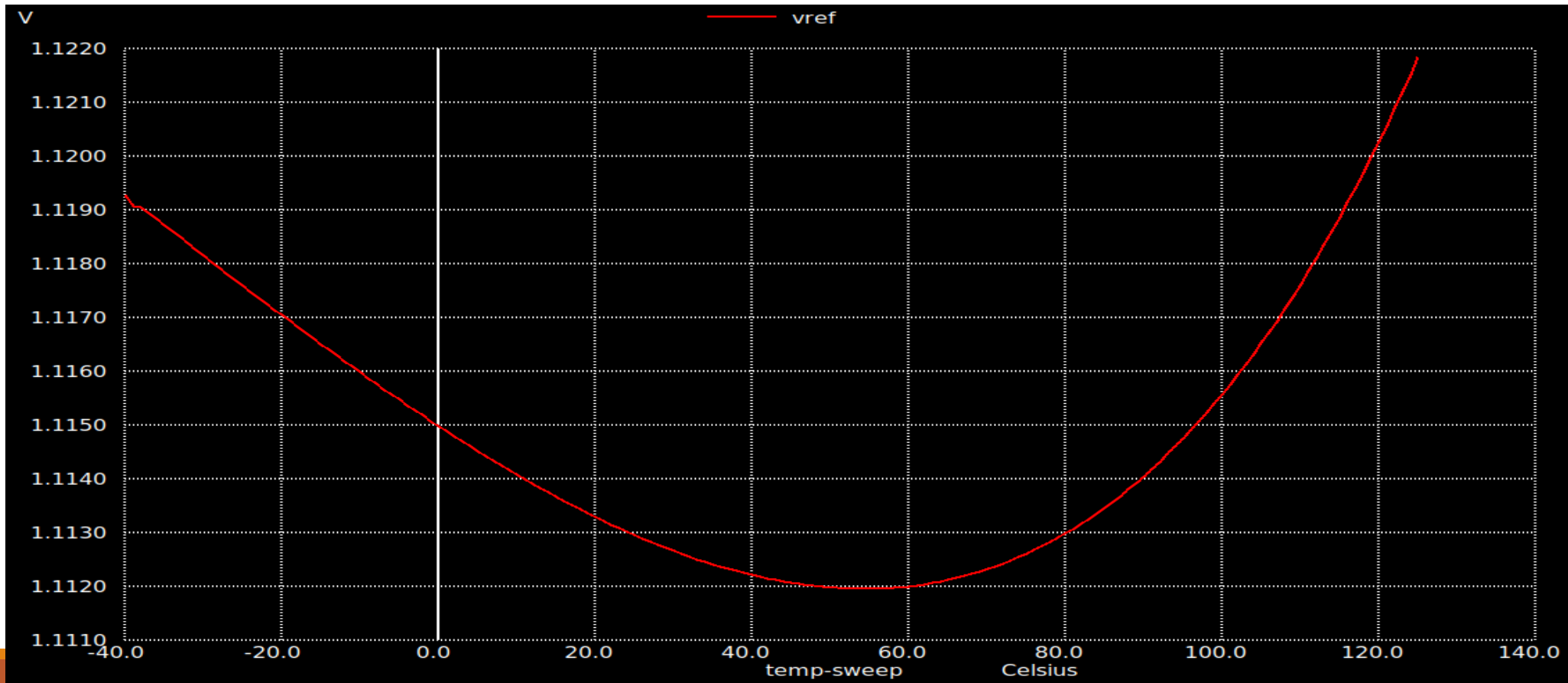
- from phase margin condition : we get (W/L) of m8

-from current mirror relation between m5,m7 we get (W/L) of m7

# Simulation of Bandgap 1.8v

## 1- DC sweep vs Temperature

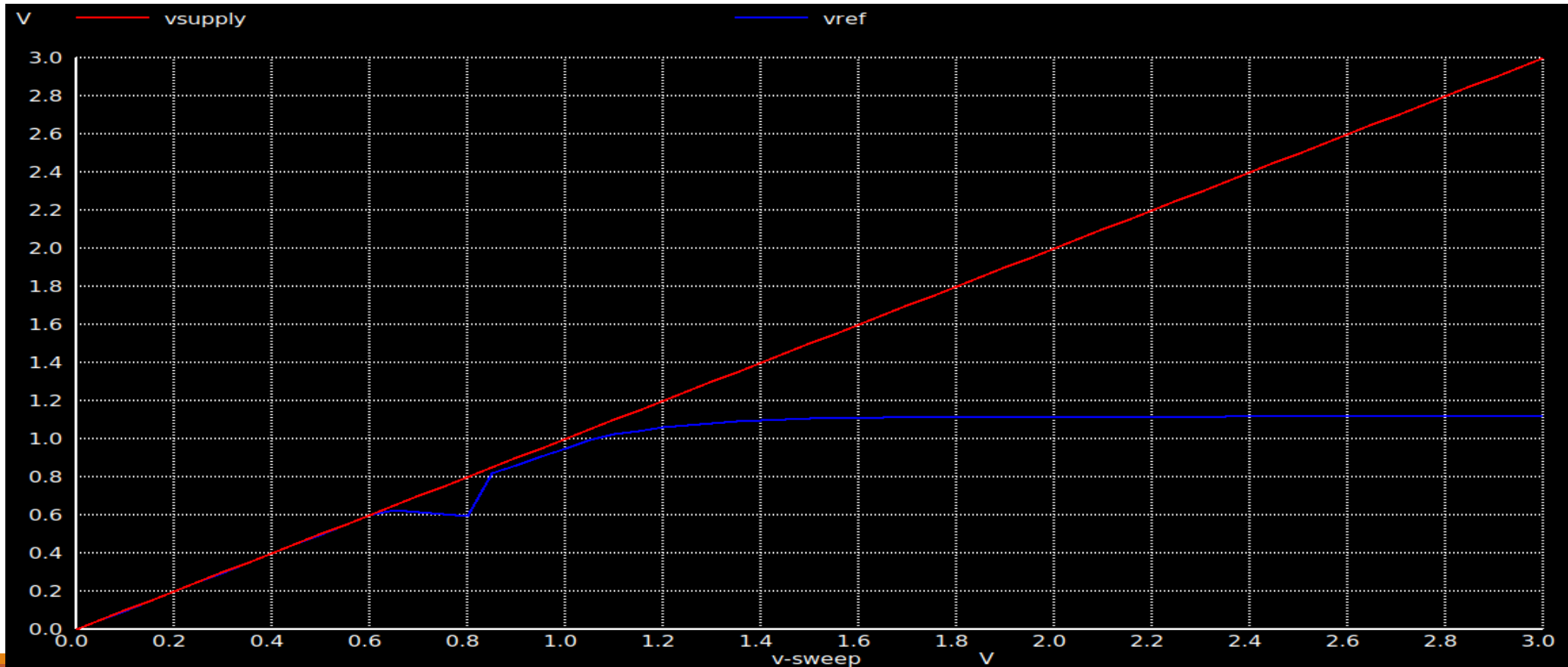
Using  $V_{dd}=1.8\text{v}$  and the temperature was swept from  $-40$  to  $125$  deg and output is 1.11



# Simulation of Bandgap 1.8v

## 2- DC sweep vs Supply voltage

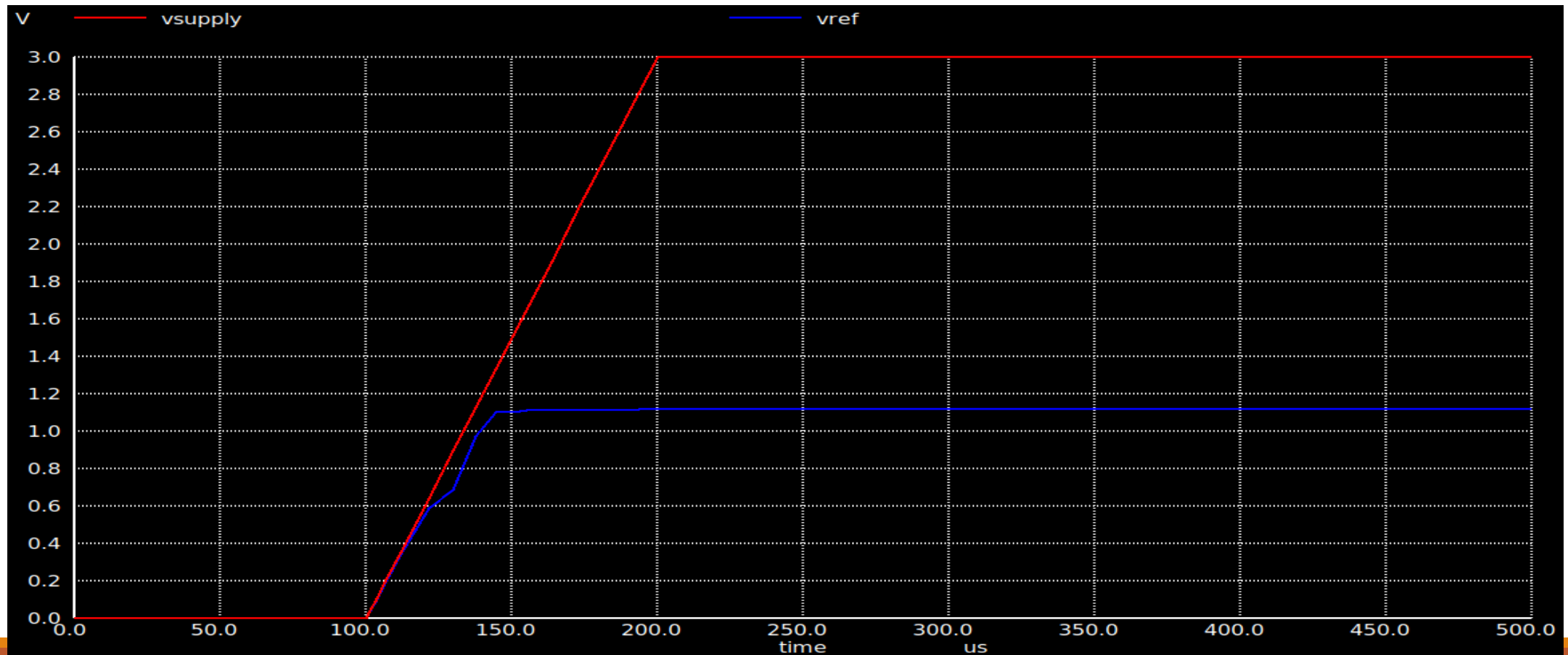
- VDD was swept from 0 to 3v and the output is 1.1v



# Simulation of Bandgap 1.8v

## 3- Transient Analysis

- A step voltage from 0 to 3v volt used with 100 us rise time and the output is 1.1v



# Simulation of Bandgap 1.8v

## 4- PSRR Analysis

- PSRR = -40 dB from 1Hz to 16 KHZ

