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Design and Analysis of A Low-Dropout Regulator For Portable Devices

Sen Li, Di Wu, Yuliang Zhang

Abstract

This paper presents detailed design and analyses of a low-dropout regulator (LDO) for applications in portable devices. The proposed circuit is characterized by simple structure, small dropout voltage (≤0.2V), large load capability (maximum load 200mA), and fast transient response (≤2.5μs undershoot recovery time) to load variations between 0 to 100mA. In addition, the overall quiescent current of the circuit is controlled within the specification (≤40μA) and hence the overall power efficiency is high. By employing ESR zero and a buffer stage which is realized by a PMOS source follower, the LDO is able to maintain stability under full range of load current. The circuit is then modeled and simulated using TSMC 0.35μm CMOS process. The discussion of obtained simulation results, along with detailed comparison with previously reported LDO topologies, are demonstrated in the concluding section of the paper for better illustration of the features of proposed LDO configuration.

I. INTRODUCTION

Portable devices, such as cell phones, tablets and smart watches, are typically handheld, light-weighted and battery-powered electronic apparatuses which enjoy increasing demand from global IT markets. In design of these devices, power management is one of the key issues for achieving product specifications such as extended run time and low-power consumption. The low-dropout regulator (LDO) is among the most popular circuit components in this field owing to its unparalleled features like low cost, small output ripple, and reduced power dissipation. Some principal requirements for the LDO include low dropout voltage, high load current capability, fast transient response to input supply variation and stability in full load range. However, these conditions are difficult to be satisfied simultaneously due to the intricate performance tradeoffs.

Previously, three improved design of LDO circuits have been studied and analyzed in details: *Chaitanya K. Chava* and *José Silva Martínez* proposed a novel frequency compensation scheme for LDO voltage regulators which can effectively overcome the stability issue. The circuit is featured by improved noise performances and output transient response (<25μs undershoot recovery time under maximum load condition) without considerably increasing the power consumption or die area[1]; In [2], *Mohammad Al-Shyoukh, Hoi Lee* and *Raul Perez* presented a method which is called buffer impedance attenuation (BIA) to realize a midway stage for driving

TABLE I: COMPARISON OF THE THREE PROPOSED LDO DESIGNS IN [1] – [3]

Parameters	**Design in [1]**	**Design in [2]**	**Design in [3]**
Technology (μm)	0.5	0.35	0.35
Input Supply Voltage (V)	3.3	2.0 ~5.5	2.0 ~ 3.3
Nominal DC Output Voltage (V)	2.8	1.8	1.8
Dropout Voltage V_{do} (V)	0.5	0.2	0.2
Maximum Load Current (mA)	100	200	10
Quiescent Current (μA)	25	20	0.68
Current Efficiency (%)	99.75	99.84	99.99
Output Voltage Variation (mV)	100	54	3
Load Step (Up / Down) Recovery Time (μs)	25 / 75	27 / 30	25 / 50
Phase Margin (Worst Case) (degrees)	60	65	57
Load Capacitor (μF)	2.2	1	1
ESR Zero Required	Yes	No	No

the PMOS pass device and achieve several notable features including pushing the non-dominant poles away from the unity gain frequency, large phase margin (>60° under worst case); low quiescent current dissipation (20μs under no-load condition) and fast transient settling behavior (<25μs undershoot recovery time under maximum 100mA load condition); *Jianping Guo* and *Ka Nang Leung* reported a design of sub-1μA CMOS low-dropout regulator in [3] with the internal compensation mechanism and an adaptive current boosting voltage buffer, which is characterized by low quiescent current (680nA), fast transient response but also limited (10mA) load capability. By thorough studying of these circuits, one may gain better understanding of the structure, operation principle, and characteristics of the linear regulators and develop critical insight to the underlying factors which influence the circuit performance.

In this paper, a design of low-dropout regulator for implementation in portable devices is presented and analyzed, using TSMC 0.35μm CMOS technology. The circuit incorporates CMOS current source for biasing purpose and a PMOS source-follower as the buffer stage, which enjoys numerous attributes including simple structure, large load capability, and fast transient response to load variations. Moreover, the dropout voltage is less than 0.2V (under 2V supply voltage) and the overall quiescent current of the circuit is less than 30μA, hence the overall power efficiency is high. The paper is organized as follows: Section II demonstrates the circuit schematics, device parameters and design procedures; Section III presents the simulation results obtained from Cadence Spectre along with explanation and discussion. A brief summary of the project is given in Section IV.

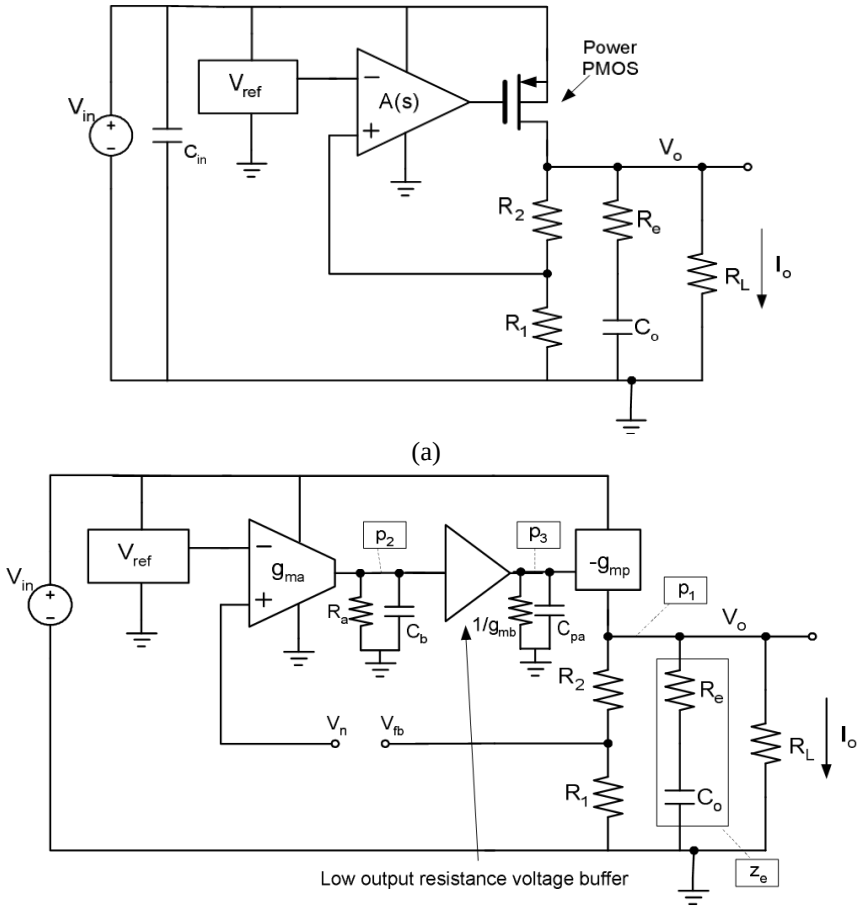

Fig. 1 Block diagrams of LDO circuits: (a) without buffer stage (b) with buffer stage

II. DESIGN OF THE LOW-DROPOUT REGULATOR

The block diagrams of the typical LDO circuit structures are shown in Fig. 1. It can be observed that there are four major components in configuration (a): voltage reference: essentially a very stable voltage insensitive to temperature and input voltage variation; error amplifier (EA): a high low-frequency gain amplifier for achieving a close to zero error signal (V_{err}= V_+ - V_-); feedback network: resistors R_{f1} and R_{f2} define the feedback factor (level shift the output voltage) and generate V_{fb} to be compared with V_{ref} to define the designed output voltage V_o; pass device: a power transistor to pass high current from the input to output. In order to obtain better improvement on stability, a buffer stage is usually incorporated in the LDO circuit, as shown in Fig. 1(b). The main function of this stage is to push non-dominant poles to higher frequency (away from the unity gain frequency) and increase the phase margin of the circuit. In this topology, the required value of the effective series resistance (ESR) R_e can be reduced and hence the overshoot and undershoot of output voltage under load step variation can be minimized. The poles and zero of the loop gain transfer function are given by:

$$p_1 = \frac{1}{r_o C_o}, p_2 = \frac{1}{R_a C_b}, p_3 = \frac{g_{mb}}{C_{pa}}, z_e = \frac{1}{R_e C_o} \quad (1)$$

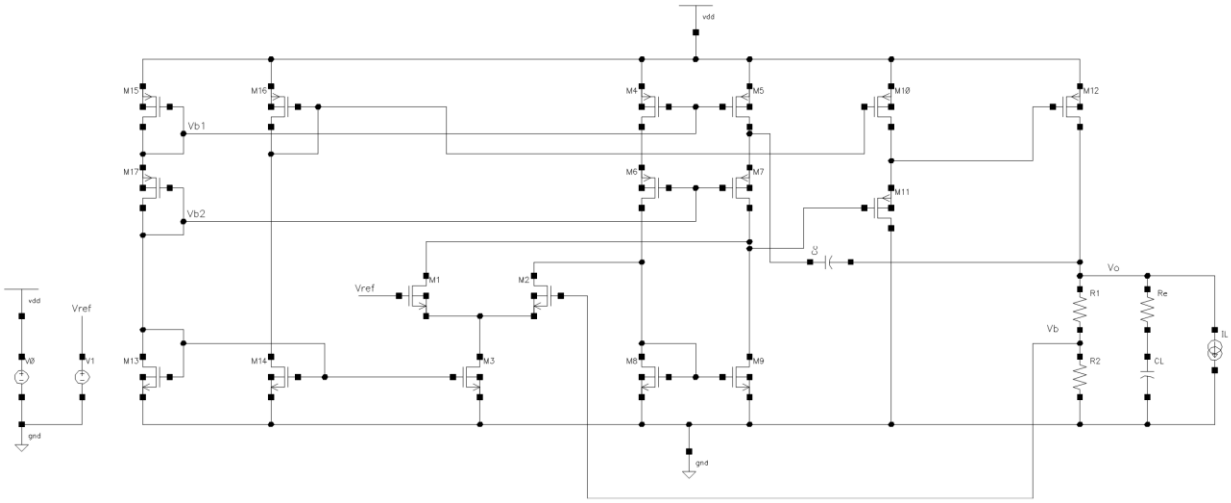

Fig. 2 Schematic of the proposed low-dropout regulator

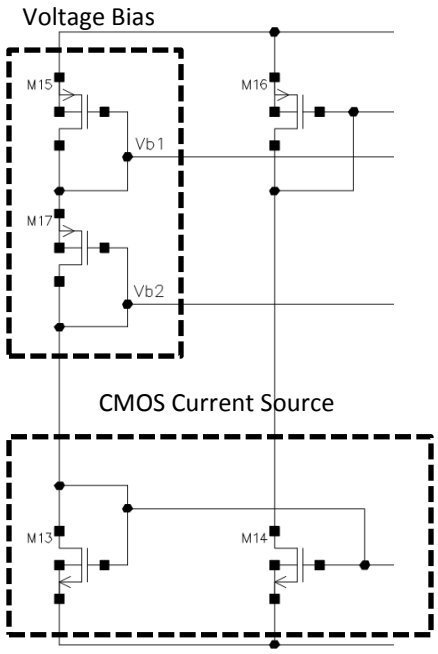

Fig. 3 Schematic of the biasing circuit

Fig. 2 shows the complete schematic of the LDO circuit in this project. The major components include: a biasing circuit (shown in Fig. 3) which sets the DC bias condition; an error amplifier (shown in Fig. 4) which is realized by a 2-stage folded cascode amplifier to produce high voltage gain and wide input common-mode range; a buffer stage (shown in Fig. 5) by employing a PMOS source-follower to push the non-dominant poles to higher frequency and ensure the stability and fast transient response of the circuit; a PMOS pass transistor with given loading condition (shown in Fig. 6). The sizes of the transistors are provided in Table II.

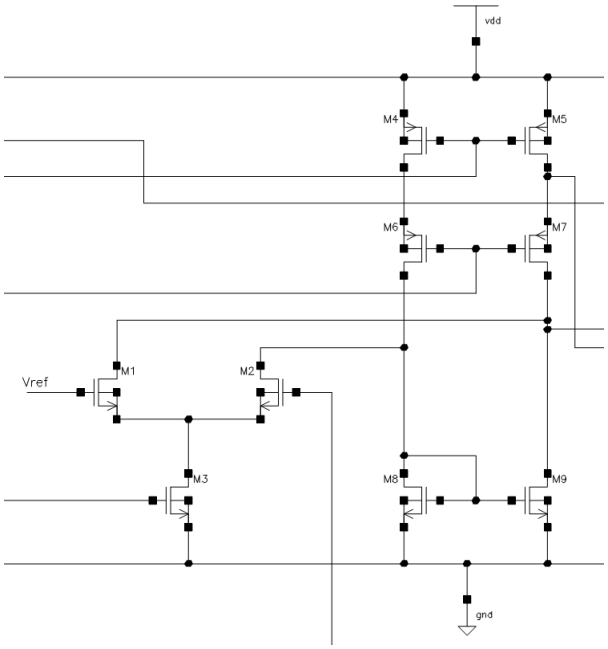

Fig. 4 Schematic of the 2-stage folded cascade amplifier as the error amplifier

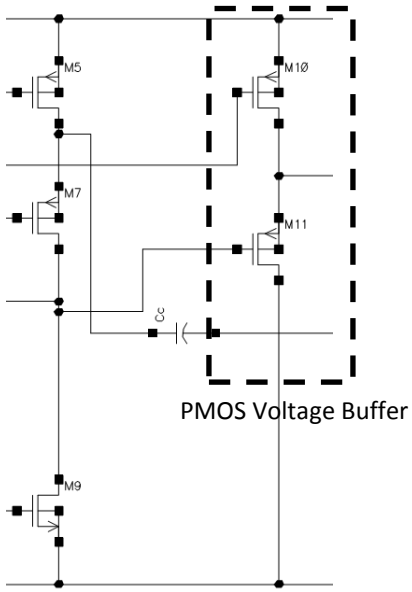

Fig. 5 Schematic of the PMOS source-follower as the buffer stage

The key steps in this LDO design are as follows. Initially, the error amplifier is constructed along with the DC bias circuits. In order to produce sufficient gain from the amplifier, the bias network is used to ensure the transistors in the cascade stage working in saturation region to exhibit high impedance at the output. Then the structure of buffer stage is selected according to some typical topologies as well as the project specifications. The final step is to establish the complete feedback network for the circuit and testing the model in Cadence. The details regarding specific parameter settings are discussed in Section III.

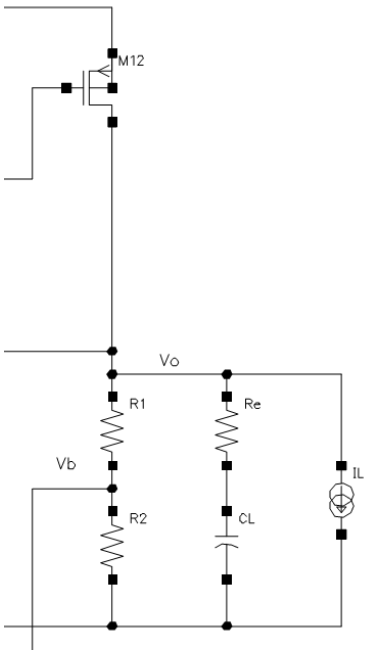

Fig. 6 Schematic of the power transistor stage and the load configuration

TABLE II: DIMENSIONS OF THE TRANSISTORS

Transistor	**Length (μm)**	**Width (μm)**
M1, M2	25	1
M3	90	1
M4, M5	15	1
M6, M7	5	1
M8, M9	1	2
M10	6	1
M11	60	1
M12	50000	0.35
M13	3	1
M14	23.5	1
M15	1.3	1
M16	2	1
M17	4	1

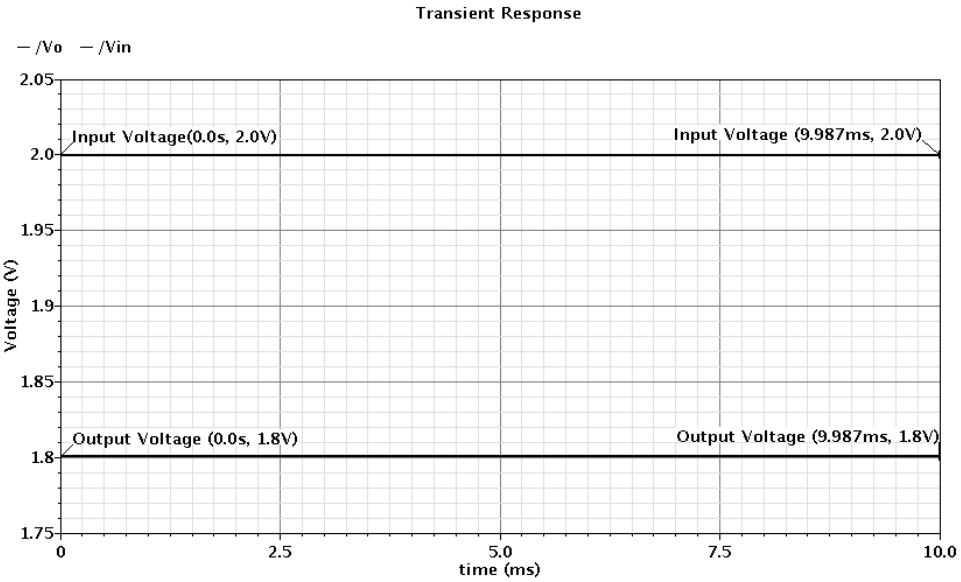

Fig. 7 Input and output voltages versus time under maximum load condition (200mA)

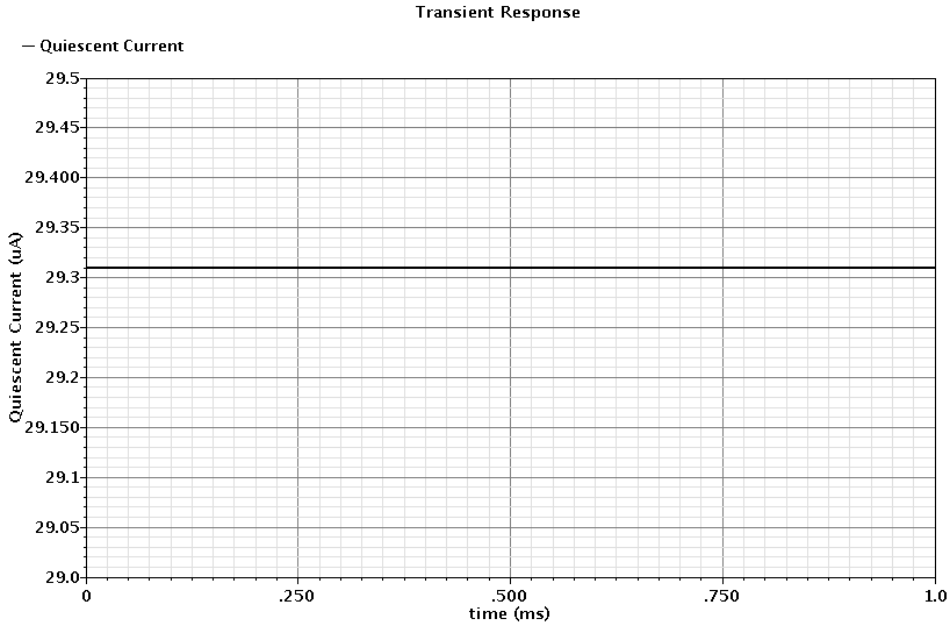

Fig. 8 Quiescent current of the LDO circuit under no-load condition

III. SIMULATION RESULTS OF THE LDO REGULATORS

In this project, the LDO circuit is realized and simulated by Cadence Spectre using TSMC 0.35μm CMOS process. The input supply voltage is 2V. The transistor ratios of the bias circuit (M_{13} - M_{17}) are selected such that the dc bias current is 2μA and the transistors in the output stage of error amplifier ($M_4 - M_9$) works in saturation region. In this case, the bias voltages V_{b1} and V_{b2} are 1.2V and 0.5V, respectively. The size of the buffer transistors (M_{10}, M_{11}) are chosen so that it can assist the circuit to push the non-dominant poles to higher frequency and stabilize the feedback loop. The size of the pass transistor M_{12} is selected such that it can deal with large load

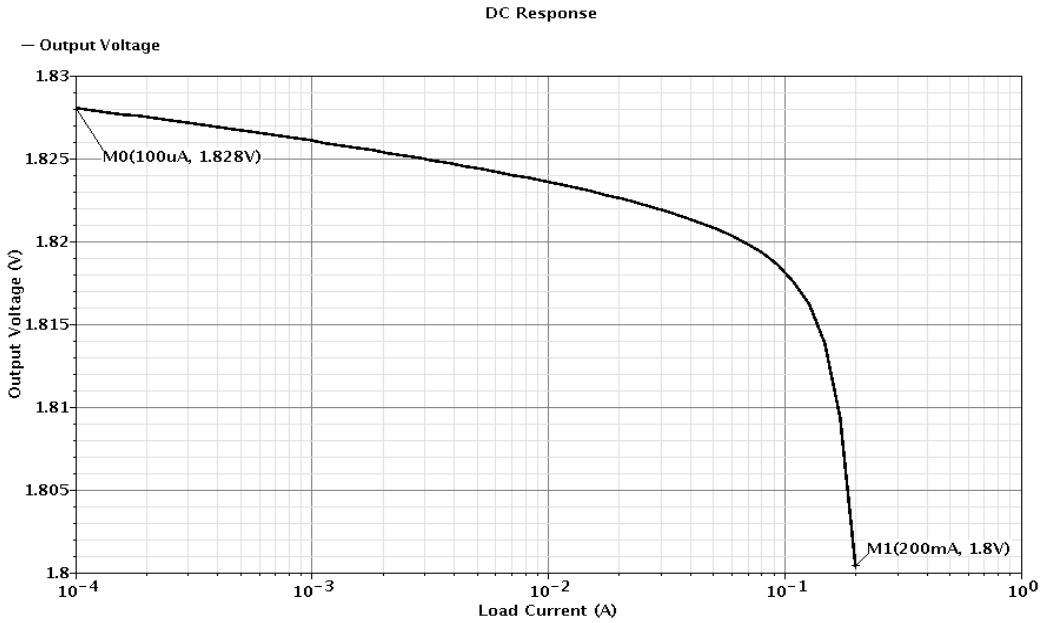

Fig. 9 Output voltage versus load current variation from 0.1mA to 200mA

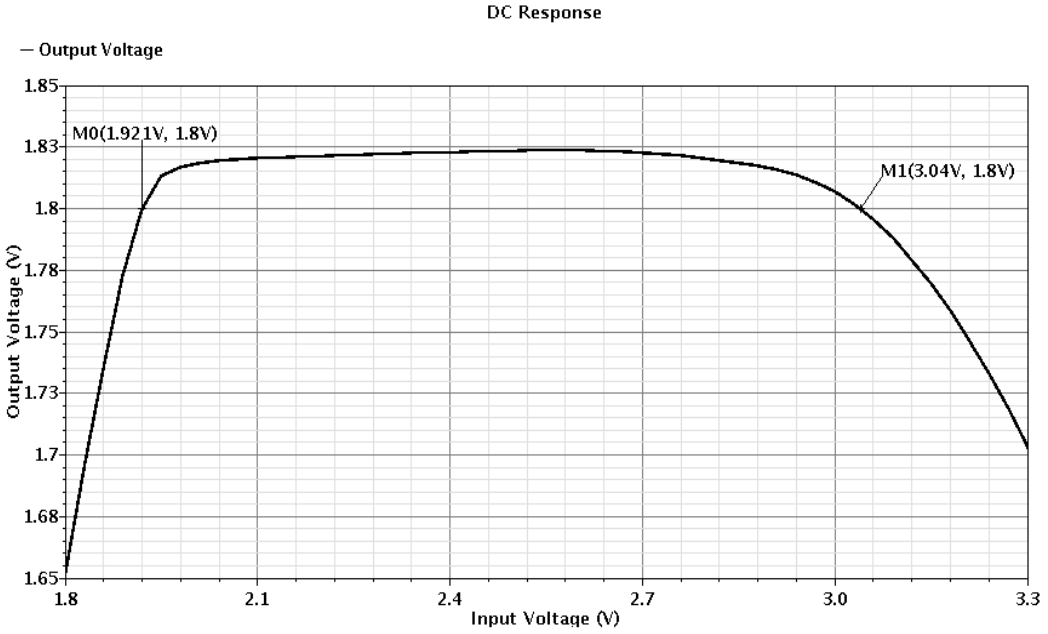

Fig. 10 Output voltage versus input voltage variation from 1.8V to 3.3V under 100mA load condition

variations with reduced dropout voltage and improved output transient response. The feedback resistances R_1 and R_2 are set to be 257 kΩ and 200 KΩ, respectively, to provide the scaled output voltage to the input of the error amplifier according to the reference voltage (0.8V). The effective series resistance (ESR) is set to be 0.2Ω and the load capacitor is 2 µF. The compensation capacitor for the amplifier C_C is adjusted to be $5pF$ for stabilization purpose.

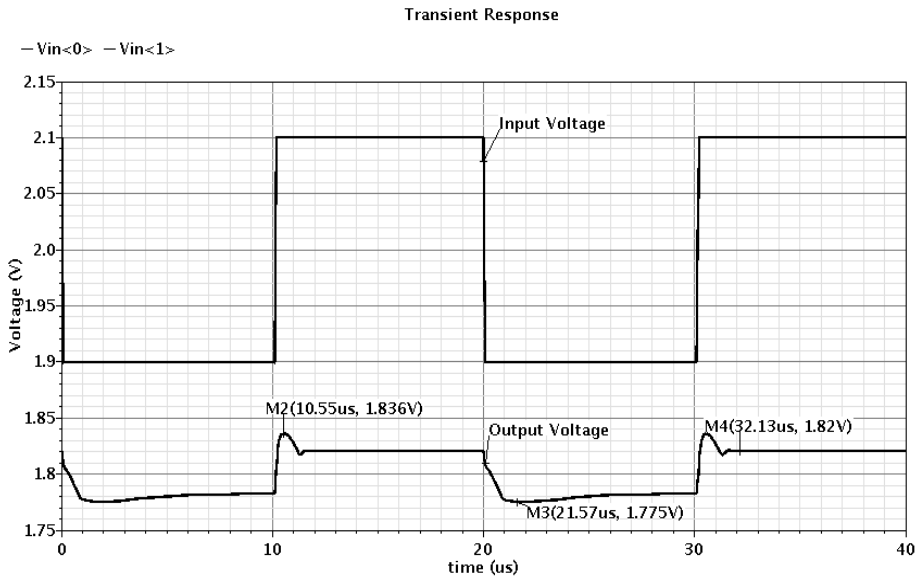

Fig. 11 Output transient response versus input variation from 1.9V to 2.1V under 100mA load condition

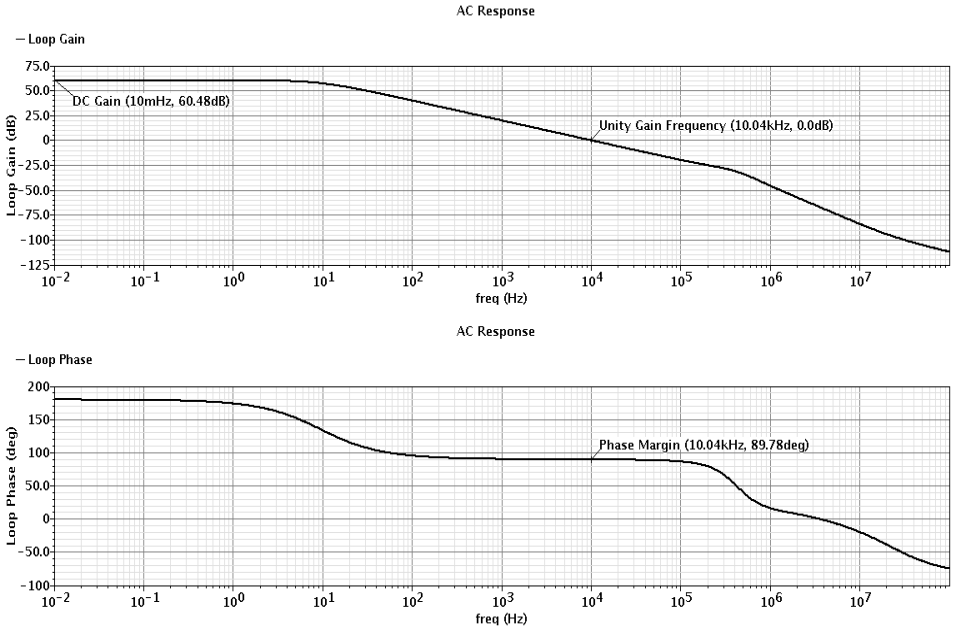

Fig. 12 Loop gain simulation results under minimum load condition (100 μA)

Fig. 7 shows the waveform of input and output voltages versus time under maximum load condition (200mA). It can be seen that both voltages are very stable in the period of 10ms. Fig. 8 clearly indicates that the quiescent current of the circuit is 29.3 μA, which is less than 40 μA specification. The output voltage versus load current varying from 0.1mA to 200mA is demonstrated in Fig. 9. The output voltage variation is only 28mV. Fig. 10 displays the output voltage versus the input voltage variation from 1.8V to 3.3V under 100mA load condition. Obviously, the dropout voltage is less than 0.2V when the input voltage is set to 2V. Fig. 11 presents the output transient response versus input variation from 1.9V to 2.1V under 100mA load condition. The overshoot and undershoot of the output voltage are less than 45mV.

Poles (Hz)

	Real	Imaginary	Qfactor
1	-9.49900e+00	0.00000e+00	5.00000e-01
2	-2.80001e+05	+/- 3.21497e+05	7.61308e-01
3	-2.19948e+06	0.00000e+00	5.00000e-01
4	-3.29059e+06	0.00000e+00	5.00000e-01
5	-1.30353e+07	0.00000e+00	5.00000e-01
6	-7.06948e+07	0.00000e+00	5.00000e-01
7	-1.70228e+08	0.00000e+00	5.00000e-01
8	-2.15929e+08	0.00000e+00	5.00000e-01
9	-5.41775e+08	0.00000e+00	5.00000e-01
10	-7.29282e+10	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(vb,0)/V5

	Real	Imaginary	Qfactor
1	-3.97887e+05	0.00000e+00	5.00000e-01
2	-1.69096e+06	0.00000e+00	5.00000e-01
3	-3.32788e+06	0.00000e+00	5.00000e-01
4	-1.30947e+07	0.00000e+00	5.00000e-01
5	2.31146e+07	0.00000e+00	-5.00000e-01
6	-6.89540e+07	0.00000e+00	5.00000e-01
7	-1.97941e+08	0.00000e+00	5.00000e-01
8	-2.20374e+08	0.00000e+00	5.00000e-01
9	-5.46791e+08	0.00000e+00	5.00000e-01
10	-5.37240e+08	+/- 8.69373e+08	9.51136e-01

Constant factor = 1.51810e-05

DC gain = 1.05674e+03

Fig. 13 Pole zero analysis results under minimum load condition (100 µA)

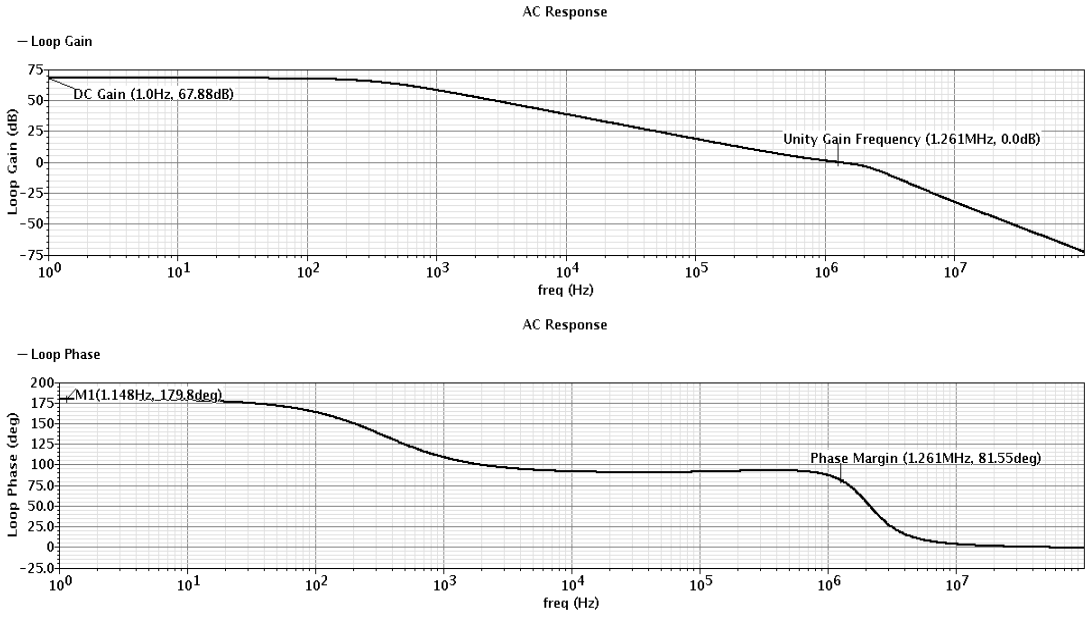

Fig. 14 Loop gain simulation results under maximum load condition (200mA)

The loop gain simulation results under minimum load current (100 µA) are shown in Fig. 12. It can be observed that the DC gain is 60.48dB (≥50dB requirement) and the unity gain frequency is 10.04 kHz. The loop gain phase margin in this case is 89.78 ° and the pole zero analysis results are given in Fig. 13. Fig. 14 shows the loop gain simulation results under maximum load condition (200mA). In this case, the DC gain is 67.88dB ((≥ 50dB requirement) and the unity gain frequency is 1.261 MHz. The loop gain phase margin in this case is 81.55 ° and the pole zero analysis results are given in Fig. 15.

Poles (Hz)

	Real	Imaginary	Qfactor
1	-3.48667e+02	0.00000e+00	5.00000e-01
2	-4.35460e+05	0.00000e+00	5.00000e-01
3	-1.16634e+06	+/- 1.73982e+06	8.97931e-01
4	-3.28832e+06	0.00000e+00	5.00000e-01
5	-1.30341e+07	0.00000e+00	5.00000e-01
6	-7.06780e+07	0.00000e+00	5.00000e-01
7	-1.70231e+08	0.00000e+00	5.00000e-01
8	-2.15930e+08	0.00000e+00	5.00000e-01
9	-5.41776e+08	0.00000e+00	5.00000e-01
10	-8.60972e+10	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(vb,0)/V5

	Real	Imaginary	Qfactor
1	-3.97887e+05	0.00000e+00	5.00000e-01
2	-1.69198e+06	0.00000e+00	5.00000e-01
3	-3.32758e+06	0.00000e+00	5.00000e-01
4	-1.30895e+07	0.00000e+00	5.00000e-01
5	-6.89095e+07	0.00000e+00	5.00000e-01
6	-1.91090e+08	0.00000e+00	5.00000e-01
7	-2.18334e+08	0.00000e+00	5.00000e-01
8	-5.26475e+08	0.00000e+00	5.00000e-01
9	-1.14996e+09	0.00000e+00	5.00000e-01
10	1.24605e+09	0.00000e+00	-5.00000e-01
11	-9.21460e+09	0.00000e+00	5.00000e-01

Constant factor = 1.46272e-05

DC gain = 2.47753e+03

Fig. 15 Pole zero analysis results under maximum load condition (200mA)

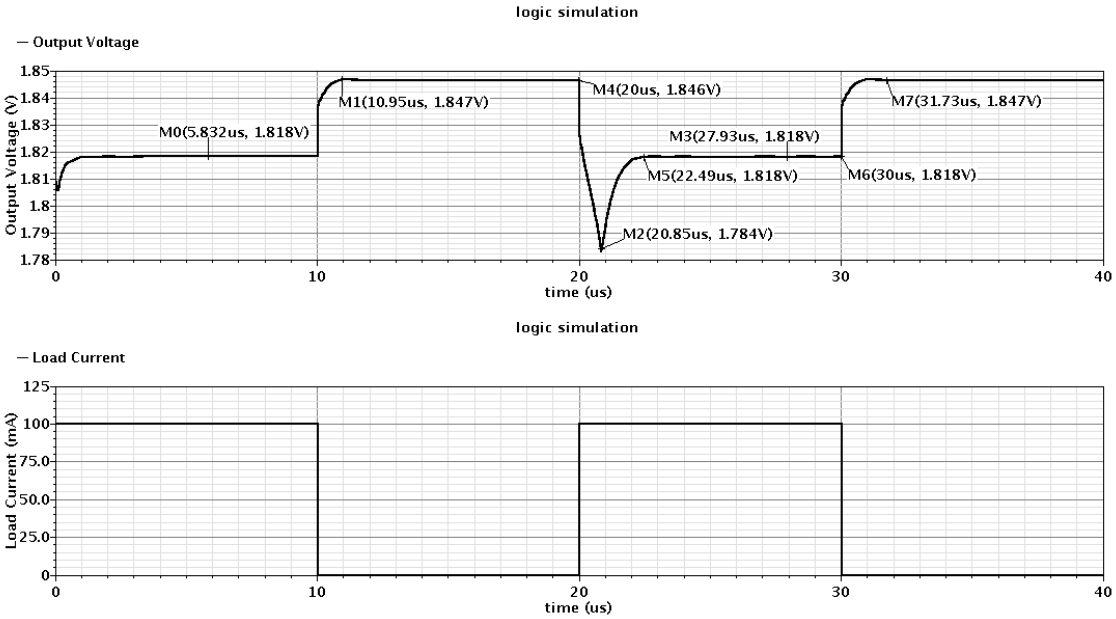

Fig. 16 Output transient response under maximum load step variation from 0mA to 100mA

Fig. 16 exhibits the output transient response under maximum load step variation from 0mA to 100mA with slew rate of 100mA/10ns. The overshoot and undershoot of the output voltage are less than 35mV and the transient recovery time is less than 2.5μs. The output transient response under maximum load step variation from 0 to 200mA is manifested in Fig 17. In this case, the dropout voltage is 0.2V and the overshoot and undershoot of the output voltage are less than 70mV, which are both within the targeted specifications.

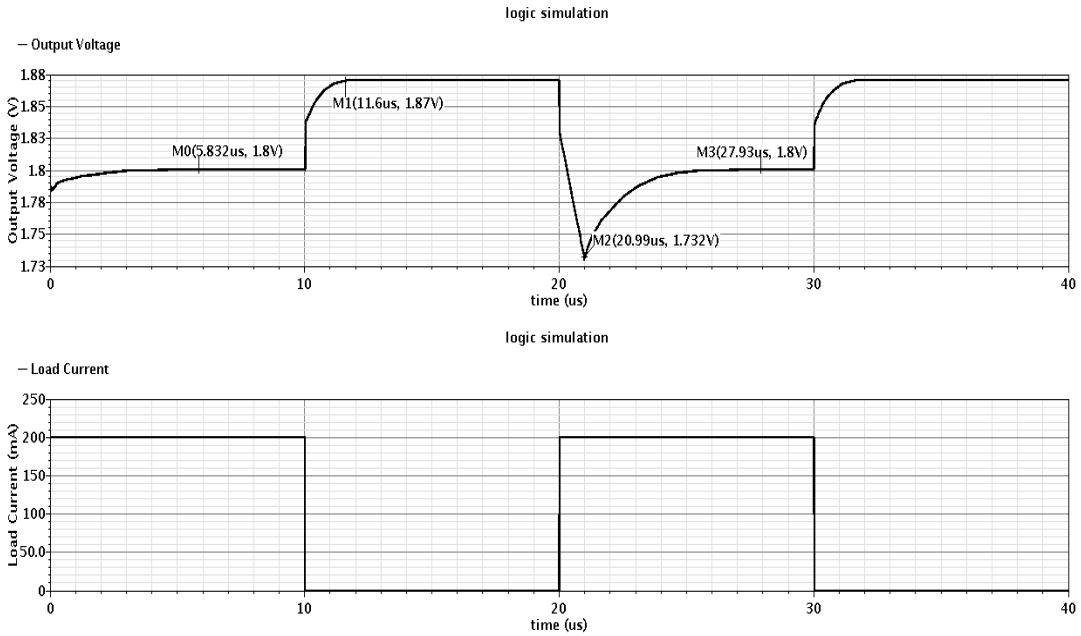

Fig. 17 Output transient response under maximum load step variation from 0mA to 200mA

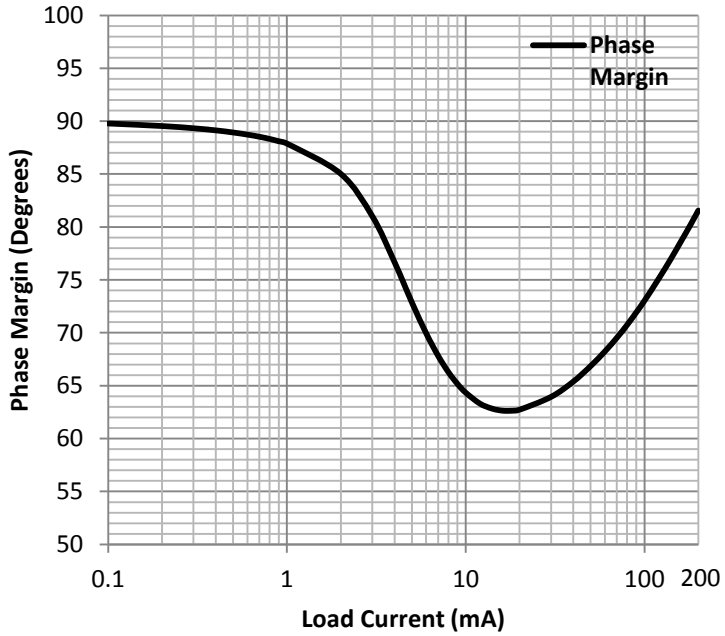

Fig. 18 Loop gain phase margin versus load current varying from 0.1mA to 200mA

The loop gain phase margin versus load current varying from 0.1mA to 200mA is displayed in Fig. 18. It can be observed that the phase margin is always greater than 60 ° with the worst case value of 62.7 °. Therefore, the LDO circuit is sufficiently stable with fast transient behavior. The loop gain phase margin and unity gain frequency under different load conditions are shown in Table III. Table IV summarizes the simulation results of the circuit.

TABLE III: LOOP GAIN PHASE MARGIN AND UNITY GAIN FREQUENCY

Load Current (mA)	**Phase Margin (Degrees)**	**Unity Gain Frequency (Hz)**
0.1	89.78	10.04K
0.5	88.93	44.69K
1	87.88	84.55K
3	81.02	228.6K
5	72.86	343.3K
10	64.34	509.4K
20	62.73	676.3K
50	66.86	898.8K
100	73.03	1.075M
200	81.55	1.261M

TABLE IV: SIMULATION RESULTS OF THE LDO REGULATOR

Parameters	**Specifications**	**Simulated Results**	**Compliance (Yes/No)**
Minimum supply voltage	≤ 2V	2V	Yes
Maximum output current	≥ 150mA	200mA	Yes
Dropout voltage	≤ 0.2V	0.2V (under maximum load condition)	Yes
Quiescent current	≤ 40 µA	29.3 µA	Yes
Output capacitor	≤ 3 µF	2 µF	Yes
Equivalent series resistor (ESR)	≤ 2Ω	0.2Ω	Yes
Minimum loop-gain magnitude	≥ 50dB	60.48dB (under minimum load condition)	Yes
Maximum undershoots and overshoots	≤ 100mV	≤ 70mV (under maximum load condition)	Yes
Transient recovery time	≤ 5 µs	≤ 2.5 µs	Yes

IV. PROJECT SUMMARY

TABLE V: COMPARISON OF THE PROPOSED LDO DESIGN WITH [1]–[3]

Parameters	Design in [1]	Design in [2]	Design in [3]	This Work
Technology (μm)	0.5	0.35	0.35	0.35
Input Supply Voltage (V)	3.3	2.0 ~5.5	2.0 ~ 3.3	2.0
Nominal DC Output Voltage (V)	2.8	1.8	1.8	1.8
Dropout Voltage V_{do} (V)	0.5	0.2	0.2	≤ 0.2
Maximum Load Current (mA)	100	200	10	200
Quiescent Current (μA)	25.	20	0.68.	29.3
Current Efficiency (%)	99.75	99.84	99.99	99.82
Output Voltage Variation (mV)	100	54	3	≤ 70
Load Step (Up / Down) Recovery Time (μs)	25 / 75	27 / 30	25 / 50	2.5/2.0
Phase Margin (Worst Case) (degrees)	60	65	57	62.7
Load Capacitor (μF)	2.2	1	1	2
ESR Zero Required	Yes	No	No	Yes

In this project, a design of low-drop regulator circuit for application in portable devices has been proposed and analyzed, by using 0.35μm TSMC CMOS process and Cadence Spectre simulation platform. The detailed comparison of this work with three previously reported designs in [1]-[3] is provided in Table V. Some key comments are worth mentioning. To begin with, this design utilizes the same CMOS process and produces identical nominal DC output voltage as the designs in [2] and [3], and the dropout voltage is less than 0.2V. In addition, the maximum load capability of this work is significantly higher than the designs in [1] and [3] and equivalent to that in [2], with minor increase in overall quiescent current. As a result, the current efficiency of the proposed circuit is over 99.8% hence the power efficiency under 2V supply voltage is very close to 90%. Moreover, the output voltage variation of this work under maximum load step change is less than 70mV, which is slightly higher than the design in [2] and much lower than that in [1]. For the design in [3], the extremely small variation (3mV) is mainly owing to its limited load current capability (10mA). Furthermore, the recovery time under load step change in this work is much shorter ($\leq 2.5\mu s$) compared to those in [1] – [3], which are all greater than 25μs. Besides, the worst-case phase margin of this design, similar to those in [1] and [2], is greater than 60 degrees, which guarantees stability of the circuit and fast output transient response in full range of load current. Finally, like the design in [1], the ESR zero is required in this work to assist stabilizing the whole circuit, with an output capacitor of 2μF which is less than 3μF specification.

On the other hand, several issues exhibit in this design, such as huge dimension of pass transistor, large output capacitor, and also reliance on ESR zero for system stability. For further improvements of the circuit's configuration and performance, more efforts should be devoted to optimize the feedback mechanism of the circuit, and, if possible, achieving the stability status with smaller output capacitor and without relying on ESR zero.

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