A gm/ID based design of high PSR low dropout regulator for SoC applications

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A g_m/I_D based Design of High PSR Low dropout Regulator for SoC Applications

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***Abstract*—A design methodology by including the finite PSR of the error amplifier to improve the low frequency PSR of the Low dropout regulator with improved voltage subtractor circuit is proposed. The g_m/I_D method based on exploiting the all regions of operation of the MOS transistor is utilized for the design of LDO regulator. The PSR of the LDO regulator is better than -50dB up to 10MHz frequency for the load currents up to 20mA with 0.15V drop-out voltage. A comparison is made between different schematics of the LDO regulator and proposed methodology for the LDO regulator with improved voltage subtractor circuit. Low frequency PSR of the regulator can be significantly improved with proposed methodology.**

I. Introduction

In a complete system on chip (SoC) solution, digital, sensitive analog and power management blocks are integrated on a single chip. A SoC solution, performs many functions which demands high-power with respect to the clock. Noise because of these digital switchings incur substantial fluctuations in the supply which in turn effects the performance of sensitve analog blocks. In a power management system a switching power converter (SWPC) is followed by a low drop-out (LDO) voltage regulator to provide isolation between the noisy SWPC output and the sensitive analog blocks. Due to the increase in operating frequencies, SWPC are operated at higher frequencies for fast transient response and to allow the use of smaller passive components to reduce area and cost [1]. At these operating frequencies, ripples appear at the output of the SWPC. So LDO regulator should have high power supply rejection (PSR) up to the switching frequencies in SoC applications.

Different techniques have been presented in the literature to improve the PSR of the LDO regulator up to higher frequency. LDO regulator with voltage subtractor stage [2] is one among them which utilizes a diode-connected transistor to drive the gate of the series pass device. But the low frequency PSR can be enhanced only by increasing the open loop gain which will be at an expense of power consumption. Low frequency PSR of the LDO regulator in [2] can be enhanced by adding an additional transistor which provides an additional path for the supply ripples to the gate of the pass device as explained in [3]. But analysis in [3] ignores the finite PSR of the error amplifier which may have significant effect on low frequency PSR of the LDO regulator. A feed-forward ripple cancellation technique was used in [4] to achieve better PSR up to 10MHz. Compared to a simple ordinary LDO, the LDO in [4] uses five on-chip resistors and three amplifiers including the error amplifier which consumes large area.

In deep sub-micron technologies, design of a complex analog circuit utilizing the traditional design techniques much deviate from specifications because long channel approximations are not valid for short channel devices. Second-Order effects has to be incorporated to attain reasonable accuracy in simulations. The g_m/I_D design method that is a unified synthesis method which utilizes all regions of operation of the MOS transistor [5]. A better speed-power compromise can be obtained when the transistors operate in moderate inversion region. This method provides a way to operate the transistor in different regions. In this method, relation between the g_m/I_D ratio and the normalized drain current $I_D/(W/L)$ is utilized as a fundamental design tool to explore the design space.

In this paper, a new design methodology is proposed to improve the low frequency PSR of LDO regulator with improved voltage subtractor stage to achieve a PSR better than -50dB up to 10MHz. In Section II, the g_m/I_D design method and its main features are explored. The complete PSR analysis of LDO regulator with improved voltage subtractor stage and the explanation of proposed design methodology is presented in section III. In Section IV, transistor level implementation of the regulator and comparison of simulation results between different schematics in [2], [3] and proposed methodology using g_m/I_D based design method is presented. Conclusions are provided in section V.

II. The g_m/I_D Method

In this method, the relation between the g_m/I_D ratio and the normalized drain current $I_{NOR} = I_D/(W/L)$ is utilized as a design tool. The choice of g_m/I_D ratio is due the following reasons [5].

1) It is related to the performances of analog circuits.
2) It provides the information regarding the device operating region.
3) It is utilized as a tool for calculating the transistor dimensions.

To illustrate this, consider the common source stage consists of a single input transistor, which is loaded by a current source load (transistor delivering a dc current I_D). We call g_m the small-signal trans-conductance and λ, channel length

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modulation parameter and the transistor small-signal output conductance g_{ds}, where g_{ds} =λ I_D.
The dc gain (A_0) and transition frequency (f_t) are given by

$$A_0 = \frac{-g_m}{I_D(\lambda_n + \lambda_p)} \quad (1)$$

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})} \quad (2)$$

The g_m/I_D ratio is a measure of the efficiency to translate current into trans-conductance i.e., greater will be the trans-conductance at a constant current for large g_m/I_D value. So, the g_m/I_D ratio is interpreted as a measure of a " trans-conductance generation efficiency " [6].

The g_m/I_D ratio is equal to the derivative of the logarithmic of I_D with respect to V_{GS} as shown in (3)

$$\frac{g_m}{I_D} = \frac{1}{I_D} * \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial log(I_D)}{\partial V_{GS}} = \frac{\partial log(I_D/(W/L))}{\partial V_{GS}} \quad (3)$$

The dependence of drain current (I_D) on V_{GS} is exponential in weak inversion while it exhibits quadratic dependence in moderate inversion and almost linear in strong inversion region of the transistor. So the above derivative is maximum in weak inversion region. The maximum value of g_m/I_D ratio is equal to 1/(η V_T) where η is the sub-threshold slope factor and V_T is the thermal voltage (27 mV). The g_m/I_D ratio decreases as the operating region changes from weak inversion to strong inversion region as shown in Fig. 1. Therefore, the g_m/I_D ratio signifies the transistor operating region.

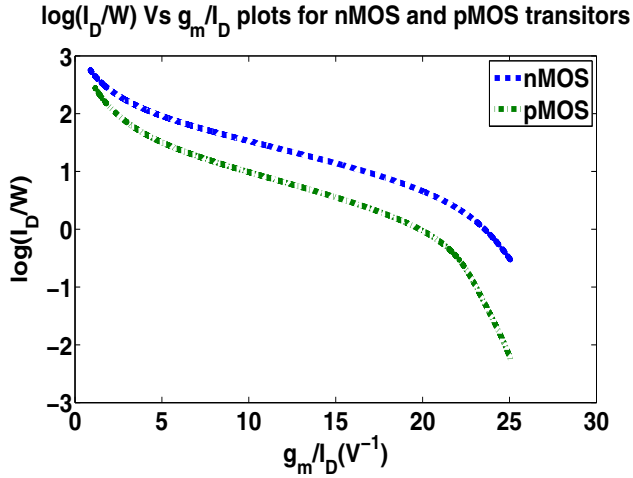

Fig. 1. log($I_D/(W)$) Vs g_m/I_D for nMOS and pMOS transistors

The normalized current I_{NOR} and the g_m/I_D ratio are independent of the transistor sizes. Therefore, the relationship between g_m/I_D and I_{NOR} exhibits a unique characteristic for all transistors of a specific type (nMOS or pMOS) for a particular technology.

The " unique " characteristics of the I_{NOR} versus g_m/I_D curve can be utilized during the design exploration, when the transistor dimensions (W/L) are unknown. Once a pair of values among g_m/I_D, g_m, or I_D has been derived from the specifications, the W/L of the transistor can be determined from pre-generated plots of particular technology. Fig. 1 shows the simulated plots of $log(I_{NOR})$ versus g_m/I_D for nMOS and pMOS transistors. Fig. 2 shows the simulated plots of $log(f_t)$ versus g_m/I_D for nMOS and pMOS transistors. The difference in I_{NOR} versus g_m/I_D for nMOS and pMOS transistors is because of difference in the mobility.

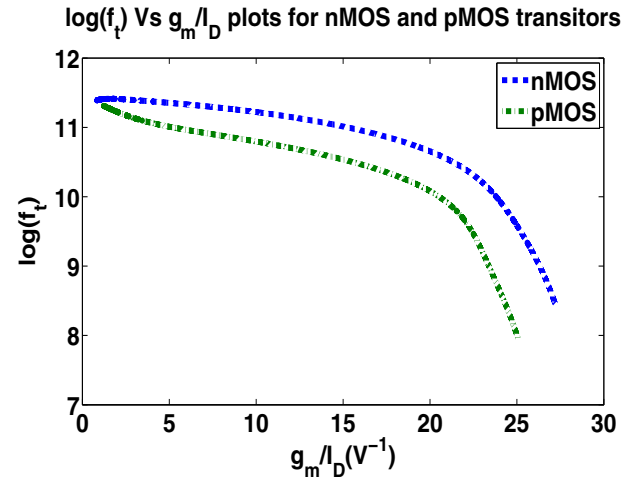

Fig. 2. log(f_t) Vs g_m/I_D for nMOS and pMOS transistors

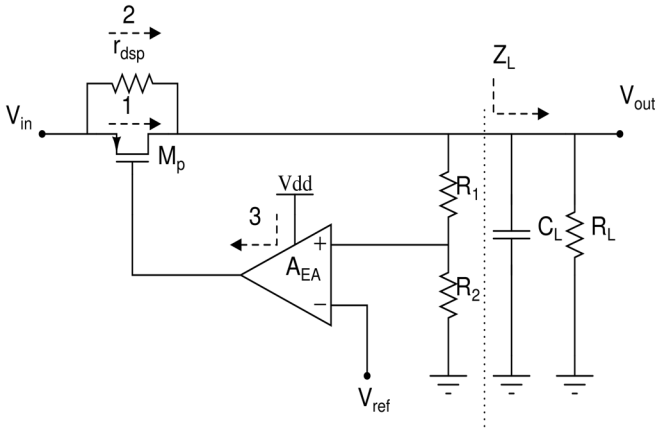

Fig. 3. Feed through of supply ripples in conventional LDO

III. PSR ANALYSIS

Finite PSR of the LDO regulator is due to the feed through of supply ripples from the input to the output through various paths. Path 1 is due to the trans-conductance of the series pass device, due to the finite output conductance (g_{dsp}) in path 2 which is significant in present technologies and path 3 is because of finite PSR of the error amplifier as shown in Fig. 3 [4]. To achieve better PSR for an LDO regulator depends on ripples at the gate of the pass transistor. The ripples appearing at the input of the LDO should be replicated at the gate of the pass transistor in order to cancel the feed through. Hence, the gate-overdrive voltage is independent

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of the input ripple. The basic idea to improve the PSR is shown in the Fig. 4, the circuit in the dashed box represents a voltage subtractor circuit. The difference between ripples through input and error amplifier is fed to the gate of the pass transistor. From Fig. 4, it is obvious that a high PSR error amplifier is utilized in order to improve the low frequency PSR of the LDO regulator. For this kind of LDO topologies, ground referenced error amplifiers are used [7].

In the actual case, part of the ripples feed through the finite output resistance (r_{dsp}) of pass transistor (M_P), and that also should be removed [4]. This can be done by increasing the ripple amplitude appearing at the gate of pass transistor to cancel the ripples that leak through r_{dsp}. So provide an additional path for the supply ripples to the gate of the pass transistor. In addition to the diode-connected transistor M_2 that was used as a voltage subtractor in [2] , another transistor M_3 acting as an adaptive current source providing an additional path for the input ripples to the pass transistor gate [3]. Finite power supply ripple rejection of the error amplifier have significant effect on the PSR of the utilized LDO topology. So low frequency PSR can be further improved by providing additional ripples through M_3.

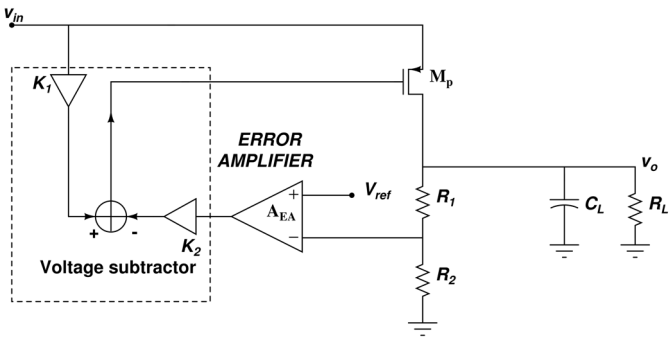

Fig. 4. Basic idea to improve the PSR of an LDO regulator

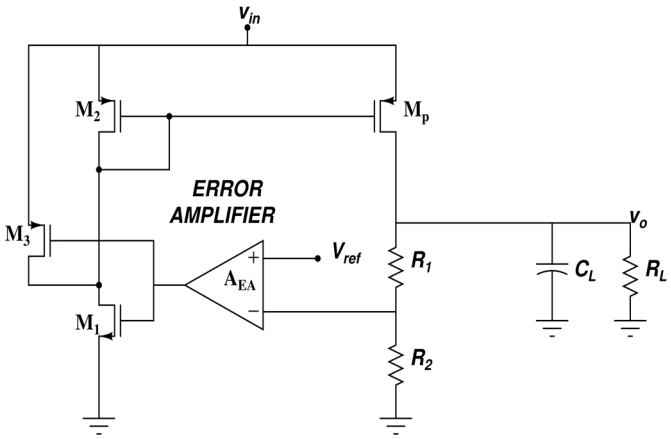

Fig. 5. Utilized LDO topology

PSR of utilized LDO

In this section, a design methodology is proposed for the design of LDO regulator in [3] by including the finite PSR of the error amplifier. The small signal model of the utilized LDO is shown in Fig. 6. g_{m1},g_{m2},g_{m3} and g_{mp} represent the trans-conductance of M_1,M_2,M_3 and M_p transistors respectively. g_{ds1},g_{ds3} and g_{dsp} represents the output conductance of M_1,M_3 and M_p transistors respectively. R_1 and R_2 are the feedback resistors, feedback factor (β) is defined as R_2/(R_1+R_2). A_{EA} represents the DC gain of the error amplifier. R_L and C_L are the load resistance and capacitance. PSR of LDO regulator can be represented as the ratio of v_{out} and v_{in}.

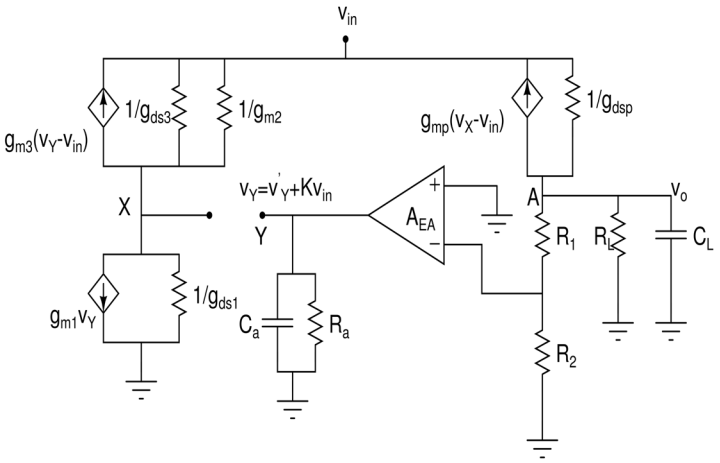

Fig. 6. Small signal model of Utilized LDO

At node X:

$$(v_x - v_{in})(g_{ds3} + g_{m2}) + g_{m3}(v_y - v_{in}) + v_x.g_{ds1} + g_{m1}.v_y = 0 \quad (4)$$

At node A:

$$(v_0 - v_{in})g_{dsp} + g_{mp}(v_x - v_{in}) + v_0 Y_L + \frac{v_0}{(R_1 + R_2)} = 0 \quad (5)$$

where Y_L is the reciprocal of impedance at output node.

$$v_y = v_y^{'} + K v_{in} \quad (6)$$

where K is supply gain factor and

$$v_y^{'} = \frac{-\beta v_0 A_{EA}}{(1 + sR_aC_a)} \quad (7)$$

neglecting g_{ds1} with respect to g_{m2} and g_{ds3} and solving Eq. (4),(5),(6) and (7) we can get

$$\frac{v_0}{v_{in}} = \frac{\left(g_{dsp} - \frac{g_{mp}g_{m3}}{g_{m2} + g_{ds3}} + K.\frac{g_{mp}(g_{m1} + g_{m3})}{g_{m2} + g_{ds3}}\right)}{\left(Y_L + g_{dsp} + \frac{(g_{m1} + g_{m3})}{g_{m2} + g_{ds3}}.\frac{\beta g_{mp} A_{EA}}{(1 + sR_aC_a)}\right)} \quad (8)$$

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LDO DC open loop gain A_{ol} is give by

$$A_{ol} = \frac{g_{m1} + g_{m3}}{g_{m2} + g_{ds3}} . \frac{g_{mp}}{G_L + g_{dsp}} . \beta A_{EA} \tag{9}$$

Now defining A_0 as

$$A_0 = \frac{\left(g_{dsp} - \frac{g_{mp} g_{m3}}{g_{m2} + g_{ds3}} + K . \frac{g_{mp}(g_{m1} + g_{m3})}{g_{m2} + g_{ds3}} \right)}{(G_L + g_{dsp})} \tag{10}$$

Now for PSR at DC:

$$\left(\frac{v_0}{v_{in}} \right)_{DC} = \frac{A_0}{1 + A_{ol}} \tag{11}$$

$$\left(\frac{v_0}{v_{in}} \right)_{DC} = \frac{\left(1 - \frac{g_{mp} r_{dsp} g_{m3}}{g_{m2} + g_{ds3}} + K \frac{g_{mp} r_{dsp} (g_{m1} + g_{m2})}{g_{ds3} + g_{m2}} \right)}{\left(1 + \frac{r_{dsp}}{R_L} \right) (1 + A_{ol})} \tag{12}$$

PSR of the utilized LDO regulator can significantly enhanced if the numerator in Eq (12) is set as close as possible to zero. In case of having only the diode-connected transistor M_2 as in [2], PSR at DC is given by

$$\left(\frac{v_0}{v_{in}} \right)_{DC} = \frac{1}{\left(1 + \frac{r_{dsp}}{R_L} \right) (1 + A_{ol})} \tag{13}$$

Above equation doesn't consider the supply gain of the error amplifier. PSR at DC can be enhanced only by improving the open loop gain A_{ol} which requires additional gain stages at an expense of power consumption.
In case of utilized LDO topology in [3], PSR at DC is:

$$\left(\frac{v_0}{v_{in}} \right)_{DC} = \frac{\left(1 - \frac{g_{mp} r_{dsp} g_{m3}}{g_{m2} + g_{ds3}} \right)}{\left(1 + \frac{r_{dsp}}{R_L} \right) (1 + A_{ol})} \tag{14}$$

From Eq (14) the PSR at DC can be significantly enhanced by making the numerator much closer to zero. In that work, supply gain the error amplifier is neglected, but power supply rejection of error amplifier has significant effect on the PSR of the utilized topology as shown in Eq (12). So low frequency PSR of the utilized LDO regulator can be enhanced by providing additional ripples through M_3 to cancel the feed through from error amplifier.

IV. Transistor level implementation and simulation results of LDO regulator

In this section, transistor level implementation of LDO regulator with improved voltage subtractor circuit using TSMC 0.18μm CMOS process is presented as shown in Fig. 7. The main specifications for which LDO regulator designed is listed in Table I. Transistors $M_4 - M_8$ forms a simple differential amplifier, M_P series pass transistor, R_1, R_2 are the feedback resistors and C_L, R_L are the load capacitance and resistance.

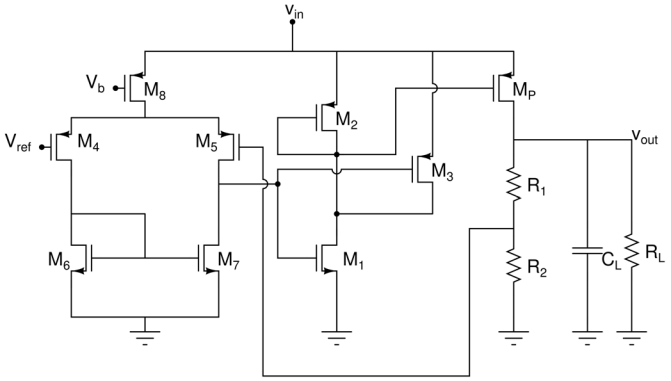

Fig. 7. Transistor level design of LDO with improved voltage subtractor

TABLE I
LDO specifications

	Specifications	
$Technology$	μm	0.18
$Inputvoltage(V_{in})$	V	$\geq$ 1.65
$Outputvoltage(V_{out})$	V	1.5
$Dropoutvoltage(V_{drop})$	V	$\leq$ 0.15
I_{Lmax}	mA	20
V_{ref}	V	0.42

A. Step by step design procedure

1) From dropout voltage (V_{drop}) specification, $V_{drop} \approx V_{dsat} \approx 0.15V$

$$\left(\frac{g_m}{I_D} \right)_P = \frac{2}{V_{drop}} = 13.33V^{-1}$$

choose L = 0.36μm to reduce the gate capacitance associated with the pass transistor.
From the I_D/W Vs g_m/I_D plot for L = 0.36μm,

$$\implies W_P \approx 10.722mm$$

2) Design of the transistors M_2 is as follows,
To ensure proper current mirroring, $(g_m/I_D)_P = (g_m/I_D)_2$ From the I_D/W Vs g_m/I_D plot for L = 0.36μm,

$$\implies W_P \approx 107.22\mu m$$

3) Choose $(g_m/I_D)_1$ = 13.33 V^{-1}, this will ensure that, no additional gain is provided by the voltage subtractor stage which may degrade phase margin. From I_D/W Vs g_m/I_D plot,

$$\implies W_1 \approx 26.093\mu m$$

4) According to the proposed design methodology, from Eq (12) make numerator as close as possible to zero, finite PSR factor (K) of the error amplifier is 0.00752, substitute the above small signal parameters in Eq.(12),

$$\implies V_{dsat} = (V_{GS})_3 - V_{th3} \approx 0.83V$$

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From above g_m/I_D value and g_{m3} value, I_{D3} can be calculated as 41.1 μA. From I_D/W Vs g_m/I_D plot W_3 can be calculated as

$$\left(\frac{g_m}{I_D}\right)_3 = 2.3V^{-1}$$

$$\implies W_3 \approx 0.9141\mu m$$

5) Design of the ground referenced error amplifier for the specifications of GBW $\geq 20MHz$, gain $\geq 30dB$ and ICMR 0.25 - 0.95 V
For input transistors M_4 and M_5: From GBW specification, choose $(g_m/I_D)_4 = 9.031V^{-1}$. From $\log(I_{NOR})$ Vs (g_m/I_D) plot, $\log(I_{NOR})$ = 0.3154 $\implies$ W_4= 55 μm
For tail current source M_8: From ICMR specification [8], choose $(g_m/I_D)_8 = 10.53V^{-1}$. From $\log(I_{NOR})$ Vs (g_m/I_D) plot, $W_8 \approx 150\mu m$.
For Load transistors M_6 and M_7: From ICMR specification, choose $(g_m/I_D)_6 = 7.518V^{-1}$. From $\log(I_{NOR})$ Vs (g_m/I_D) plot, $\log(I_{NOR})$ = 0.9123 $\implies$ $W_6 \approx 9.18\mu m$.

Simulation results for the PSR of the utilized LDO regulator using LTspice tool is as shown in the Fig. 8, here we can see that PSR is above -50dB up to few MHz. LDO regulator

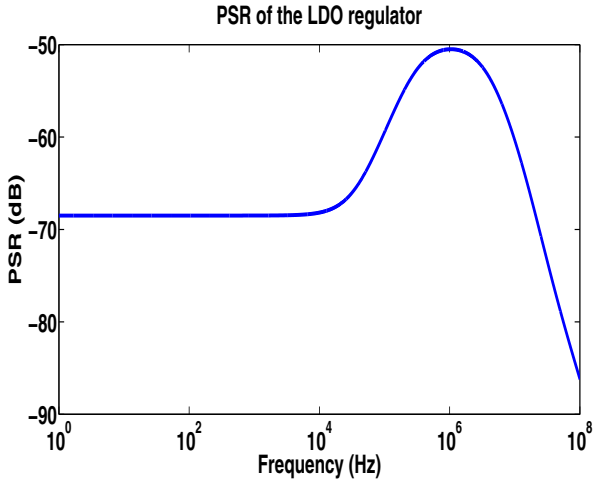

Fig. 8. Simulation result for PSR of the LDO utilizing the proposed methodology

is simulated for a voltage subtractor circuit as shown in [2], by adding M_3 transistor without considering the PSR of the error amplifier as shown in [3] and using the above proposed methodology as explained in Eq (12). From Fig. 9, proposed design methodology shows the significant improvement in the low frequency PSR.

Table II shows the comparison between the proposed methodology and results of the different schematics shown as in [2], [3]. From the simulation results, consider the supply gain of the error amplifier to achieve a better PSR while using the LDO topology in [3]. Using the proposed design methodology,

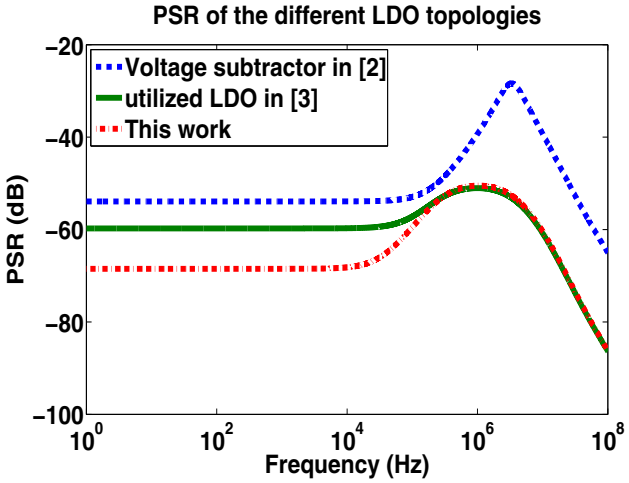

Fig. 9. Simulation result for PSR of different LDO topologies

TABLE II
UTILIZED LDO RESULTS

	units	[1][1]	[2][2]	this work
$Technology$	μm	0.18	0.18	0.18
$Inputvoltage(V_{in})$	V	$\geq$ 1.65	$\geq$ 1.65	$\geq$ 1.65
$Outputvoltage(V_{out})$	V	1.5	1.5	1.5
$Dropoutvoltage(V_{drop})$	V	$\geq$ 0.15	$\geq$ 0.15	$\geq$ 0.15
I_{Lmax}	mA	20	20	20
I_Q^3	μA	351	371	391
$PSR@DC$	dB	-53.9	-59.76	-68.52
$PSR@1MHz$	dB	-39.3	-51.03	-50.5
$PSR@4MHz$	dB	-29.1	-53.99	-53.5
$loadregulation$	(mV/mA)	0.43	0.42	0.36
$lineregulation$	(V/V)	0.0032	0.0022	0.0015

[1] designed accroding to [2]
[2] designed accroding to [3].
[3] excluding the biasing circuits.

a low PSR error amplifier can be used to achieve a better low frequency PSR for the utilized LDO regulator.

B. Effect of ESR and ESL on PSR performance

The large output capacitance (C_L) of 3 μF is used at the output node to achieve better phase margin and pole-zero cancellation in PSR expression as explained in [3]. Large capacitance is associated with effective series resistance (ESR) and effective series inductance (ESL). After the frequency (f_{LC}), capacitor behaves like an inductor and increases its impedance with frequency. PSR of the LDO regulator degrades as the impedance of the capacitor increases as explained in [7]. PSR starts degrading at lower frequencies when compared with PSR of the LDO regulator without ESR and ESL. PSR simulation results of the LDO regulator by including the ESR ($\approx 5m\Omega$) and ESL ($\approx 0.75nH$) of the C_L is shown in Fig. 10.

C. Layout of LDO regulator

Final layout of the LDO regulator using the proposed design methodology is laid out using TSMC 0.18μm CMOS process as shown in Fig. 11 using Electric VLSI tool.

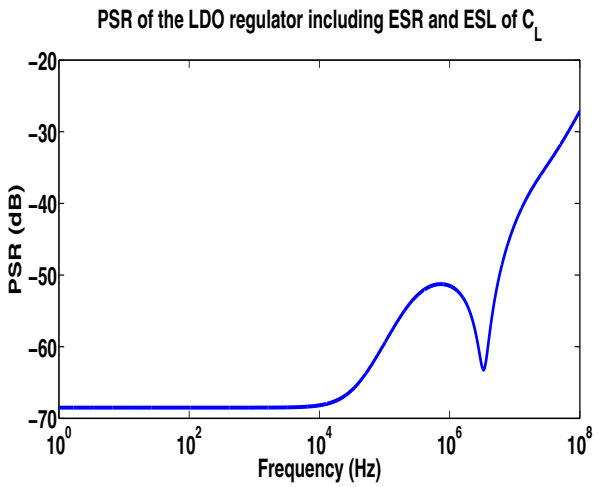

Fig. 10. PSR of the LDO regulator including ESR and ESL of C_L

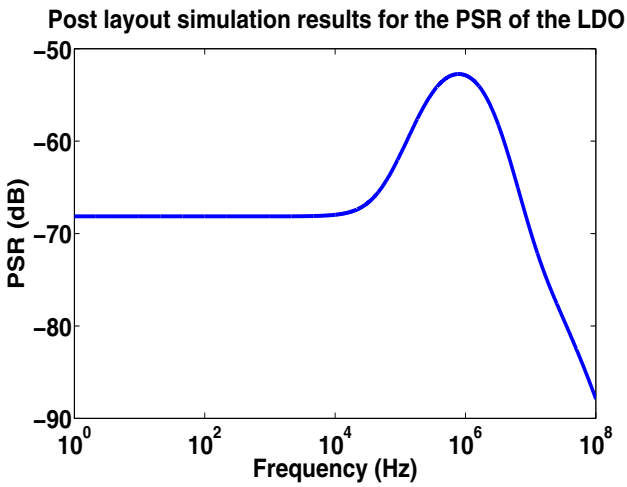

Fig. 12. Post layout simulation results for the PSR of LDO regulator

Simulation results for the PSR of the LDO regulator is shown in the Fig. 12. Small variation in the low frequency PSR is due to the parasitic resistances and small variation in the device sizes.

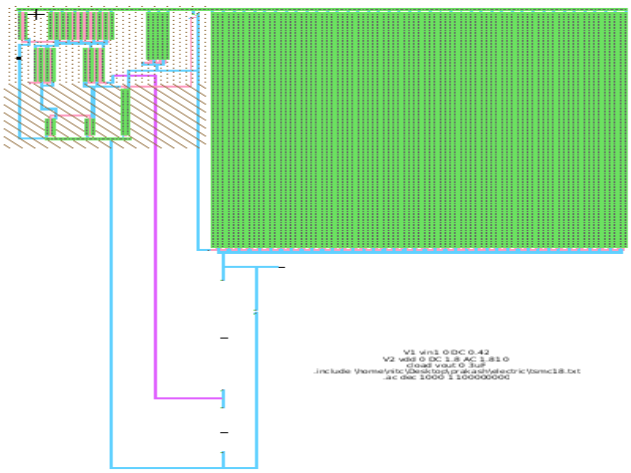

Fig. 11. Final LDO layout

V. Conclusion

In this paper, a design methodology is proposed by considering the finite PSR of the error amplifier to improve the low frequency PSR of the LDO regulator with improved voltage subtractor stage. At higher frequencies, PSR degrades because of ESR and ESL of the C_L. From the simulation results, PSR of this LDO regulator is observed to be above -50dB up to 10MHz, hence these LDO regulators are suitable for SoC applications. A design methodology known as g_m/I_D method, which utilizes few pre-generated plots and less number of iterations to calculate the transistor dimensions of the LDO regulator.

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