

## Design and Implementation of CMOS Telescopic Op-Amp for Bio-Medical Applications

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**Abstract** - Operational Amplifiers (Op-Amps) are the basic integral part of all analog VLSI designs and mixed VLSI designs. For bio-medical applications, the Op-Amp with higher common mode voltage and low noise is essential to evaluate qualitatively the electrocardiogram (ECG) signal and electroencephalography (EEG) signal in the diagnosis process for more accurate treatment of patients. Medical instruments with qualitative signals help the doctors to efficiently reduce the time in the diagnosis process. Generally folded cascode Op-Amp find uses in many of the applications, but it has heavy current consumption to achieve the required transconductance (gm), it is noisier and consumes more power. There is a need for an Op-Amp with less power, less noise and more gm. Folded cascode Op-Amp can be replaced with telescopic Op-Amp at the output stage to enhance the common mode input voltage. Telescopic circuits require half of the supply current as that of folded cascode circuit to obtain the same amount of peak current output and transconductance, with much reduced noise in telescopic Op-Amp. As this configuration takes lower currents, the speed of operation increases. Our work reported here concentrates on the design of higher gain and high slew rate Op-Amp, which would be able to measure bio-medical signals like ECG, EEG etc with higher clarity. The Op-amp is able to produce a gain of 81dB, Phase Margin greater than 450, improved Unity Gain Bandwidth (UGB) of 4.03MHz, with a power less than 190μW. The design can be implemented with 0.18μm CMOS technology with 1.8V power supply. The cadence virtuoso tools were used for this design.

**Keywords** - Op-amp, Bio-potentials, ADCs, 2 Stage Op-Amp design, Folded Cascode op-amp, telescopic

### I. INTRODUCTION

Bio-potential signals can be defined as the electrical signals which are running over the human body to activate and control number of activities in the human biological system. In bio-medical instruments, bio-potential amplifier is the key block that amplifies the weak bio-potential signals such as ECG, EEG, etc signals to the level of that can be analyzed perfectly and can be used by the physician [1]. These signals are supposed to not to distorted the quality due to any noise during the acquisition process. The bio-potentials have embedded dc-offsets known as Differential Electrode Offset (DEO), due to the distinction in the half cell potentials of the electrodes participated in signal acquisition, and the signals are filtered out before or during the acquisition process to avoid saturating the bio-potential amplifier [9]. Amplifier should selectively amplify the only portion of bio-potential signal of interest while the rest of the portion and the signals should be capable to attenuate. Electromagnetic and electrostatic interferences from the mains of buildings are sources of signal noise in bio-potential acquisition process. When an alternating current (AC) flows through the conductor, an electromagnetic field (EMF) would be established around the conductor, and this EMF cuts across the loop of conductors to generate electromotive force (e.m.f), this is the principle of generator.

The similar effect occurs when the main's current of a building generates an EMF and field in turn cuts through the loop formed by the human body, the leads between the electrodes and the input of the bio-potential amplifier, and the bio potential amplifier itself [8] as shown in fig.1.

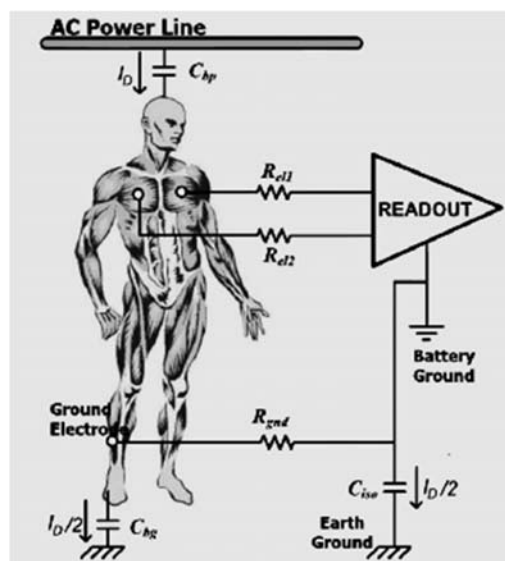


Fig.1: Electrostatic Interference to Human Body

Hence the unwanted AC signal has been generated, and is same for both the inputs of bio-potential amplifier. On the other hand, unwanted interference can be produced due to electrostatic effects. In the fig.1, Cbp is the capacitance between the mains and the human body, Cbg capacitance exists in between device body and the real ground.

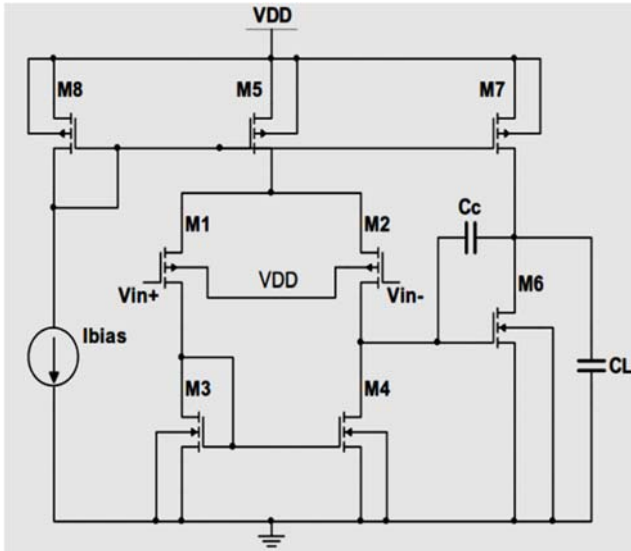


Fig.2: Basic Two stage Op-Amp[11]

Ciso is the capacitance between the circuit ground and the earth. Re1 and Re2 are the circuit leads resistances [10]. Displacement current,  $I_D$ , flows into the body through the capacitances and splits about equally between the isolation capacitance and the body to ground capacitance. The Potential drop has been established as the result of the current across the ground resistance, defined as a common mode signal at the amplifier's inputs. This problem motivates towards the design of a telescopic Op-Amp which can be able to speed up the process with higher quality. Few types of OTA based designs to assess the bio-medical signals have been presented in [4] with 109.07  $\mu\text{W}$  static power and 1.2 V supply voltage, in [2] with 198.6 nW static power and 0.6 V voltage supply and in [3] with 6.7  $\mu\text{W}$  power dissipation from 1.8 V voltage supply. Most of the amplifier designers were concentrated on low power only. Low power Programmable amplifier with low noise has been discussed in [6], produces static power of 140  $\mu\text{W}$  and noise of 2nV/radic Hz in 0.35 $\mu\text{m}$  technology with 3.5V supply.

## II. CURRENT WORK

Basic two stage Op-Amp circuit diagram has been presented in the fig.2, and the device scaling procedure is presented. There are different types of Op-Amp cascode configurations like simple cascode configuration, multi level cascode configuration, gain boosted cascode configuration and folded cascode configuration. This section describes

about the existing literature about the two stage conventional Op-Amp design concepts, and also the folded cascode (FC) concepts and the design routes [5]. The basic folded configuration has presented in the fig.3 and the model large signal characteristics presented in fig.4.

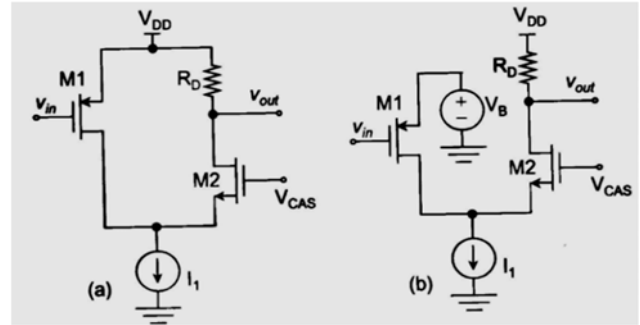


Fig.3: Folded Cascode Amplifier (FCA) concept [12]

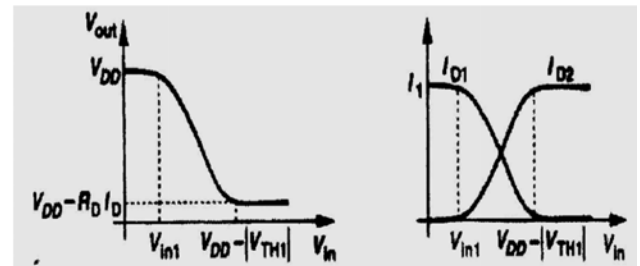


Fig.4: FCA Large Signal Characteristics [12]

Single stage amplifier produces the gain as in eq.1 without using cascode concept, and when the folded cascode concept is added its gain, the gain would as in eq.2:

$$A_v = g_m \times r_o \quad (1)$$

$$A_v = (g_m \times r_o)^2 \quad (2)$$

Two stage folded cascode Op-Amp: Traditional FC Op-Amp configuration has been presented in the fig.5.

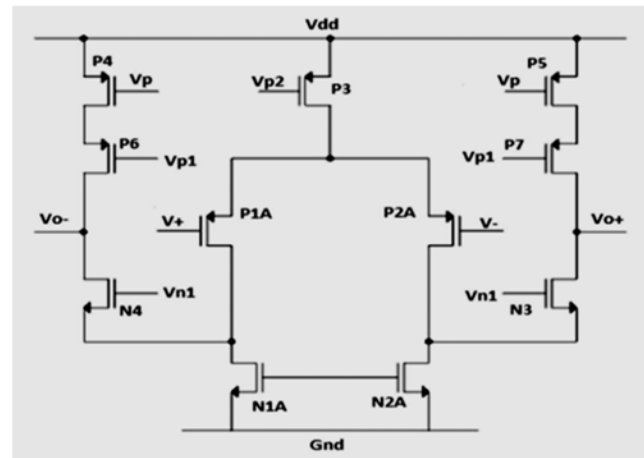


Fig.5: Conventional folded cascode [14]

Like differential amplifier, the folded cascode configuration doesn't demand the exact matching of the currents since the extra current can flow in or outward of the current mirror circuits. With the FC concept, the second-order effects can be minimized. Using structure can optimize second-order performance indicator. In conventional cascode configuration, as the input transistors and cascode transistors are stacked jointly, the bias current can be mutually delivered, although the bias current (ISS) fed to the input devices only in FC [12]. There are few benefits from the folded concept, better input common mode range (ICMR), self compensation, output common mode range is decoupled from the ICMR and higher voltage swings. FC Op-amp gain is usually lower than the traditional cascode Op-Amp due to low impedance devices are in parallel. A two stage FC Op-Amp is pictured in the fig.6.

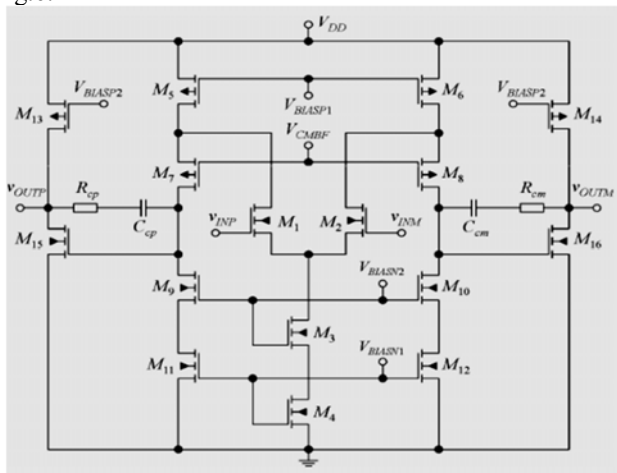


Fig 6: Two stage folded cascode Op-Amp

A single current source implemented using cascode technique is enough to drive the amplifier. Higher output voltage swing against the common-mode level sensitivity to the device mismatches can be made possible with the folded topology. In FC amplifier, the output stage is push-pull type hence it can either sink or source the load. The FC configuration consumes more static power than the conventional designs. Many CMOS ICs are designed to drive the capacitive loads, hence the folded amplifiers operate on the capacitive loads. Hence the Op-Amp design for gain and slew rates more than the conventional Op-Amps is the basic requirement, and can be achieved only with capacitive loads, and the voltage buffer is not necessarily required to accomplish lower output impedance.

Moreover, this configuration has a pole at the folding junction, which is far below compared to the pole at the node in the conventional cascode configuration. This is due to the possible existence of more parasitic capacitance in this structure. The benefit of this low folding pole is to improve the sufficient phase margin (PM) consequently achieves self-compensate with this structure. The compensation in the

Op-Amp is usually achieved by the amount of load capacitance added. Thus, whenever, the load capacitance rises, then the Op-Amp's stable rises. Whenever, there is a node at the Op-Amp's output with high impedance that can perfectly drive the capacitive loads, hence the performance of the Op-Amp would be improved. Admittance and transconductance of Op-Amp are equal magnitudes, hence they have less impedance [16]. The Setback in folded amplifiers is that the current runs in the third branch and the pole location at the folding node.

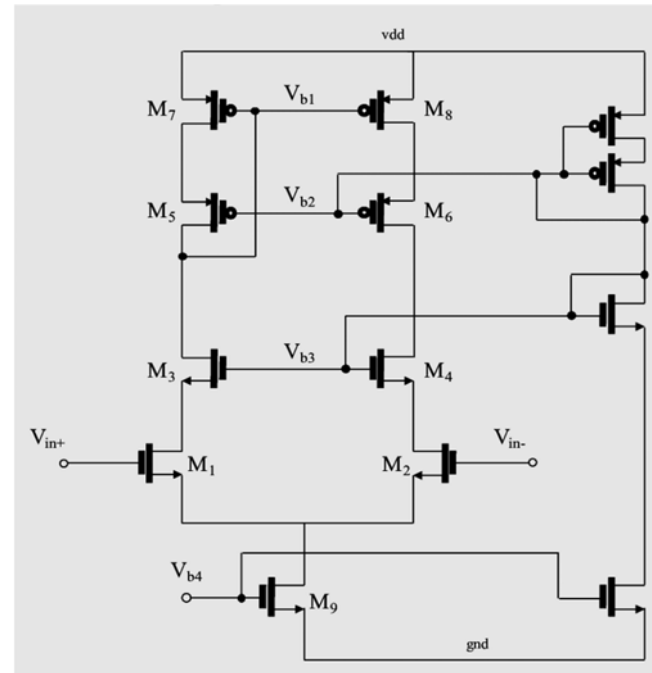


Fig.7: Two stage telescopic Op-Amp

FC Op-Amp has an important feature, which permits the level of input common mode voltage to be very near to the power supply voltage range. NMOS input, forces the gate pole of common-mode level towards VDD, and PMOS input, moves it towards ground. In comparison to conventional Op-Amp configuration, the folded configuration has higher amount of gain and a pole, which causes the Op-Amp results higher voltage swing at the output. Since, when compared to the two-stage or multi-stage amplifiers, a single pole amplifier has a benefit of having higher PM thereby improved stability. An added advantage of this amplifier is the huge small signal gain, and is more suitable for the deep negative feedback [15]. The concept of folded configuration benefit is that the boosting of cascode amplifier output voltage swing. As pictured in the fig.6, the input transistors are folded either to VDD or ground in this Op-Amp circuit. Moreover at the folding node, two tail current sources have been connected. Due to these tail current sources' overdriven potential, the voltage swing of folded amplifier is higher, but the gain is significantly low as compared to the telescopic amplifier.

The most vital parameter of present day transistor is its trans-conductance. Hence, the modern Op-Amps are known as trans-conductor Op-Amp or operational trans-conductance amplifier (OTA). FC Op-Amps, compared to the normal amplifiers, have a bigger output voltage swing. With the comparatively massive output swing, the input and output may be short circuited, and it makes easier for choice of input common-mode level. As the FC doesn't have the current source, the voltage swing difference of ' $V_{Dsat}$ ' between the two, but compared to telescopic it will have more noise, because of the folded legs. FC configuration has been wide applications.

### III. DESIGN METODOLOGY

Telescopic (TC) amplifiers are more stable and less noise compared to the folded amplifiers. Generally, in TC configurations, loads are tail current sources ( $V_{Dsat}$ ) which are used to keep it in the saturation. As the loads are tail currents, there is a limited input and output swings in contrast to the folded concept. Hence, there is a negative voltage swing as a function of input common mode. There is one dominant pole hence the stability is relatively more. In the telescopic designs, the speed is higher than the speed in the folded design, but the major short come is the maintaining the required swing when the telescopic is designed for low potentials. FC configuration has been wide applications than the telescopic structure.

**Two Stage Telescopic Op-Amps:** A gain boosted TC amplifier has presented in [7] SMIC 0.35 $\mu$ m technology with 3.3V power supply, and resulted a maximum DC gain of 128dB and 161 MHz unity gain frequency. A two-sage TC Op-Amp circuit is shown in the fig.7. The Op-Amp with vastly different levels of complexity is used to realize functions ranging from dc bias generation to high-speed amplification or filtering. Stage-1– Useful for noise disposal, requires level interpretation to the second stage, and degrades the Miller compensation. Stage-2- For self compensating, to build the proficiency of the Miller compensation, and expands power supply rejection ratio (PSRR). In a situation where the normal mode input voltage extend require not be huge, for example in an inverting mode integrator, FC output stage may be replaced with a TC cascode configuration. The adaptive Op-Amp just needs a supply current which is halved of the folded configuration required for a similar most extreme output current and gm appeared as in the fig 6. In addition, the additional noise and offset of the additional current sources in the FC arrange are absent here. A weakness is that the lowest supply voltage level requires is higher than that of the folded variant required. The low supply voltage ruled out the stacking of multiple cascode to meet the high gain specifications. This, along with the high slew rate required for low settling times, strongly suggested that the use of a 2-stage Op-Amp topology to reduce the gain constraint per stage. This also allows the optimization of the first stage for gain and the

stage-2 for high slew rate and output swing. The low noise spec suggests that the attempt to minimize the use of number of components could act as the noise sources. This, alongside the genuinely tolerant output swing spec, would be best met with a single-ended topology.

Inside these confinements, just a bunch of standard designs are plausible for the first stage (high gain) of the Op-Amp. For the primary stage a simple TC stage has been considered, and for the second stage, a simple common source stage with sufficient slew rate is enough if is biased with about 50uA current source, hence, more complex Class A and Class AB driving stages are unnecessary. The resulting topology is a single-ended TC Op-Amp which drives a common source configured output stage. The schematic circuit of both the configurations has been presented in the figures, fig.8 and fig.9. The design procedure of the two stage configuration is depicted below

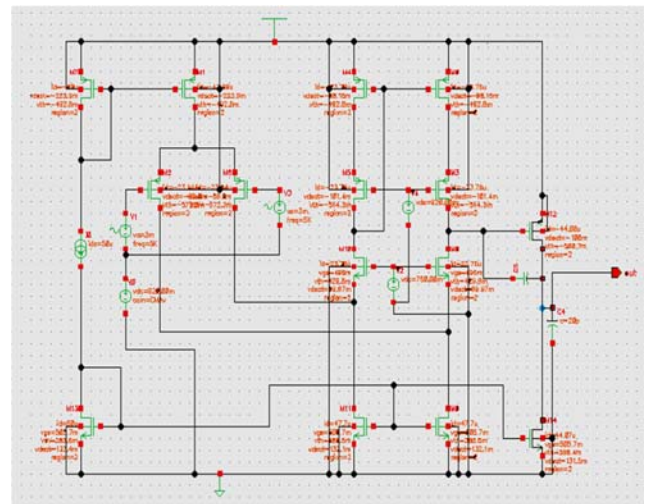


Fig 8: Two stage folded cascode Op-Amp

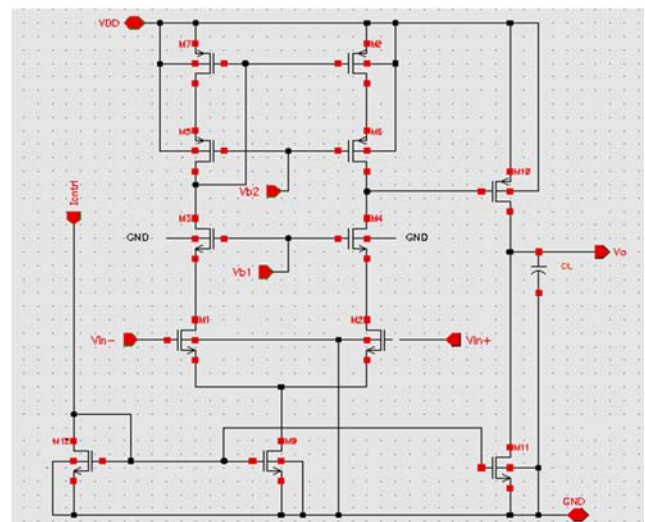


Fig.9: proposed Two stage telescopic Op-Amp

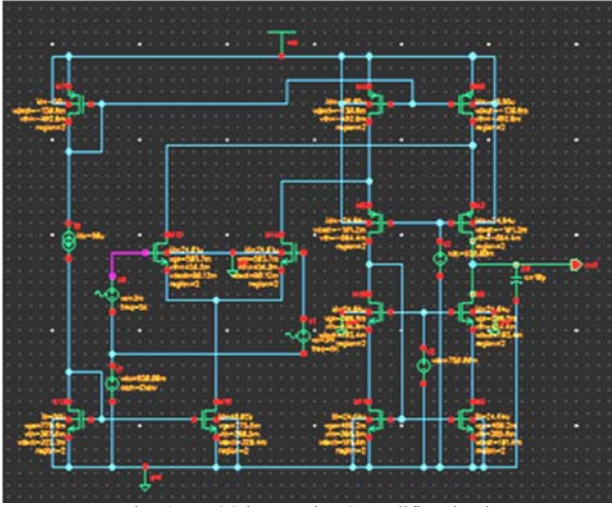


Fig.10 NMOS input pair FC amplifier circuit

**Power Consumption and Maximizing Slew Rate:** Fro the specs provided, 200  $\mu$ W of power and 1.8V supply, assume that the total 100  $\mu$ A current allocated between the biasing circuit and the two stages. Gain and Transistor Length: Usually, in the design all the transistors are in equal sizes except the transistors in biasing circuit. Size of the devices can be optimized based on the amplifier gain requirement, and at the same time circuit run time also important parameter. Since the circuit DC gain is expressed as in eq.3.

$$A_v \approx \frac{1}{2} (g_{m1} r_{o1} \times g_{m3} r_{o3} \times g_{m10} r_{o10}) \quad (3)$$

**Transistor Width and Trans-conductance:** The transistor trans-conductance gain is mainly depends on the transistor width as the length of the device is fixed for a particular technology. Hence by approximating the VDS of particular set of transistors, different optimizations can be made between gm and W, gm and ro, fT and ID and W for the specific operating point. After number of iterations, the VDS for transistors 10 and 11 can be chosen VDS10=0.2V and VDS11=0.1V in the second stage. In first stage, VDS1 = VDS3=100mV and VDS5 = VDS7 =150mV, and assume the  $C_c \approx 15pF$ . The required unity-gain bandwidth is approximately 10MHz. This produced the relation:

$$\begin{aligned} W_1 &= 2\pi \times 10M \approx g_{m2} C_c \\ \therefore g_{m1} &= g_{m2} = g_{m3} = g_{m4} \approx 314.16\mu S \\ g_{m5} &= g_{m6} \approx 600\mu S \end{aligned} \quad (4)$$

#### i) Stage-1 Calculations

- $I_1 = SR \times C_L$
- Bias currents:  $I_{11}$  &  $I_9$  are to be considered as 1.2 to 1.5 times of  $I_1$  so as to keep away from the zero currents at  $I_{10}$  &  $I_8$  branches.

- Aspect Ratios, W/L,  $S_9 = S_{11} = \frac{2I_{11}}{K'N \times V_{DS,S_{11}}^2}$ ,

$$S_{10} = S_8 = \frac{2I_{10}}{K'N \times V_{DS,S_{10}}^2}, \quad S_5 = S_3 = \frac{2I_5}{K'N \times V_{DS,S_5}^2}$$

$$S_4 = S_0 = \frac{2I_4}{K'N \times V_{DS,S_4}^2}, \quad S_2 = S_6 = \frac{GB^2 \times C_L^2}{K'P \times I_1}$$

- The total Power Dissipation,  $P_D = V_{DD}(I_4 + I_1 + I_0)$

- $S_{10} = S_8 = S_{13} = S_{11} = S_9 = \frac{2 \times 65\mu}{300\mu \times 0.15 \times 0.15} = 19.26$

$$\therefore W = 19.26\mu, \quad L = 1\mu$$

$$V_{OV} = \frac{V_{DD} - V_{out\max}}{2} \text{ And is } 0.15V \text{ for worst}$$

case current flow condition

- $S_0 = S_4 = S_3 = S_5 = \frac{2 \times 65\mu}{60\mu \times 0.15 \times 0.15} = 96.3$  ;

$$\therefore W = 96.3\mu \text{ \& } L = 1\mu \text{ here } V_{OV} = \frac{V_{out\min} - V_{DD}}{2}$$

- $S_2 = S_6 = \frac{(20\pi \times 10^6)^2 (10^{-11})^2}{3000 \times 10^{-12}} = 96.3$  ;

$$\therefore W = 92.02\mu \text{ \& } L = 0.7\mu$$

- $S_7 = S_1 = \frac{2 \times 50\mu}{60\mu \times 0.24 \times 0.24} = 29$  ;  $\therefore W = 29\mu$

$$\text{ \& } L = 1\mu$$

#### ii) Stage-2 Calculations

- $S_{10} = S_{14}$

- $S_{12} = \frac{2I_{11}}{K'P \times V_{DS,S_{11}}^2} = \frac{100\mu}{60\mu \times 0.12 \times 0.12} = 115.74$

$$\therefore W = 81\mu \text{ \& } L = 0.7\mu$$

#### iii) Miller Compensation

- $C_c = (2C_{gd3} + C_{db3}) + (2C_{gd8} + C_{db8}) + (2C_{gs12})$

- where  $C_{gdn} = 2CGDOn * Wn$  \&  $C_{gdp} = 2CGDOp * Wp$

- similarly  $C_{gsn} = 2CGSOn * Wn$  \&  $C_{gsp} = 2CGSOp * Wp$

- $C_{dbn} = C_{jwl} + C_{jsw} (Wn +$



$2Ls)$  and  $Cdbp = Cjwl + Cjsw (Wp + 2Ls)$

- $Cjswln = 1.03 * 10^{-9}$  –  
3 ;  $Cjswlp = 1.14 * 10^{-9}$  – 3
- $Cjswn = 134pF$  ;  $Cjswp = 174pF$
- $Cdbn = ((1.03 * 10^{-9})(19.26u)) + (134pF(19.6u + 2u)) = 0.0226pF$
- $Cdbp = ((1.14 * 10^{-9})(96.3u)) + (174pF(96.3u + 2u)) = 0.126pF$
- $Cc = (2(2(235pF) * 19.26u) + 0.023pF) + (2(2(205.4pF) * 96.3u) + 0.16pF) +$

$$(2(2(05.4pF)80u)) = 0.311pF$$

#### iv) Load Capacitance for Two Stage Folded Cascade Op-Amp

- $CL = (2Cgdn12 + Cdbn12) + (2Cgdp14 + Cdbp14)$
- $CL = ((4 * 235pF * 19.26u) + 0.0226pF) + ((4 * 205pF * 80u) + 0.059pF) = 0.1653pF$

The optimized design sizes of all the transistors after tuning to meet the given specifications based on the above analytical approach are listed in the table 1.

TABLE I. OBSERVATIONS FROM THEORETICAL TO PRACTICAL

Transistors	ID (μA)		V <sub>ov</sub> (overdrive)		g <sub>m</sub> (μ)		GBP	
	Theory	Practical	Theory	Practical	Theory	Practical	Theory	Practical
M4,M5,M6,M9	50	41.01	0.2	0.178	-	-	5MHz	3.05MHz
M0,M3	50	41.01	0.3	0.296	341	246.2		
M8,M2	50	41.01	0.3	0.28	341	316		
M7	100	82.02	0.4	0.4	-	-		

#### IV. SIMULATION RESULTS AND DISCUSSIONS

Single stage and two stage Conventional, folded cascade and telescopic amplifiers have been designed in 0.18μm CMOS technology, and simulated using Cadence virtuoso tools. The results are presented in this section.

i) Single stage FCA: Single FCA designed, its transient response for the input voltage V<sub>DS</sub> =1.8V and frequency 5kHz frequency simulation results are shown in the fig.11, the magnitude and phase plots from the AC analysis are presented in the fig.12 and the power plot is in fig.13.

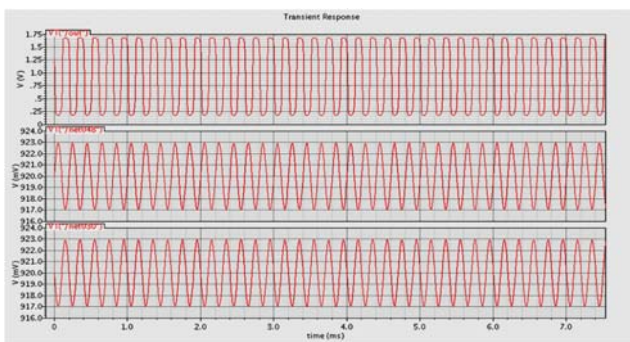


Fig.11: Single stage FCA transient response

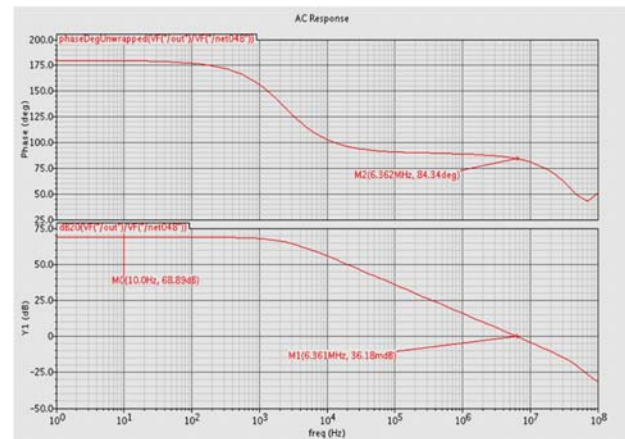


Fig.12. Single stage FCA AC response

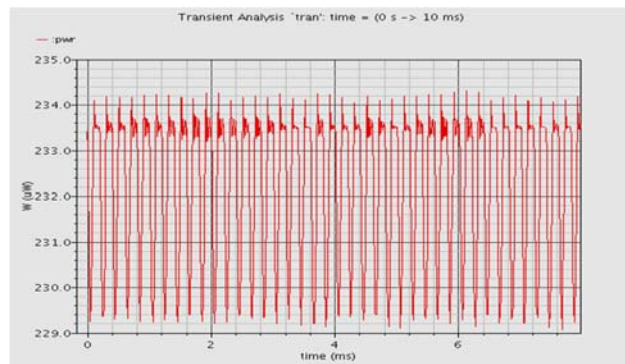


Fig.13: Single stage FCA power plot around 231μW

From the results, it is observed that the  $GM=68.89\text{dB}$ ,  $PM=84.340$  and  $GBP=6.36\text{MHz}$ . The input noise  $=0.00140797$  and output noise  $=3.40002e-7$ . From the dB plot of CMRR for the single stage FC Op-Amp with  $V_{ov}$  of  $0.15\text{V}$  for all other MOSFETs rather than input pair. The static power is  $231\mu\text{W}$ , the input supply voltage  $=1.8\text{V}$  and output voltage swing is  $1.0\text{V}$

ii) Two Stage FC Op-Amp: The two stage FC op-amp transient response for the  $V_{DS}=1.8\text{V}$  and  $5\text{kHz}$  frequency simulation results are shown in the fig.10, the magnitude and phase plots from the AC analysis are presented in the fig.14 and fig.15.

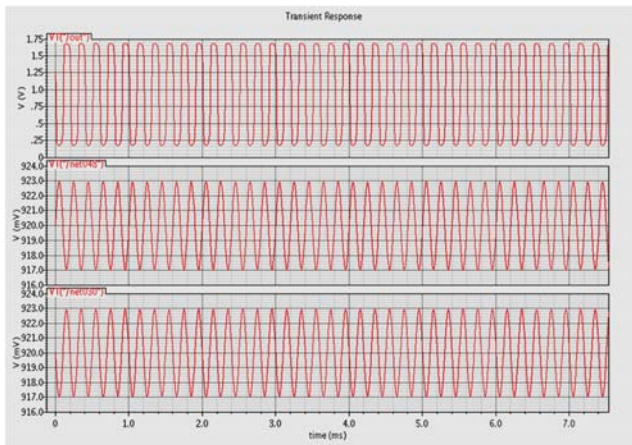


Fig 14: Transient response

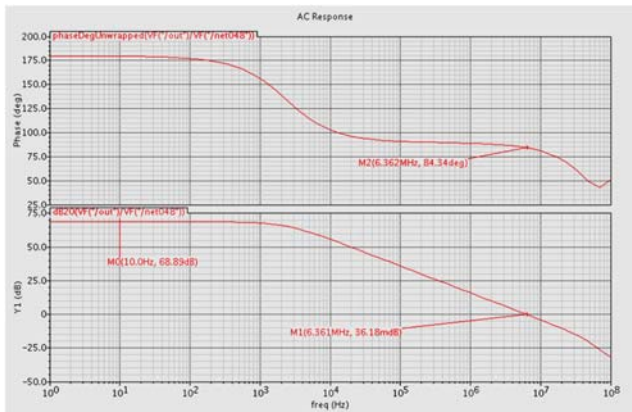


Fig 15: AC Response and Phase Plot

From the graphs, the following results are observed.  $GM=68.89\text{dB}$ ,  $PM=84.40$  and  $UGB=6.35\text{MHz}$ . The CMRR is  $98.3\text{dB}$  which is a better value for an Op-Amp. The total Power consumption of this design is  $0.32\text{mW}$ . For the input voltage  $1.8\text{V}$  the maximum output swing is  $1.45\text{V}$ .

iii) NMOS input pair FCA with  $0.15\text{V}$  overdrive for all MOSFETs: The two stage FCA with NMOS input pair shown in the fig.10 simulation results are presented in figures fig.16 and fig.17.

From the above results it is observed that this FCA produces the  $GM=69.5\text{dB}$ ,  $PM=84.850$  and  $GBP=6.56\text{MHz}$ . For the input supply voltage  $1.8\text{V}$  produces the maximum output swing  $1.21\text{V}$ , and for the input noise  $=0.00158096$  and output noise is  $1.73436e-7$ . From the dB plot, the CMRR is observed as  $108.3\text{dB}$ . The static Power of this circuit is  $243\mu\text{W}$ .

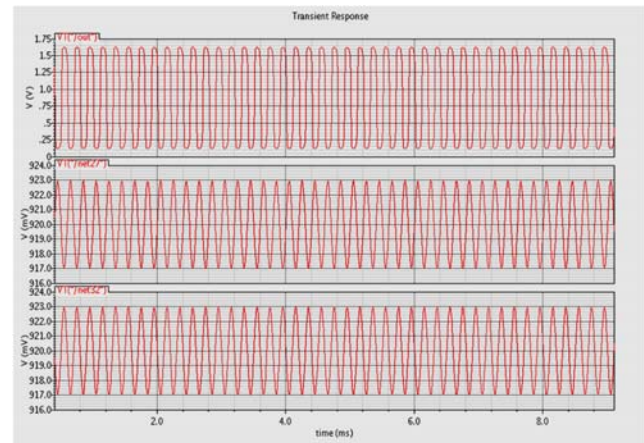


Fig.16: Transient Response

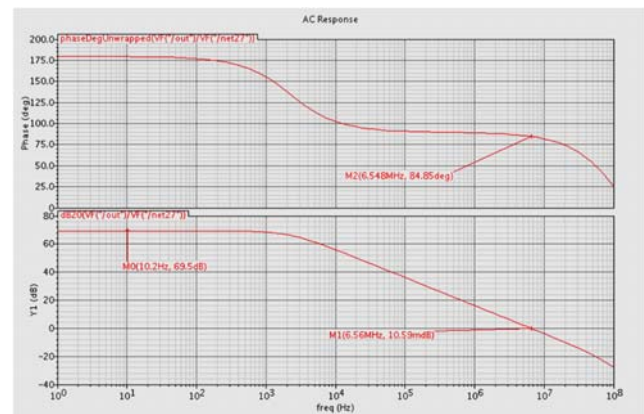


Fig.17: AC analysis

iv) Two stage FC Op-Amp with miller compensation: The two stage FCA with miller compensation circuit results are presented in the figures fig.16, fig.17, fig.18 and fig.19. From the graphs and the following results observed.  $GM=87.57\text{dB}$ ,  $PM=50.40$  and  $UGB=835.5\text{KHz}$ . The input and output noises are  $0.00136472$  and  $2.97865e-08$  respectively. The CMRR is  $104.3\text{dB}$  which is a better value for an Op-Amp. The total Power consumption of this design is  $0.32\text{mW}$ . For the input voltage  $2\text{V}$  the maximum output swing is  $1.5\text{V}$



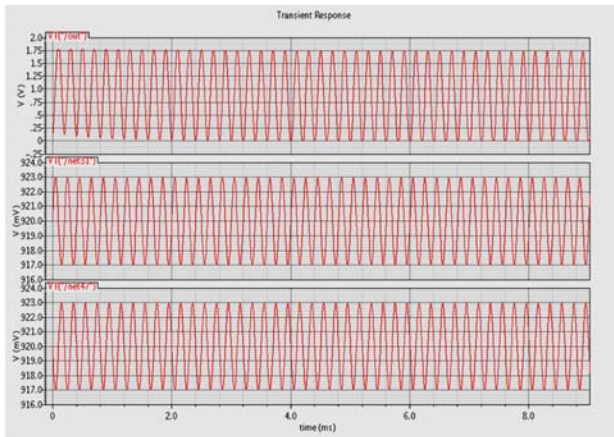


Fig.18: Two stage FCA Transient response

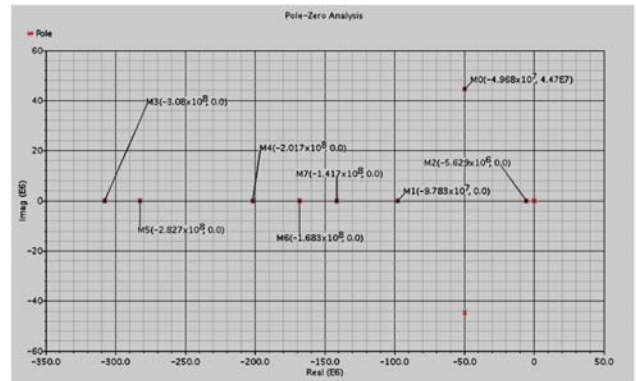


Fig.21: Pole analysis of two stage FCA for stability

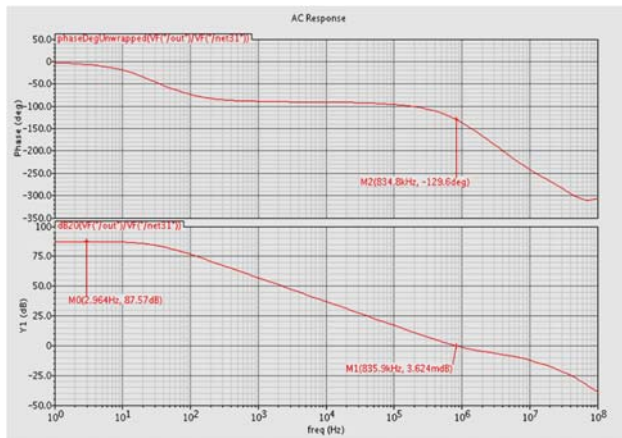


Fig.19: AC response plot

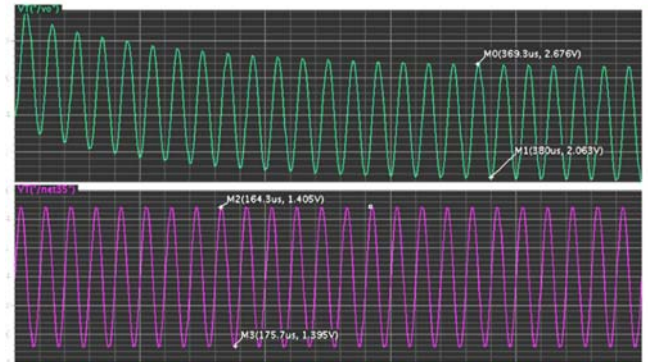


Fig.22 Transient response for single stage TC amplifier

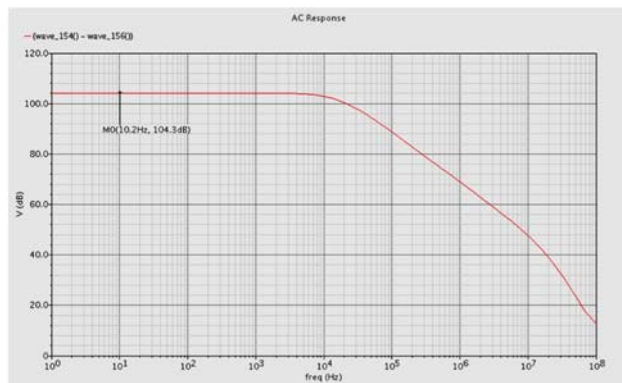


Fig.20: dB plot for CMRR

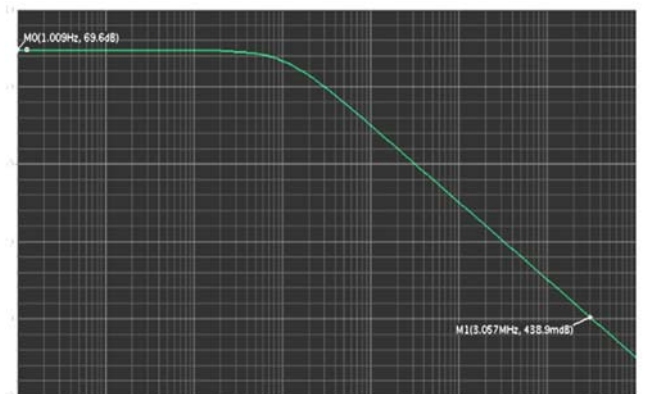


Fig.23 AC analysis with gain in dB and UGB in MHz

v) Single Stage Telescopic Op-Amp: Single stage telescopic amplifier designed, its transient response for the  $V_{DS} = 2.8V$  and 5kHz frequency simulation results are shown in the fig.22, the magnitude and phase plots from the AC analysis are presented in the fig.23 and fig.24.



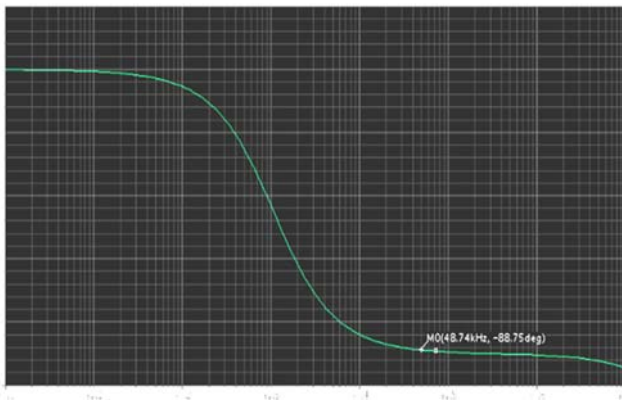


Fig.24 TC amplifier Phase margin in degrees

From these results it can be observed that the GM and PM of the proposed TC amplifier are All MOSFETs are said to operate only in saturation region.  $I_D$  observed as  $82.02\mu A$ . Gain of 69.64 dB is observed with UGB 3.057MHz from dB plot. For the 2.8V input voltage, the maximum output voltage swing is 1.4V.

vi)Two Stage Telescopic Op-Amp: the two stage telescopic Op-Amp transient response for the  $V_{DS}=2V$  and frequency=5kHz, the simulation results are shown in the fig.25, the magnitude and phase plots from the AC analysis to get the PM and GM are presented in the fig.26 and fig.27.

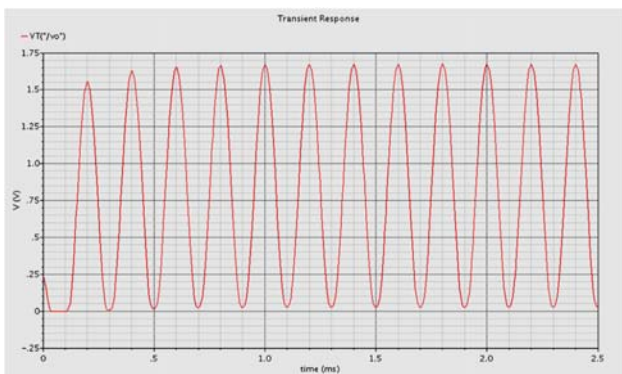


Fig.25: two stage TC Amp transient response

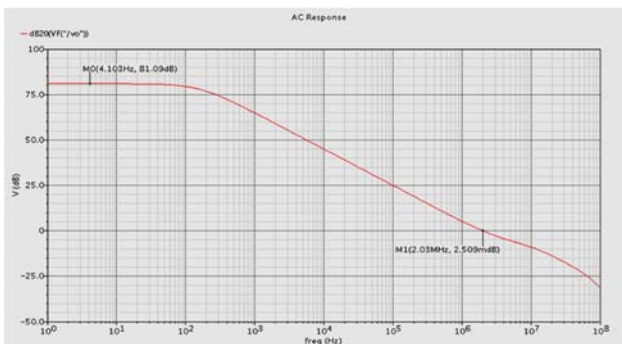


Fig.26: Magnitude plot for GM with UGB

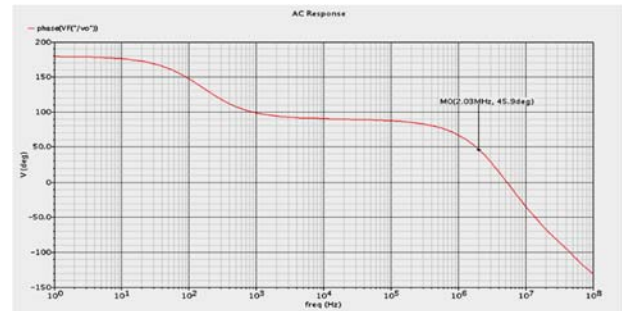


Fig 27: Phase plot for PM and UGB

From the comparison results of TC amplifier with all other FC with and without compensation, gain boosting methods etc are presented in the table II, after the references section. From these, it can be seen that the gain and phase margins of the proposed TC amplifier and GM is greater than 80dB, PM > 450 along with UGB of 6.03MHz. The static power is as low as  $<143\mu W$  and High CMRR of 128.4dB.

## V. CONCLUSION

In this paper, a two-stage TC Op-Amp design procedure of has been presented, disused merits against the two-stage FC configuration. From the results, it is observed that, the TC configuration is more useful with respect to the GM and PM, low power consumption and noise and finally more slew rate. For biomedical applications, high gain and low noise are the most important parameters, hence telescopic Op-Amp is preferred.

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TABLE II: DESIGN RESULTS OF BOTH THE OP-AMPS

Parameter	Spec.	Design[1]	gain boosted FC [14]	Two stage FC[13]	2 stage FC without compensation	2 stage FC with overdrive	2 stage FC with miller comp	Proposed Telescopic
Technology, ( $\mu$ m)	0.18	0.09	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage, V	1.8	1.2	1.8	3.3	1.8	1.8	1.8	1.8
Open Loop Gain (dB)	60-80	72.9	81	96.29	68.89	69.5	87.57	84.34
Phase Margin (degree)	45-60	42	45.9	83.5	84.4	84.85	50.4	68.89
Gain Bandwidth, MHz	2.03	3.12	2.03	1.21	6.35	6.56	835kHz	6.36
Slew Rate, V/ $\mu$ sec	0.02	103	0.02	123	92.2	105	71	0.01
Output Swing, V	1.34 V	0.82	1.34	1.22	1.45	1.21	1.5	1.625
CMRR, dB	>100	47.9	66.1	82.6	98.3	108.3	104.3	128.4
Power Consumption, $\mu$ W	190	63.73	197	220	320	243	320	143