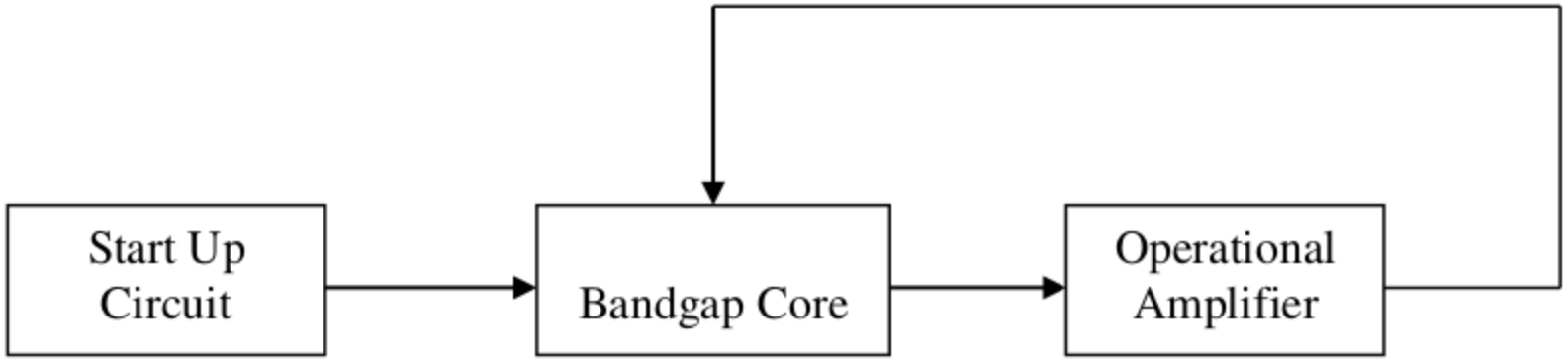
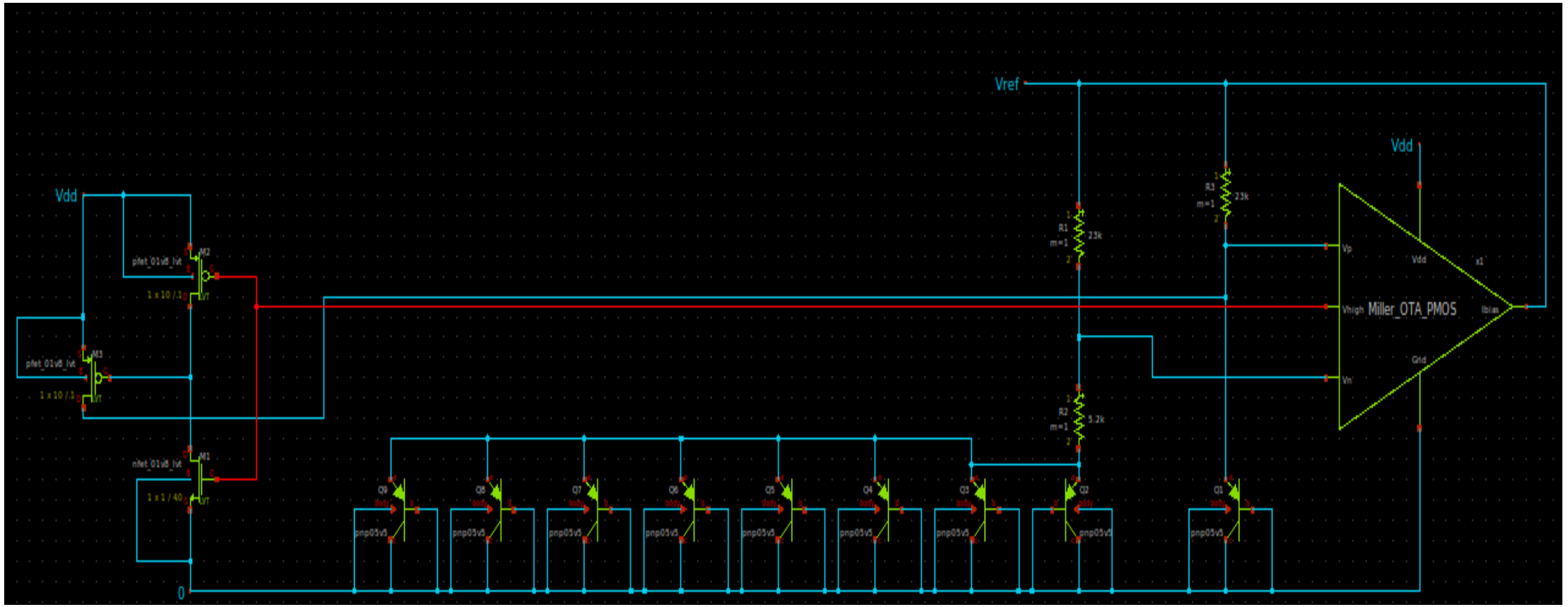
Bandgap Design

Proposed Band-gap Design

The block diagram of the circuit is given below:



Design of BGR using 1.8v supply



Proposed Band-gap Design
1- Band-gap core analysis

- $VR2 = I2 \times R2$

$= ((VBE2 - VBE1) / R3) \times R2$

$= VT \ln(n) \times (R2 / R3)$

$= VT \ln(8) \times (R2/R3)$

Where: [n = 8 for our circuit] and $VT=KT/q$.

- VR2 is a positive TC which is 1.94 mV/°C for the BJT's used in this circuit.

- Vout =Vref= VR2 + VBE2, thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).

2- Band-gap core analysis

Vref = a1 VR2 + a2 VBE = const. => dVref/dT = a1 dVR2/dT + a2 dVBE/dT = 0

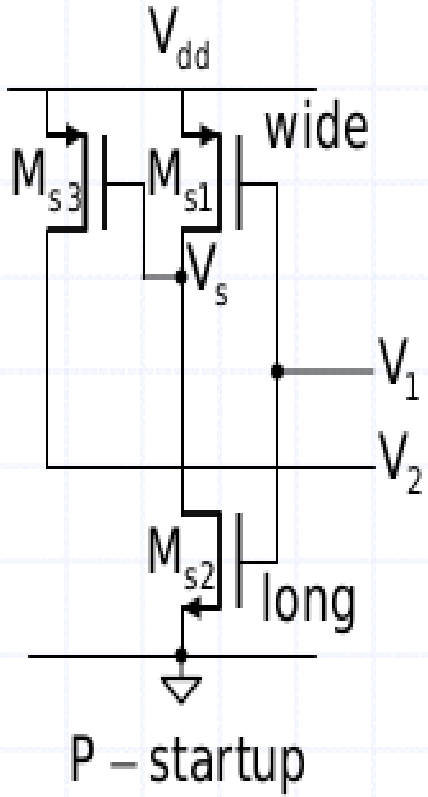
So a1(85uv/k) - a2(1.6mv/k) = 0

Since CTAT slope is greater than PTAT slope we will make a2=1 and vary a1 to make PTAT slope increasing to reach CTAT slope:

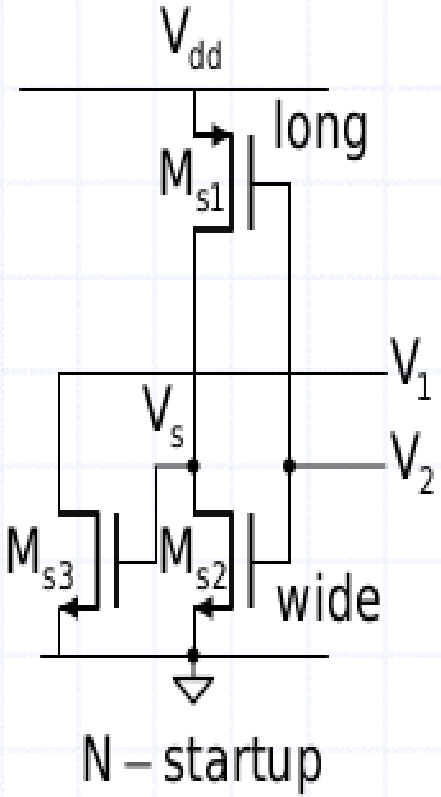
So a1=1.6m/85u => a1=19 = (R2/R1)*ln(8)

Let I=30uA then R1=VTln(8)/I = 2k ohm and R2= a1R1/ln(8) = 18k

Proposed Band-gap Design
2- Start-up Circuit schemes



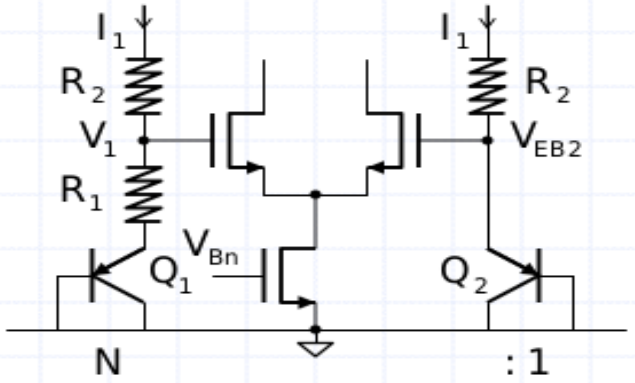
P – startup



N – startup

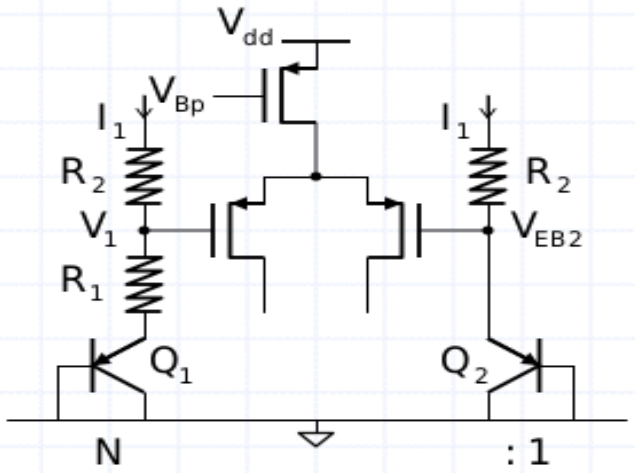
3- Choosing input stage of OTA

Let the gate overdrive voltage be $V_{gsn}-V_{tn} = |V_{gsp}|-|V_{tp}| = V_{ov}$.



For NMOS input, we need
$V_{EB2} > V_{tn} + 2V_{ov}$

V_{EB2} ranges from 0.5V to 0.7V
$\Rightarrow V_{tn} < 0.2V$
$\Rightarrow$ too tough to be satisfied



For PMOS input, we need
$V_{dd} > V_{EB2} + |V_{tp}| + 2V_{ov}$

For V_{EB}=0.64V, $|V_{tp}|$=0.44V, V_{ov}=0.15V
$\Rightarrow V_{dd}(min) = 1.38V.$

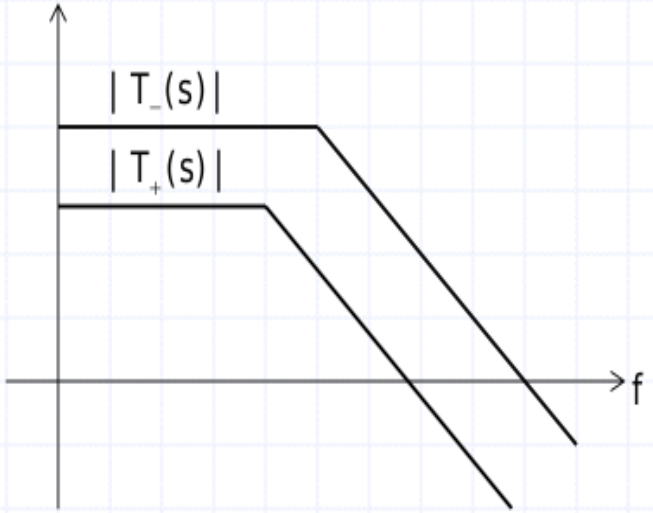
4- Stability of Bandgap

Negative feedback loop:

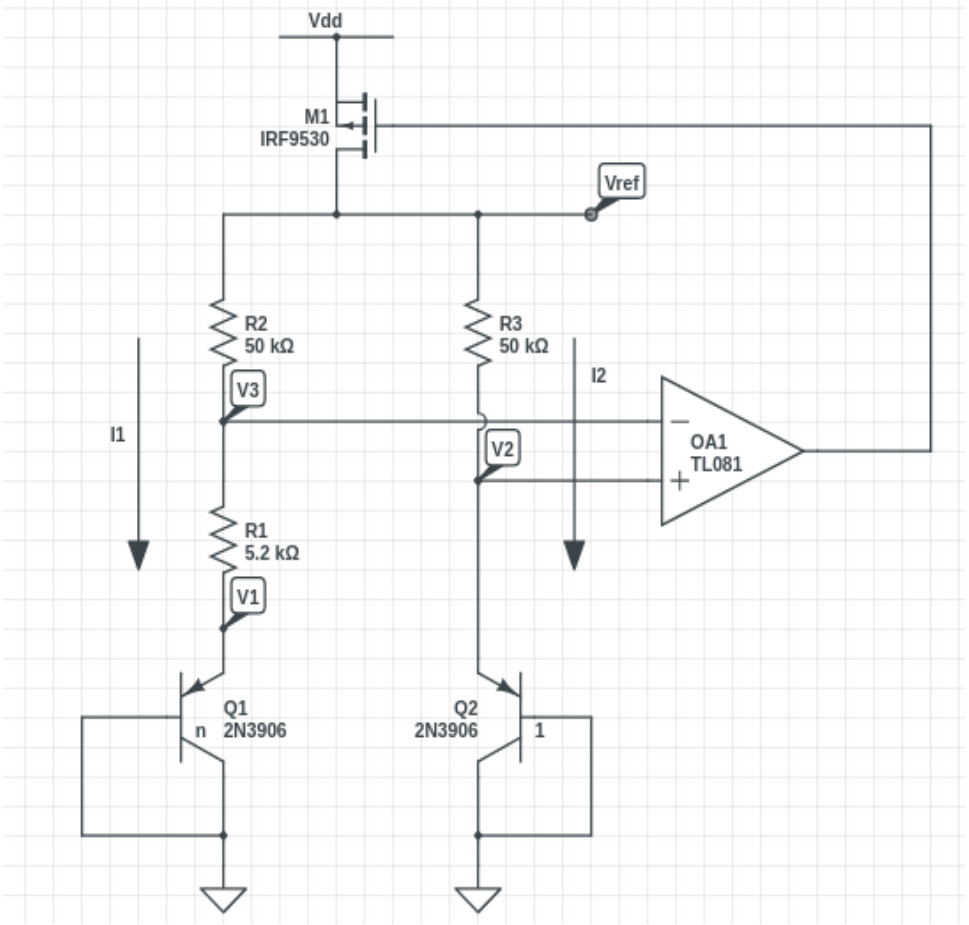
$$T_{-} = \frac{1 + g_{m1}R_1}{1 + g_{m1}(R_1 + R_2)} \times A(s)$$

Positive feedback loop:

$$T_{+} = \frac{-1}{1 + g_{m1}R_2} \times A(s)$$

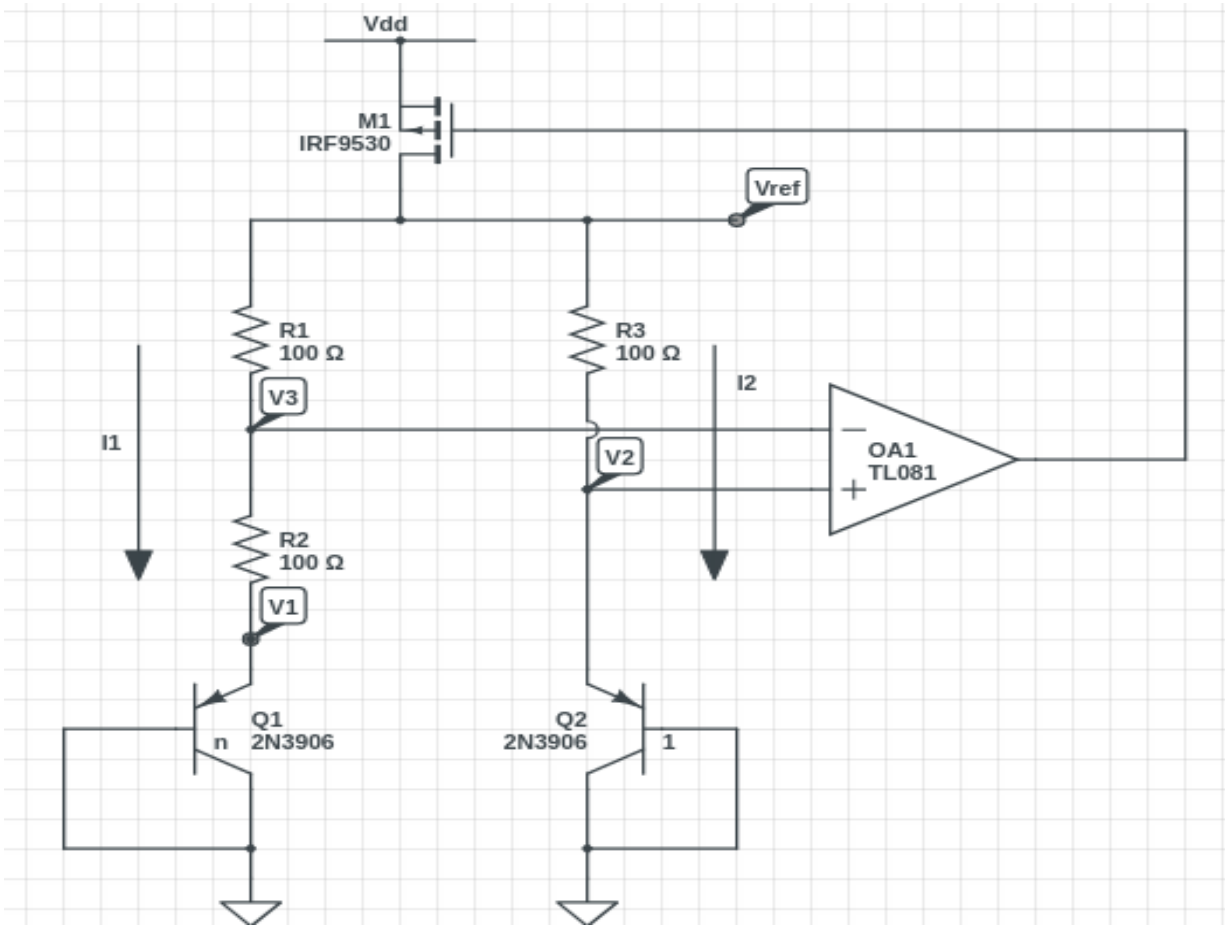


For stability, we need $|T_{-}| > |T_{+}|$, and this criterion is satisfied by the above two relations.

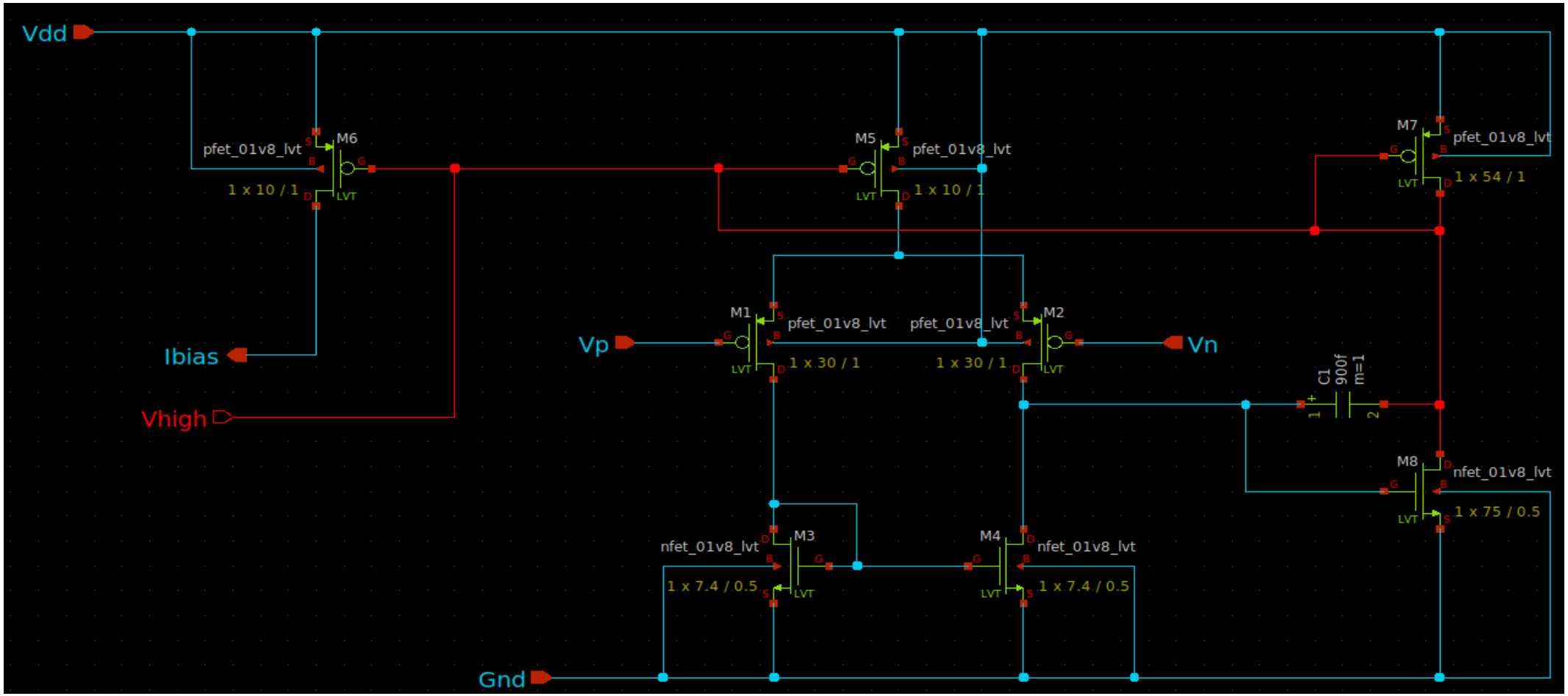


Analysis of BGR circuit

I2 = Io exp(v2/vt) , I1 = n * Io exp(v1/vt)
So v1-v2 = vt ln(I1/nI2)
I1=I2
v3 = I1*R2 + v1 = v2
Vref = I1 * R1 + v3 and Vref = I2* R3 + v2
I1=I2=(v2-v1)/R2 so I1=vt/r2 ln(n)
Vref = vt*(R3/R2)*ln(n) + v2 = 1.2v
Vref = -------PTAT--------- + CTAT = 1.2v
Using I1=I2= 10 µA , n=8
From above equation R2=5.2kΩ
R3=R1=50kΩ



OTA schematic



Analysis of OTA

- Two stage miller OTA used with the following specs:-

DC gain = 60 dB , GBW = 30 MHZ , Phase margin >= 60 deg , ICMR = 0.8v : 1.6v

Slew rate = 20v / microsec , C load = 2pf , Vdd = 1.8v

- Miller cap Cc >= 0.22 to achieve PM >= 60 deg so Cc = 800fF

- from Slew rate equation : SR = I5 / Cc we get I5 = 20 microAmp

- from GBW eauation: GBW = gm1 / 2πCc we get gm1 then (W/L) of m1,m2

- from ICMR+ equation : we get (W/L) of m3,m4

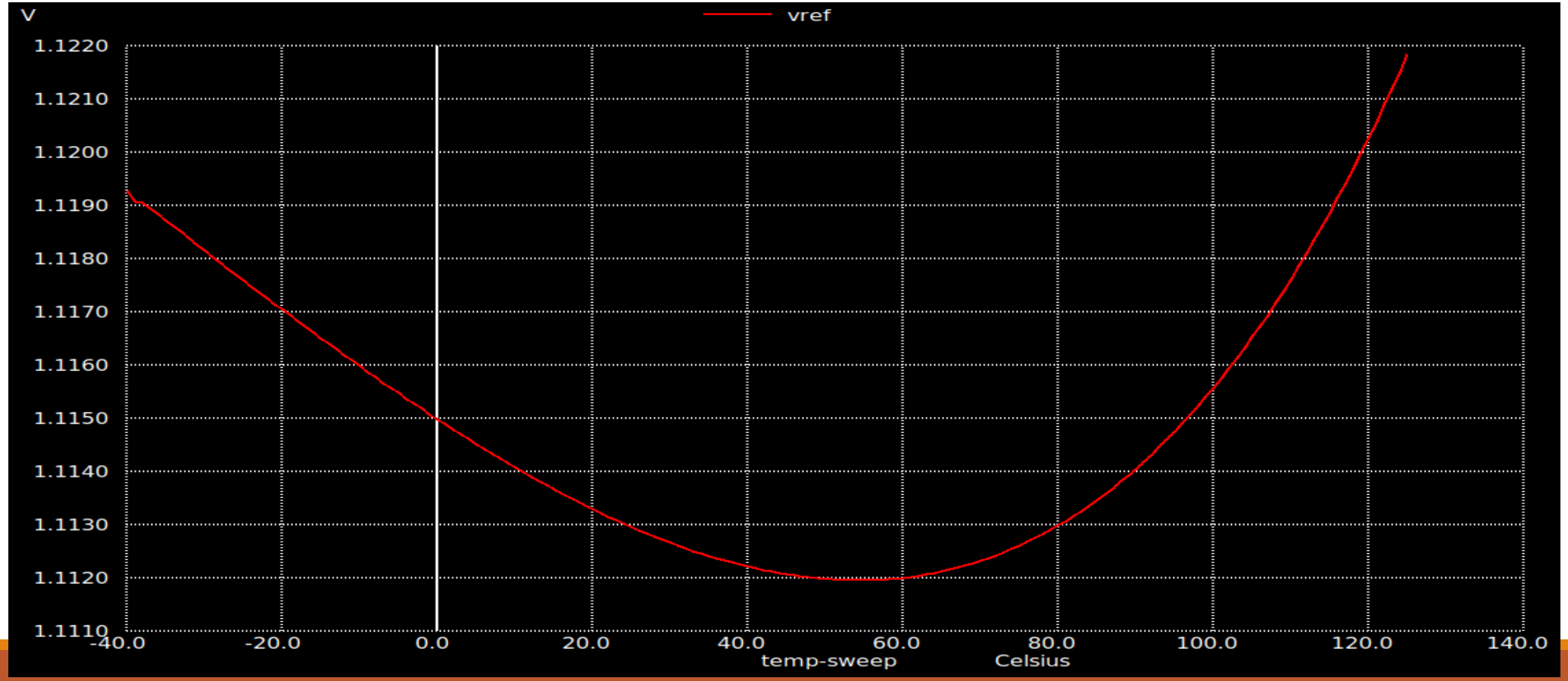
- from ICMR- eqatution : we get (W/L) of m5,m6

- from phase margin condition : we get (W/L) of m8

-from current mirror relation between m5,m7 we get (W/L) of m7

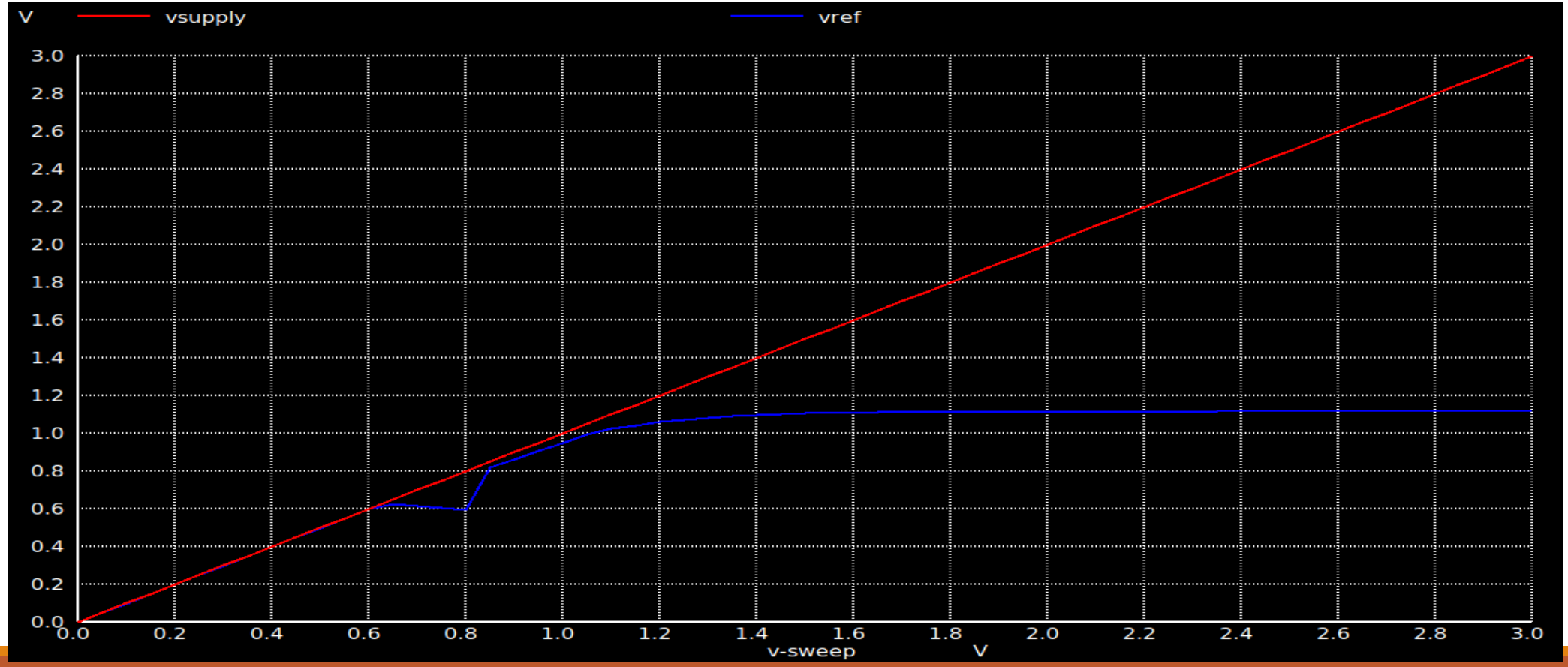
Simulation of Bandgap 1.8v
1- DC sweep vs Temperature

Using Vdd=1.8v and the temperature was swept from –40 to 125 deg and output is 1.11



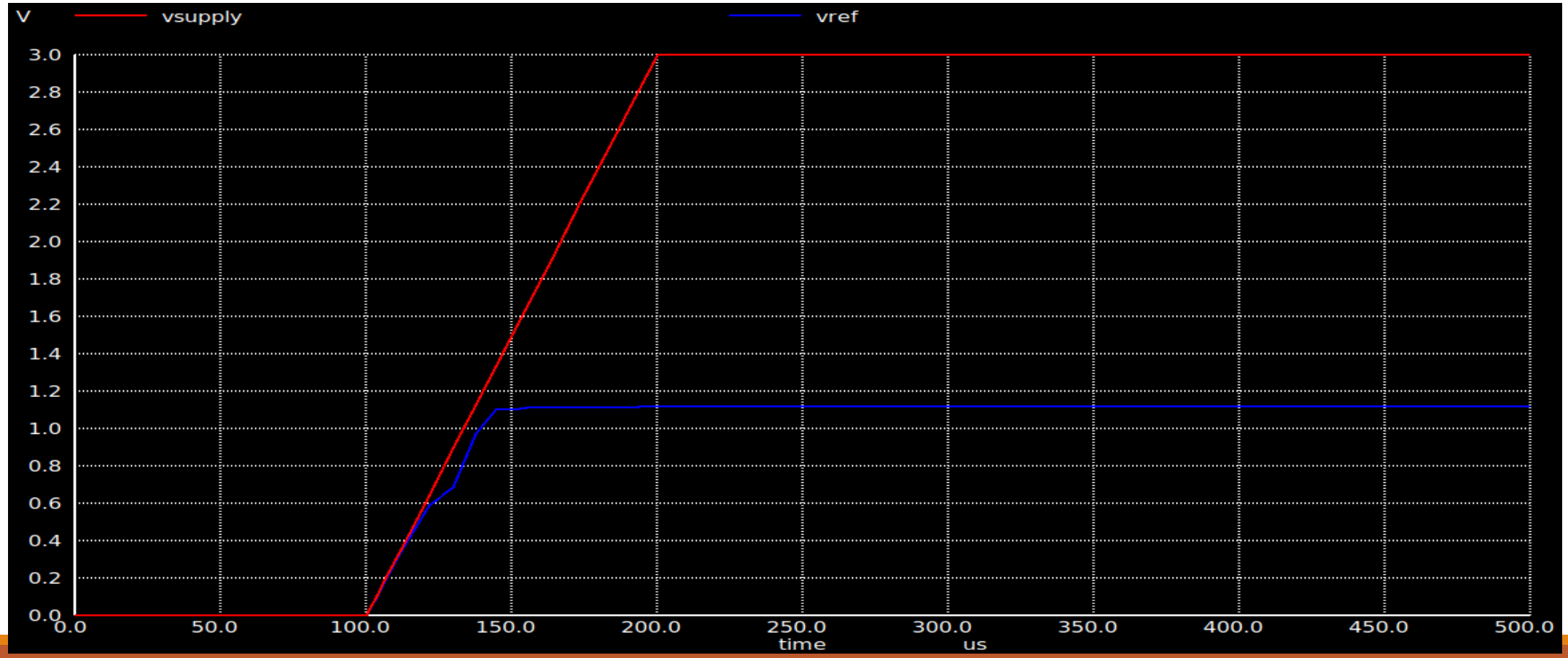
Simulation of Bandgap 1.8v
2- DC sweep vs Supply voltage

- VDD was swept from 0 to 3v and the output is 1.1v



Simulation of Bandgap 1.8v
3- Transient Analysis

- A step voltage from 0 to 3v volt used with 100 us rise time and the output is 1.1v



Simulation of Bandgap 1.8v
4- PSRR Analysis

- PSRR = -40 dB from 1Hz to 16 KHZ