Analysis and Development of A Trusted Low Dropout Regulator (LDO) Model for Intellectual Property (IP) Reuse Aiming at System Verification

DISSERTATION

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By

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Abstract

In recent years, with the explosive increase of the wireless communication and consumer electronics products, the advanced system solutions which have powerful computation capability and multi functions are in great demand in the market. Among the various solutions, System on Chip (SoC) is being widely exploited due to the fact that it has the highest level of integration of a large quantity of reusable intellectual property (IP) blocks such as microprocessor, memory block, interface block, RF block, and power management blocks. The success of a SoC design mainly relies on the available reusable IP blocks provided by the IP vendors. Given the trusted reusable IP blocks, a SoC system can be delivered to the market in a very timely way. Therefore, both powerful computation capability with multi functions and great productivity can be implemented at the same time by using SoC. However, the quality assurance of the reusable IP blocks is vital to the successful SoC design.

In this dissertation, we analyzed and developed trusted Low Dropout Regulator (LDO) models for intellectual property (IP) reuse aiming at system verification. The LDOs were designed with TI (Texas Instrument) Analog System Lab Kit (ASLK) Pro kit and verified by using TI TINA simulation tools. Based on the performance of the LDOs, high level models of the LDOs in MATLAB are given for initial system validation. In addition, the Verilog-AMS behavior models are presented to cover the full functions of the LDOs. The correctness and effectiveness of the models are verified under Cadence design

environment. The proposed models not only satisfy the reusable IPs quality assurance for SoC application but also indicate the practical issues with the use of building component ICs from ASLK Pro kit. Therefore, they can be used as trusted reusable IP blocks for design and verification of SoC.

Dedication

This document is dedicated to my family.

Acknowledgments

I would like to show my sincere appreciation and upmost thanks to Dr. Steven B. Bibyk for his guidance, encouragement, and support during my journey towards the doctoral degree. It gave me pleasure to work under his guidance. It is impossible to complete this research without his supports and encouragement.

I would also like to thank Professor Wu Lu and Professor Jin Wang for serving my dissertation committees and giving me many invaluable comments and suggestions.

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Finally, I would like to express my deepest gratitude to my wife Carrie Gao for her incredible love and inspiration, and my family for their infinite support and encouragement.

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Publications

1. Wei Liu, Waleed Khalil, M. Ismail, and Edith Kussener "A Resistor-Free Temperature-Compensated CMOS Current Reference", in *Proc. IEEE International Symposium on Circuits and Systems* (*ISCAS*), 2010, pp. 845-848

2. John Hu, Wei Liu, and M. Ismail "Sleep-mode ready, area efficient capacitor-free low-dropout regulator with input current-differencing", *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 1, pp. 107-112, Apr. 2010
3. John Hu, Wei Liu, Waleed Khalil, M. Ismail "Increasing Sleep-Mode Efficiency by Reducing Battery Current Using a DC-DC Converter", in *Proc. IEEE int. Midwest Symp. on Circuits and Systems* (*MWSCAS*), 2010, pp. 53-56.
4. E. Kussener, F. Rudolff, F. Guigues, H. Barthelemy, Wei Liu, John Hu and M. Ismail "50 nA, 1 V Nanowatt Resistor-Free Compact CMOS Current References", in *Proc. IEEE Int. Conference on Electronics, Circuits, and Systems* (*ICECS*), 2010, pp. 1212-1215.

Fields of Study

Major Field: Electrical and Computer Engineering

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Chapter 1 Introduction

1.1 Motivation

Today, with the rapid development of information technologies, more and more smart things are created and distributed to provide us higher capability of communications, entertainment, education, and working productivity. Among them, the typical applications include smart phone, smart watch, smart thermostat, etc. In addition, there are more and more smart things to appear in a larger scale such as smart home, even smart cities. The implementation of smart home/cities relies on the deployment of wireless network system which consists of a large quantity of sensors. For example, the sensors in smart home are used to monitor many variable factors in our living environment such as temperature, light, air pollution, water, and weather. For smart cities, more variables like traffic condition as well as epidemic surveillance are monitored and the sensed data are provided to the city administration. All of the above smart things are built with many electronics devices. Therefore, the successful implementation of them is heavily determined by the trustworthiness and availability of the building electronics devices.

The driving force behind today's electronics industry is the famous Moore's Law. In 1965, Gordon E. Moore stated that the number of transistors on integrated circuits would double every 18-24 months [1]. With the never-ending increasing of semiconductor processing capability, the design productivity gap emerged and expended as a result of designer productivity's inability to keep pace with it. Figure 1.1 shows the productivity gap.

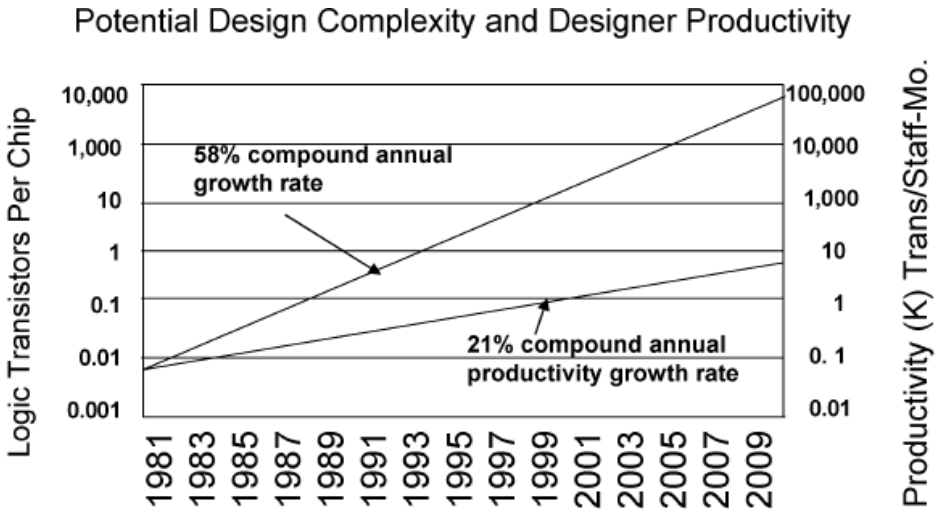

Figure 1.1 The design productivity gap. From Ref. [2]

The top line represents the increase in available semiconductor processing capability (58% increase annually), and the bottom line shows the increase in designer productivity (only 21% increase annually).

However, there are many efforts made to narrow or minimize the gap. These efforts include System-on-Chip (SoC) and System-in-Package (SiP) which are shown in Figure 1.2.

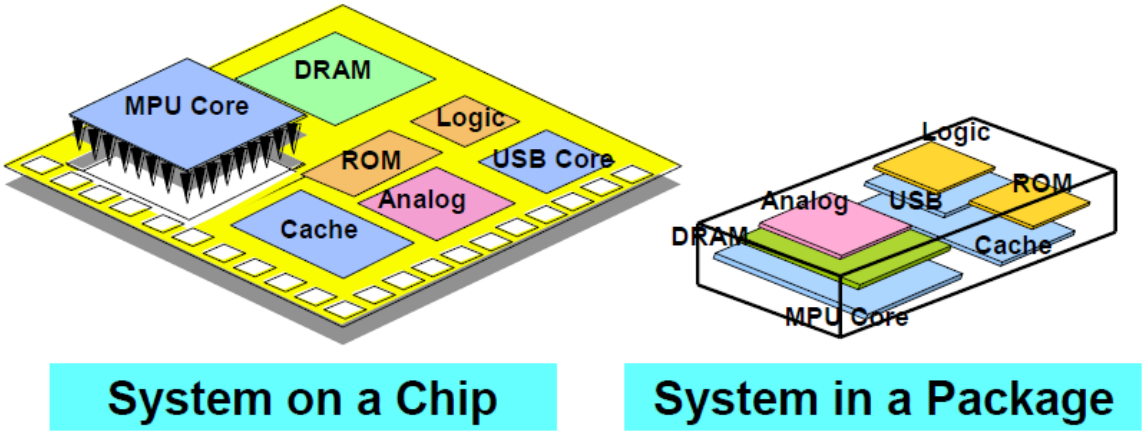

Figure 1.2 System-on-Chip (SoC) and System-in-Package (SiP). From Ref. [3]

As shown in Figure 1.2, SoC is built on one single semiconductor chip with verified intellectual property (IP) blocks including microprocessors, digital blocks, analog blocks, memory blocks, and interface blocks. These IP blocks are normally reusable and are delivered by different vendors.

SiP is built by packaging separate chips into a system within a common substrate. The individual chips were built with the same or different technologies (bipolar, CMOS, BiCMOS, or compound semiconductor process).

The selection of SoC or SiP for a given product is mainly determined by the trade-offs between many factors such as product performance, production cost, product to market time, etc. In this dissertation, we only concentrate on the generation and establishment of trust models of the building IP blocks for SoC design. The trust models are needed not only for the high level system initial validation but also for the low level behavioral description in detail.

As shown in Figure 1.2, SoC design heavily relies on the verified IP blocks. Therefore, the development of the required IP blocks with high reliability becomes the key to the successful design of SoC. This dissertation is focused on the development of a trusted model for reusable IP blocks in SoC designs.

1.2 Objectives

Basically, IP blocks can be classified into three groups: soft IP, hard IP, and firm IP [4].

Soft IP blocks are built with high level description languages like Very High Speed Integrated Circuit Hardware Description Language (VHDL) or Verilog. The end user has to perform their own synthesis process to achieve the desired performance after getting the soft IPs from vendors. Due to the process independent feature and highly developed digital Electronics Design Automation (EDA) tools, soft IPs are widely applied for the development of digital blocks. However, the performance of soft IP blocks is hard to predict precisely and varies depending on the different implementation processes.

Hard IP blocks are provided with the complete physical implementation (layout files and the associated verification information). Therefore, the end user has more confidence to expect the desired performance of the blocks after applying them in their designs. However, the heavy process dependent feature limits the portability of hard IP blocks to other different processes. Analog and mixed signal blocks as well as digital bocks are delivered as hard IP blocks.

Firm IP blocks have the both features of soft IP and hard IP. Design parameters are provided to the end user so that the performance of the blocks could be tuned to reach the desired specification. Therefore, Firm IP blocks behave more flexible than hard IP blocks and easier to predict the performance than soft IP blocks.

Creating a reusable IPs requires good understanding of circuits design, different hardware description language (HDL) coding skills, and circuit simulation engine algorithms. In recent years, many works have been done to investigate and develop new methods to create reusable IPs [5-9].

However, the reusable IPs quality assurance issues are arising with the widely using of these blocks in SoC designs. The quality assurance issue is caused by the low reliability of the IPs due to lack of sufficient verification and incomplete coverage of the specification for all parameters [10]. Therefore, development of trusted reusable IPs is becoming more vital and urgent in today's SoC designs.

In this dissertation, we describe the analysis and development of a trusted Low dropout (LDO) block for IP reuse which includes the circuit design, experimental verification, high level modeling for system validation and Verilog-AMS behavioral model. The circuit was built and verified with TI Analog System Lab Kit (ASLK) Pro. The high level models were derived from the extraction of the circuit design and implemented with MATLAB. These models have the highest level of abstraction and are not necessarily to cover the full functions. They are needed to enable the initial system validation which is advantageous in the early design and development stage. The behavior model of the proposed reusable IP was provided with Verilog-AMS and it is able to cover the full

functions of the IPs. They can be easily integrated into the system for performing co-simulation together with other function blocks.

1.3 Organization

The dissertation is organized as follows:

An introduction of TI Analog System Lab Kit (ASLK) Pro and LDO regulator are presented in Chapter 2. Moreover, the structure of conventional LDO was reviewed and analyzed. Also, the most important parameters of conventional LDO are listed. Analysis and designs of the discrete LDOs with ASLK Pro kit are addressed in Chapter 3. With the given macro models of the two general-purpose OPAMP ICs (TL082, LM358), the small-signal analysis of the two circuits are presented in detail. In addition, special attention was given to the analysis of TL082 OPAMP whose application is severely limited by the single supply operation issue. Chapter 4 presents high level system models of the LDOs for initial system validation with MATLAB tool. The proposed high level models provide an efficient way to predict the most important performance of LDO system: AC stability and Power Supply Rejection (PSR). Verilog-AMS behavioral model of the proposed LDOs is described in Chapter 5. Specifically, an obscure error of TL082 OPAMP (output latch-up issue) is addressed and embodied in the Verilog-AMS model. Moreover, the verification of the behavioral models is also included in this chapter. The summary of all the works and the future works to be done are given in Chapter 6.

Chapter 2 Introduction to TI ASLK Pro and Low Dropout (LDO) Regulator

2.1 Introduction to TI ASLK Pro

TI ASLK Pro is developed for engineering students to perform analog lab experiments and provide a cost efficient platform/test bed for students to realize analog system using general purpose ICs [11]. The picture of TI ASLK Pro kit is shown in Figure 2.1:

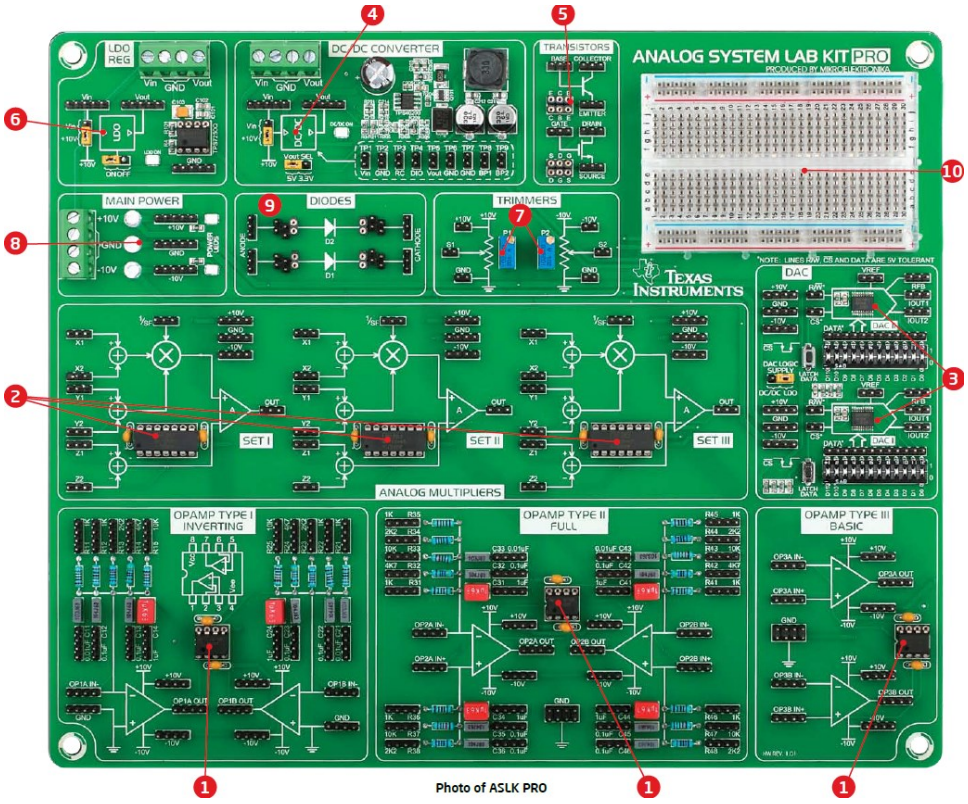

Figure 2.1 Picture of TI ASLK Pro kit. From Ref [11]

2.1.1 **The description of TI ASLK Pro Kit**

The ICs provided in TI ASLK Pro are listed below:

1). General-purpose operational amplifier: 3

2). Wide-bandwidth precision analog multiplier: 3

3). 12-bit parallel-input multiplying digital-to-analog converter: 2

4). Wide-input non-synchronous buck-type DC/DC controller: 1

5). Transistor sockets: 2

6). Low dropout regulator: 1

7). 1 KΩ trimmers (potentiometer): 2

8). Screw terminals: 1

9). Diode sockets: 2

10). General-purpose area

In addition to the ICs, the kit also includes the various connectors as well as dual power supplies.

TI ASLK Pro uses the following software as simulation tools.

TINA/Pspice/any SPICE simulator

FilterPro

SwitcherPro

For more information about TI ASLK Pro, please visit

http://www.ti.com/tool/aslkpro

2.1.2 **TI TINA**

TINA is a powerful circuit simulation tool based on a "Simulation Program with Integrated Circuit Emphasis"(SPICE) engine. It has a library which includes TI analog macro models and active/passive component models [12].

More information about TI TINA is available at the following websites:

http://www.ti.com/tool/tina-ti

2.2 Introduction to Low dropout (LDO) Regulator

Power management circuits (PMC) can be found in almost all battery-powered devices because they can provide multiple output voltages and extend the battery's lifetime. PMCs provide not only efficient distribution of required voltage or current levels, but also on and off controls for all functional blocks in electronics equipment. With the rapid development of wireless communication and consumer electronics products, battery-powered portable devices are highly demanded. Therefore, more power management circuits are needed in the market with higher power efficiency, smaller device size, and cheaper price. Three topologies in PMCs gained wide use because of their respective merits: Low drop-out regulator (LDO), switching power converter, and switching capacitor converter. Among the various kinds of topologies, LDO is the most widely used one since it has significant advantages over other circuits:

1. Cost

Today, the price for one single LDO Integrated Circuit (IC) is only several to tens of cents.

2. High power efficiency

The majority of power dissipated by LDO is from pass element device and inherently limited by the low dropout characteristic. Also, the quiescent current of LDO is normally quite low (below 100 μA).

3. Good transient response

The small output voltage ripple (undershoot/overshoot) under large output load current change prevents the possible failures of the loading circuits.

4. Low noise

The LDO output contains much lower noise components than other power management circuits such as switching regulator (inductor based) and switching cap regulator (capacitor based).

For example, in a typical CDMA handset design shown in Figure 2.2, there are totally 11 independent LDO circuits are required to provide separate power supplies [13].

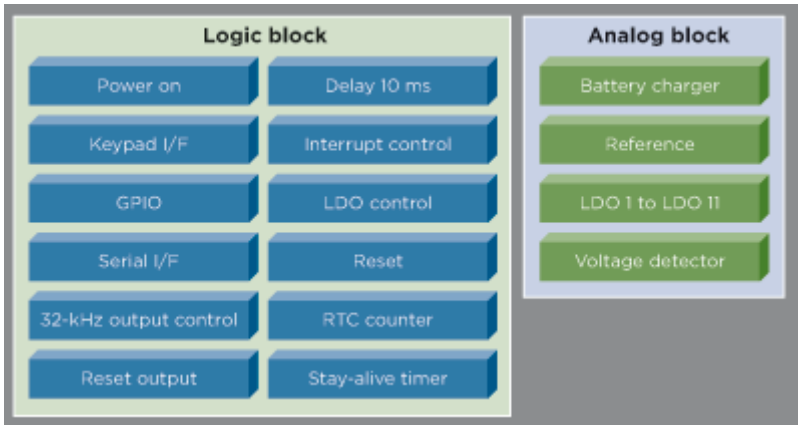

Figure 2.2 A typical CDMA handset power management system. From Ref. [13]

The continuous size shrink of portable devices put more stringent requirements on the printed-circuit-board (PCB) design. Therefore, designs with small PCB real estate and improved performance are highly demanded in high-level integration solutions such as system-on-chip (SoC), system-in-package (SiP), and system-on-package (SoP). Compared to the numbers of the required external components for switching regulators or

switching cap regulator, LDO has gained dominance over other power management topologies because it normally requires only one external capacitor for frequency compensation.

Basically, the frequency compensation of LDO can be classified into two categories: external frequency compensation and internal frequency compensation. The ideal behind external frequency compensation is the use of the external output capacitor as the dominant pole. Therefore, the external output capacitor has to be chosen large enough to guarantee the stability of the LDO. There are a lot of LDO topologies with the external capacitor frequency compensation [14-56].

Unlike external compensation, the internal frequency compensation mainly relies on the connection of compensation capacitors with internal nodes. Therefore, the dominant pole is formed inside the LDO. However, the loading capacitance at the output of LDO has to be carefully limited because the pole formed by the output loading capacitance may move closer to the dominant pole and pose a threat to the stability of the LDO.

In recent years, there are more and more LDO topologies with internal compensation techniques are presented [57-99]. They are widely adopted in high level integration like SoC design due to the fact that the removal of large external capacitor at the LDO output saves valuable PCB real estate.

Most of conventional LDO designs adopt the external capacitor frequency compensation since the large external capacitor provides the frequency compensation and good transient response, as well as low noise performance. The external capacitor contributes not only the dominant pole to the LDO system but also a left-half-plane (LHP) zero to

improve the phase margin. The zero is directly from the equivalent series resistance (ESR) of the external capacitor. The selection of proper external capacitor with safe ESR range should be carefully made because the system robustness heavily relies on the combination of the external capacitor and its associated ESR value. The details of external frequency compensation of conventional LDO design are given in the following section.

2.2.1 **Review of Conventional LDO Structure**

An off-chip external capacitor at the LDO output is required to ensure the ac stability and transient performance in conventional LDO shown in Figure 2.3. The large external capacitor is used to create the dominant pole and provide an instantaneous charge source for transient load changes. The conventional LDO consists of an error amplifier, a pass element (MPT), resistor feedback network (R_1 and R_2), and an output capacitor C_L. C_{GS} and C_{GD} represent the parasitic gate-source and gate-drain capacitance of the pass element transistor MPT and R_{ESR} represents the Equivalent Series Resistance (ESR) of the output capacitor C_L.

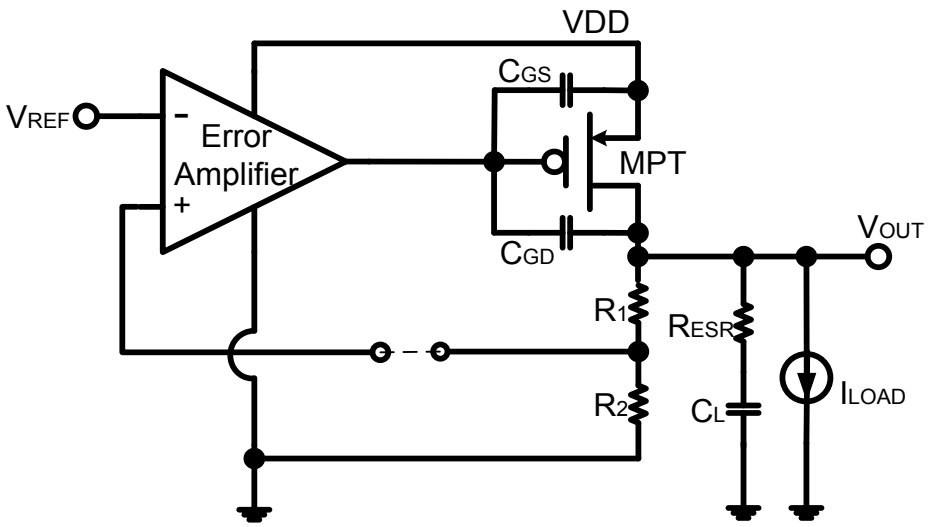

Figure 2.3 Schematic of conventional LDO structure

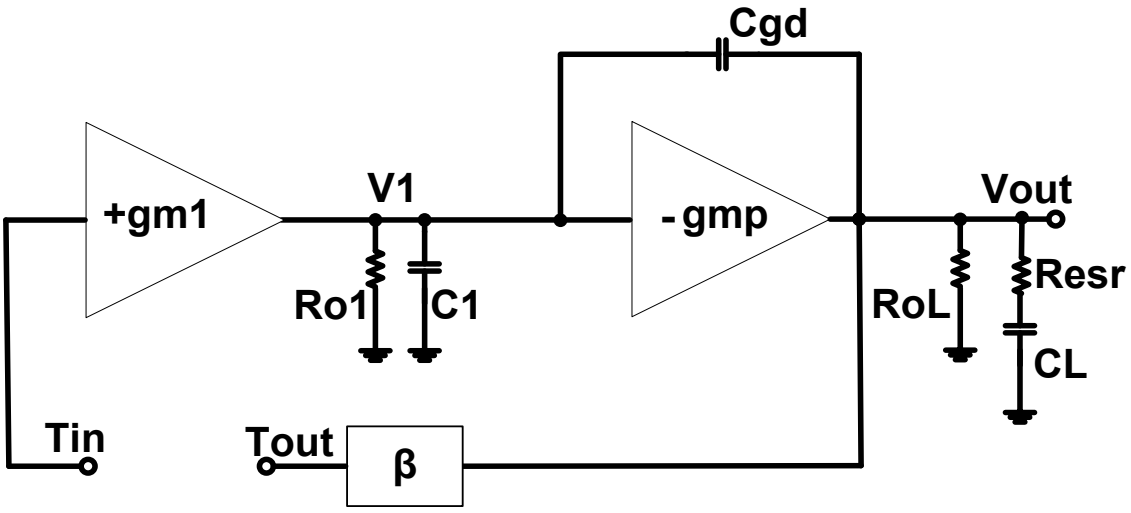

Figure 2.4 Small signal model of conventional LDO

By breaking the feedback loop shown in Figure 2.3, the small signal model of the conventional LDO is shown in Figure 2.4. Applying Kirchhoff's Current Law (KCL) at node V_1 and V_{out}, we can get the two equations as below:

$$sC_{GD}V_{OUT} - (\frac{1}{R_{O1}} + sC_{GD} + sC_1)V_1 = -g_{m1}T_{in} \tag{2.1}$$

$$(\frac{1}{R_{oeq}} + sC_{GD} + sC_{LT})V_{OUT} + (g_{mp} - sC_{GD})V_1 = 0 \tag{2.2}$$

Also, we have

$$T_{OUT} = \beta V_{OUT} \tag{2.3}$$

$$C_{LT} = \frac{sC_L}{1 + sR_{esr}C_L} \tag{2.4}$$

$$\beta = \frac{R_2}{R_1 + R_2} \tag{2.5}$$

By combing (2.1) to (2.5), the transfer function of the conventional LDO structure is given by (2.6)

$$F(s) = \frac{-\beta g_{mEA} g_{mP} R_{O1}[R_{OL} \parallel (R_1 + R_2)](1 + sC_L R_{ESR})(1 - s\frac{C_{GD}}{g_{mP}})}{[1 + s(C_{GS} + g_{mP}R_{OL}C_{GD})R_{O1}]\{1 + sC_L[R_{ESR} + R_{OL} \parallel (R_1 + R_2)]\}} \tag{2.6}$$

where g_{mEA} and g_{mP} refer to the transconductance of the error amplifier and the pass element, and R_{O1} and R_{OL} represent the output resistance of the error amplifier and the pass element. $A_{mP}R_{OL}$ is the voltage gain of the pass element device. Therefore, there are two poles and two zeroes in the conventional LDO structure:

$$P_1 = \frac{1}{C_L[R_{ESR} + R_{OL} \parallel (R_1 + R_2)]} \tag{2.7}$$

$$P_2 = \frac{1}{R_{O1}(C_{GS} + g_{mP}R_{OL}C_{GD})} \tag{2.8}$$

$$Z_1 = \frac{-1}{C_L R_{ESR}} \tag{2.9}$$

$$Z_2 = \frac{g_{mP}}{C_{GD}} \tag{2.10}$$

P_1 is the dominant pole and normally locates at very low frequency since the output capacitor C_L can be as large as microfarad magnitude. P_2 is the non-dominant pole and generated by the output resistance of the error amplifier and gate capacitance of the pass element device. Z_1 is a LHP zero generated by the ESR of the output capacitor C_L and has a fixed value once the output capacitor is determined. Z_2 is a RHP zero generated by the gate-drain capacitance of the pass element device and normally can be ignored since it locates at very high frequency. The typical frequency response of the conventional LDO is shown in Figure 2.5. By carefully allocating the location of zero which is set by the output capacitor C_L and its ESR, the stability of conventional LDO can be guaranteed for all load conditions.

The transient performance of the conventional LDO is mainly determined by the closed-loop bandwidth of the LDO system and the slew rate of the error amplifier. The recovery time of transient load step response of conventional LDO is reversely proportional to the closed-loop bandwidth and the slew rate current of the error amplifier. Therefore, proper closed-loop bandwidth design and careful current allocation should be made to achieve a fast recovery for transient load step response.

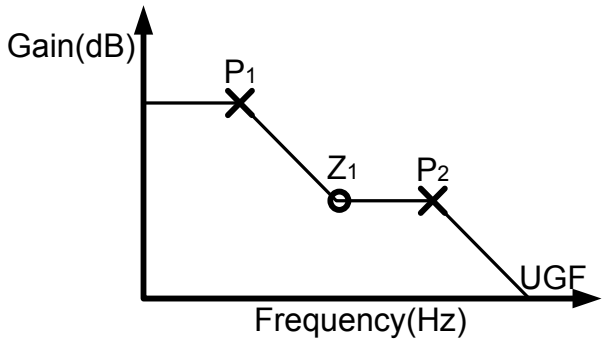

Figure 2.5 The typical frequency response of the conventional LDO

2.3 The important parameters of LDO

The key performance metrics of LDO include line regulation, load regulation, power supply rejection (PSR), line step response, load step response, drop-out voltage, and static current consumption. These metrics well define the LDO's ability to regulate the output voltage against variations from the operating environment. All of these metrics are closely related with the variables from the environment like load current, input power supply, and operating temperature.

Line Regulation

Line regulation is a DC metric which describes the power supply dependency of the LDO output voltage. Here, if the DC voltage variations at the LDO's output and the power supply under a fixed load I_{load} current are noted as ΔV_{out} and ΔV_{in} respectively, the line regulation can be defined as:

$$LINE\_REG = \frac{\Delta V_{out}}{\Delta V_{in}}|_{Iload} \tag{2.11}$$

Load Regulation

Load regulation is another DC metric which describes the load current dependency of the LDO output voltage. Similarly, given a fixed power supply voltage V_{in}, if the DC voltage variations at the LDO's output are ΔV_{out} and the DC changes in load current are ΔI_{load} respectively, the load regulation is defined as:

$$LOAD\_REG = \frac{\Delta V_{out}}{\Delta I_{load}}|_{Vin} \tag{2.12}$$

From equation (2.12), the load regulation actually is the output resistance of the LDO. Therefore, the load regulation can be rewritten as:

$$LOAD\_REG = \frac{\Delta V_{out}}{\Delta I_{load}}|_{Vin} = \frac{R_{OL}}{1 + A_{OL}\beta}|_{Vin} \tag{2.13}$$

where R_{OL} is the open-loop output resistance of the LDO, A_{OL} is the open-loop gain, β is the feedback factor. From equation (2.13), it is clear that the load regulation can be improved by increasing the open-loop gain A_{OL}.

Power Supply Rejection (PSR)

Power supply rejection describes the LDO's output voltage variations caused by the changes in power supply within the entire frequency spectrum. Therefore, the definition of the PSR should include the PSR values in different frequencies (-40 dB at DC, -30 dB at 10 KHz, etc.).

Drop-Out Voltage

Drop-out voltage is defined as the minimum voltage difference between the input power supply voltage and the output voltage and can be described in Figure 2.6.

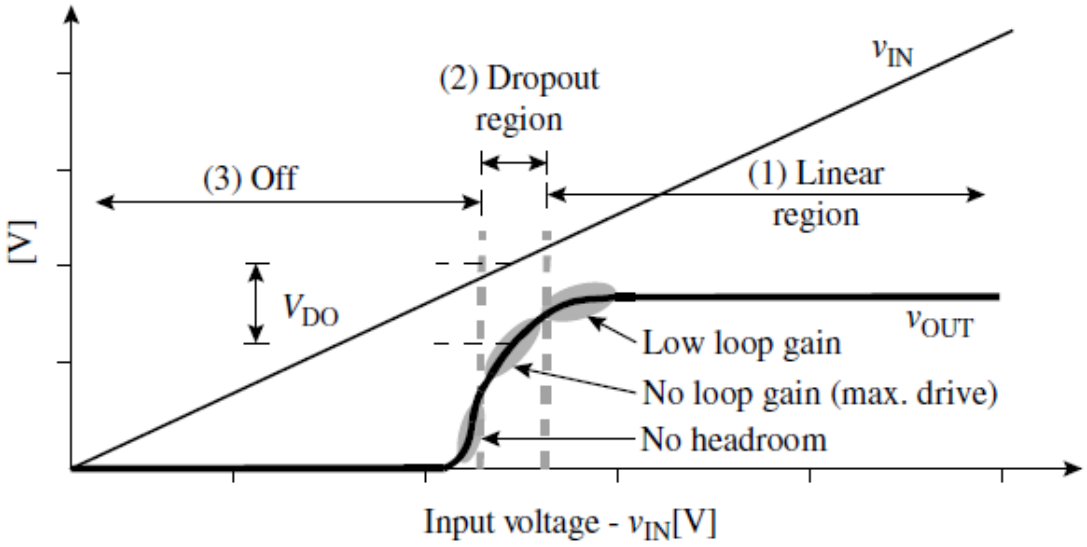

Figure 2.6 Input-output relationship of the conventional LDO. From Ref. [100]

The three operation regions of the conventional LDO are off, dropout, and linear [100]. The LDO is said to be operated in off region when the input voltage is lowered to a point so that the internal devices cannot work properly. Then, with the increase of the input voltage, the internal devices start to work with few loop gain. The LDO under this situation behaves like a resistance with almost constant difference between input voltage and output voltage. At this point, the LDO is operated in dropout region. When the input voltage continually rises to a point where the loop gain starts to increase, the LDO is operated in linear region.

Line Step Response

Line step response is used to evaluate the transient performance of a LDO against the variations from the power supply. Therefore, the noise injected from the power supply can be quantified and limited by this metric. Line step response is normally achieved by injecting small perturbation to the input voltage and observing the resulting output voltage ripples.

Load Step Response

Similarly, load step response is used to measure the transient performance of a LDO against the sudden change in load current. By observing the output voltage responses, the maximum output voltage variations and the system's settling time can be evaluated. The load step response is determined by the external capacitor, the internal slew-rate condition, the loop bandwidth frequency, and the ESR of external capacitor. Better response performance can be achieved by carefully analyzing the circuit topologies and making trade-off between different parameters.

Load Current Range

The current driving capability of the regulator is described by output current range. Nowadays, this range can span several orders of magnitude in various applications. Therefore, the design of LDOs with guaranteed stability over several orders of magnitude load change is challenging.

Static Current

Static current is used to describe the ground current in the LDO. As shown in Figure 2.3, the static current comes from the error amplifier, and the resistor feedback network (R_1 and R_2). The large resistors normally are chosen in order to make the static current as low as possible.

Input Supply Voltage Range

Input Supply Voltage Range is defined as a supply voltage range within which the regulator is able to regulate the input supply to the desired output voltage level while maintaining the nominal current driving capability.

Power Efficiency

Power Efficiency is defined as the ratio of delivered power to the source power and can be expressed as [100]:

$$\eta = \frac{P_d}{P_s} = \frac{V_{out} I_{load}}{V_{in} I_{in}} = \frac{V_{out} I_{load}}{V_{in} (I_{load} + I_q)} < \frac{V_{out}}{V_{in}} \tag{2.14}$$

where P_d is the delivered power to the load, and P_s is the source power from supply, I_{load} is the load current, I_q is the quiescent current of LDO. Therefore, the maximum power efficiency of LDO is theoretically the ratio between the output voltage and input voltage.

Chapter 3 Analysis and Design of two Discrete LDOs with TI ASLK Pro Kit

In this chapter, the analysis and design of two discrete LDOs with TI ASLK Pro kit are presented. The two LDOs are built with two general-purpose OPAMP ICs from TI ASLK kit (TL082 and LM358). TL082 is a monolithic JFET-Input operational amplifier which consists of high-voltage JFET and bipolar transistors. It features high slew rate, low offset and input bias current, and low offset-voltage temperature coefficient. In addition, it has wide common mode and differential voltage ranges as well as output short circuit protection. LM358 is a monolithic integrated circuit (IC) which includes two independent operational amplifiers consisting of bipolar transistors, diodes, resistors, and capacitors. It features wide supply range, low supply current, low input offset voltage and low input bias current.

3.1 Introduction to TL082 OPAMP

The schematic and symbol of TL082 OPAMP are shown in Figure 3.1 and Figure 3.2.

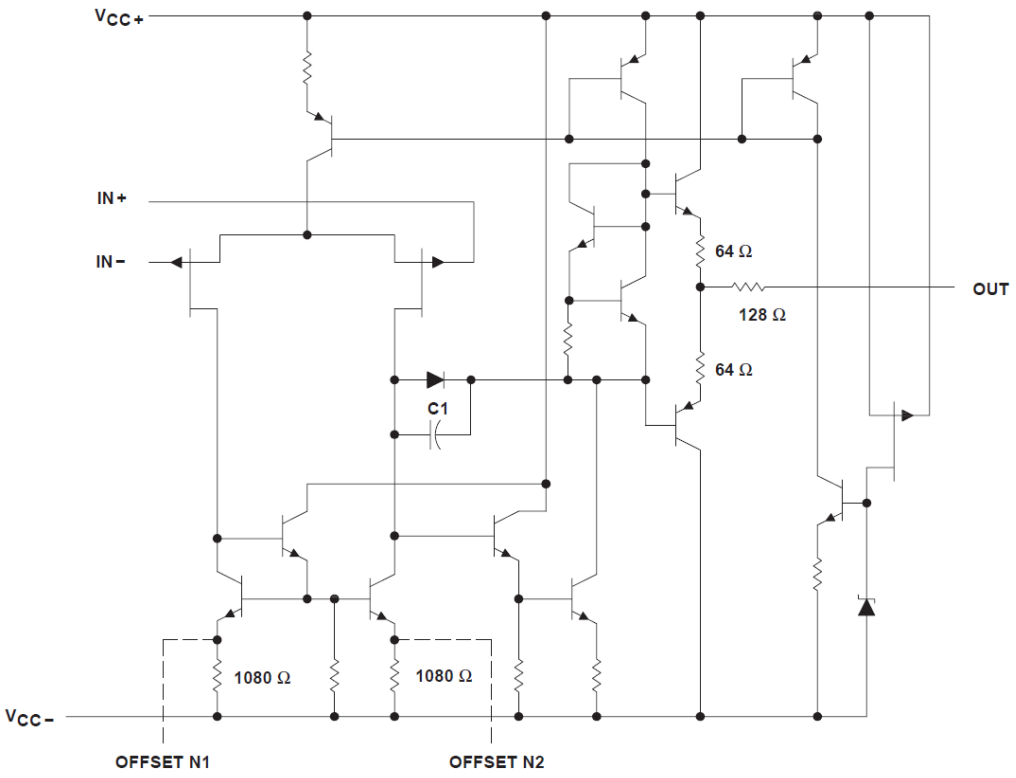

Figure 3.1 Schematic of TL082 OPAMP

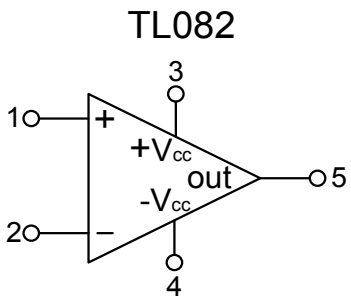

Figure 3.2 Symbol of TL082 OPAMP

The map between the schematic and symbol of TL082 OPAMP is shown in Table 3.1 as below:

Table 3.1 The Map Between the schematic and symbol of TL082 OPAMP

Pin Name in Schematic	Pin Name in Symbol	Remarks
IN +	1	Non-inverting Input
IN -	2	Inverting Input
VCC +	3	Positive Supply Voltage
VCC -	4	Negative Supply Voltage
OUT	5	Output Voltage

In order to characterize the performance of TL082 OPAMP, a macro model is given here in Figure 3.3:

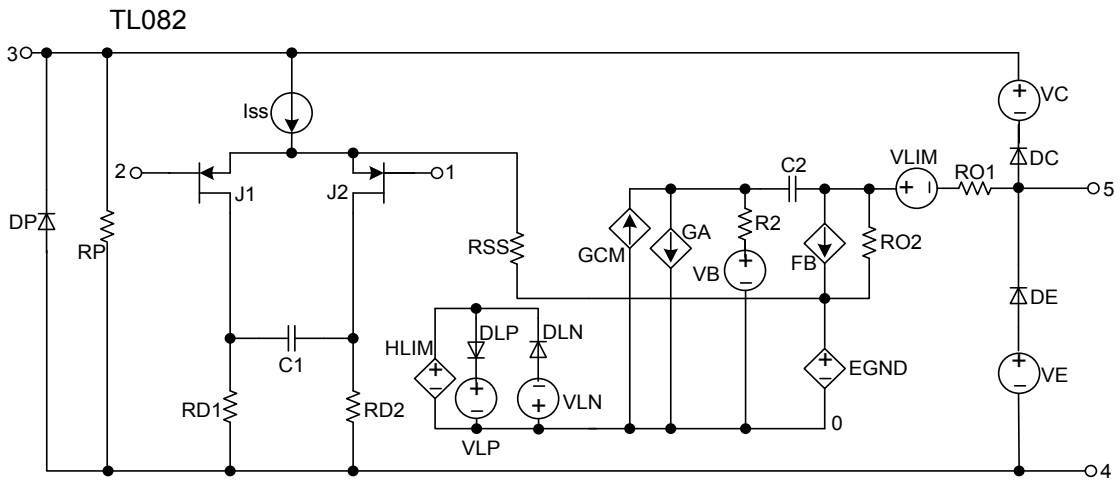

Figure 3.3 Macro model of TL082 OPAMP

J_1, J_2, C_1, R_{D1}, and R_{D2} form the first stage, while DC, DE, VC, and VE form the output voltage limiting stage.

3.1.1 **The AC analysis of TL082 OPAMP**

As shown in Figure 3.3, the input stage of TL082 OPAMP consists of JFET J_1, J_2, capacitor C_1, resistor R_{D1}, and R_{D2}. The non-dominant pole $P_{non\text{-}dom}$ can be expressed as below:

$$P_{non-dom} = \frac{1}{(R_{D1} + R_{D2})C_1} \tag{3.1}$$

The dominant pole is generated by resistor R_2, R_{O2}, capacitor C_2, voltage source V_B, and current controlled current source F_B. In order to figure out the dominant pole, the

intermediate stage macro model is simplified to the following one because $V_B = 0$ and $E_{GND} = 0$.

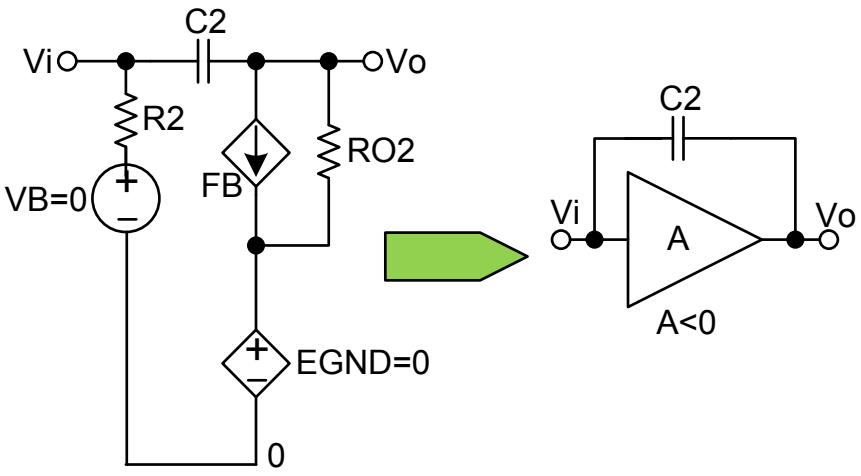

Figure 3.4 Simplified intermediate stage macro model of TL082 OPAMP

Since

$$I(V_B) = \frac{V_i}{R_2} \tag{3.2}$$

$$I(F_B) = k * I(V_B) = k * \frac{V_i}{R_2} \tag{3.3}$$

$$V_O = -I(F_B)R_{O2} = -k * R_{O2}\frac{V_i}{R_2} \tag{3.4}$$

$$A = \frac{V_O}{V_i} = -k * \frac{R_{O2}}{R_2} \tag{3.5}$$

The dominant pole can be expressed as

$$P_{-3dB} = \frac{1}{R_2 * |A| * C_2} = \frac{1}{k * R_{O2} * C_2} \tag{3.6}$$

In order to verify the AC analysis of the TL082 OPAMP, a simulation was performed by using TI TINA tools. The test bench of the simulation is shown in Figure 3.5.

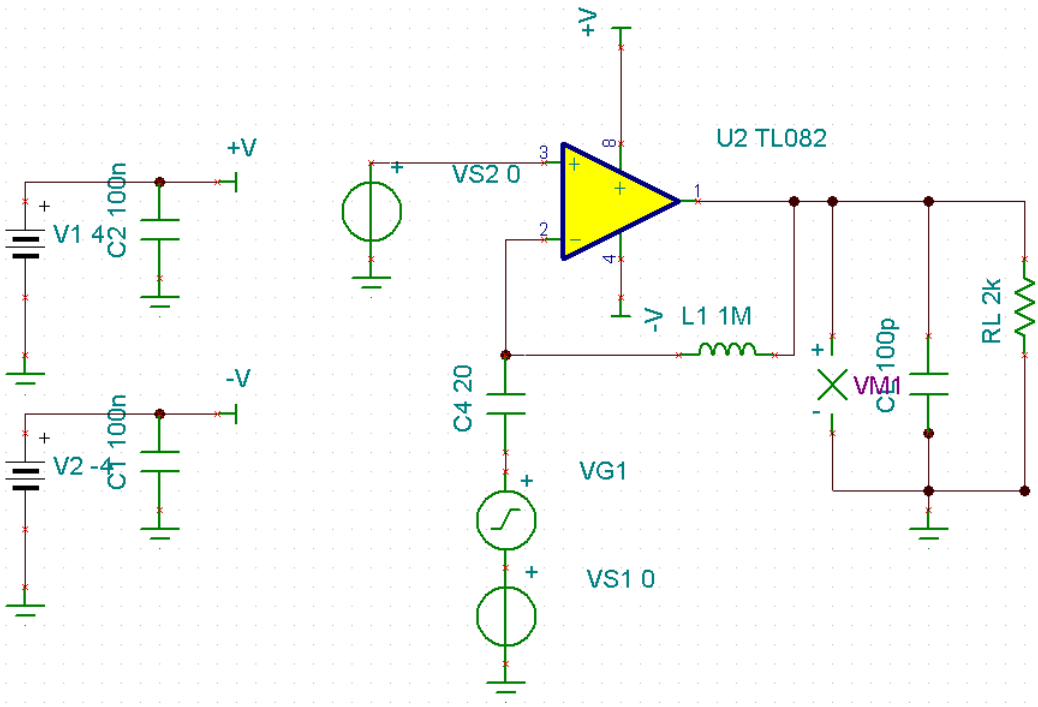

Figure 3.5 AC analysis test bench of the TL082 OPAMP in TI TINA

The simulation result and performance summary are shown in Figure 3.6 and Table 3.2, respectively.

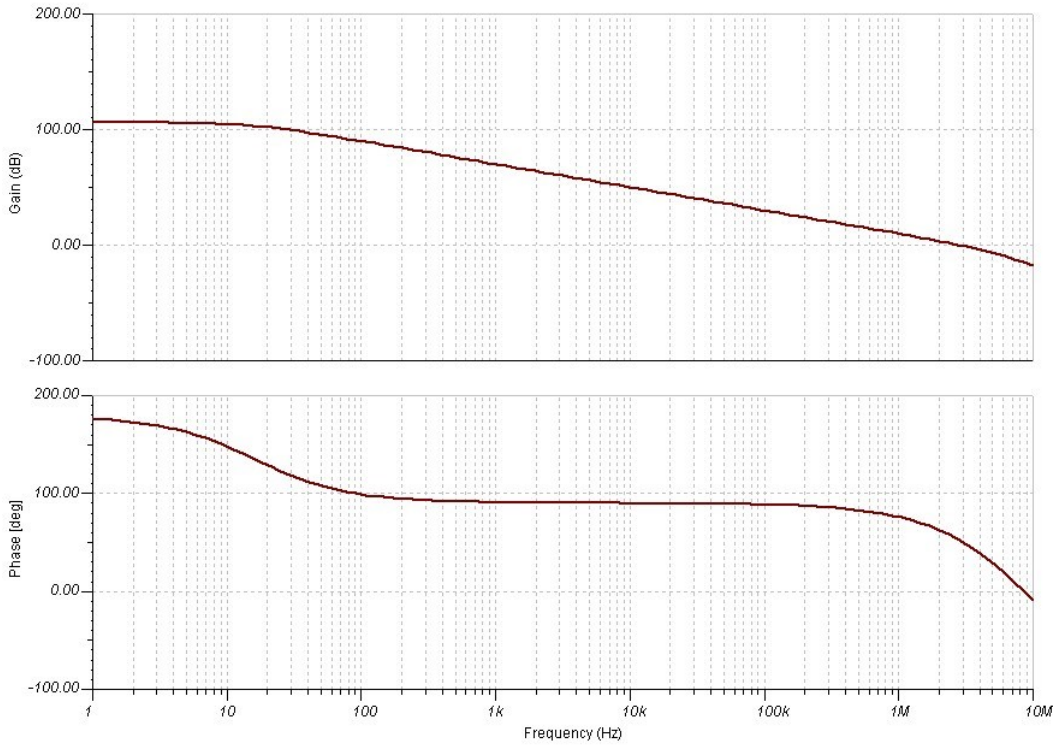

Figure 3.6 AC analysis simulation of the TL082 OPAMP in TI TINA

Table 3.2 The performance summary of TL082 OPAMP

Specs	**Value**	**Remarks**
Adc	106dB	DC Voltage Gain
UGF	3MHz	Unity-Gain Frequency
P-3dB	15Hz	Dominant Pole

3.1.2 **Single supply operation issue in the TL082 OPAMP**

In Figure 3.3, E_{GND} is a voltage controlled voltage source (VCVS) which is used to set

up the internal zero reference node voltage:

$$E_{GND} = \frac{1}{2}\left[V(3,0) + V(4,0)\right] \tag{3.7}$$

The above expression is equal to zero when V(3,0) and V(4,0) are set to positive and negative supply rails. Otherwise, E_{GND} generates a non-zero reference node voltage which will cause the model to malfunction.

For example, if V(3,0) = 5V, V(4,0) = 0V, then E_{GND} = 2.5V. The middle-rail voltage generates incorrect DC operating points internally. In addition, the dominant pole cannot be generated correctly by the model. Thus, the macro model of TL082 OPAMP fails to work because of the incorrect dc operating points and ac characteristic.

3.1.3 **The Proposed Discrete LDO Based on TL082 OPAMP**

Based on the previous analysis of TL082 OPAMP, a discrete Low Drop-Out (LDO) voltage regulator was proposed in this section. The main summary of performance is listed in Table 3.3 as below:

Table 3.3 Performance of the proposed LDO based on TL082 OPAMP

Technology	Discrete Components
Input Voltage (Vin)	4V
Output Voltage (Vout)	3V
Output Current	100mA
Line Regulation	120mV/V@100mA
Load Regulation	-0.226μV/mA@Vin=4V
Output Capacitance	10μF
ESR Resistor	1Ω
PSRR (1-100KHz)	-16.6dB @1KHz -16.56dB @10KHz -16.46dB @100KHz

Here, a monolithic TL082 OPAMP, a Zener diode MZPD2.7, and a PMOSFET IRFU9222 are used to build the LDO and function as error amplifier, voltage reference, and pass element, respectively. The schematic of the LDO is shown in Figure 3.7 as below:

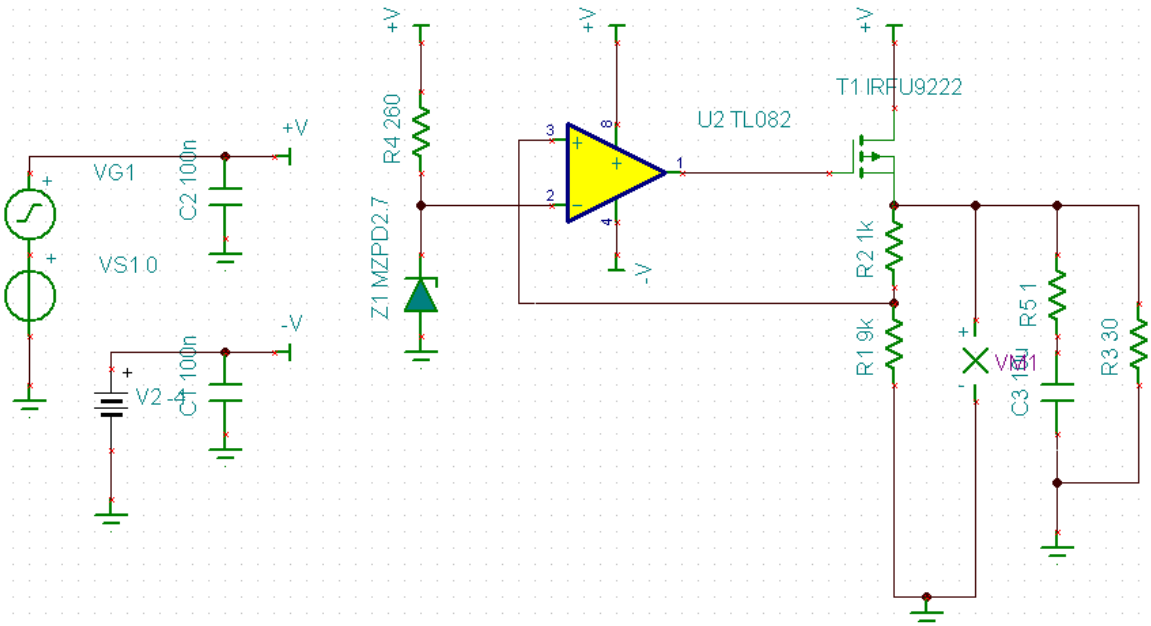

Figure 3.7 The schematic of the LDO design based on TL082 OPAMP

In addition to the error amplifier, voltage reference, and pass element mentioned above, the resistor string which functions as voltage divider is implemented by resistor R_2 and R_1. C_3 and R_5 are adopted as output load capacitor and *ESR* resistor. R_3 is used to model the load current. Dual supply voltages must be provided to TL082 OPAMP. Otherwise, the internal reference voltage EGND would not be zero.

3.1.4 **The Performance of the Proposed Discrete LDO Based on TL082 OPAMP**

In order to verify the performance of the proposed LDO, a bunch of simulations were performed with different test benches. These simulations are classified into three categories:

i). Static Characteristics (Line Regulation/ Load Regulation)

ii). Dynamic Characteristics (Line Step Response/ Load Step Response/ Start-up)

iii). AC Small Signal Characteristics (Stability/ Power Supply Rejection (PSR))

Next, these important characteristics were validated by performing various simulations accordingly.

1) Line Regulation

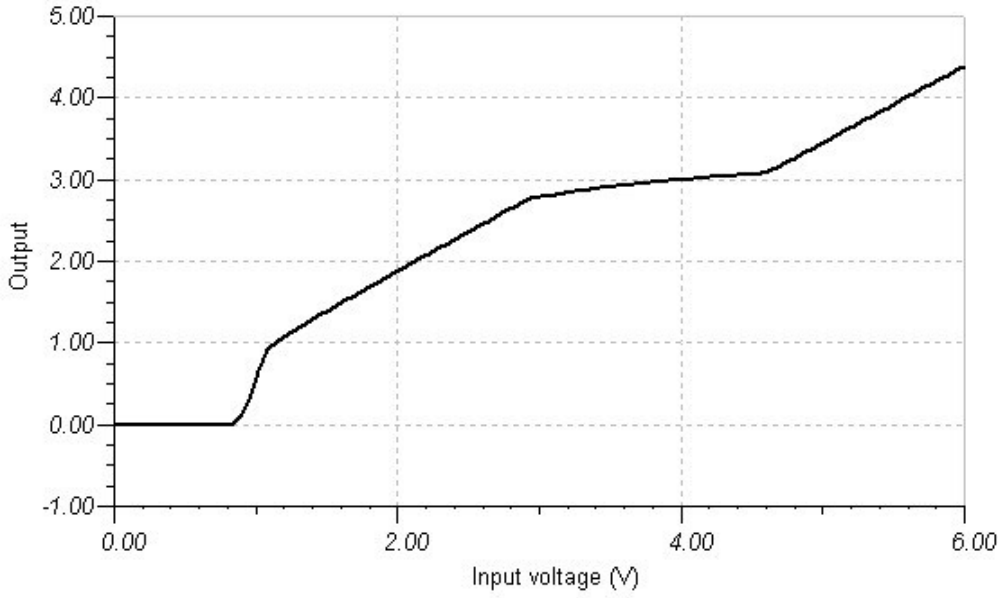

Figure 3.8 Line regulation of the proposed LDO based on TL082 OPAMP

Figure 3.8 shows the line regulation simulation of the proposed LDO. The line regulation can be easily calculated by applying equation (2.11).

2) Load Regulation

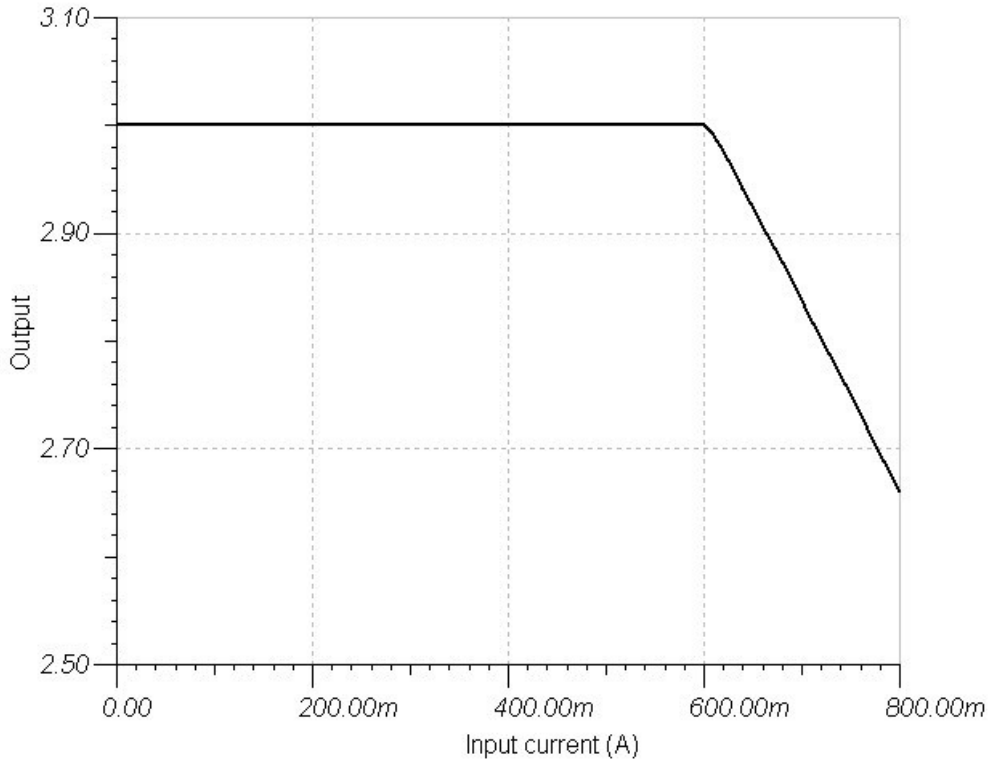

Figure 3.9 Load regulation of the proposed LDO based on TL082 OPAMP

Load regulation is shown in Figure 3.9 and can be calculated by applying equation (2.12). As shown in Figure 3.9, the proposed LDO based on TL082 OPAMP is able to drive load current as large as 600 mA.

3) Line Step Response

Line step response simulation was performed by applying DC supply voltage with a square wave perturbation. As shown in Figure 3.10, when a peak-to-peak 200 mV square wave was applied on supply voltage, the LDO output voltage underwent a ripple of about 32 mV.

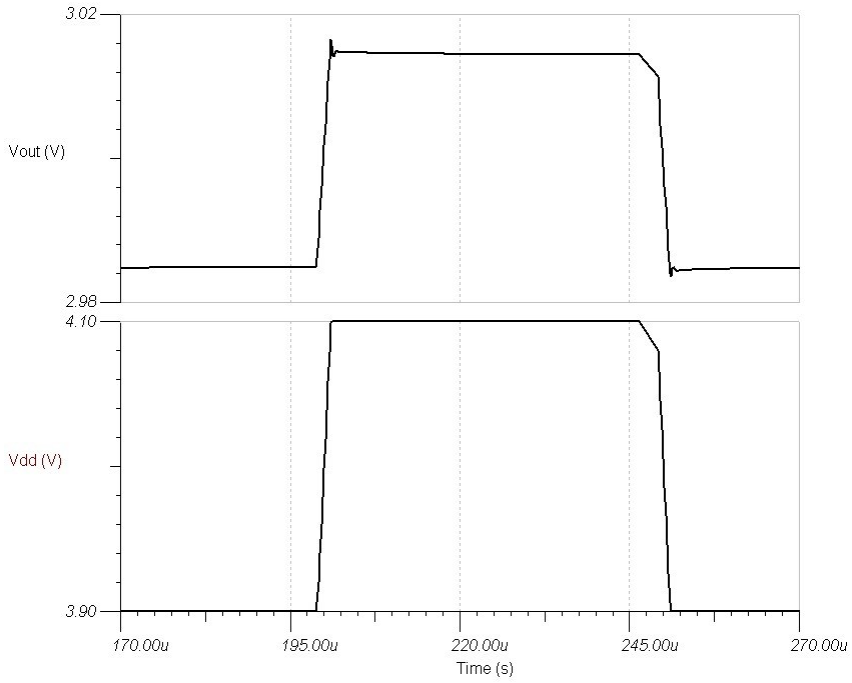

Figure 3.10 Line step response of the proposed LDO based on TL082 OPAMP

4) Load Step Response

A sudden load current change is applied to the LDO output to perform load step response. Figure 3.11 shows the load step response of the proposed LDO when a sudden load current change (100 mA) is applied to the LDO output. From the simulation results, the undershoot voltage and overshoot voltage of the proposed LDO are both 90 mV. Also, the settling times for both undershoot and overshoot are around 2 μS.

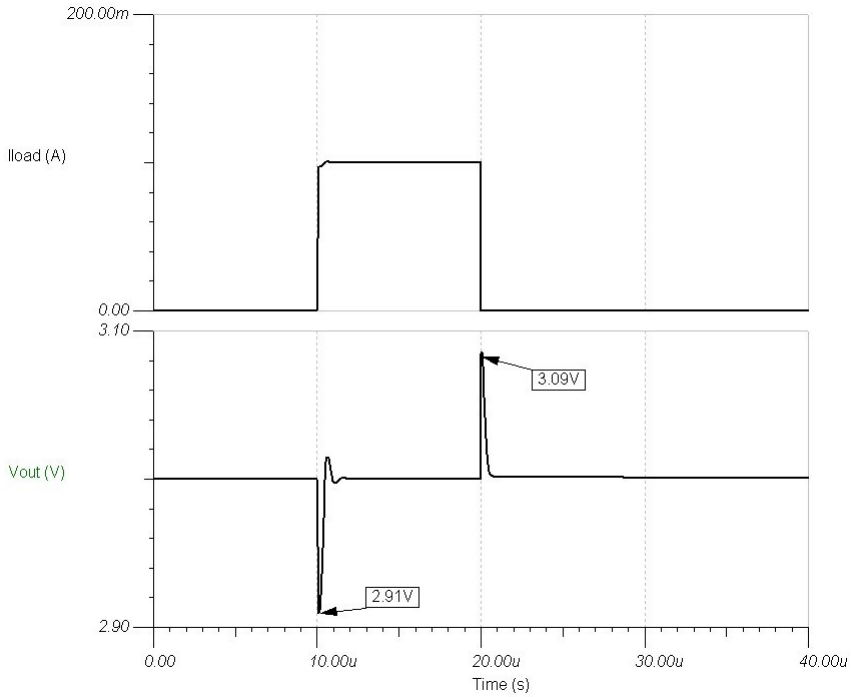

Figure 3.11 Load step response of the proposed LDO based on TL082 OPAMP

5) Start-up

Start-up test is performed by applying a supply voltage ramp to the LDO under test and observing its functionality. Figure 3.12 shows the start-up test response of the proposed LDO when the supply voltage ramps in 1 µS. The settling time for start-up test can be easily obtained from Figure 3.12 and it is around 30 µS.

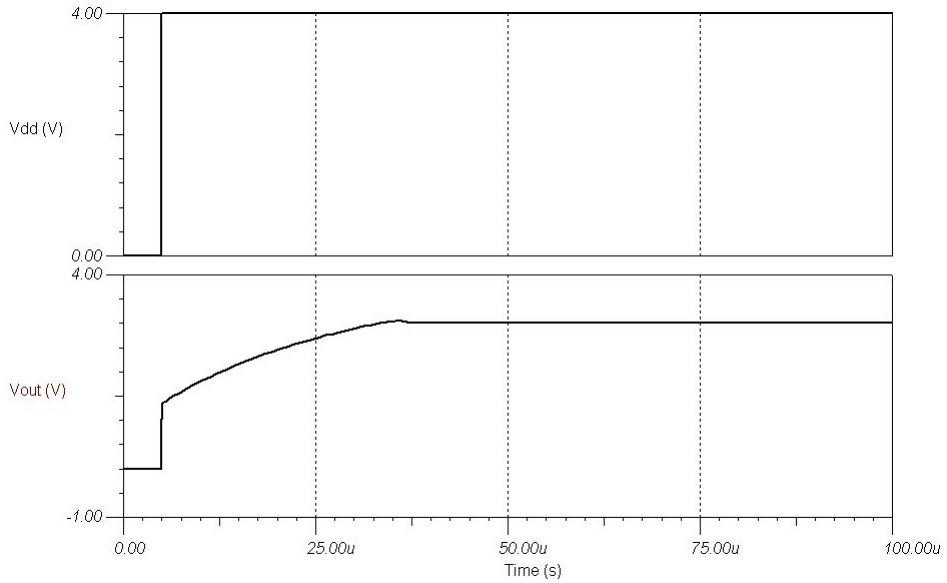

Figure 3.12 Startup of the LDO based on TL082 OPAMP

6) AC Stability

By cutting the loop at the non-inverting pin of error amplifier in Figure 3.7 and injecting small signal at the breaking point, the AC small signal stability of the proposed LDO can be analyzed. Figure 3.13 shows the simulation results of the AC stability. The three groups of curves represent Gain and Phase frequency characteristics under three loading conditions (0, 50 mA, 100 mA). The AC stability results are summarized in Table 3.4.

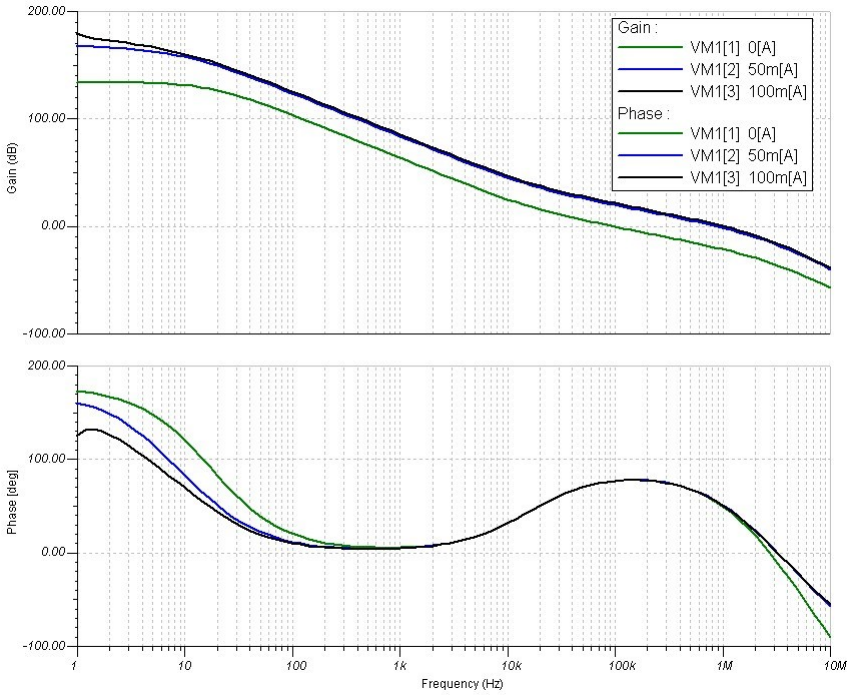

Figure 3.13 AC stability simulation of the LDO based on TL082 OPAMP

Table 3.4 AC Stability summary of the proposed LDO based on TL082 OPAMP

Load Current	Unity Gain Frequency	Phase Margin
0	97.8KHz	76.73
50mA	896.76KHz	54.67
100mA	1.03MHz	49.87

7) Power Supply Rejection (PSR)

PSR was performed by applying small signal perturbation in power supply within the entire frequency spectrum. As shown in Figure 3.14, the PSR of the proposed LDO keeps below -16dB from DC to 100 KHz and degrades worst around 1.5 MHz. The poor PSR characteristic of the proposed LDO mainly comes from the reference generation block

consisting of R_4 and Z_1 shown in Figure 3.7. The PSR of the reference generation block is simply equal to $\frac{Z(Z_1)}{Z(Z_1)+R_4}$ since Z_1 and R_4 actually form a voltage divider. ($Z(Z_1)$ is the impedance of diode Z_1).

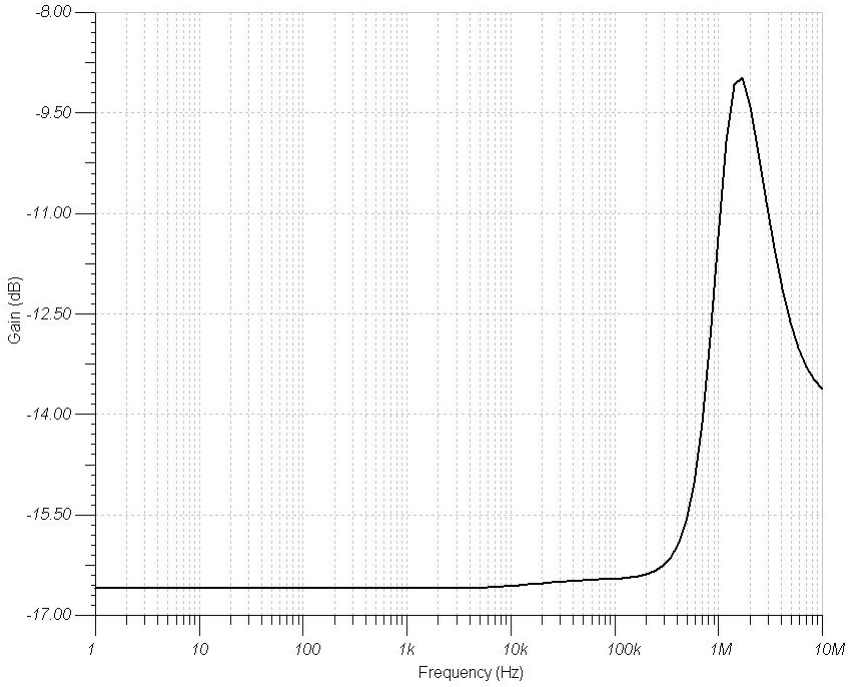

Figure 3.14 PSR simulation of the LDO based on TL082 OPAMP

3.2 Introduction to LM358 OPAMP

LM358 is a monolithic integrated circuit (IC) which includes two independent operational amplifiers consisting of bipolar transistors, diodes, resistors, and capacitors. It features wide supply range, low supply current, low input offset voltage and low input

bias current. The symbol and schematic of LM358 OPAMP are shown in Figure 3.15 and Figure 3.16.

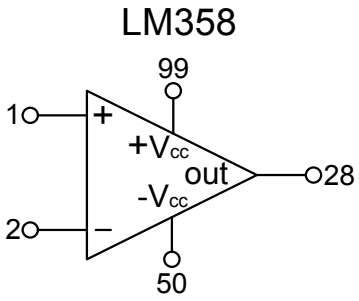

Figure 3.15 Symbol of LM358 OPAMP

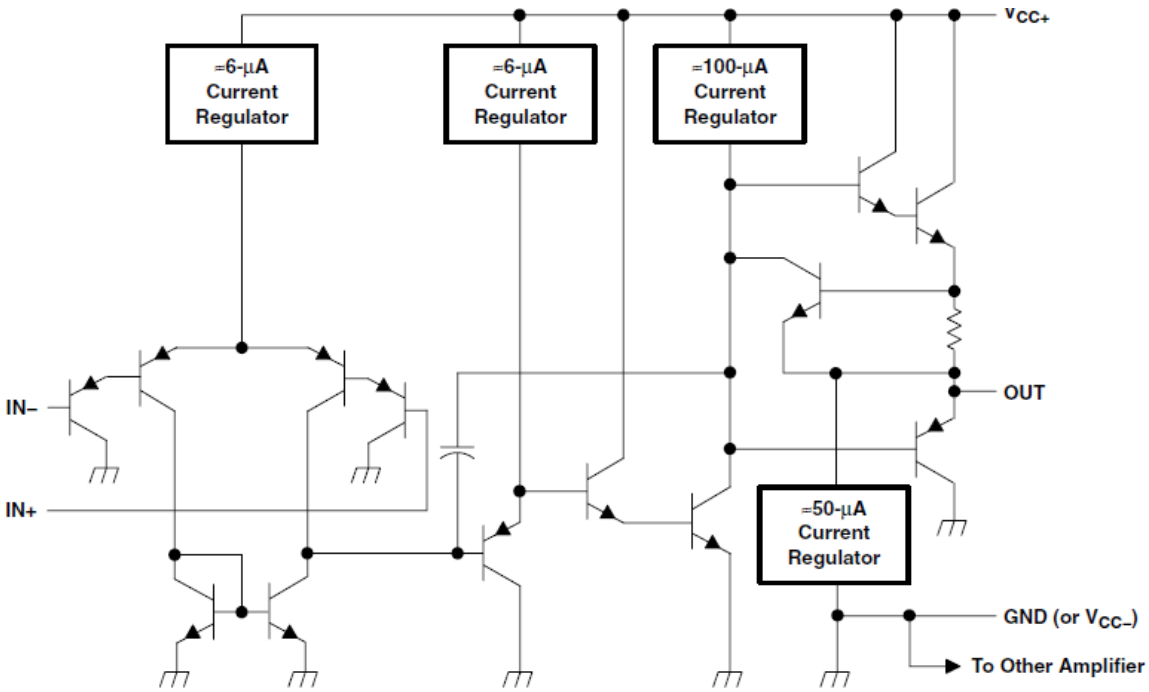

Figure 3.16 Schematic of LM358 OPAMP

The map between the schematic and symbol of LM358 OPAMP is shown in Table 3.5 as below:

Table 3.5 The Map Between the schematic and symbol of LM358 OPAMP

Pin Name in Schematic	Pin Name in Symbol	Remarks
IN +	1	Non-inverting Input
IN -	2	Inverting Input
VCC +	99	Positive Supply Voltage
VCC -	50	Negative Supply Voltage
OUT	28	Output Voltage

In order to characterize the performance of LM358 OPAMP, a macro model is given here in Figure 3.17 as below:

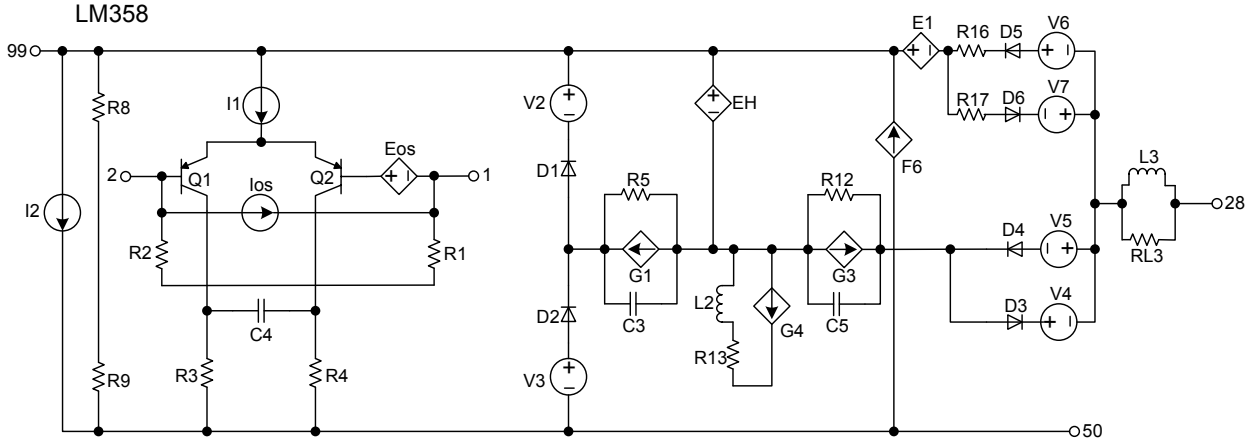

Figure 3.17 Macro model of LM358 OPAMP

The first stage consists of Q_1, Q_2, C_4, R_3, and R_4, while C_3, R_5, and G_3 form the dominant pole stage.

3.2.1 **The AC analysis of LM358 OPAMP**

As shown in Figure 3.18, the input stage of LM358 OPAMP consists of two bipolar transistors Q_1, Q_2, capacitor C_4, resistor R_3, and R_4. The non-dominant pole P_2 can be expressed as below:

$$P_2 = \frac{1}{(R_3 + R_4)C_4} \tag{3.8}$$

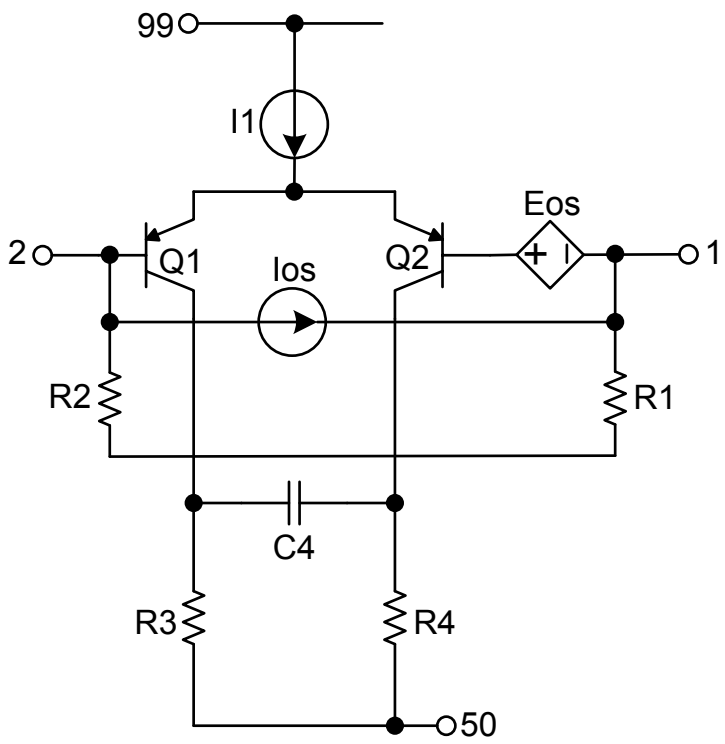

Figure 3.18 Simplified first stage macro model of LM358 OPAMP

The dominant pole is generated by resistor R_5, capacitor C_3, and voltage controlled current source G_3. As shown in Figure 3.19, the dominant pole is expressed as below:

$$P_{-3dB} = \frac{1}{R_5 C_3} \tag{3.9}$$

G_3, C_5, R_{12} generate the non-dominant pole P_3 like below:

$$P_3 = \frac{1}{R_{12} C_5} \tag{3.10}$$

G_4, L_2, R_{13} generate the zero Z_1 like below:

$$Z_1 = \frac{R_{13}}{L_2} \tag{3.11}$$

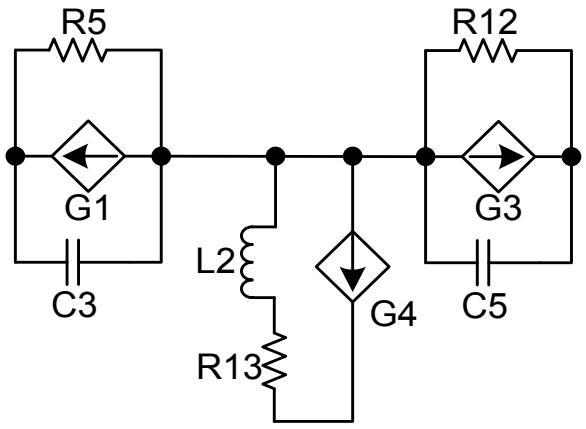

Figure 3.19 Simplified intermediate stage macro model of LM358 OPAMP

In order to verify the AC analysis of the LM358 OPAMP, a simulation was performed by using TI TINA tools. The test bench of the simulation is shown in Figure 3.20.

The simulation result and performance summary are shown in Figure 3.21 and Table 3.6, respectively.

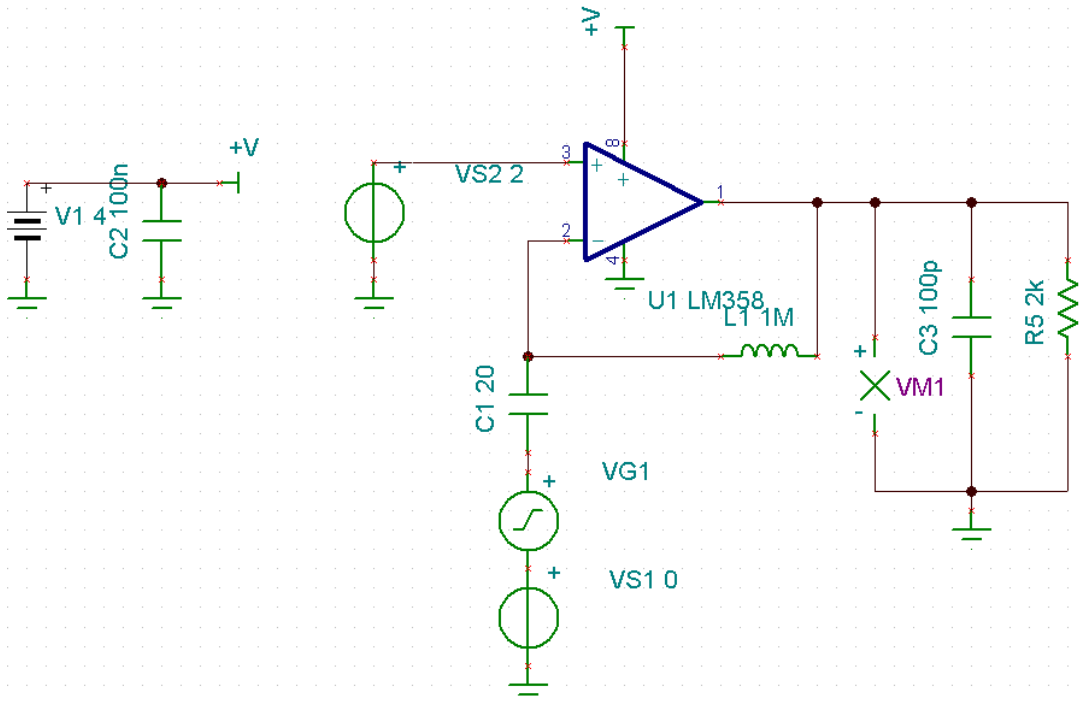

Figure 3.20 AC analysis test bench of the LM358 OPAMP in TI TINA

Table 3.6 The performance summary of LM358 OPAMP

Specs	Value	Remarks
Adc	100dB	DC Voltage Gain
UGF	786KHz	Unity-Gain Frequency
P_{-3dB}	7.86Hz	Dominant Pole

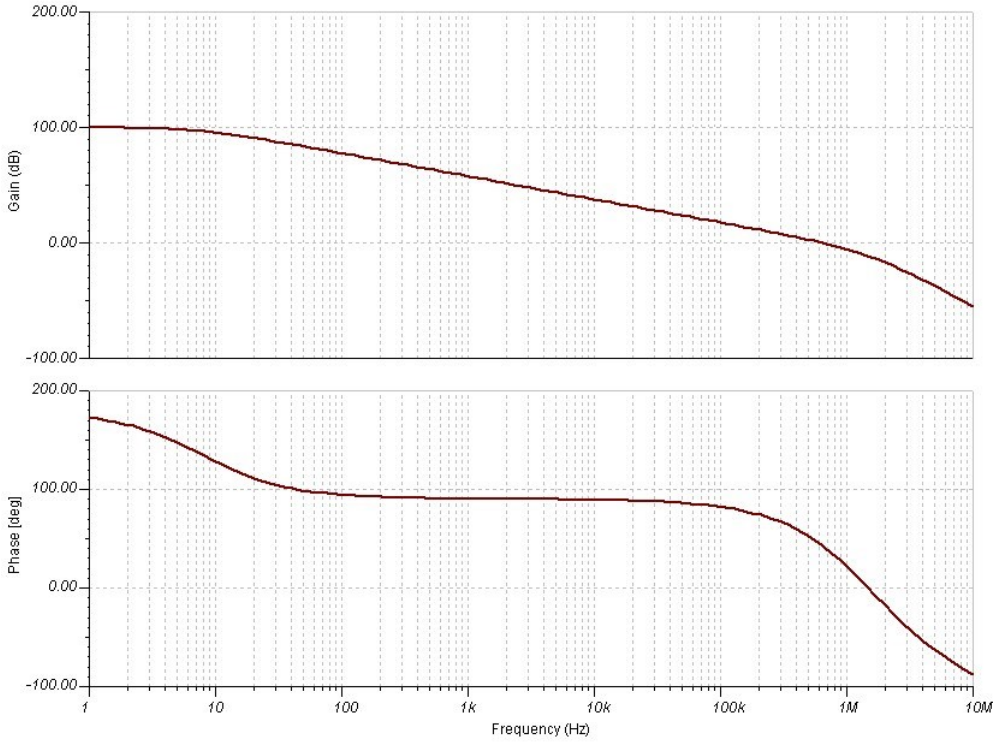

Figure 3.21 AC analysis simulation of the LM358 OPAMP in TI TINA

3.2.2 **The Proposed Discrete LDO Based on LM358 OPAMP**

A reference LDO design based on LM358 OPAMP is given below to validate the implemented LDO on ASLK Pro design kits. The main summary of performance is listed in Table 3.7 as below:

Table 3.7 Performance of the proposed LDO based on LM358 OPAMP

Technology	Discrete Components
Input Voltage (Vin)	4V
Output Voltage (Vout)	3V
Output Current	100mA
Line Regulation	130mV/V@100mA
Load Regulation	-4.77μV/mA@Vin=4V
Output Capacitance	10μF
ESR Resistor	1Ω
PSRR (1-100KHz)	-16.59dB @1KHz -16.43dB @10KHz -16.25dB @100KHz

Here, a monolithic LM358 OPAMP, a Zener diode MZPD2.7, and a PMOSFET IRFU9222 are used to build the LDO and function as error amplifier, voltage reference, and pass element, respectively. The schematic of the LDO is shown in Figure 3.22 as below:

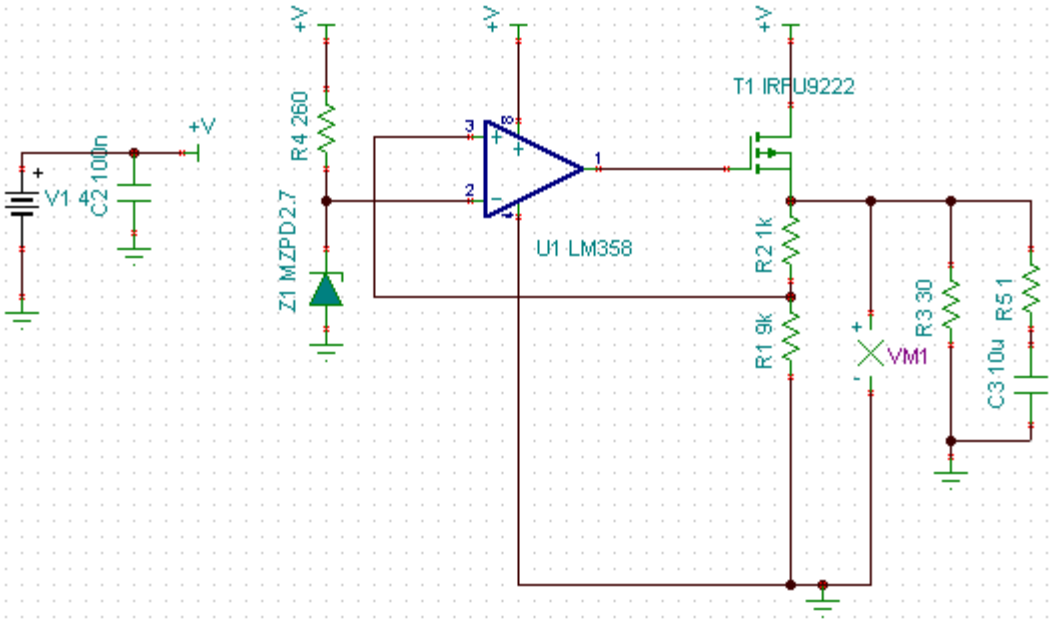

Figure 3.22 Schematic of the LDO based on LM358 OPAMP

In addition to the error amplifier, voltage reference, and pass element mentioned above, the resistor string which functions as voltage divider is implemented by resistor R_2 and R_1. C_3 and R_5 are adopted as output load capacitor and ESR resistor. R_3 is used to model the load current.

3.2.3 **The Performance of the Proposed Discrete LDO Based on LM358 OPAMP**

In order to verify the performance of the proposed LDO, a bunch of simulations were performed with different test benches. These simulations are classified into three categories:

i). Static Characteristics (Line Regulation/ Load Regulation)

ii). Dynamic Characteristics (Line Step Response/ Load Step Response /Start-up)

iii). AC Small Signal Characteristics (Stability/ Power Supply Rejection (PSR))

Next, these important characteristics were validated by performing various simulations accordingly.

1) Line Regulation

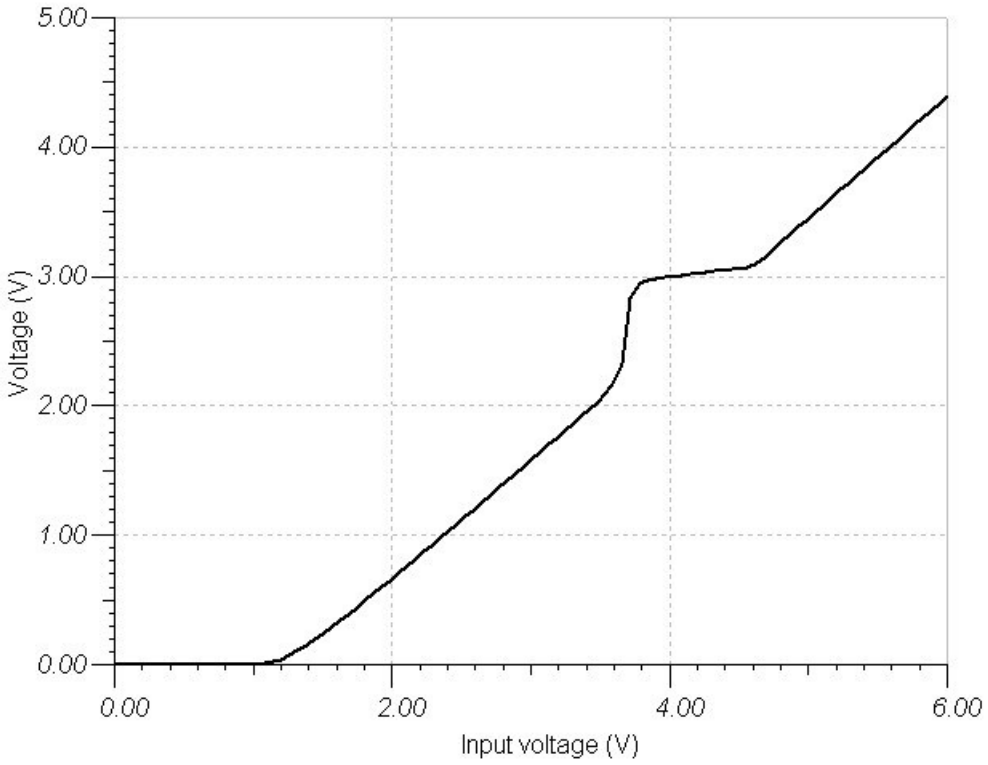

Figure 3.23 Line regulation of the proposed LDO based on LM358 OPAMP

Figure 3.23 shows the line regulation simulation of the proposed LDO. The line regulation can be easily calculated by applying equation (2.11).

2) Load Regulation

Load regulation is shown in Figure 3.24 and can be calculated by applying equation (2.12). As shown in Figure 3.24, the maximum load current of the proposed LDO based on LM358 OPAMP is around 150 mA.

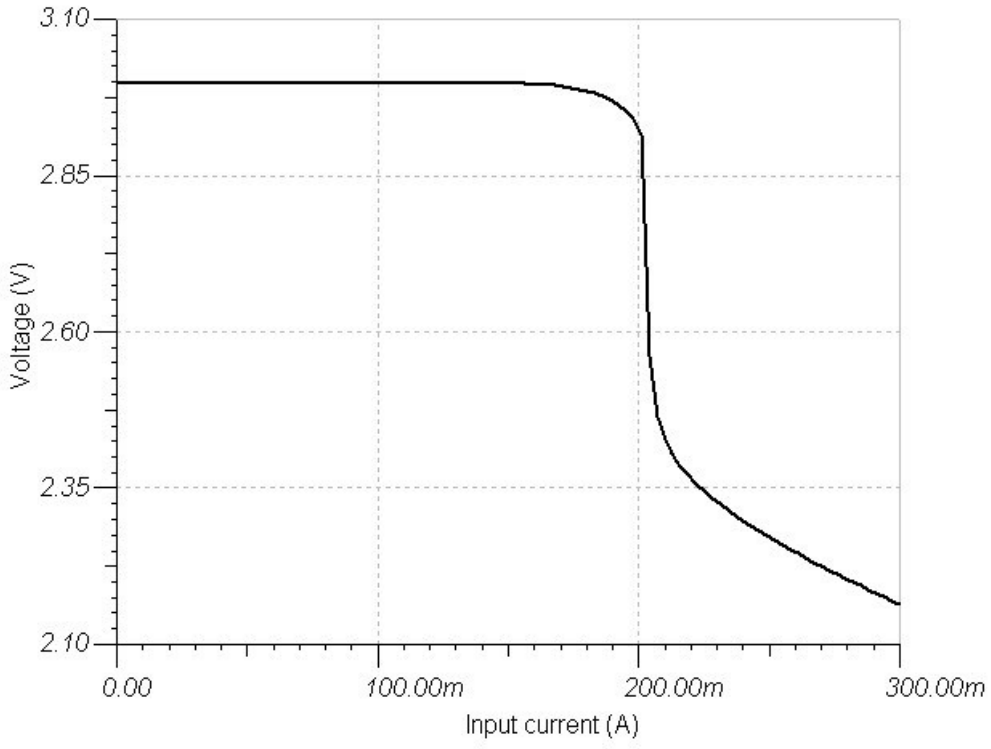

Figure 3.24 Load regulation of the proposed LDO based on LM358 OPAMP

3) Line Step Response

Line step response simulation was performed by applying DC supply voltage with a square wave perturbation. As shown in Figure 3.25, when a peak-to-peak 200 mV square wave was applied on supply voltage, the LDO output voltage underwent a ripple of about 36 mV.

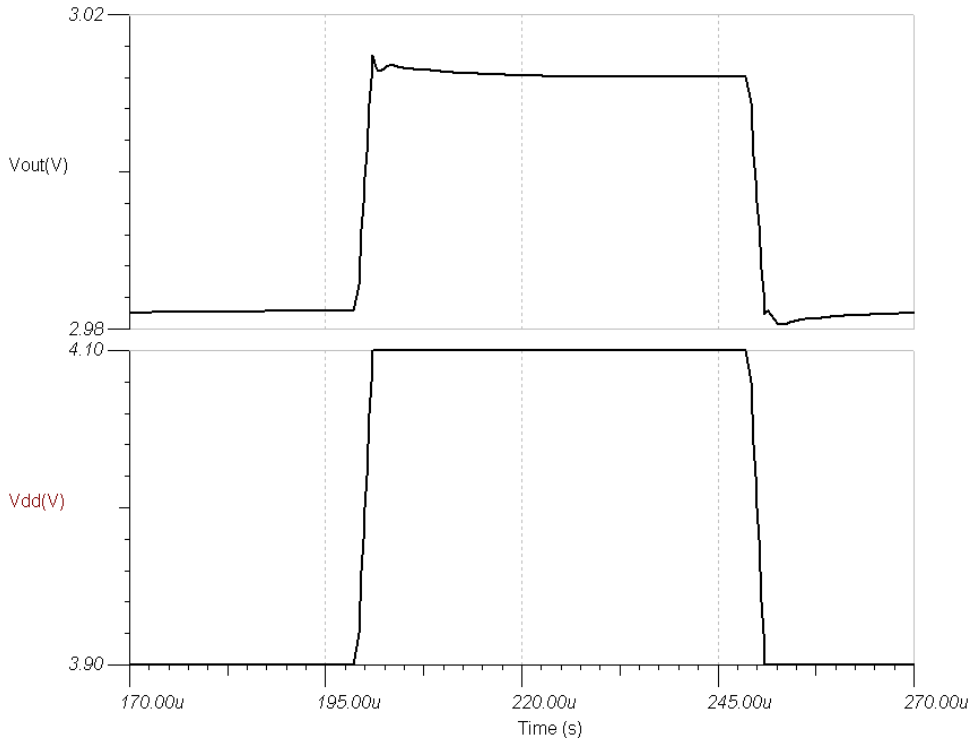

Figure 3.25 Line step response of the proposed LDO based on LM358 OPAMP

4) Load Step Response

A sudden load current change is applied to the LDO output to perform load step response. Figure 3.26 shows the load step response of the proposed LDO when a sudden load current change (100 mA) is applied to the LDO output. From the simulation results, the undershoot and overshoot voltages of the proposed LDO are 100 mV and 92 mV, respectively. Also, the settling times for both undershoot and overshoot are around 4 µS.

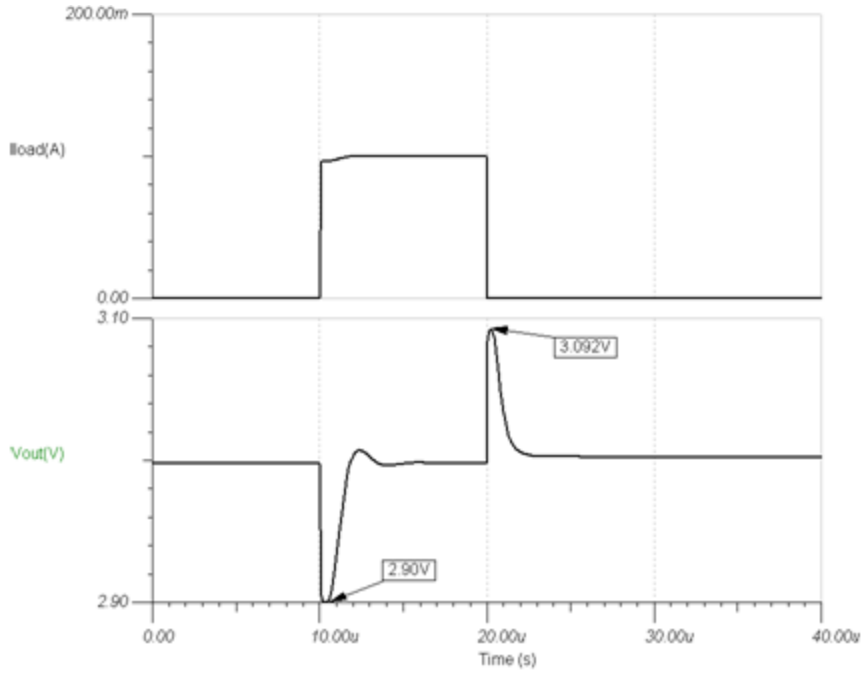

Figure 3.26 Load step response of the proposed LDO based on LM358 OPAMP

5) Start-up

Start-up test is performed by applying a supply voltage ramp to the LDO under test and observing its functionality. Figure 3.27 shows the start-up test response of the proposed LDO when the supply voltage ramps in 1 µS. The settling time for start-up test can be easily obtained from Figure 3.27 and it is around 130 µS.

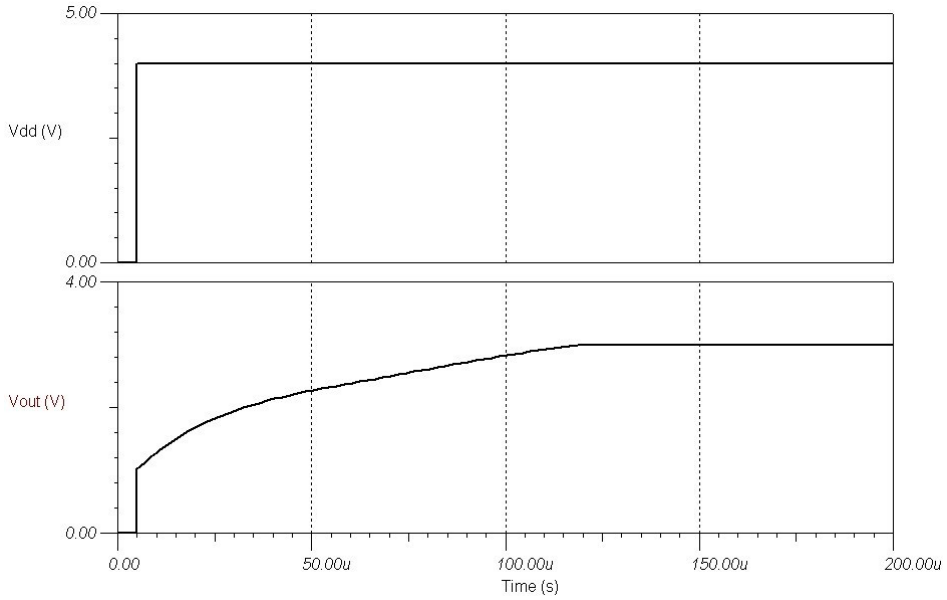

Figure 3.27 Startup of the LDO based on TL082 OPAMP

6) AC Stability

By cutting the loop at the non-inverting pin of error amplifier in Figure 3.22 and injecting small signal at the breaking point, the AC small signal stability of the proposed LDO can be analyzed. Figure 3.28 shows the simulation results of the AC stability. The three groups of curves represent Gain and Phase frequency characteristics under three loading conditions (0, 50 mA, 100 mA). The AC stability results are summarized in Table 3.8.

Table 3.8 AC Stability summary of the proposed LDO based on LM358 OPAMP

Load Current	Unity Gain Frequency	Phase Margin
0	25.83KHz	54.65
50mA	210.33KHz	54.93
100mA	253.77KHz	49.24

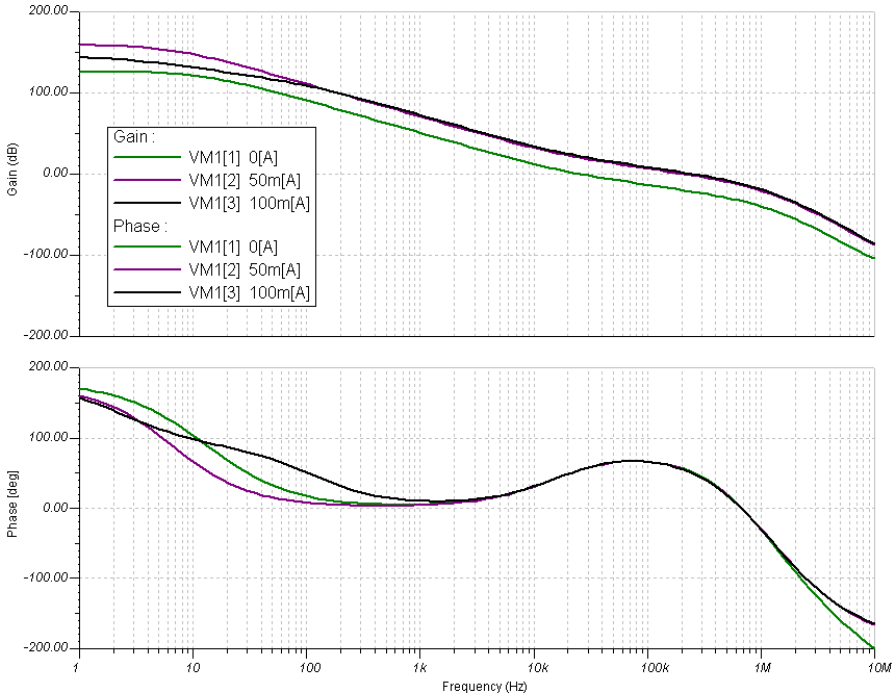

Figure 3.28 AC stability simulation of the LDO based on LM358 OPAMP

7) Power Supply Rejection (PSR)

PSR was performed by applying small signal perturbation in power supply within the entire frequency spectrum. As shown in Figure 3.29, the PSR of the proposed LDO keeps below -16dB from DC to 100 KHz and degrades from 300 KHz. The poor PSR characteristic of the proposed LDO mainly comes from the reference generation block consisting of R_4 and Z_1 shown in Figure 3.22. The PSR of the reference generation block is simply equal to $\frac{Z(Z_1)}{Z(Z_1)+R_4}$ since Z_1 and R_4 actually form a voltage divider. ($Z(Z_1)$ is

the impedance of diode Z_1).

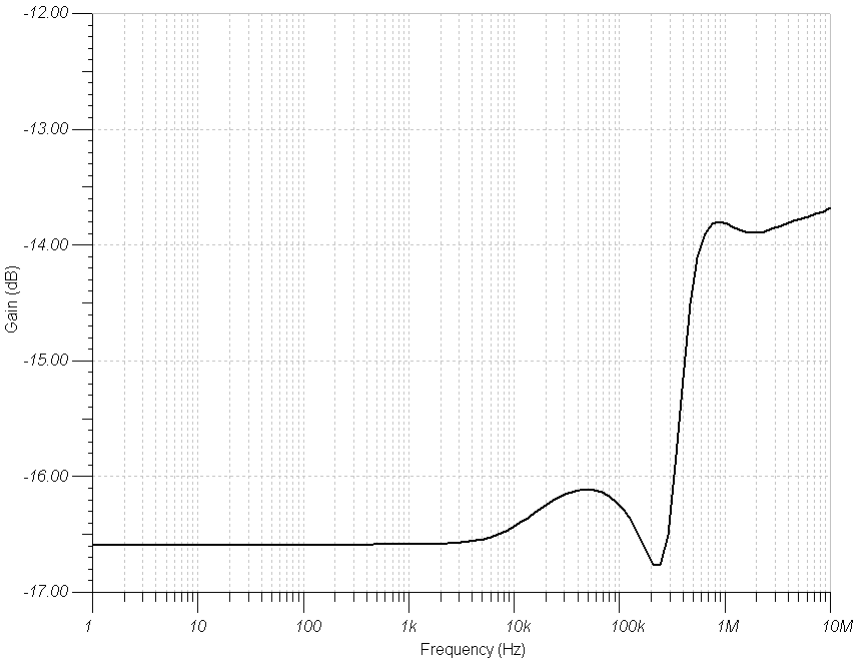

Figure 3.29 PSR simulation of the LDO based on LM358 OPAMP

Chapter 4 System model of the proposed LDOs

The system model of LDO is crucial for the top level simulation and verification of a SoC (System on Chip) system design because the system designer could easily make use of the reusable IP block model to identify and verify the system's performance requirements. Moreover, the flexibility of the system model provides system designer more freedom to optimize the system's performance and dynamic response. Meanwhile, the conciseness of the system model facilitates the system simulation and results in improvement on design efficiency.

4.1 System model of the TL082 based LDO

The whole system of LDO can be modeled as a negative feedback system shown in Figure 4.1:

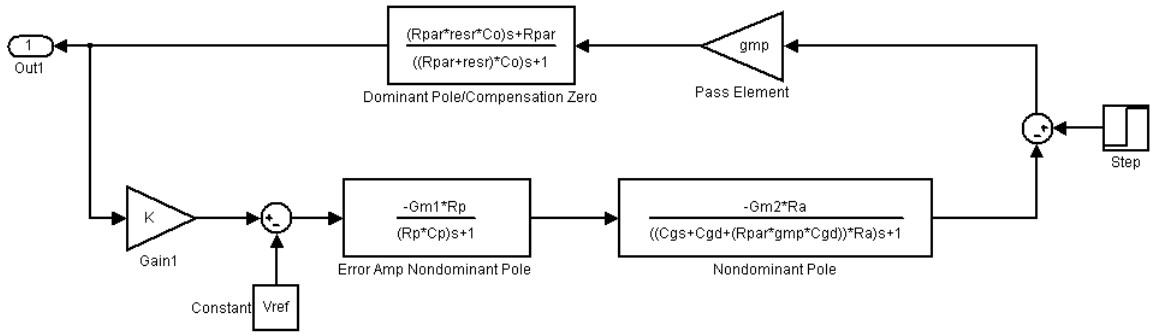

Figure 4.1 System model of the proposed LDO

where

G_{m1}: The error amplifier's 1st stage transconductance

G_{m2}: The 2nd stage transconductance of the error amplifier

R_p: The output resistance of the error amplifier's 1st stage

C_p: The output parasitic capacitance of the error amplifier's 1st stage

R_A: The output resistance of the error amplifier's 2nd stage

C_{gs}: Gate-source capacitance of the pass element transistor

C_{gd}: Gate-drain capacitance of the pass element transistor

g_{mp}: The transconductance of the pass element transistor

R_{par}: The output impedance of the LDO

C_o: The output capacitance

K: Feedback factor

Here, the error amplifier is modeled based on a two-stage structure which has a total gain of $G_{m1}G_{m2}R_pR_A$. K is the feedback factor of $\frac{R_1}{R_1 + R_2}$.

4.1.1 **AC stability over load conditions analysis on TL082 LDO system model**

By fitting the variables in the model with the design parameters in section 3.1.3, we can work out the values for the variables and make use of the models to predict the performance of the LDO. Figure 4.2 is AC stability simulation result of the proposed TL082 LDO based on the system model of the LDO.

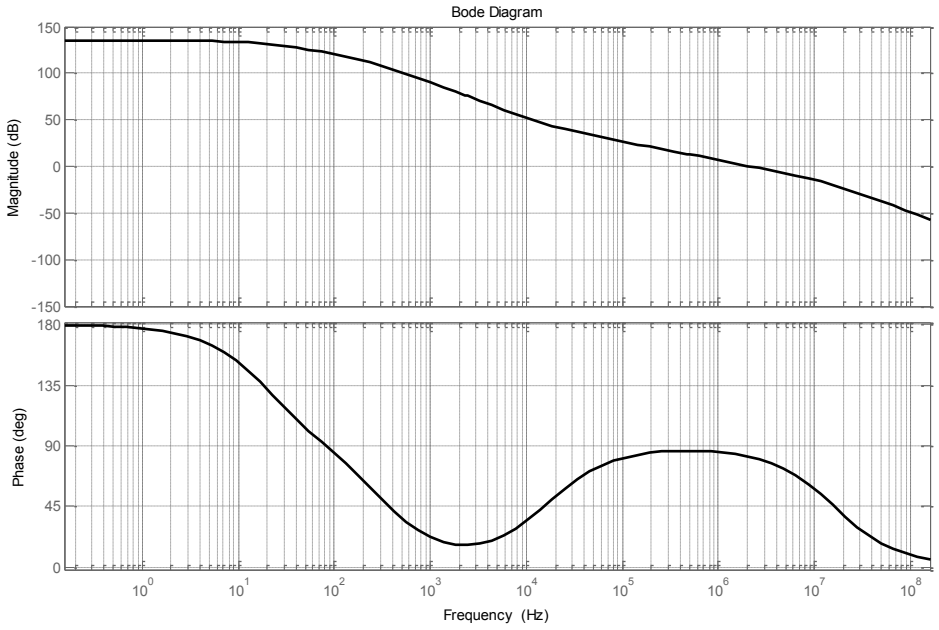

Figure 4.2 AC stability simulation result of the proposed TL082 LDO

A similar ac stability simulation under three different loading conditions (0, 50 mA, 100 mA) can also be obtained by varying the output impedance of the LDO R_{par}. The corresponding simulation results are shown in Figure 4.3.

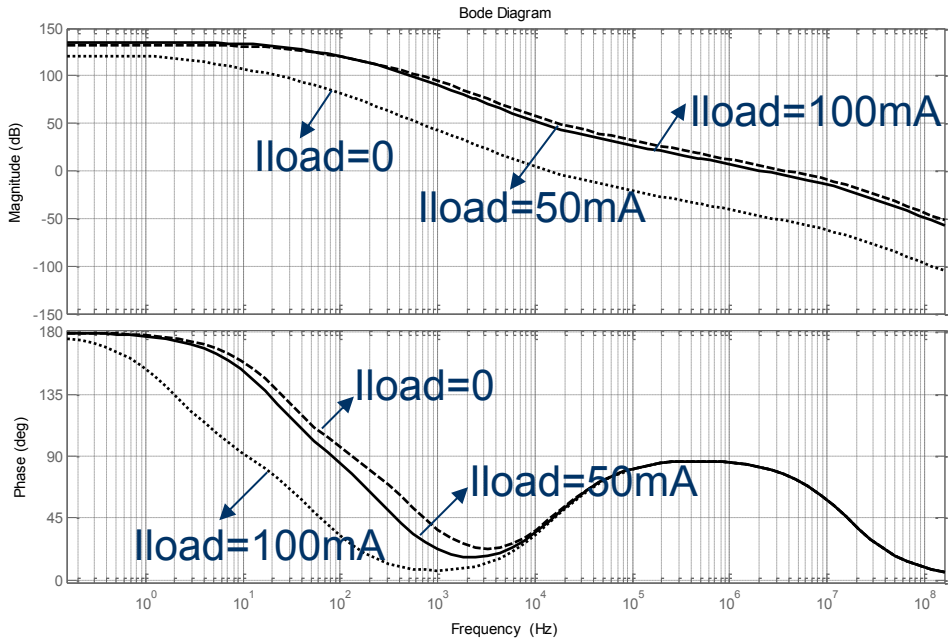

Figure 4.3 AC stability simulation result of the proposed TL082 LDO at 0mA/50mA/100mA load current

4.1.2 **AC stability over output capacitor analysis on TL082 LDO system model**

In addition to the analysis of the proposed LDO's ac stability over loading conditions, the ac stability over output capacitor should also be analyzed since the output capacitor normally dominates the stability of the LDO and transient performance.

As indicated in section 2.1 and equations from (2.6) to (2.10), the dominant pole p_1 and LHP zero Z_1 are both generated from the external output capacitor. Hence, the analysis of the proposed LDO stability over output capacitor is crucial for the application of the proposed LDO since the effective output capacitor range could be investigated and listed for the safe operation of the LDO.

By sweeping the output capacitor from 1 μF to 100 μF and recording the corresponding phase margin of the LDO system, the ac stability over output capacitor is shown in Figure 4.4 as below:

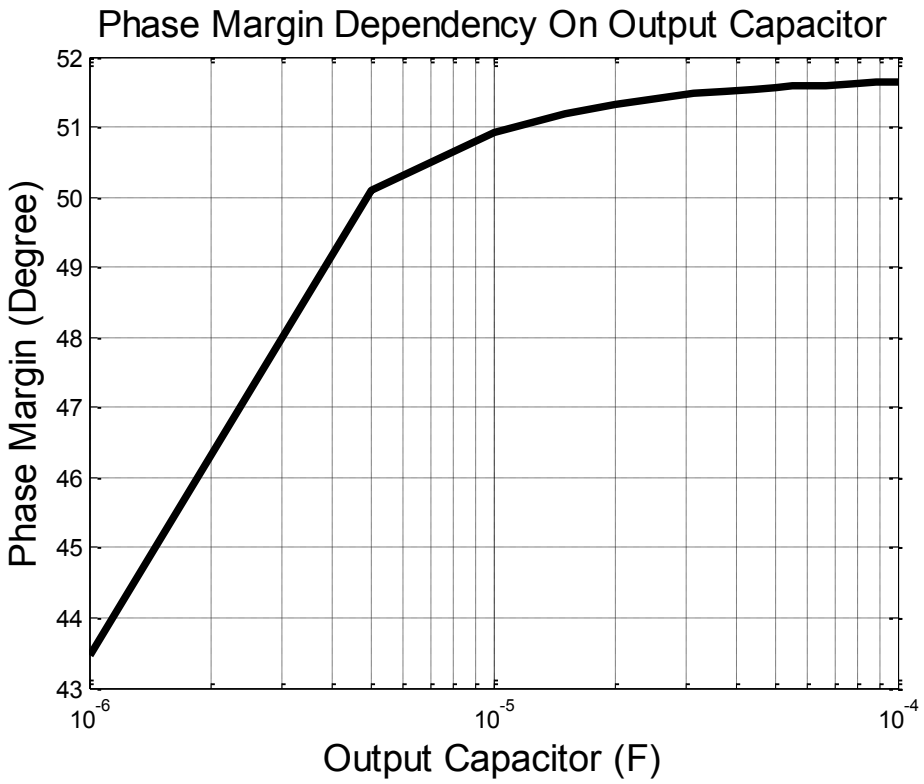

Figure 4.4 AC stability simulation result of the proposed TL082 LDO for different external output caps (ESR=1Ω)

As shown in Figure 4.4, we can conclude that the stability of the proposed LDO becomes better with the larger output capacitor. However, the large output capacitor normally occupies large PCB (Printed Circuit Board) area and its cost is more expensive. Moreover, the large capacitor results in longer setting time because of large RC time constant. Therefore, the choice of the output capacitor has to be made carefully.

4.1.3 **AC stability over output capacitor ESR based on TL082 LDO system model**

As discussed in the above section, LHP zero Z_1 is generated from output capacitor as well its ESR. The stability of the proposed LDO can be guaranteed by carefully allocating the location of zero which is set by the output capacitor C_O and its ESR. Here, a simulation is performed by sweeping ESR value from 0.1Ω to 5Ω and the simulation results are shown in Figure 4.5:

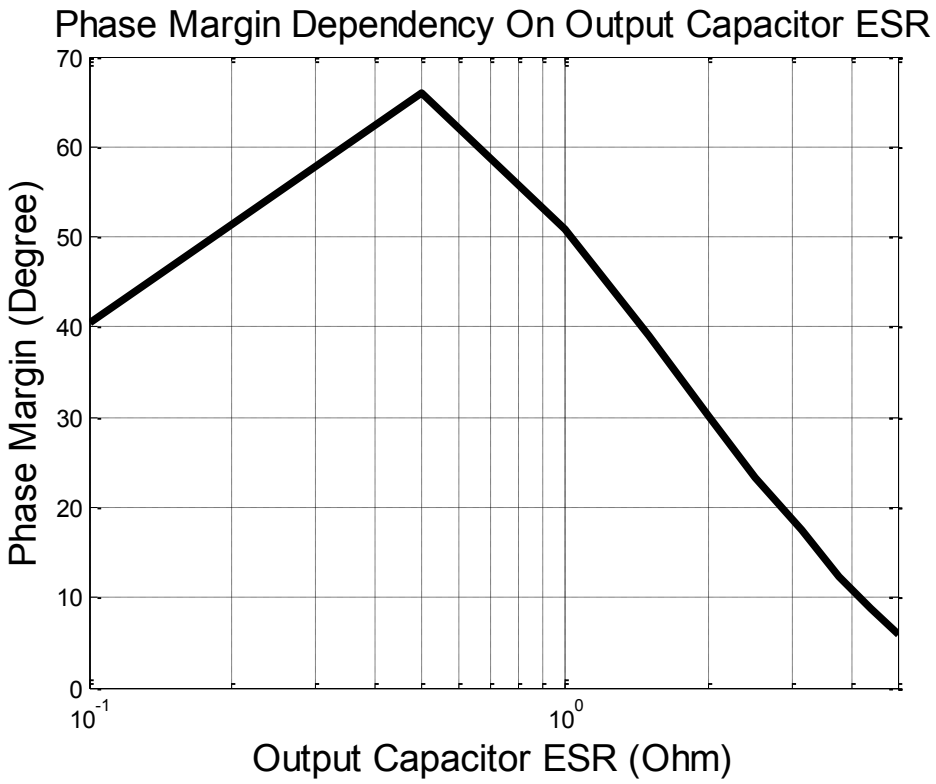

Figure 4.5 AC stability simulation result of the proposed TL082 LDO for different output capacitor ESR (C_O = 10 μF)

From the simulation shown in Figure 4.5, it is obvious that there is an optimum ESR of 0.5Ω to maximize phase margin (66° when ESR = 0.5Ω). However, the ESR value of output capacitor is difficult to be exactly determined due to variations from manufacturing process, package, and operational environment such as temperature, humidity, etc. Therefore, an ESR value range is necessary to implement stable operation of the proposed LDO. For safe operation of the proposed LDO, a phase margin above 50° has to be achieved. The ESR range is thus able to be determined from 0.2Ω to 1Ω.

4.2 System model of the LM358 based LDO

The system model of the LM358 based LDO can be modeled as same as the one in Figure 4.1. We still need to analyze the stability of the proposed LDO over load conditions, output capacitor, and ESR of output capacitor.

4.2.1 **AC stability over load conditions analysis on LM358 LDO system model**

By fitting the variables in the model with the design parameters in section 3.3.2, we can work out the values for the variables and make use of the models to predict the performance of the LDO. Figure 4.6 is AC stability simulation result of the proposed LM358 LDO based on the system model of the LDO.

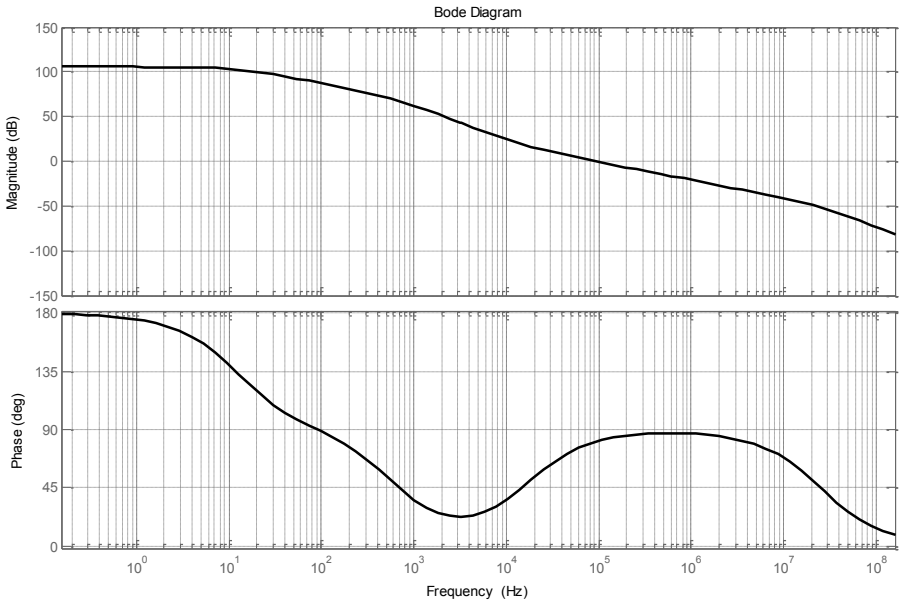

Figure 4.6 AC stability simulation result of the proposed LM358 LDO

A similar ac stability simulation under three different loading conditions (0, 50 mA, 100 mA) can also be obtained by varying the output impedance of the LDO R_{par}. The corresponding simulation results are shown in Figure 4.7.

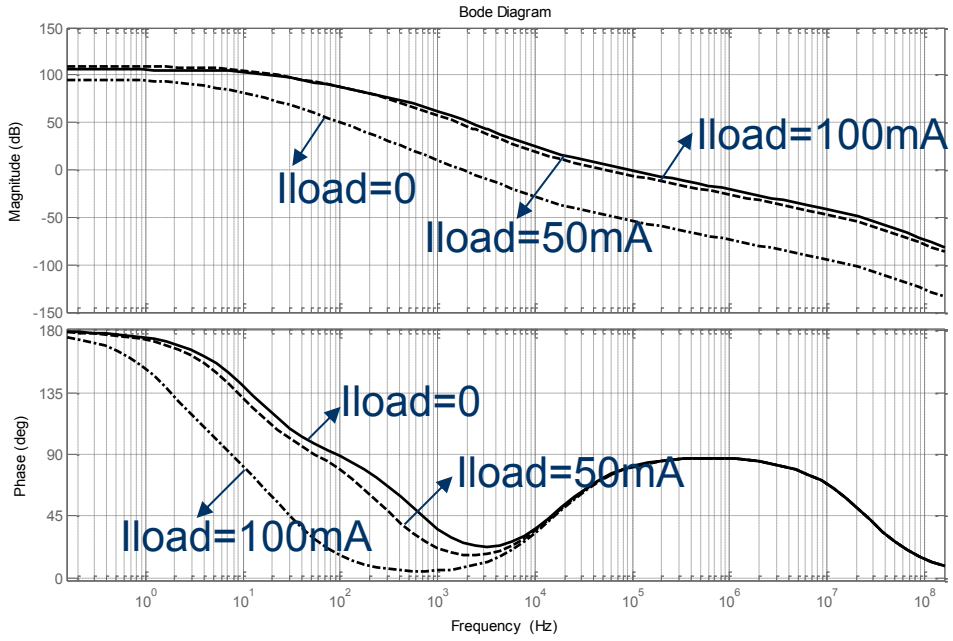

Figure 4.7 AC stability simulation result of the proposed LM358 LDO at 0mA/50mA/100mA load current

4.2.2 **AC stability over output capacitor based on LM358 LDO system model**

In addition to the analysis of the proposed LDO's ac stability over loading conditions, the ac stability over output capacitor should also be analyzed since the output capacitor normally dominates the stability of the LDO and transient performance.

As indicated in section 2.1 and equations from (2.6) to (2.10), the dominant pole p_1 and LHP zero Z_1 are both generated from the external output capacitor. Hence, the analysis of the proposed LDO stability over output capacitor is crucial for the application of the proposed LDO since the effective output capacitor range could be investigated and listed

for the safe operation of the LDO.

By sweeping the output capacitor from 1 μF to 100 μF and recording the corresponding phase margin of the LDO system, the ac stability over output capacitor is shown in Figure 4.8 as below:

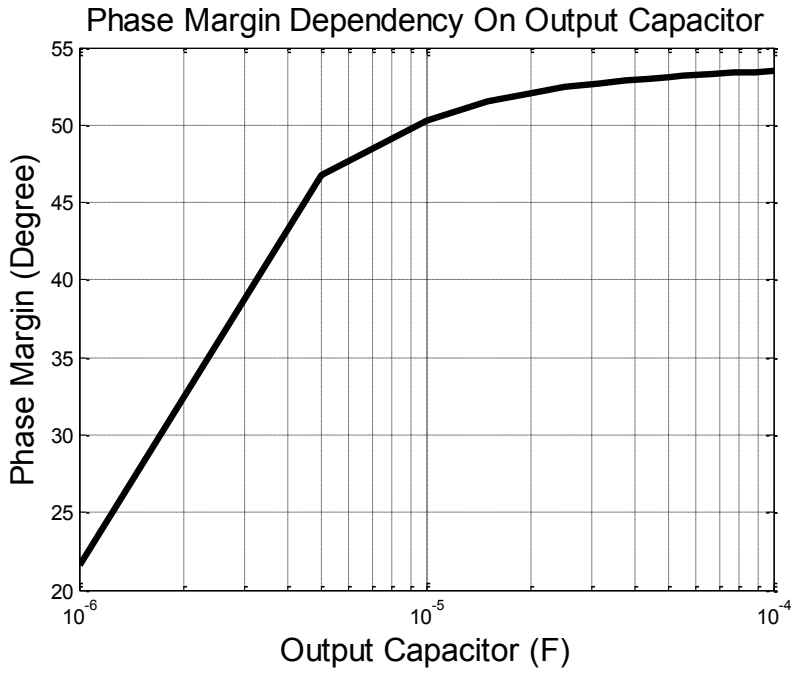

Figure 4.8 AC stability simulation result of the proposed LM358 LDO for different external output caps (ESR=1Ω)

As shown above, we can conclude that the stability of the proposed LDO becomes better with the larger output capacitor. However, the large output capacitor normally occupies large PCB area and its cost is more expensive. Moreover, the large capacitor results in longer setting time because of large RC time constant. Therefore, the choice of the output capacitor has to be made carefully.

4.2.3 **AC stability over output capacitor ESR based on LM358 LDO system model**

As discussed in the above section, LHP zero Z_1 is generated from output capacitor as well its ESR. The stability of the proposed LDO can be guaranteed by carefully allocating the location of zero which is set by the output capacitor C_O and its ESR. Here, a simulation is performed by sweeping ESR value from 0.1Ω to 5Ω and the simulation results are shown in Figure 4.9:

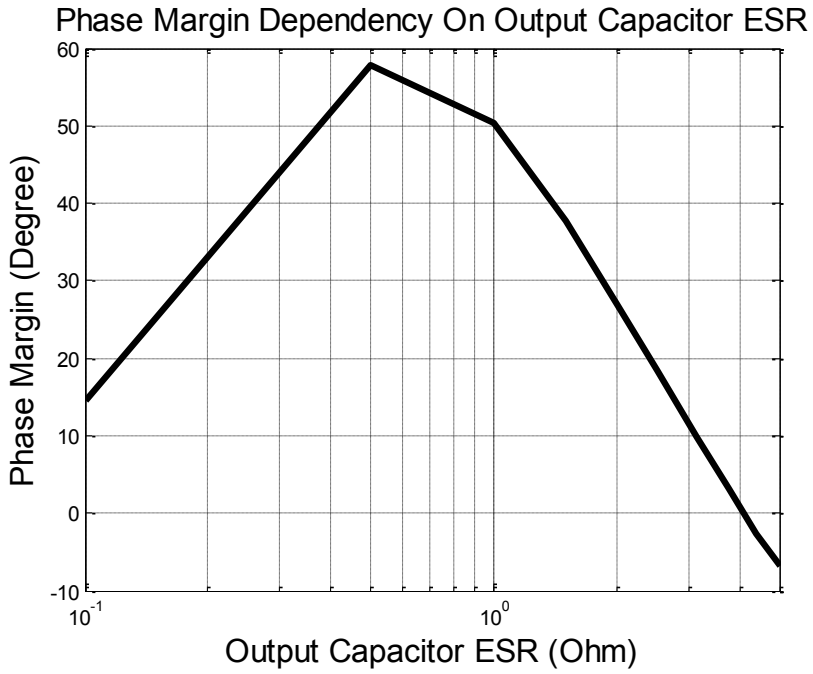

Figure 4.9 AC stability simulation result of the proposed LM358 LDO for different output capacitor ESR (C_O = 10 μF)

From the simulation shown in Figure 4.9, it is obvious that there is an optimum ESR of 0.5Ω to maximize phase margin (58° when ESR = 0.5Ω). However, the ESR value of

output capacitor is difficult to be exactly determined due to variations from manufacturing process, package, and operational environment such as temperature, humidity, etc. Therefore, an ESR value range is necessary to implement stable operation of the proposed LDO. For safe operation of the proposed LDO, a phase margin above 50° has to be achieved. The ESR range is thus able to be determined from 0.4Ω to 1Ω.

4.3 PSR models of the proposed LDOs (TL082 and LM358)

Power Supply Rejection (PSR) is an important characteristic of LDO since this parameter is used to measure LDO's capability to suppress the noise from supply voltage within the entire frequency spectrum. It is a very useful metric for screening the proper devices for target applications such as clean DC voltage generation with noisy power supply. Figure 4.10 describes the model for PSR analysis of the conventional LDO in section 2.1.

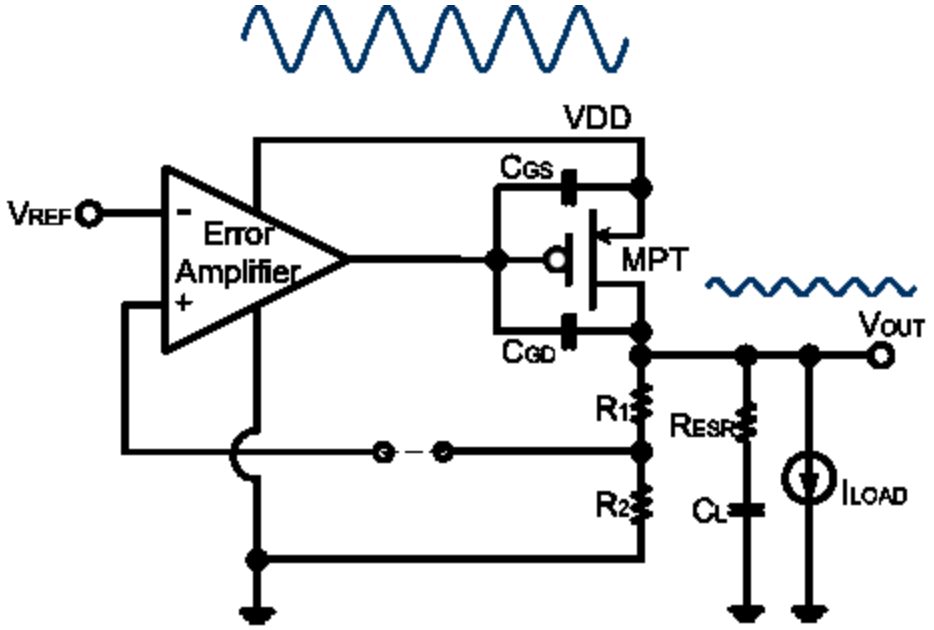

Figure 4.10 Model for PSR analysis of the conventional LDO

As shown in Figure 4.10, there are four main paths from supply voltage VDD to LDO output V_{out} [34]:

1. From Error Amplifier (PSR_1)
2. From Vref Block (Normally Bandgap Reference PSR_2)
3. The conductance of the pass element MPT (PSR_3)
4. The feedback loop (PSR_4)

The total PSR of the conventional LDO is the sum of the four main paths:

$$PSR_{LDO} = PSR|_{1,2} + PSR|_{3,4} \tag{4.1}$$

Next, let's discuss the $PSR|_{1,2}$ and $PSR|_{3,4}$, respectively.

4.3.1 $PSR|_{1,2}$ model of the proposed LDO

The finite PSR of error amplifier and reference block both degrade the overall PSR performance of LDO by modulating themselves into the system transfer function. There are many papers addressing the LDO design with high PSRR error amplifier. Also, many high PSRR voltage reference designs were presented. Since PSR of error amplifier and reference block both contribute to the overall PSR in similar way, $PSR|_{1,2}$ can be expressed as

$$PSRR_{1,2} = \frac{g_{mp} R_{par} A_{err\_amp}}{1 + K A_{err\_amp} g_{mp} R_{par}} (PSRR_{EA} + PSR_{BGR}) \tag{4.2}$$

where A_{err_amp} is the voltage gain of the error amplifier, and $PSRR_{EA}$, PSR_{BGR} are PSR of the error amplifier and voltage reference (bandgap reference) respectively. Therefore, the model for $PSR|_{1,2}$ (from error amplifier and voltage reference) is shown in Figure 4.11.

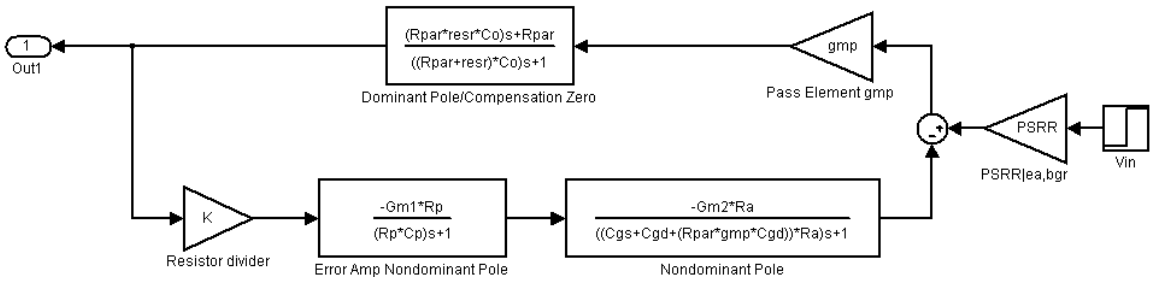

Figure 4.11 Model for $PSR|_{1,2}$ (from error amplifier and voltage reference)

4.3.2 $PSR|_{3,4}$ model of the proposed LDO

$PSR|_{3,4}$ represent the PSR from the finite conductance of the pass element MPT and the feedback loop. With the rapid advancement of manufacturing process, the PSR from the finite conductance of the pass element is becoming significant due to the shrinking feature size of the transistor. The PSR from the feedback loop is determined by the open-loop gain of the loop. Hence, $PSR|_{3,4}$ can be expressed as

$$PSR_{3,4} = \frac{1 + g_{mp} rds}{1 + KA_{err\_amp} g_{mp} rds + \frac{rds}{R_{par}}} \tag{4.3}$$

where r_{ds} is the channel resistance of the pass element MPT.

Figure 4.12 shows the model for $PSR|_{3,4}$ (from the conductance of the pass element MPT and the feedback loop).

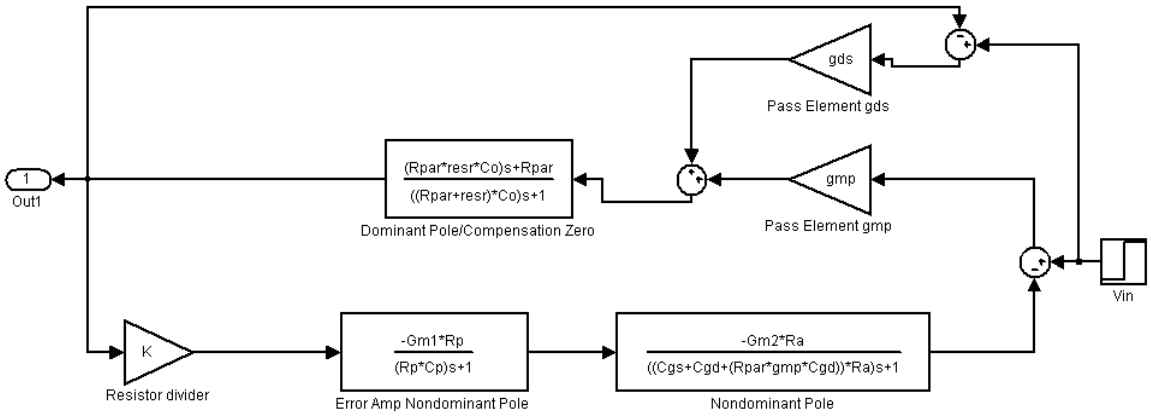

Figure 4.12 Model for $PSR_{3,4}$ (from the conductance of the pass element MPT and the feedback loop)

4.3.3 *PSR* model of the proposed LDO based on TL082 OPAMP

Based on the models in section 4.3.1 and 4.3.2 as well as equation (4.1), an overall AC simulation can be performed to predict the PSR characteristic of the proposed LDO. Figure 4.13 shows the simulation result for PSR of TL082 OPAMP based LDO.

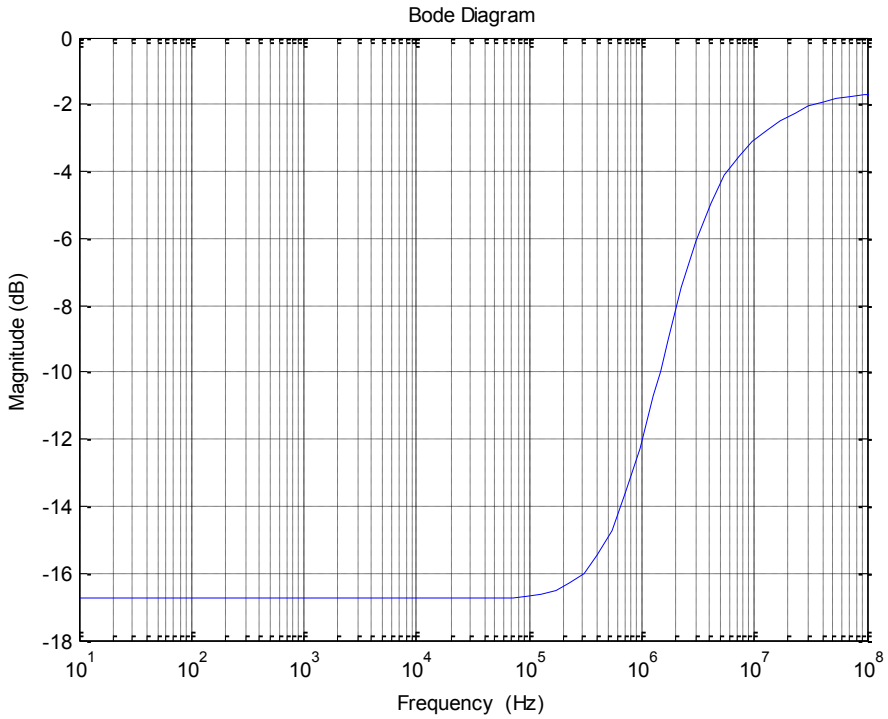

Figure 4.13 Simulation for PSR of TL082 LDO

As shown in Figure 4.13, the PSR is around -17 dB from 10 Hz to 100 KHz and begins to degrade from 200 KHz and above. The poor PSR at low frequency is caused by the

reference block consisting of the diode and resistor. The supply noise is only attenuated by the divider formed by R_4 and Z_1 shown in Figure 3.7. The worst case happens at high frequency since the PSR at high frequency is dominated by the ESR of the output capacitor and the channel resistance of the pass element MPT.

4.3.4 *PSR* model of the proposed LDO based on LM358 OPAMP

Similarly, an overall AC simulation of LM358 OPAMP based LDO was performed to predict the PSR characteristic of the proposed LDO. The simulation result is shown in Figure 4.14.

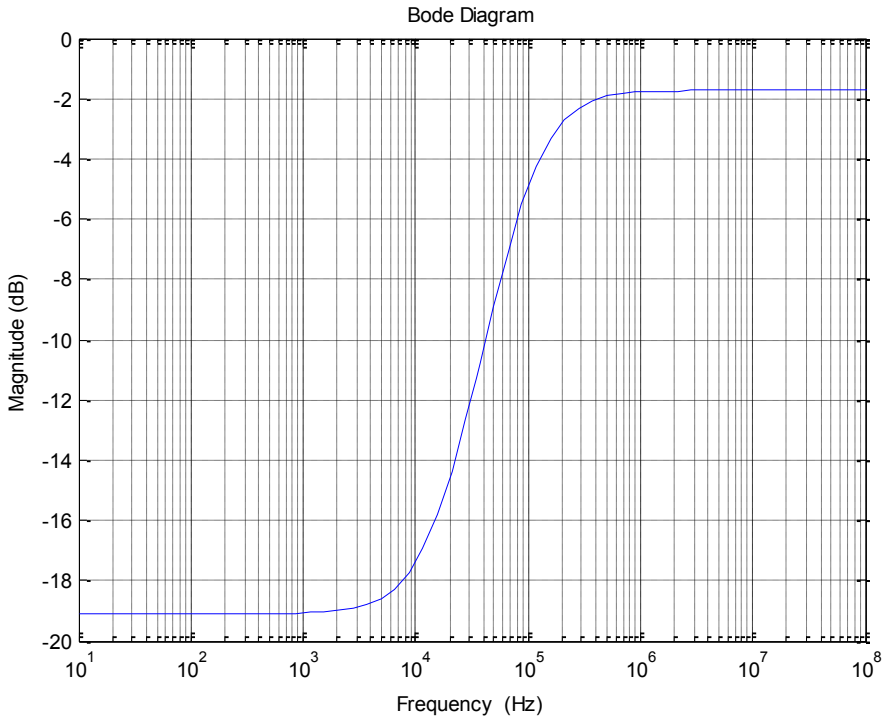

Figure 4.14 Simulation for PSR of LM358 LDO

Similar to Figure 4.13, the PSR is maintained around -19 dB from 10 Hz to 2 KHz and begins to degrade from 3 KHz and above. The poor PSR at low frequency is also caused by the reference block consisting of the diode and resistor. The supply noise is only attenuated by the divider formed by R_4 and Z_1 shown in Figure 3.22. The worst case happens at high frequency for the same cause for TL082 LDO.

Chapter 5 AMS behavioral model of the proposed LDOs

The Verilog-AMS behavioral model is used to facilitate the system design from top to down and is being widely used in industries. Figure 5.1 shows a typical "Top-Down" design flow.

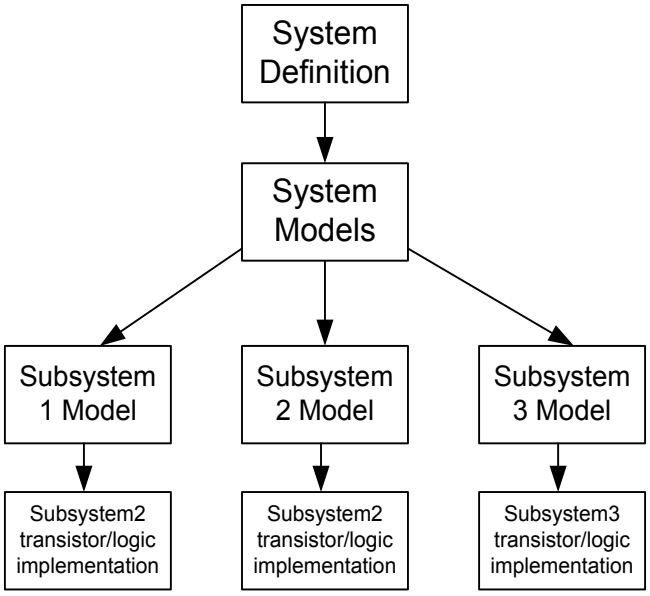

Figure 5.1 A typical "Top-Down" design flow

A system is initially defined and modeled in system level. Then, this system is divided into different subsystems called subsystem1, subsystem2, and subsystem3 with corresponding models. These behavioral models are to be verified to check if the system requirements are met. The transistor/logic implementation of these subsystems could not be started unless the system specifications are met by successfully verifying these behavioral models.

As shown in Figure 5.2, the behavioral level model can be used to efficiently describe a subsystem. Moreover, it provides greater design flexibility than its transistor level counterpart. Therefore, the system could be finished in a more efficient way.

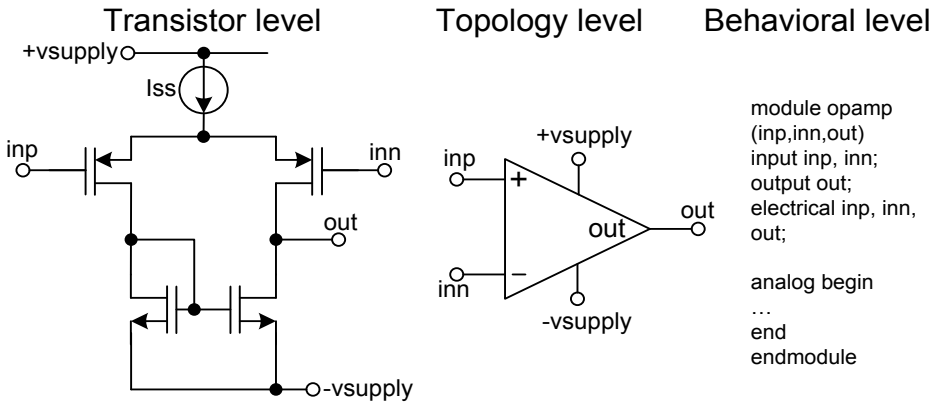

Figure 5.2 Different levels of description of subsystem

In this section, AMS behavioral models of the proposed LDOs are presented. These models are developed based on the behavioral characteristics of the proposed LDOs and their effectiveness is successfully verified by various simulations.

At first, the topology of the error amplifier model is provided as below:

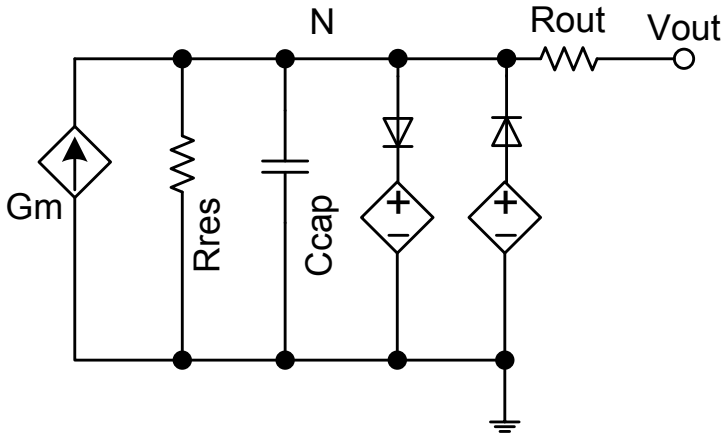

Figure 5.3 Topology of the error amplifier model

where G_m is the transconductance of the error amplifier, R_{res} and C_{cap} form the dominant pole, and the two diodes with controlled voltage sources are used to express the saturated I-V characteristics when the supply voltages get close to either V_{dd} or V_{ss}. The dc output resistance is the sum of R_{res} and R_{out}, while the ac output resistance is only Rout since the capacitance C_{cap} shorts the node N to ground.

In order to simplify the modeling of LDO system, the pass element is modeled as a current switch. The "on" and "off" of the switch are controlled by the voltage difference between its two terminals. Also, the voltage reference and resistor feedback blocks are not modeled for greater flexibility since different resistor ratio combined with constant reference voltage could generate almost any desired output voltages.

5.1 The Verilog-AMS model of TL082 OPAMP based LDO

In this section, the Verilog-AMS LDO model based on TL082 OPAMP is provided and the overall simulations are executed to verify the effectiveness of the model.

5.1.1 The Verilog-AMS model of TL082 OPAMP

The symbol of the Verilog-AMS model of TL082 OPAMP is shown below:

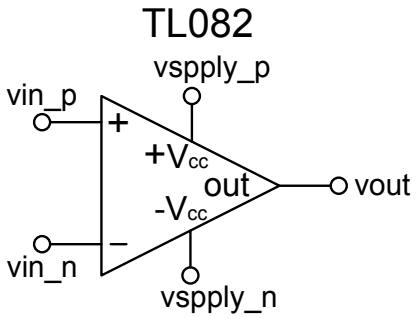

Figure 5.4 Symbol of TL082 OPAMP Verilog-AMS model

vin_p: Non-inverting Input

vin_n: Inverting Input

vspply_p: Positive Supply Voltage

vspply_n: Negative Supply Voltage

vout: Output Voltage

The Verilog-AMS model of TL082 OPAMP is listed as below:

```
**************************************************************
`include "discipline.h"
`include "constants.h"
module opamp (vout, vin_p, vin_n, vspply_p, vspply_n);
  inout  vin_p , vin_n;
  inout  vspply_p, vspply_n;
  output vout;
  electrical vin_p, vin_n, vout, vspply_p, vspply_n, vn;

   parameter real        gain = 199526.231497 exclude 0.0;
   parameter real      pole_freq = 15;
   parameter real        rdc = 300;
   parameter real        rac = 100;
   parameter real        vin_offset = 0.003;

   real ccap, vnom, r_res, gm_nom, vin_val;
   `define fclip(V,isat,dV) isat*exp(4.6*(V)/(dV))
    analog begin

      @(initial_step or initial_step("dc", "ac", "tran", "xf")) begin
          r_res = rdc - rac;
```

```
        gm_nom = gain/r_res;
        ccap = 1/(`M_TWO_PI * pole_freq * gain / gm_nom);
      end

     vin_val=  V(vin_p, vin_n) + vin_offset;
     // ------ contribution of current
    I(vn, vspply_n) <+ -gm_nom*vin_val;
    I(vn, vspply_n)  <+ (V(vn, vspply_n) - 0.5*(V(vspply_p)-V(vspply_n)))/r_res;
    I(vn, vspply_n)  <+ ddt(ccap*V(vn, vspply_n));
    I(vn, vspply_n)  <+ `fclip(V(vn, vspply_p),1,40m) - `fclip(V(vspply_n, vn),1,40m);
     // ------ output stage
       I(vn, vout) <+ V(vn, vout) / rac;
    end
  endmodule
**********************************************************************
```

Here, a `fclip function is defined to generate diode-like voltage limiting.

AC simulation is executed to validate the effectiveness of TL082 OPAMP model. The simulation testbench is shown in Figure 5.5:

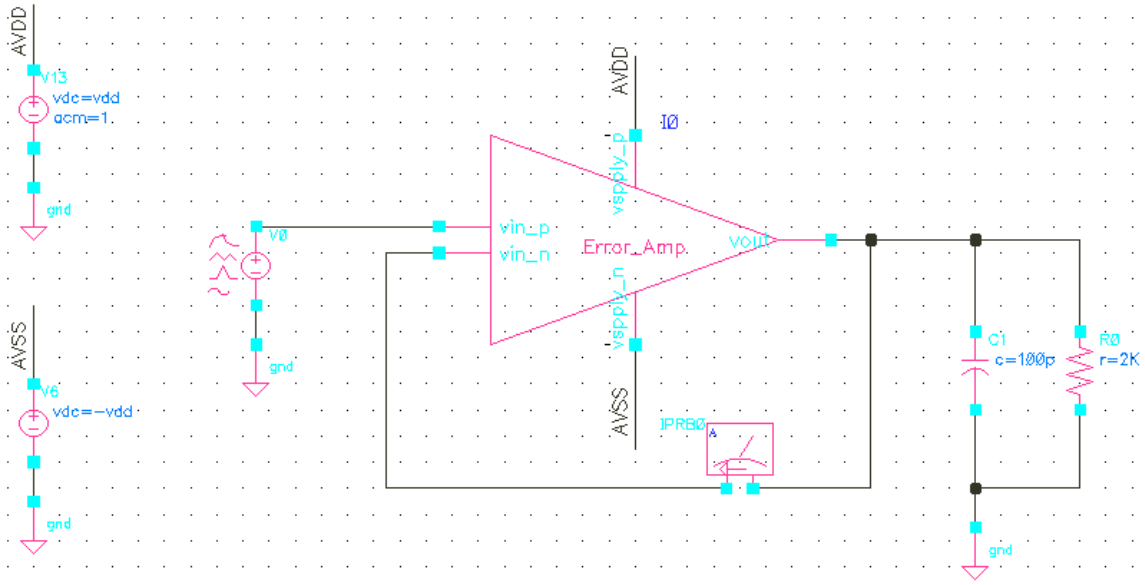

Figure 5.5 Simulation testbench of TL082 Verilog-A model

Figure 5.6 shows the simulation result.

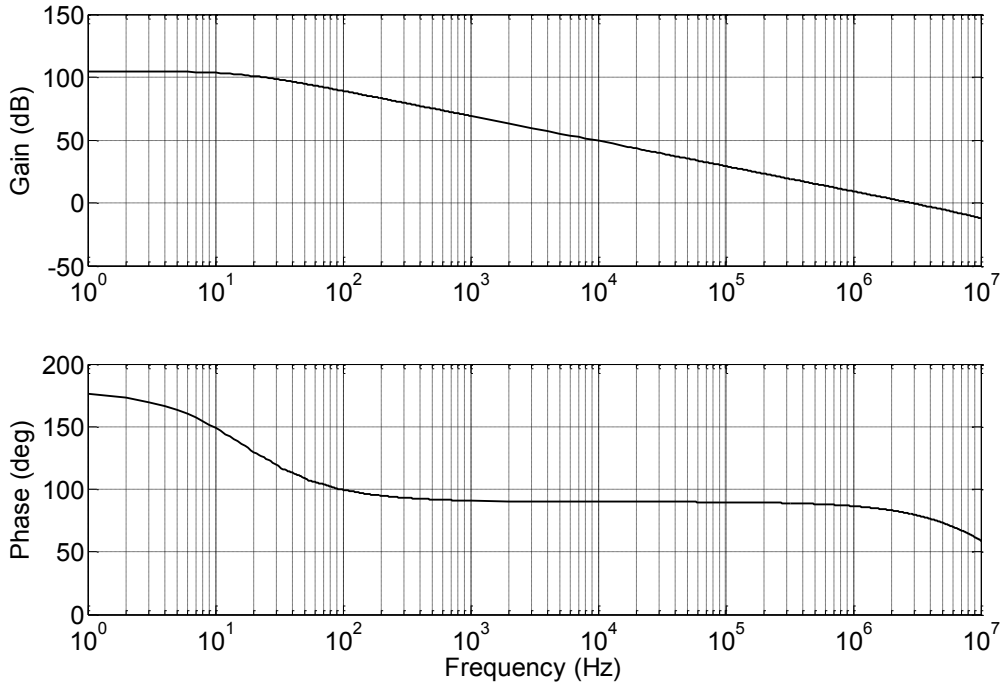

Figure 5.6 Simulation result of TL082 OPAMP Verilog-A model

Compared with the simulation result shown in Figure 3.6, the Verilog-A model of TL082 OPAMP is able to provide the same ac characteristics as those in Table 3.2.

5.1.2 **Output latch-up issue of TL082 OPAMP**

The output voltage of TL082 OPAMP IC jumps to the positive supply rail when the common-mode input voltage gets relatively close to the negative supply rail. This issue is not included in the TL082 OPAMP macro model provided in the TINA tool. Actually the output latch-up issue is caused by the common-mode input voltage exceeding allowable

limits of the device. In order to model this phenomenon, the Verilog-AMS model of TL082 OPAMP need to be revised accordingly. The overall model will be shown as below:

The Verilog-AMS model of TL082 OPAMP is listed as below:

```
**********************************************************************
`include "discipline.h"
`include "constants.h"
module opamp (vout, vin_p, vin_n, vspply_p, vspply_n);
inout vin_p , vin_n;
inout vspply_p, vspply_n;
output vout;
electrical vin_p, vin_n, vout, vspply_p, vspply_n, vn, voutt;

parameter real gain = 199526.231497 exclude 0.0;
parameter real pole_freq = 15;
parameter real rdc = 300;
parameter real rac = 100;
parameter real cap2 = 100e-12;
parameter real vin_offset = 0.003;

real ccap, vnom, r_res, gm_nom, vin_val;
`define fclip(V,isat,dV) isat*exp(4.6*(V)/(dV))
```

```
analog begin
@(initial_step("dc", "ac", "tran", "xf")) begin
r_res = rdc - rac;
gm_nom = gain/r_res;
ccap = 1/(`M_TWO_PI * pole_freq * gain / gm_nom);
end
vin_val= V(vin_p, vin_n) + vin_offset;
// ------ contribution of current
I(vn, vspply_n) <+ -gm_nom*vin_val;
I(vn, vspply_n) <+ (V(vn, vspply_n) - 0.5*(V(vspply_p)-V(vspply_n)))/r_res;
I(vn, vspply_n) <+ ddt(ccap*V(vn, vspply_n));
I(vn, vspply_n) <+ `fclip(V(vn, vspply_p),1,40m) - `fclip(V(vspply_n, vn),1,40m);
// ------ output stage
I(vn, voutt) <+ V(vn, voutt) / rac;
I(voutt, vspply_n) <+ ddt(cap2*V(voutt, vspply_n));
V(vout) <+ (abs(V(vin_p,vspply_n)) <= 0.7) ? V(vspply_p) : V(voutt);
end
**************************************************************
```

Figure 5.7 is the testbench of TL082 OPAMP output latch-up.

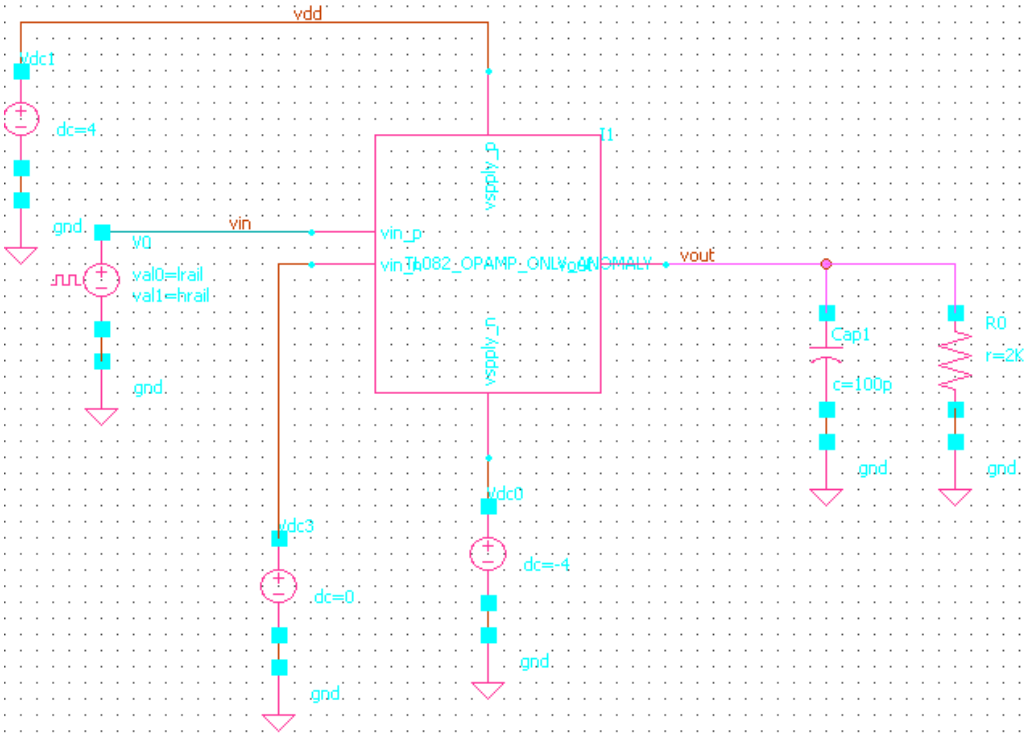

Figure 5.7 The testbench of TL082 OPAMP output latch-up

Where I_1 is the TL082 OPAMP Verilog-AMS model, V_{dc1} and V_{dc0} are the positive and negative supply rails respectively. V_{dc3} is the dc voltage source and V_0 is the input signal. C_{ap1} and R_0 model the output load of TL082 OPAMP. The simulation results are shown in Figure 5.8.

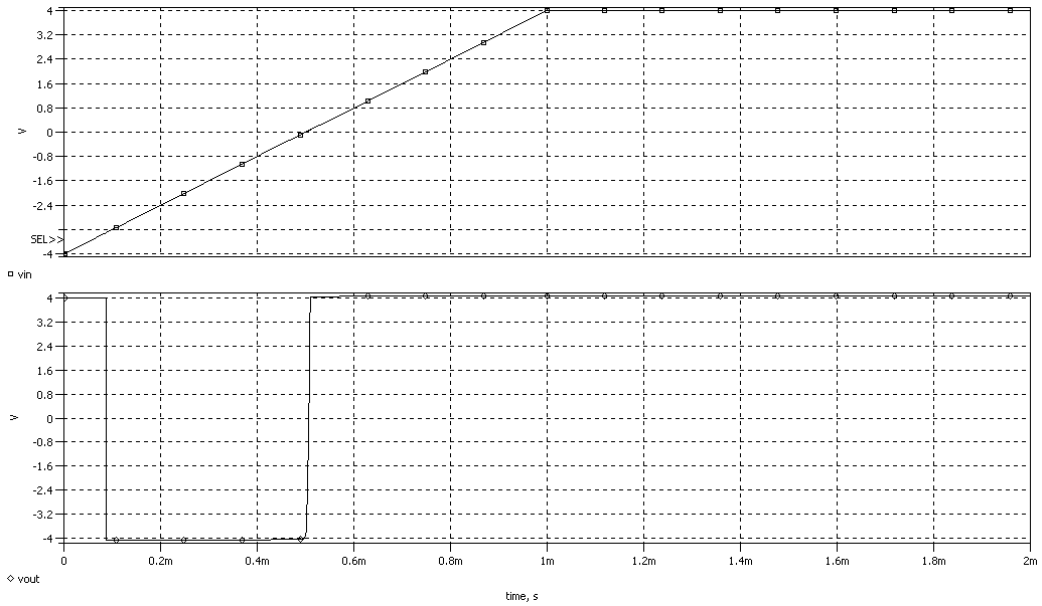

Figure 5.8 The simulation result of TL082 OPAMP output latch-up

TL082 OPAMP is powered by dual voltage supplies. (-4 V/ 4 V). The simulation is done by ramping the non-inverting input "vin" from -4 V to 4 V in 1 mS while keeping the inverting input constant (dc = 0). As shown in Figure 5.8, the output voltage "vout" is incorrectly latched to positive supply rail when "vin" is quite close to the negative supply rail. As time goes on, the output voltage "vout" comes back to normal value (negative supply rail) when "vin" exceeds the negative supply rail by a constant value.

5.1.3 **The Verilog-AMS model of pass element of TL082 OPAMP LDO**

The symbol of the Verilog-AMS model of pass element is shown below:

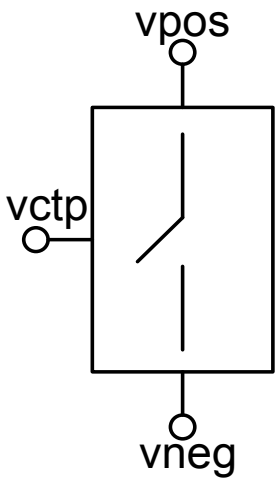

Figure 5.9 Symbol of pass element Verilog-AMS model

vpos: switch input

vneg: switch output

vctp: switch control signal

The verilog-A model of the pass element is listed as below:

****

```
`include "discipline.h"
`include "constants.h"


`define OPEN   1
`define CLOSED 0


module current_switch (vpos, vneg, vctp);
  inout  vpos , vneg, vctp;
```

```
electrical vpos , vneg, vctp;

 parameter real        vthr = 1.0;
 integer   switch_state;
 parameter real      kval = 0.518;

 analog begin
        @(cross(V(vpos, vctp) - vthr, 0.0, 1u));
        if ((V(vpos, vctp) - vthr) > 0.0)
          switch_state = `CLOSED;
        else
          switch_state = `OPEN;
        if (switch_state == `OPEN)
                I(vpos, vneg) <+ 0.0;
        else
            I(vpos, vneg) <+ kval*(V(vpos) - V(vctp) - vthr)*(V(vpos) - V(vctp) - vthr);
        end
    endmodule
```

****

Where kval is calculated by using the fitting number from TINA model:

Surface mobility: 300 cm^2/Vs

Oxide thickness: 100 nm

Channel length: 2 μm

Channel width: 200 mm

Therefore, the calculated Kval = 0.5*μn*Cox*(W/L) = 0.518 A/V².

In order to model the pole caused from the parasitic capacitance of the pass element, a capacitance (C_{cap2}) is added at the output of the error amplifier model:

The modified topology of the error amplifier is shown as below:

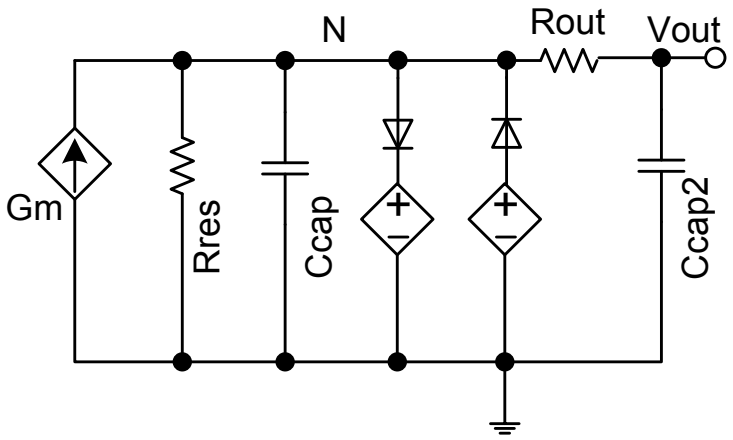

Figure 5.10 Modified topology of the error amplifier model

where C_{cap2} is the added capacitor to model the parasitic effects of pass element.

Therefore, the output stage of Veilog-AMS model of the TL082 OPAMP is changed as:

****

// ------ output stage

I(vn, vout) <+ V(vn, vout) / rac;

I(vout, vspply_n) <+ ddt(ccap2*V(vout, vspply_n));

end

****

5.1.4 **The Verilog-AMS model of TL082 OPAMP LDO**

Based on the previous models of TL082 OPAMP and pass element, a Verilog-AMS model for TL082 OPAMP based LDO was proposed in this section. The schematic of the LDO Verilog-AMS model with voltage reference and resistor divider is shown in Figure 5.11 as below:

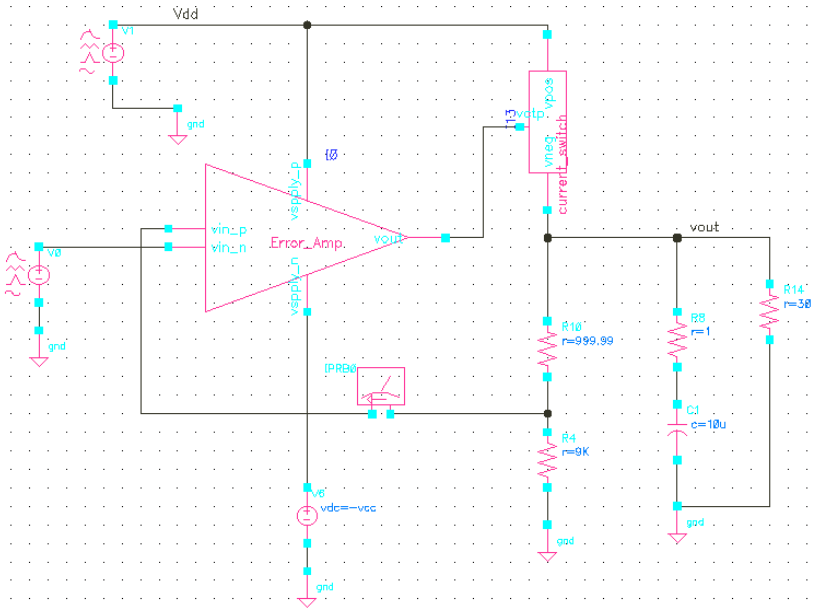

Figure 5.11 The schematic of LDO Verilog-AMS model with voltage reference and resistor divider

Here, R_{10} and R_4 form the resistor divider and voltage source V_0 is the reference voltage. C_1 is the output capacitor and R_8 is the ESR of C_1 capacitor. R_{14} is the output equivalent

resistance of load current.

5.1.5 The Performance of the proposed Verilog-AMS model of LDO Based on TL082 OPAMP

Similar to Chapter 3, a bunch of simulations were performed with different test benches to verify the effectiveness of the proposed Verilog-AMS model.

1) Line Regulation

Figure 5.12 shows the line regulation simulation result. The excellent line regulation comes directly from the ideal voltage reference V_0.

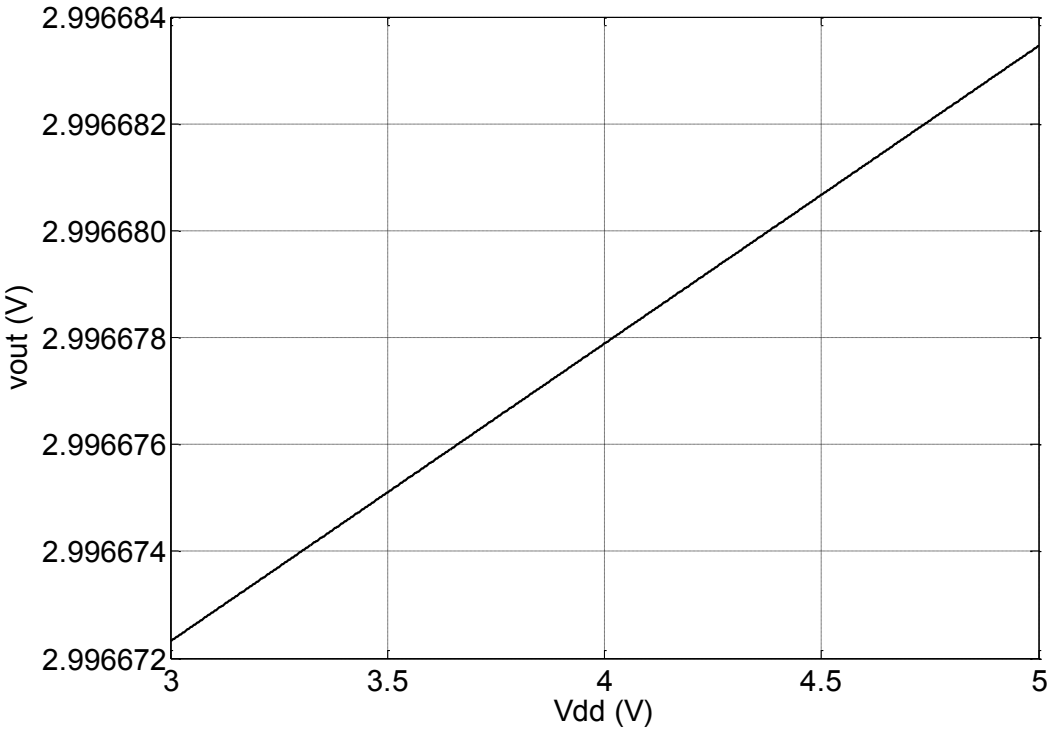

Figure 5.12 Line regulation of the proposed Verilog-AMS model of the LDO based on TL082 OPAMP

2) Load Regulation

Load regulation is shown in Figure 5.13 and can be calculated by applying equation (2.12). The superior load regulation is a result of ideal current sourcing capability of the pass element model.

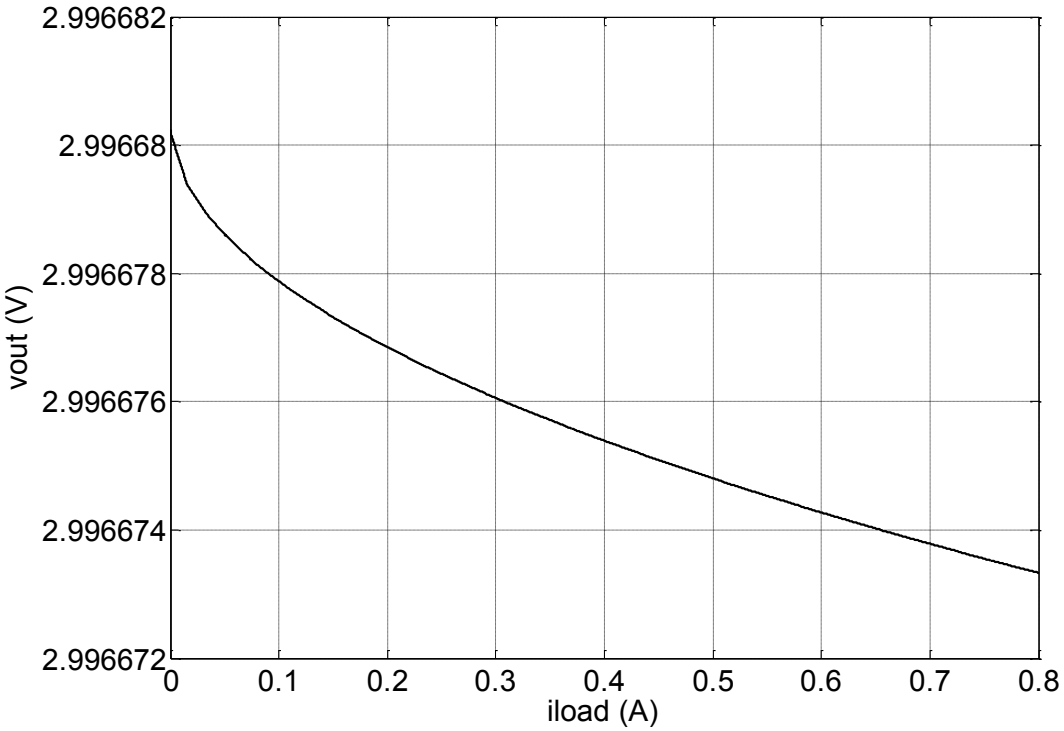

Figure 5.13 Load regulation of the proposed Verilog-AMS model of the LDO based on TL082 OPAMP

3) Line Step Response

Line step response simulation was performed by applying DC supply voltage with a square wave perturbation. As shown in Figure 5.14, when a peak-to-peak 200 mV square wave was applied on supply voltage, the LDO output voltage underwent a ripple of about 25 mV.

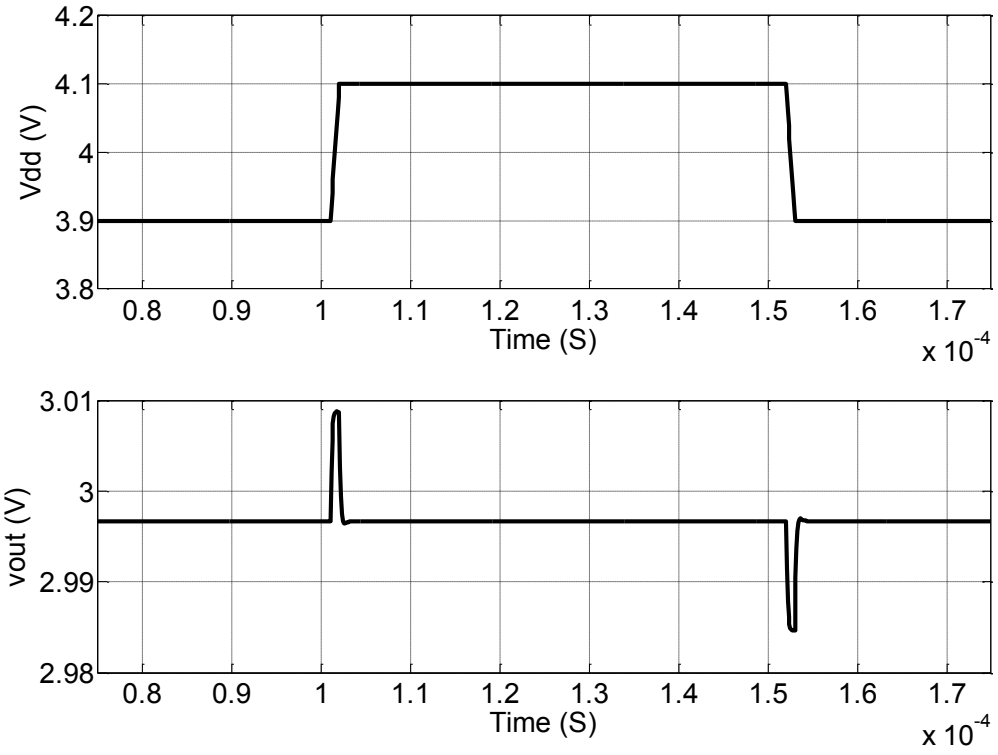

Figure 5.14 Line step response of the proposed Verilog-AMS model of LDO based on TL082

4) Load Step Response

A sudden load current change is applied to the LDO output to perform load step response. Figure 5.15 shows the load step response of the proposed LDO when a sudden load current change (100 mA) is applied to the LDO output. From the simulation results, the undershoot voltage and overshoot voltage of the proposed LDO are 70 mV and 100 mV, respectively. Also, the settling times for both undershoot and overshoot are both within 2 μS.

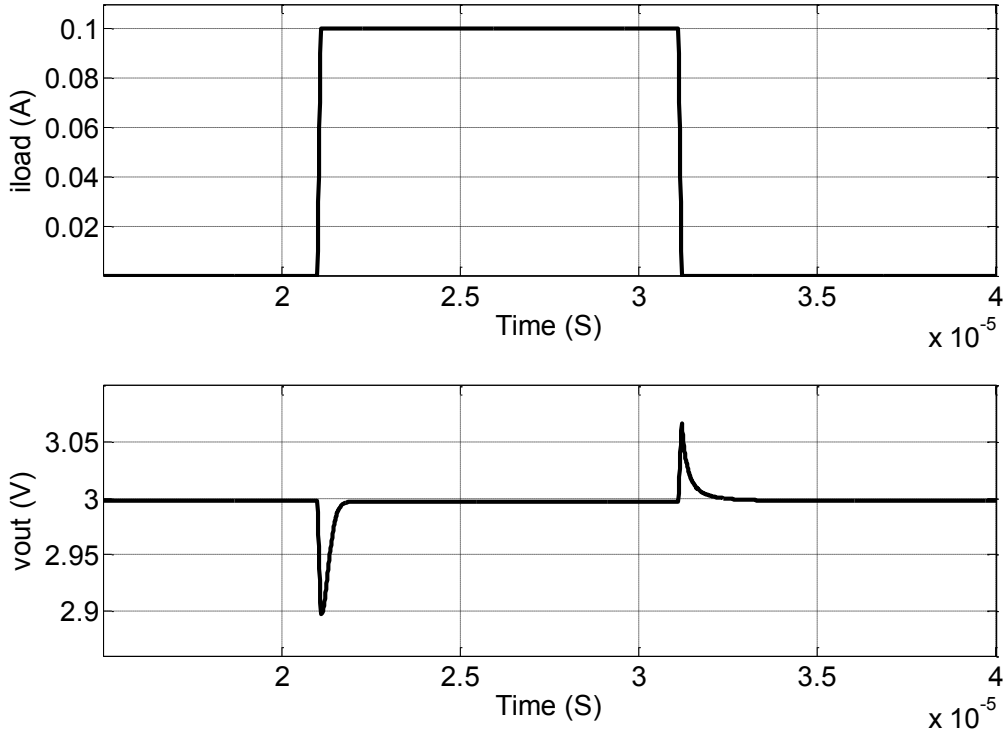

Figure 5.15 Load step response of the proposed Verilog-AMS model of LDO based on TL082

5) AC Stability

The AC small signal stability of the proposed LDO can be analyzed by cutting the loop at the non-inverting pin of error amplifier in Figure 5.11 and injecting small signal at the breaking point. Figure 5.16 shows the simulation results of the AC stability. The three groups of curves represent Gain and Phase frequency characteristics under three loading conditions (0 mA: “red”; 50 mA: “yellow”; 100 mA: “blue”). The AC stability results are summarized in Table 5.1.

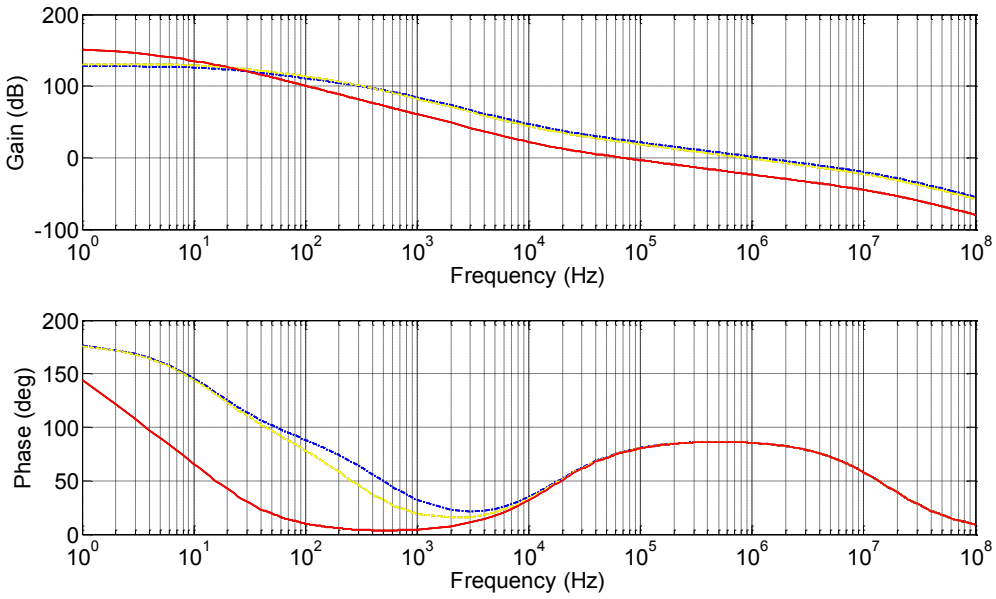

Figure 5.16 AC stability simulation of the proposed Verilog-AMS model of LDO based on TL082 OPAMP

Table 5.1 AC Stability summary of the proposed Verilog-AMS model of LDO based on TL082 OPAMP

Load Current	Unity Gain Frequency	Phase Margin
0	67.73KHz	76.56
50mA	838.72KHz	85.92
100mA	1.16MHz	85.06

6) Power Supply Rejection (PSR)

PSR was performed by applying small signal perturbation in power supply within the entire frequency spectrum. As shown in Figure 5.17, the PSR of the proposed LDO keeps below -110dB at DC degrades worst around 200 KHz. The excellent low frequency PSR characteristic of the proposed LDO mainly comes from the ideal voltage reference source V_0 shown in Figure 5.11.

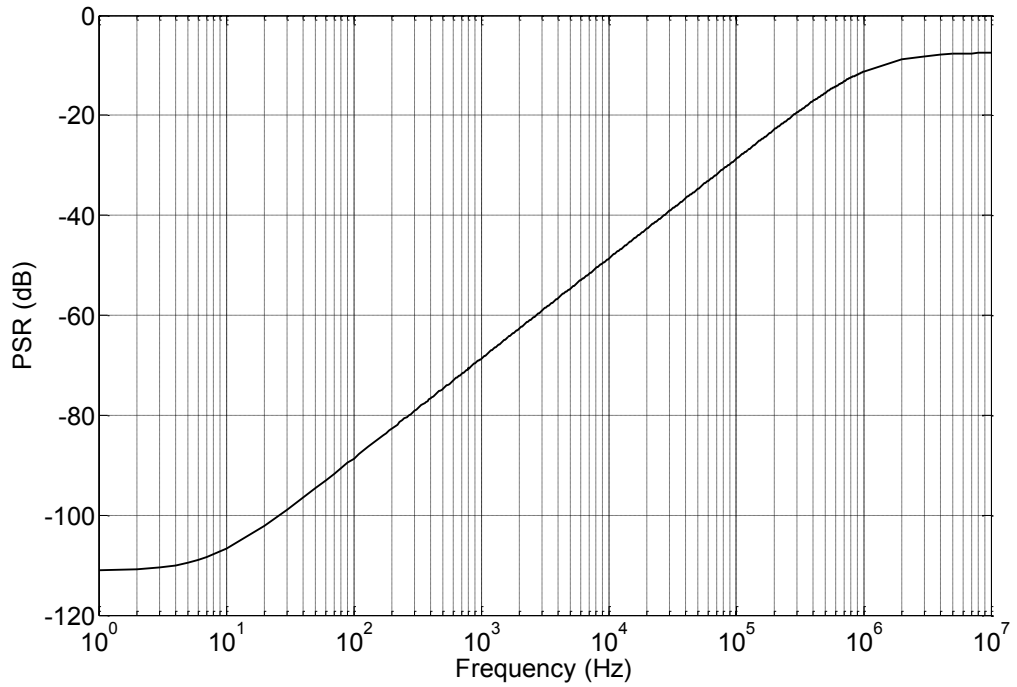

Figure 5.17 PSR simulation result of the proposed Verilog-AMS model of LDO based on TL082 OPAMP

5.2 The Verilog-AMS model of LM358 OPAMP based LDO

In this section, the Verilog-AMS LDO model based on LM358 OPAMP is provided and the overall simulations are executed to verify the effectiveness of the model.

5.2.1 **The Verilog-AMS model of LM358 OPAMP**

The symbol of the Verilog-AMS model of LM358 OPAMP is shown below:

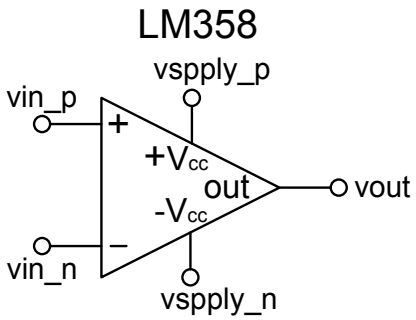

Figure 5.18 Symbol of LM358 OPAMP Verilog-AMS model

vin_p: Non-inverting Input

vin_n: Inverting Input

vspply_p: Positive Supply Voltage

vspply_n: Negative Supply Voltage

vout: Output Voltage

The Verilog-AMS model of LM358 OPAMP is listed as below:

****

```
`include "discipline.h"
`include "constants.h"
module opamp (vout, vin_p, vin_n, vspply_p, vspply_n);
  inout  vin_p , vin_n;
  inout  vspply_p, vspply_n;
  output vout;
  electrical vin_p, vin_n, vout, vspply_p, vspply_n, vn;

   parameter real         gain = 100000.00 exclude 0.0;
   parameter real      pole_freq = 7.86;
   parameter real         rdc = 300;
   parameter real         rac = 100;
   parameter real         vin_offset = 0.003;

   real ccap, vnom, r_res, gm_nom, vin_val;
   `define fclip(V,isat,dV) isat*exp(4.6*(V)/(dV))
    analog begin

      @(initial_step or initial_step("dc", "ac", "tran", "xf")) begin
          r_res = rdc - rac;
          gm_nom = gain/r_res;
          ccap = 1/(`M_TWO_PI * pole_freq * gain / gm_nom);
```

```
        end


        vin_val=  V(vin_p, vin_n) + vin_offset;
        // ------ contribution of current
        I(vn, vspply_n) <+ -gm_nom*vin_val;
 I(vn, vspply_n)  <+ (V(vn, vspply_n) - 0.5*(V(vspply_p)-V(vspply_n)))/r_res;
 I(vn, vspply_n)  <+ ddt(ccap*V(vn, vspply_n));
I(vn, vspply_n)  <+ `fclip(V(vn, vspply_p),1,40m) - `fclip(V(vspply_n, vn),1,40m);
 // ------ output stage
I(vn, vout) <+ V(vn, vout) / rac;
end
endmodule
**********************************************************************
```

AC simulation is executed to validate the effectiveness of LM358 OPAMP model. The simulation testbench is shown in Figure 5.19:

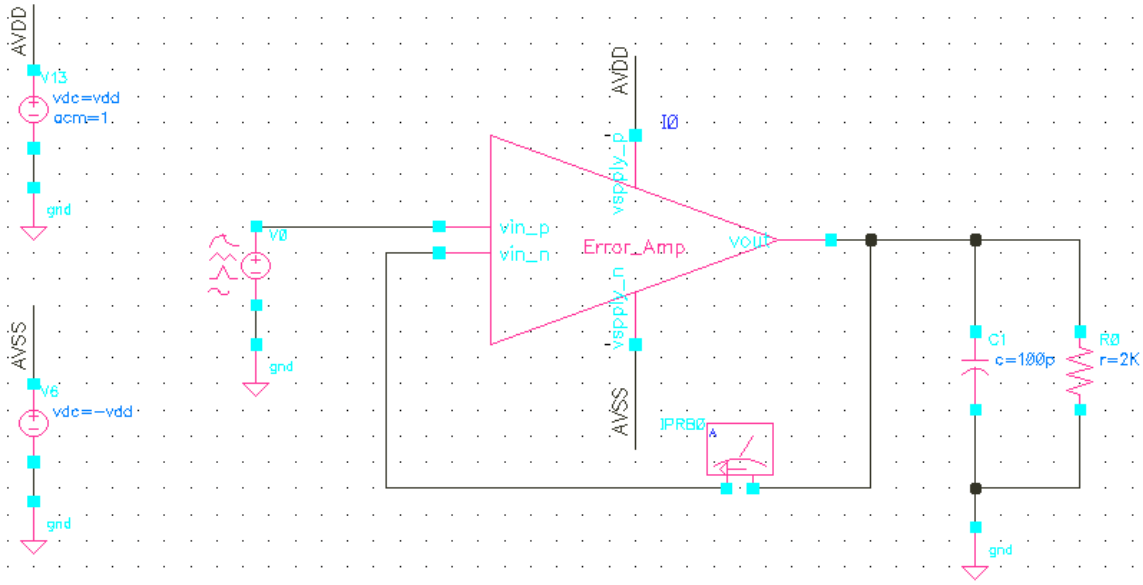

Figure 5.19 Simulation testbench of LM358 Verilog-A model

Figure 5.20 shows the simulation result.

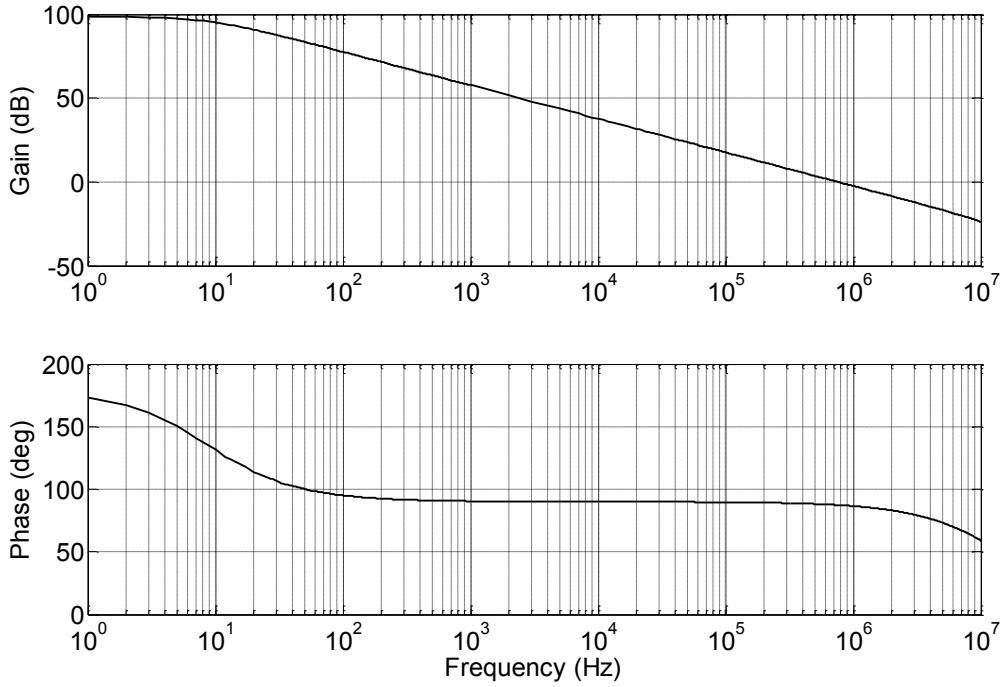

Figure 5.20 Simulation testbench of LM358 Verilog-AMS model

Compared with the simulation result shown in Figure 3.21, the Verilog-AMS model of LM358 OPAMP is able to provide the same ac characteristics as those in Table 3.7.

5.2.2 **The Verilog-AMS model of pass element of LM358 OPAMP LDO**

The symbol of the Verilog-AMS model of pass element is shown below:

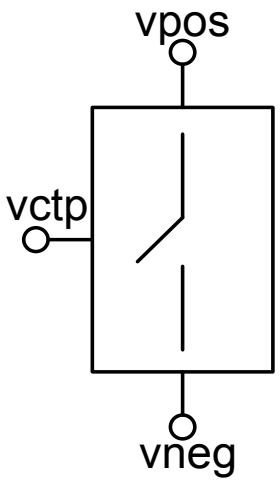

Figure 5.21 Symbol of pass element Verilog-AMS model

vpos: switch input

vneg: switch output

vctp: switch control signal

The verilog-A model of the pass element is listed as below:

****

```
`include "discipline.h"
`include "constants.h"


`define OPEN   1
`define CLOSED 0


module current_switch (vpos, vneg, vctp);
  inout  vpos , vneg, vctp;
```

```
electrical vpos , vneg, vctp;

 parameter real        vthr = 1.0;
 integer   switch_state;
 parameter real      kval = 0.518;

 analog begin
        @(cross(V(vpos, vctp) - vthr, 0.0, 1u));
        if ((V(vpos, vctp) - vthr) > 0.0)
          switch_state = `CLOSED;
        else
          switch_state = `OPEN;
        if (switch_state == `OPEN)
                I(vpos, vneg) <+ 0.0;
        else
           I(vpos, vneg) <+ kval*(V(vpos) - V(vctp) - vthr)*(V(vpos) - V(vctp) - vthr);
        end
endmodule
```

****

where kval is calculated by using the fitting number from TINA model:

Surface mobility: 300 cm^2/Vs

Oxide thickness: 100 nm

Channel length: 2 μm

Channel width: 200 mm

Therefore, the calculated Kval = 0.5*μn*Cox*(W/L) = 0.518 A/V².

In order to model the pole caused from the parasitic capacitance of the pass element, a capacitance (C_{cap2}) is added at the output of the error amplifier model:

The modified topology of the error amplifier is shown as below:

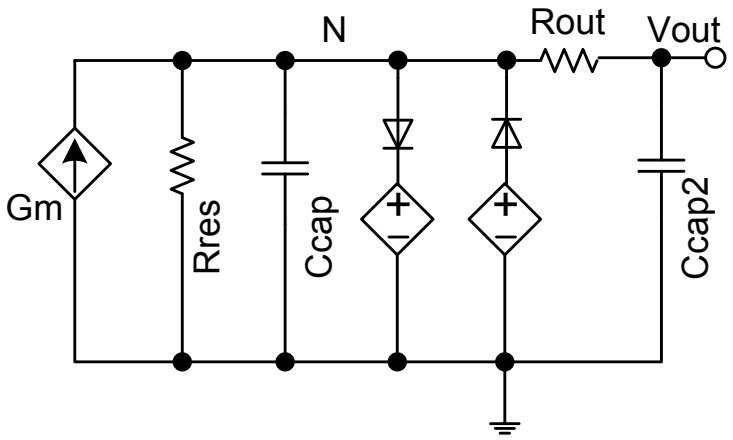

Figure 5.22 Modified topology of the error amplifier model

where C_{cap2} is the added capacitor to model the parasitic effects of pass element.

Therefore, the output stage of Veilog-AMS model of the LM358 OPAMP is changed as:

****

```
// ------ output stage
        I(vn, vout) <+ V(vn, vout) / rac;
        I(vout, vspply_n) <+ ddt(ccap2*V(vout, vspply_n));
```

end

****

5.2.3 The Verilog-AMS model of LM358 OPAMP LDO

Based on the previous models of LM358 OPAMP and pass element, a Verilog-AMS model for LM358 OPAMP based LDO was proposed in this section. The schematic of the LDO Verilog-AMS model with voltage reference and resistor divider is shown in Figure 5.23 as below:

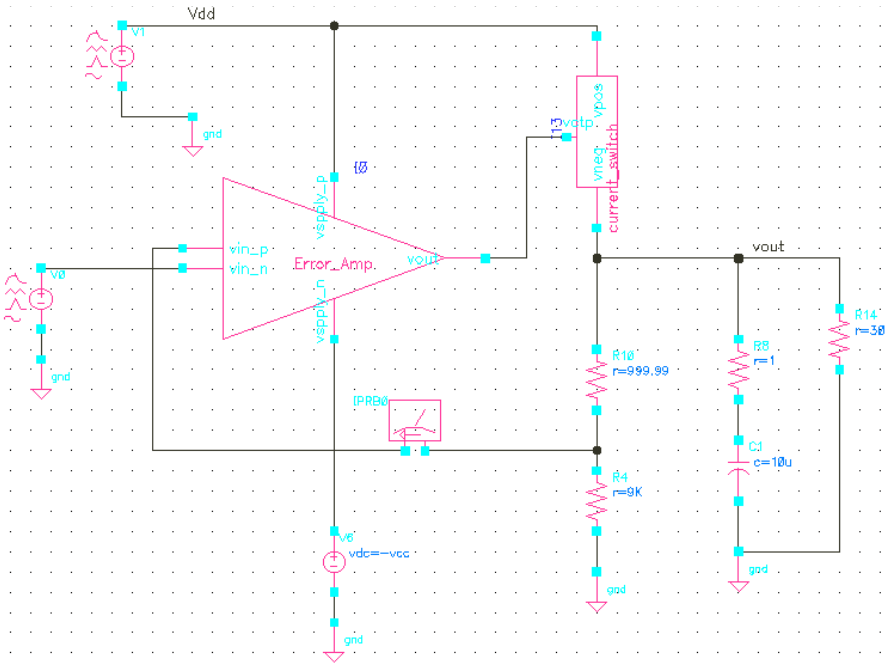

Figure 5.23 The schematic of LDO Verilog-AMS model with voltage reference and resistor divider

Here, R_{10} and R_4 form the resistor divider and voltage source V_0 is the reference voltage. C_1 is the output capacitor and R_8 is the ESR of C_1 capacitor. R_{14} is the output equivalent resistance of load current.

5.2.4 The Performance of the proposed Verilog-AMS model of LDO Based on LM358 OPAMP

Similar to Chapter 3, a bunch of simulations were performed with different test benches to verify the effectiveness of the proposed Verilog-AMS model.

1) Line Regulation

Figure 5.24 shows the line regulation simulation result. The excellent line regulation comes directly from the ideal voltage reference V_0.

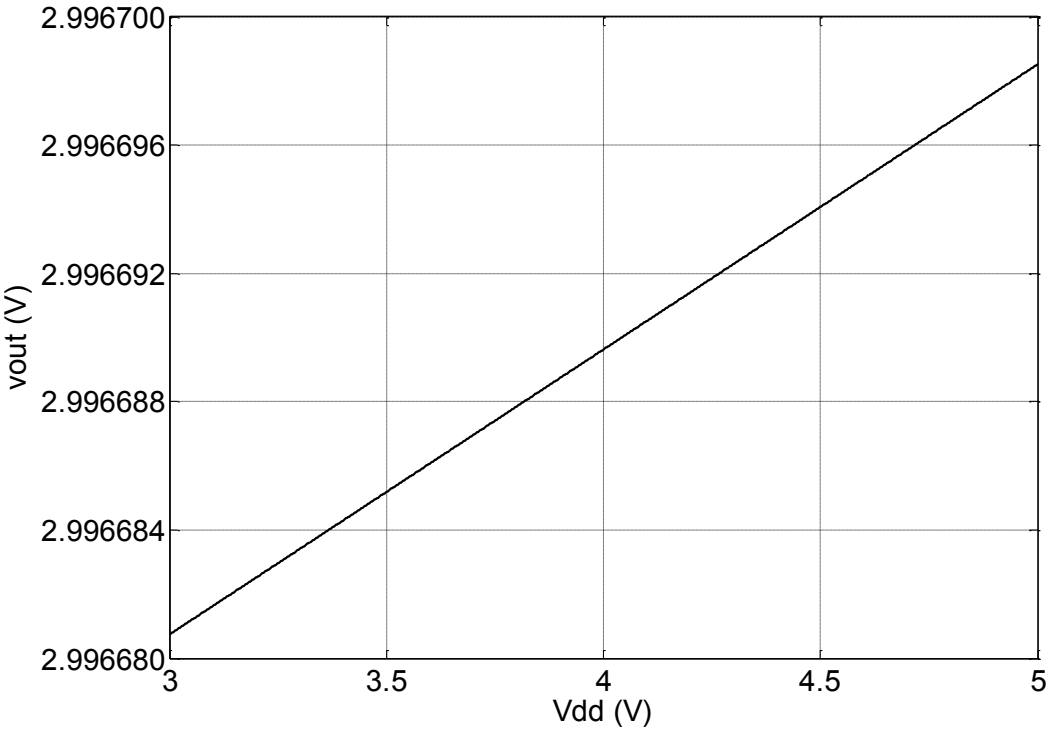

Figure 5.24 Line regulation of the proposed Verilog-AMS model of the LDO based on LM358 OPAMP

2) Load Regulation

Load regulation is shown in Figure 5.25 and can be calculated by applying equation (2.12). The superior load regulation is a result of ideal current sourcing capability of the pass element model.

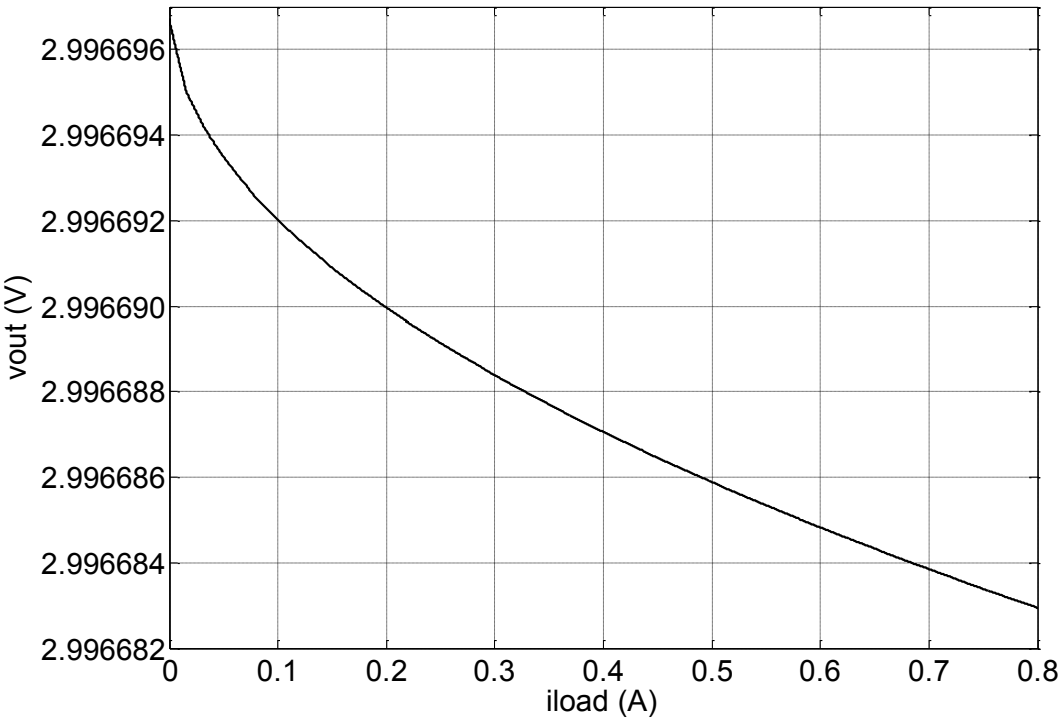

Figure 5.25 Load regulation of the proposed Verilog-AMS model of the LDO based on LM358 OPAMP

3) Line Step Response

Line step response simulation was performed by applying DC supply voltage with a square wave perturbation. As shown in Figure 5.26, when a peak-to-peak 200 mV square wave was applied on supply voltage, the LDO output voltage underwent a ripple of about 40 mV.

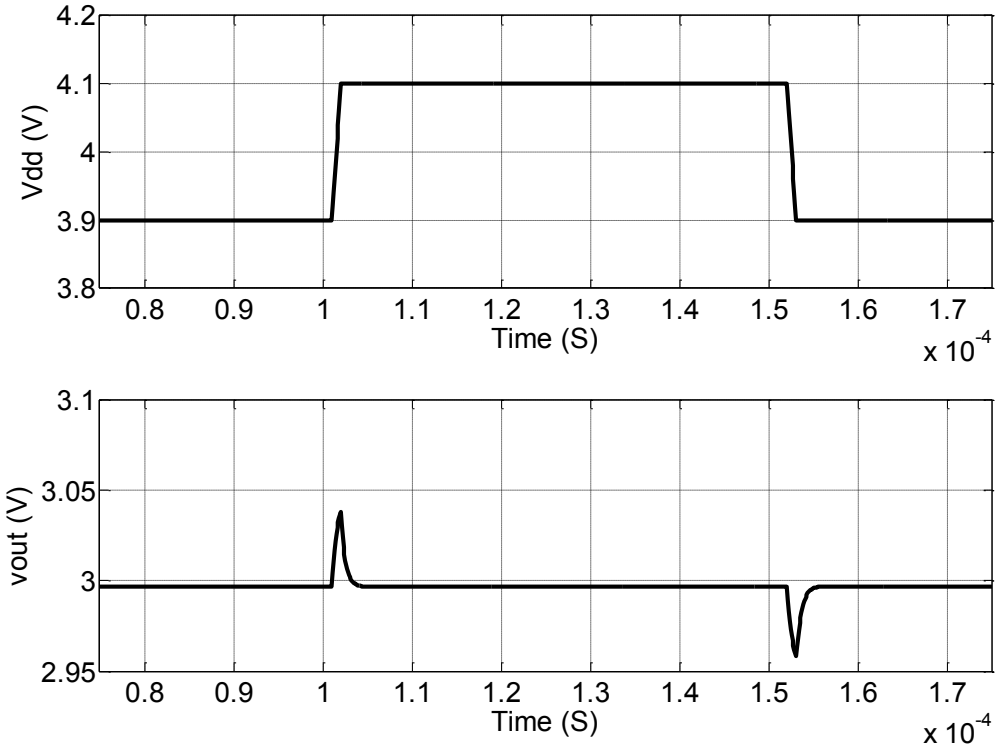

Figure 5.26 Line step response of the proposed Verilog-AMS model of LDO based on LM358

4) Load Step Response

A sudden load current change is applied to the LDO output to perform load step response. Figure 5.27 shows the load step response of the proposed LDO when a sudden load current change (100 mA) is applied to the LDO output. From the simulation results, the undershoot voltage and overshoot voltage of the proposed LDO are 90 mV and 100 mV, respectively. Also, the settling times for both undershoot and overshoot are both within 4 μS.

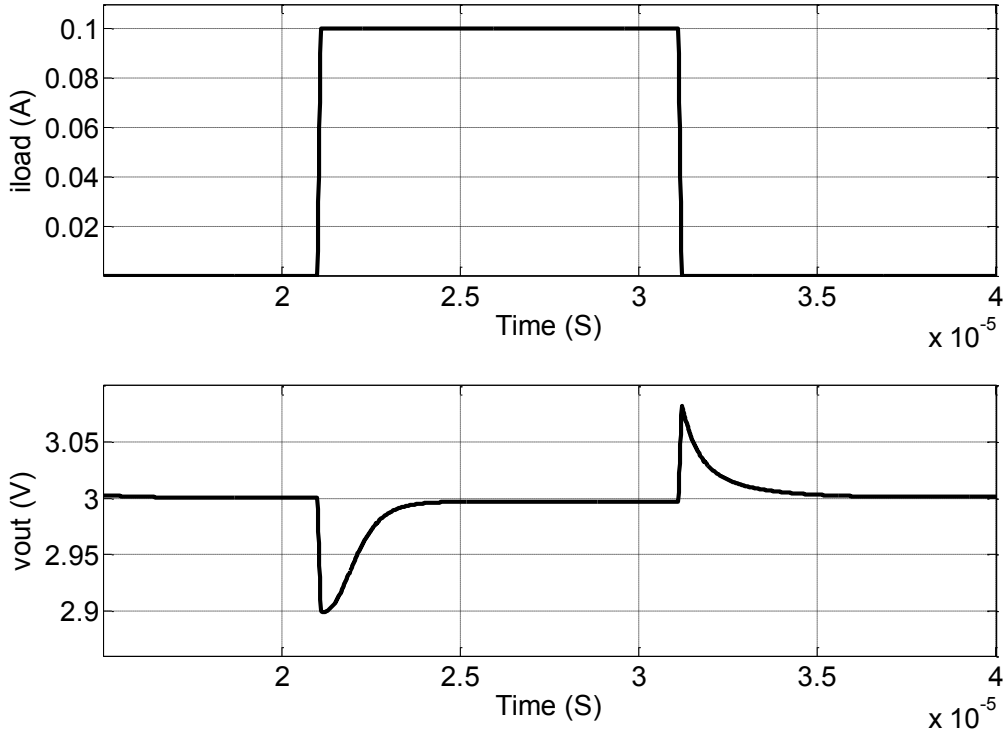

Figure 5.27 Load step response of the proposed Verilog-AMS model of LDO based on LM358

5) AC Stability

The AC small signal stability of the proposed LDO can be analyzed by cutting the loop at the non-inverting pin of error amplifier in Figure 5.23 and injecting small signal at the breaking point. Figure 5.28 shows the simulation results of the AC stability. The three groups of curves represent Gain and Phase frequency characteristics under three loading conditions (0 mA: “red”; 50 mA: “yellow”; 100 mA: “blue”). The AC stability results are summarized in Table 5.2.

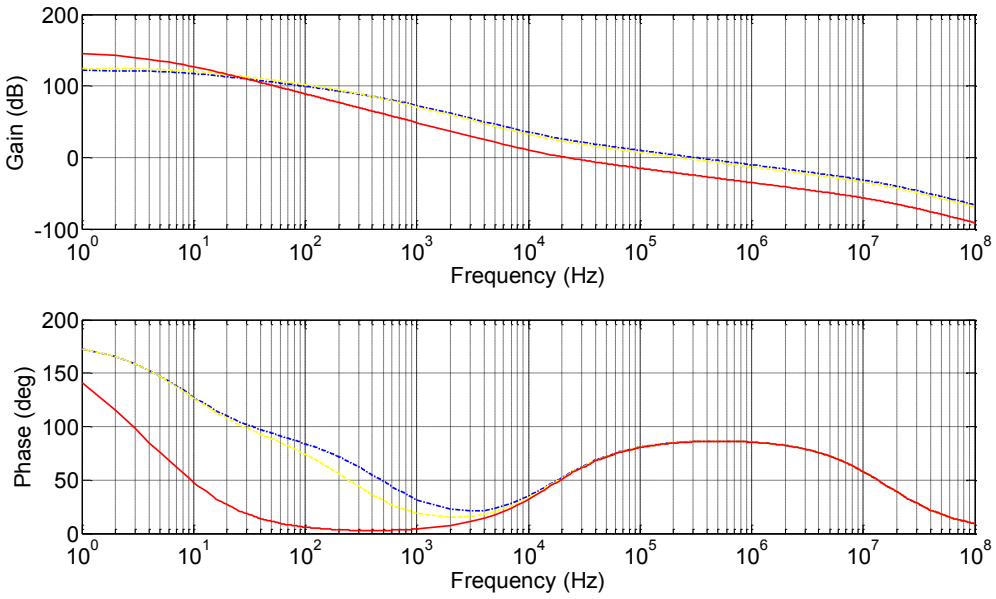

Figure 5.28 AC stability simulation of the proposed Verilog-AMS model of LDO based on LM358 OPAMP

Table 5.2 AC Stability summary of the proposed Verilog-AMS model of LDO based on LM358 OPAMP

Load Current	Unity Gain Frequency	Phase Margin
0	21.53KHz	53.48
50mA	221.09KHz	85.16
100mA	306.77KHz	86.02

6) Power Supply Rejection (PSR)

PSR was performed by applying small signal perturbation in power supply within the entire frequency spectrum. As shown in Figure 5.29, the PSR of the proposed LDO keeps below -105dB at DC degrades worst around 1 MHz. The excellent low frequency PSR characteristic of the proposed LDO mainly comes from the ideal voltage reference source V_0 shown in Figure 5.23.

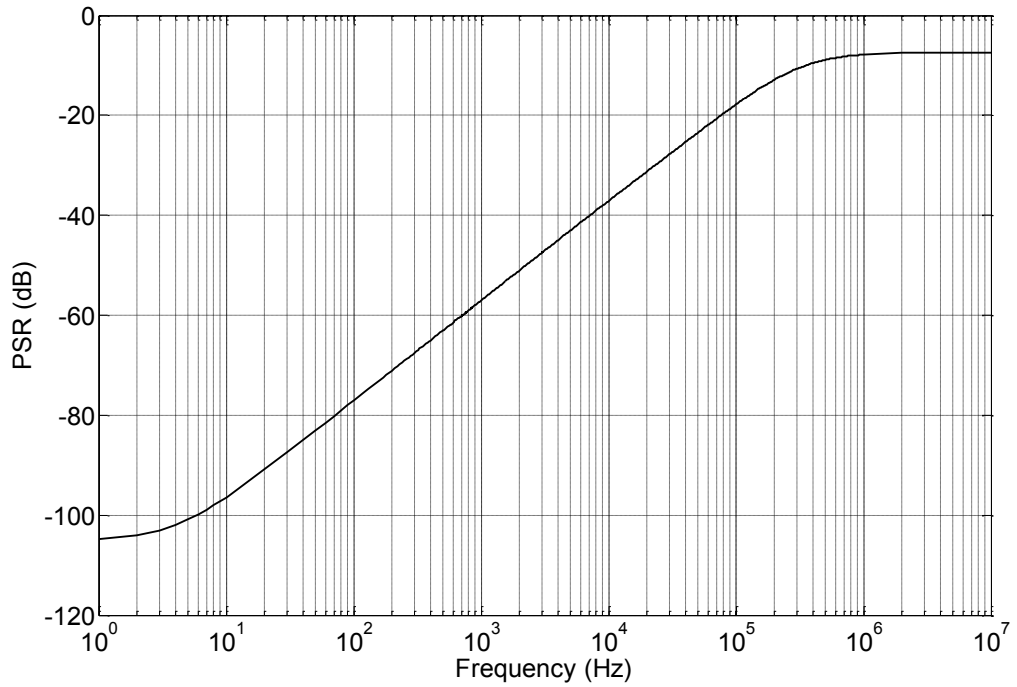

Figure 5.29 PSR simulation of the proposed Verilog-AMS model of LDO based on LM358 OPAMP

Chapter 6 Conclusion and Recommendations

This dissertation presents the analysis and development of trusted Low Dropout Regulator (LDO) models for intellectual property (IP) reuse aiming at system verification. In order to establish the trusted models and allow system designer to use them to predict the possible obscure error in IP block, LDO is chosen to act as the example in this dissertation. Two LDOs are built from discrete parts in the TI Analog System Lab Kit (ASLK) Pro and verified with TI TINA simulation tool. Two general purpose ICs (TI TL082 and TI LM358 OPAMPs) are adopted to act as the error amplifiers of the discrete LDOs. The analysis of the macro models and performance of the two OPAMPs are included. Moreover, the single supply operation issue and obscure error (output latch-up issue) of TL082 OPAMP are also addressed. Based on the design and analysis of the two LDOs, high level models of the proposed LDOs for system validation is presented in MATLAB tool. The high level models are used to verify the LDO system stability and

power supply rejection (PSR). In addition, the LDO system stability over output capacitor and its associated equivalent series resistance (ESR) range are also analyzed. Therefore, the proposed high level models not only provide an efficient solution on system level verification but also ease the selection of external capacitor with proper ESR range for stability compensation.

In order to facilitate the integration of the high level models into top level system for co-simulation with other blocks, Verilog-AMS models of the two LDOs are presented and verified with Cadence design environment. Moreover, the output latch-up issue with the use of TL082 OPAMP was indicated and included into its Verilog-AMS model. The simulation results from the Verilog-AMS models and those from the original designs in TI TINA tool are well matched. Therefore, the quality assurance of the proposed models is guaranteed because the models provide the better description of the functions and performance than the ones from the vendor.

In summary, this dissertation covers the basic concepts and the implementation of trusted models for IP reuse at system verification with examples of modeling of LDOs built with TI ASLK Pro kit. The analysis and design methods presented in this dissertation can be applied in other similar designs. The models proposed in this dissertation can be used in high level system design such as SoC as trusted reusable IP blocks. The well-matched performance and guaranteed quality assurance will lead to a more efficient design and implementation of higher level system.

Based on the reusable IP block models developed in this dissertation, the prototype implementation of LDO designs can be realized efficiently by utilizing the discrete parts

in ASLK. Moreover, the performance of the LDO can be optimized by making use of the models and the analysis proposed.

However, this dissertation is not made to find the general solution to the obscure errors happening in the electronics devices, but rather to ignite the fire in future research and industrial cooperation on that topic. The possible research may include the creation of industrial standard for the trusted electronics devices design, manufacturing, packaging, and products distribution. The author believes that the future research on the trusted electronics design will lead to a big change to the present electronics industry and bring highly trusted devices without obscure errors.

The work included in this dissertation can be extended by adding the reference block to the models. Thus, the complete trusted LDO models for IP reuse can be generated. The reference block may include the temperature characteristics and input power supply dependency. With the inclusion of reference block into the current work, the behavior of the complete LDO models are much closer to that in the real circuits and the enhanced models are expected to cover all the specifications indicated in LDO datasheet.

The other future works include the addition of various issues found in the experiments with ASLK Pro kit into the models. Thus, the quality assurance of the reusable IP blocks can be greatly enhanced.

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