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Bandgap Reference Voltage Generation Using a Two-Stage Operational Amplifier

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This thesis is submitted to the Department of Electrical & Electronic Engineering, Bangladesh University of Engineering and Technology for the partial fulfillment of the degree of Bachelor of Science in Electrical & Electronic Engineering

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
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DECLARATION

This thesis has been performed by the authors undersigned under the supervision of Dr. Mohammad Jahangir Alam and has not been submitted elsewhere for any degree or diploma.

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Dedication

To our beloved parents

&

Our late friends
Russel Mahmud & Ahmed Al Faisal

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It is with due gratefulness we would like to convey our gratitude to Almighty Allah for HE has made all of these possible.

Dr. Mohammad Jahangir Alam, Associate Professor, Department of EEE, BUET, our thesis supervisor has given us much of his valuable time to guide us through all those hard times. His unparallel dedication has kept us on track. Working according to his suggestions we have managed to improve our circuit to perform the best.

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Shopan din Ahmad Hafiz

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Abstract

With the pass of time the electronics have become more sophisticated and tend to show very little resilience towards change of any thing such as power supplied to it. Because of the performance is being optimized for the best output the variables that may have effect have very little room for change and in almost every electronic gadget we expect a constant power supply.

A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits, usually with an output voltage around 1.25 V, close to the theoretical bandgap of silicon at 0°K.

The operation principle of bandgap voltage references is quite straightforward. The voltage difference between two diodes, often operated at the same current and of different junction areas, is used to generate a **p**roportional **t**o **a**bsolute **t**emperature (PTAT) current in a first resistor. This current is used to generate a voltage in a second resistor. This voltage in turn is added to the voltage of one of the diodes (or a third one, in some implementations). The voltage across a diode operated at constant current, or here with a PTAT current, is **c**omplementary **t**o **a**bsolute **t**emperature (CTAT—reduces with increasing temperature), with approximately −2 mV/°K. If the ratio between the first and second resistor is chosen properly, the first order effects of the temperature dependency of the diode and the PTAT current will cancel out. The resulting voltage is about 1.2–1.3 V, depending on the particular technology, and is close to the theoretical bandgap of silicon at 0°K. The remaining voltage change over the operating temperature of typical integrated circuits is on the order of a few millivolts. This temperature dependency has a typical parabolic behavior.

Since the output voltage is by definition fixed around 1.25 V for typical bandgap reference circuits, the minimum operating voltage is about 1.4 V, as in a CMOS circuit at least one drain-source voltage of a FET (field effect transistor) has to be added. Our work concentrates on finding alternative solutions, in which for example currents are summed instead of voltages, resulting in a lower theoretical limit for the operating voltage.

CHAPTER 1

INTRODUCTION

1.1 Theory of Bandgap

Reference voltages or currents that exhibit little dependence on temperature prove essential in many analog circuits. It is interesting to note that, since most process parameters vary with temperature, if a reference is temperature-independent, then it is usually process- independent as well.

How do we generate a quantity that remains constant with temperature? We postulate that if two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a zero TC. For example, for two voltages V_1 and V_2 that vary in opposite directions with temperature, we choose a_1 and a_2 such that

$$a_1 \frac{dV_1}{dT} + a_2 \frac{dV_2}{dT} = 0$$

Obtaining a reference voltage, $V_{REF} = a_1V_1 + a_2V_2$ with zero TC.

We must now identify two voltages that have positive and negative TCs. Among various device parameters in semiconductor technologies, the characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative TCs. Even though many parameters of MOS devices have been considered for the task of reference generation bipolar operation still forms the core of such circuits.

1.2 Negative-TC Voltage

The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a pn-junction diode exhibits a negative TC. We first obtain the expression for the TC in terms of readily-available quantities.

For a bipolar device we can write

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\text{Where} \quad V_T = \frac{kT}{q}$$

The saturation current I_S is proportional to $\mu k T n_i^2$, where μ denotes the mobility of minority carriers and n_i is the intrinsic minority carrier concentration of silicon. The temperature dependence of these quantities is represented as

$$\mu \propto \mu_0 T^m, \text{ where } m \approx -\frac{3}{2},$$

And $n_i^2 \propto T^3 \exp\left[-\frac{E_g}{kT}\right]$, where $E_g \approx 1.12$ eV is the bandgap energy of silicon.

Thus,

$$I_S = bT^{m+4} \exp\left[-\frac{E_g}{kT}\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where b is a proportionality factor. Writing $V_{BE} = V_T \ln(I_c/I_S)$. We can now compute the TC of the base-emitter voltage. In taking the derivative of V_{BE} with respect to T we must know the behavior of I_C as a function of the temperature. To simplify the analysis, we assume for now that I_C is held constant.

Thus,

$$\frac{\delta V_{BE}}{\delta T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\delta I_S}{\delta T} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

Thus from (1),

$$\frac{\delta I_S}{\delta T} = b(4+m)\, T^{m+3} \exp\left[-\frac{E_g}{kT}\right] + bT^{m+4} \exp\left[-\frac{E_g}{kT}\right]\left[\frac{E_g}{kT^2}\right] \quad \ldots\ldots (3)$$

Therefore,

$$\left(\frac{V_T}{I_S}\right)\frac{\delta I_S}{\delta T} = (4+m)\frac{V_T}{T} + \left[\frac{E_g}{kT^2}\right] \quad \ldots\ldots (4)$$

From (2) and (4),

$$\frac{\delta V_{BE}}{\delta T} = \frac{V_T}{T}\ln\left(\frac{I_C}{I_S}\right) - (4+m)\frac{V_T}{T} - V_T\left[\frac{E_g}{kT^2}\right]$$

$$= \frac{V_B - (4+m)V_T - \frac{E_g}{q}}{T} \quad \ldots\ldots (5)$$

Equation (5) gives the temperature coefficient of the base-emitter voltage at a given temperature T, revealing dependence on the magnitude of V_{BE} itself. With $V_{BE} \approx 750$ mV and T = 300°K, $\frac{\delta V_{BE}}{\delta T} \approx -1.5$ mV/°K.

From (5), we note that the temperature coefficient of V_{BE} itself depends on the temperature, creating error in constant reference generation if the positive-TC quantity exhibits a constant temperature coefficient.

1.3 Positive-TC Voltage

If two bipolar transistors operate at unequal current densities, then the *difference* between their base-emitter voltages is directly proportional to the absolute temperature. For example, as shown in Fig. 1.1, if two identical transistor (I_{s1}= I_{s2}) are biased at collector currents of nI_o and I_o and their base currents are negligible, then

$$\Delta V_{BE} = V_{BE1} - V_{BE}$$

$$= V_T \ln\left(\frac{nI_o}{I_{s1}}\right) - V_T \ln\left(\frac{I_o}{I_{s2}}\right)$$

$$= V_T \ln(n) \ldots\ldots\ldots\ldots (6)$$

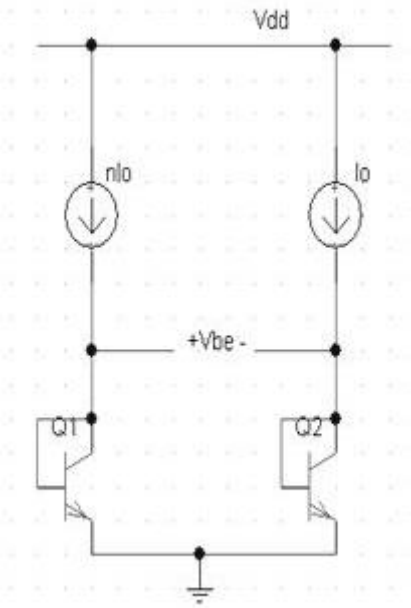

Fig. 1.1 Generation of PTAT Voltage

Thus, the V_{BE} difference exhibits a positive temperature coefficient:

$$\frac{\delta V_{BE}}{\delta T} = \frac{k}{q}\ln(n) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

Interestingly, this TC is independent of the temperature or behavior of the collector currents.

1.4 Bandgap Reference

With the negative and positive-TC voltages obtained above, we can now develop a reference having a normally zero temperature coefficient.

We write, $V_{REF}= a_1V_{BE}+a_2V_T \ln(n)$, where $V_T \ln(n)$ is the difference between the base-emitter voltages of the two bipolar transistors operating at different current densities. How do we choose a_1 and a_2?

Since at room temperature $\frac{\delta V_{BE}}{\delta T} \approx -1.5\ \text{mV}/°K$

Whereas $\frac{\delta V_T}{\delta T} \approx 0.087\ \text{mV/K}$

We may set $a_1 = 1$ and choose $a_2 \ln(n)$ such that,

$a_2 \ln(n)(0.0875\text{mV/K})=1.5\text{mV/K}$. That is $a_2 \ln(n) \approx 17.2$, indicating that for zero TC:

$$V_{REF} = V_{BE}+17.2V_T \approx 1.25 \quad \text{..... (8)}$$

Let us now devise a circuit that adds V_{BE} to $17.2V_T$. First consider the circuit shown in Fig. 1.2 where base currents are assumed negligible, transistor Q_2 consists of n units connected in parallel and Q_1 is a unit transistor. Suppose we somehow force that V_{01} and V_{02} are kept equal. Then $V_{BE1} = RI+ V_{BE2}$ and $RI= V_{BE1} - V_{BE2} = V_T \ln(n)$. Thus,

$V_{02} = V_{BE2} + V_T \ln(n)$, which implies that V_{02} can be used as a temperature independent reference if $\ln(n) \approx 17.2$

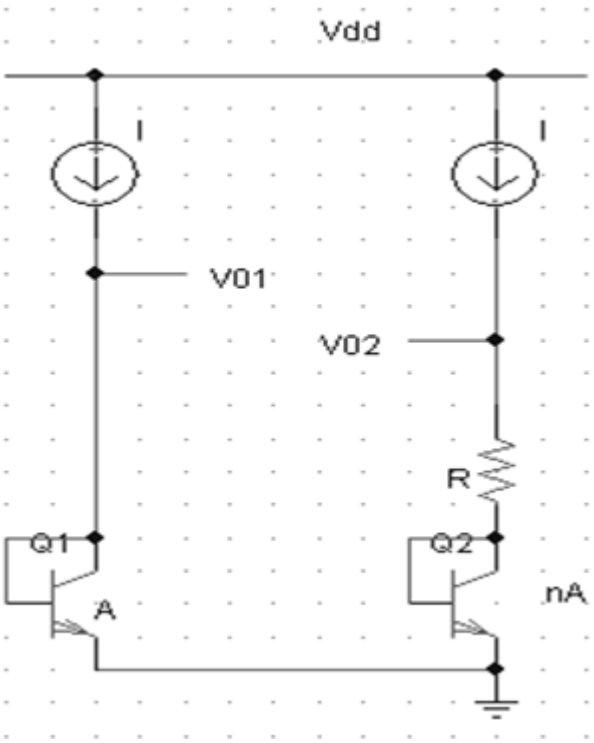

Fig. 1.2 Conceptual Generation of Temperature Independent Voltage

The circuit of Fig. 1.2 requires two modifications to become practical. First a mechanism has to be included to guarantee $V_{01} = V_{02}$. Second, since ln(n) =17.2 translates to a prohibitively large n, the term $RI = V_T \ln(n)$ must be scaled up by a reasonable factor. Fig. 1.3 is an implementation where both criteria are satisfied.

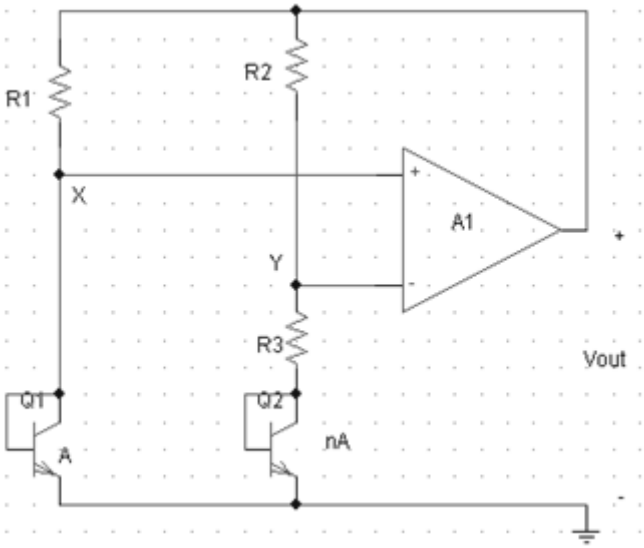

Fig. 1.3 Actual Implementation of the Concept Shown in Fig. 1.2

Here the amplifier A1 senses the voltages at X and Y generates an output voltage which drives the top terminal of R_1 and R_2 in such a way that the circuit settles to approximately equal voltages at X and Y. The reference voltage is obtained at the output of the amplifier rather than at the point X or Y. because the output of the Op-amp has an expression similar to (8).For this circuit the output is,

$$V_{out} = V_{BE2} + V_T \ln(n) \frac{R_2+R_3}{R_3} \quad \text{..... (9)}$$

$$= V_{BE2} + V_T \ln(n) \left(\frac{R_2}{R_3} + 1\right)$$

For a zero-TC we must have

$$\left(\frac{R_2}{R_3} + 1\right) \ln(n) \approx 17.2$$

For example we may chose n=31 and $R_2 / R_3 = 4$.

1.5 Compatibility with CMOS technology

In our derivation of a temperature independent voltage we relied on the exponential characteristics of the bipolar devices for both negative and positive TC quantities. Though we used npn transistors in our derivation in CMOS process, npn transistors cannot be fabricated easily. We must therefore seek structures those can be easily fabricated in a standard CMOS technology that exhibits such characteristics.

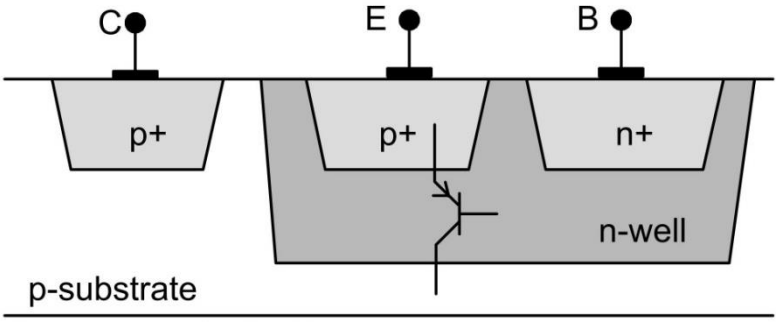

Fig. 1.4 Realization of a pnp Bipolar Transistor in CMOS Technology

In n-well process a pnp transistor can be formed as depicted in Fig. 1.4. An n-well is made in the p-substrate and inside the n-well a p+ region is built that serves as the emitter. The n-well itself acts as the base and the p–type substrate acts as the collector. The collector thus is connected to the most negative supply (usually ground).Thus the circuit of Fig. 1.3 becomes that of Fig. 1.5.

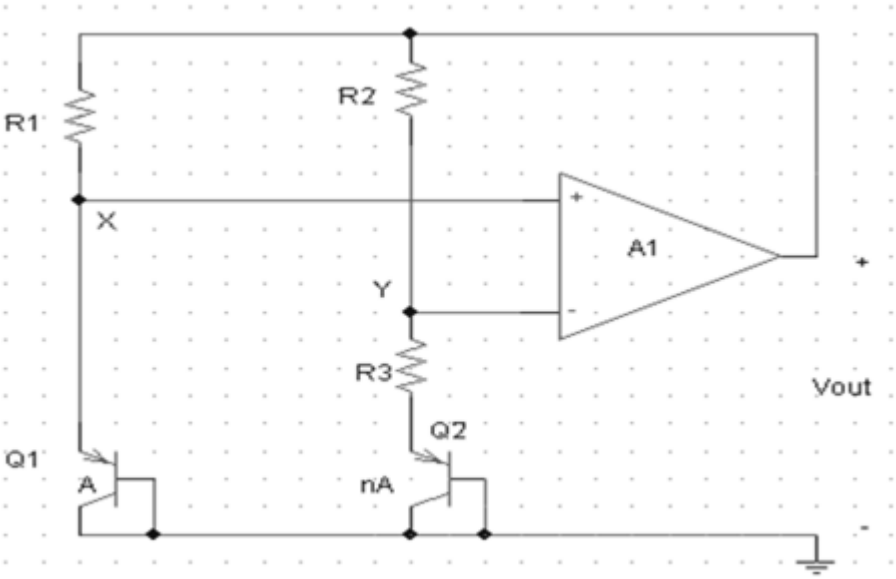

Fig. 1.5 Circuit of Fig. 1.3 Implemented with pnp Transistors

1.6 Bandgap Core

The bandgap core acts as an oscillator. Looking at Fig. 1.5 we can see that there is no direct connection of the core with the power supply. The core is driven by the output of the Op-amp. The two point X and Y are connected to the input of the Op-amp. This is like the connection used in Wien-bridge oscillator. The connection to the positive input terminal acts as the positive feedback and the connection to the negative terminal acts as the negative feed back. When the circuit is turned on the positive feedback prevails and the output voltage increases. However as the output voltage reaches a certain level the negative feed back at that point equals the positive feedback. So output cannot exceed that value. As a result the output of the Op-amp settles at that point.

To demonstrate the fact the circuit of Fig. 1.6 was simulated in Hspice. The V_{DD} was swept and the voltages V1 and V2 were plotted.

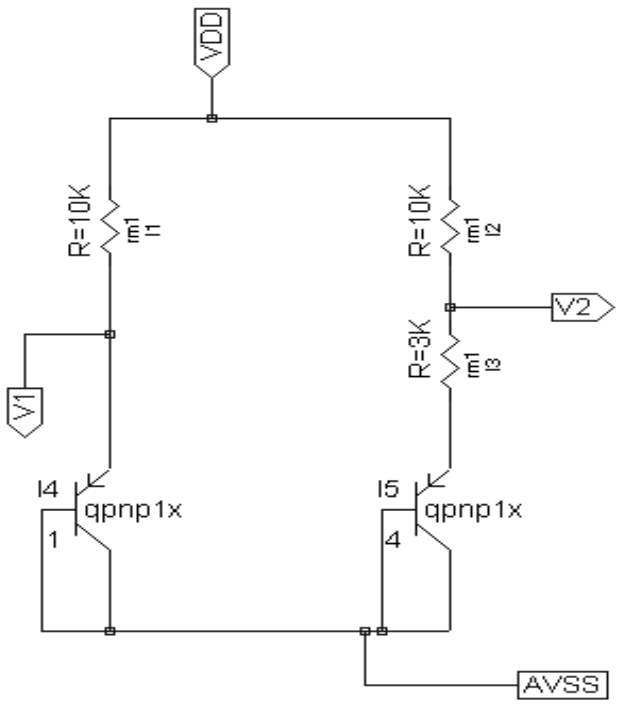

Fig. 1.6 Bandgap Core

The simulated plot is shown in the following figure.

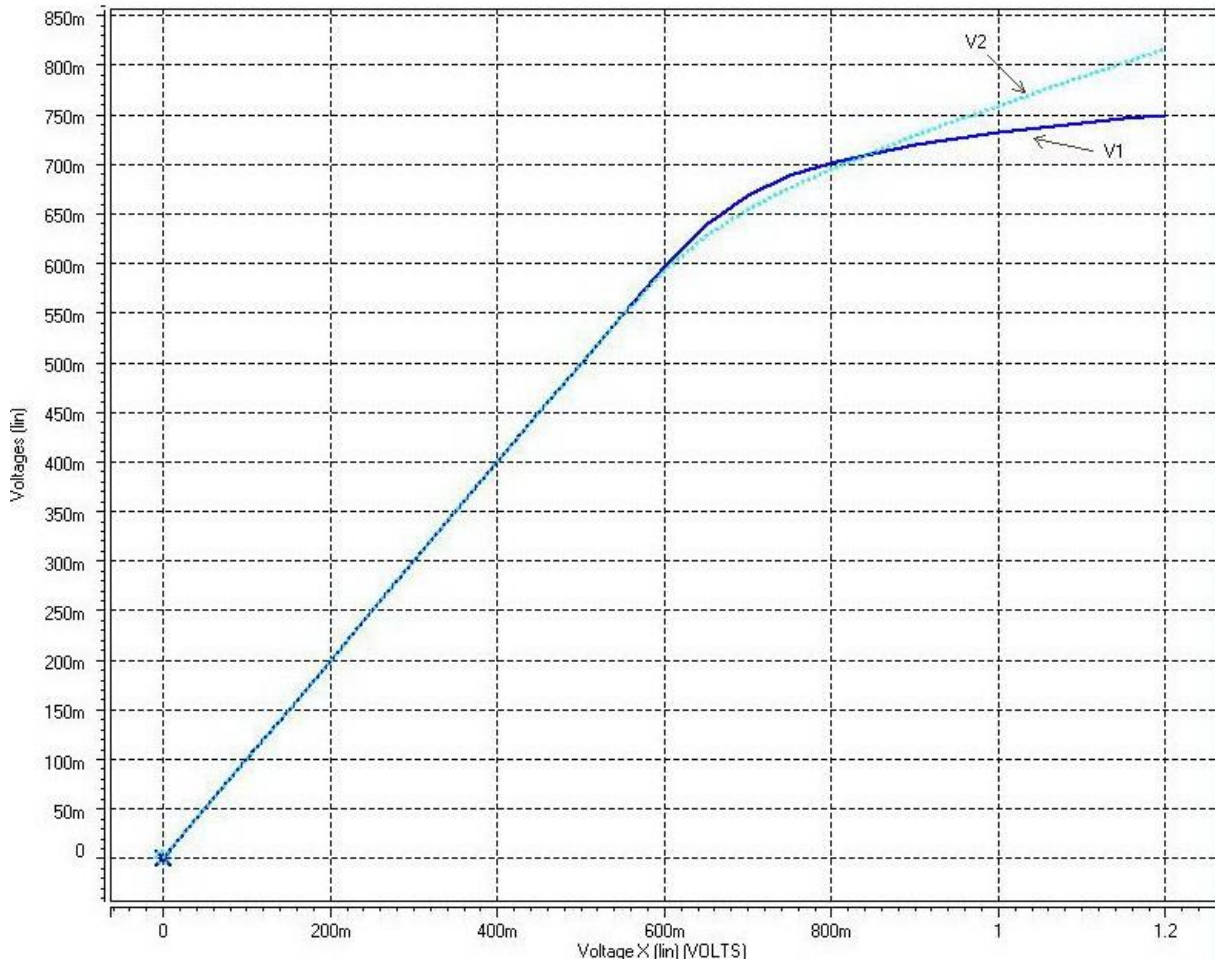

Fig. 1.7 V_1 vs. V_{DD} or V_2 vs. V_{DD} Curves for the Bandgap Core Shown in Fig. 1.6

Now when the circuit is turned on, if somehow the output increases above zero volt, from the curve we see that V1 > V2. Since V1 is connected to the positive input of the Op-amp and V2 is connected to the negative input terminal of the Op-amp the output of the Op-amp will tend to increase which will further increase the difference between V1 and V2. However, as the output of the Op-amp reaches about 0.8 volt we see that the difference between V1 and V2 decreases to zero. And the curve of V1 and V2 intersect at about 0.85 volt. That means after that point V2>V1 and the Op-amp will tend to give negative output, which in reality will lower the Op-amp output. So, the output of the Op-amp will settle at the intersection of the two curves.

Now the purpose of connecting the bandgap core to the output of the Op-amp not the power supply is to make the bandgap core operation independent of the power supply. Since the Op-amp gain is infinite, basic circuit analysis shows that the Op-amp output is independent of the power supply.

Thus if we use two elements in this configuration and the two elements are such that there voltage curves cut at a fixed point, and their two points are connected to the input terminals of the Op-amp in the proper way the Op-amp output will be power supply independent. For example the circuit in Fig. 1.8 will yield a supply independent output.

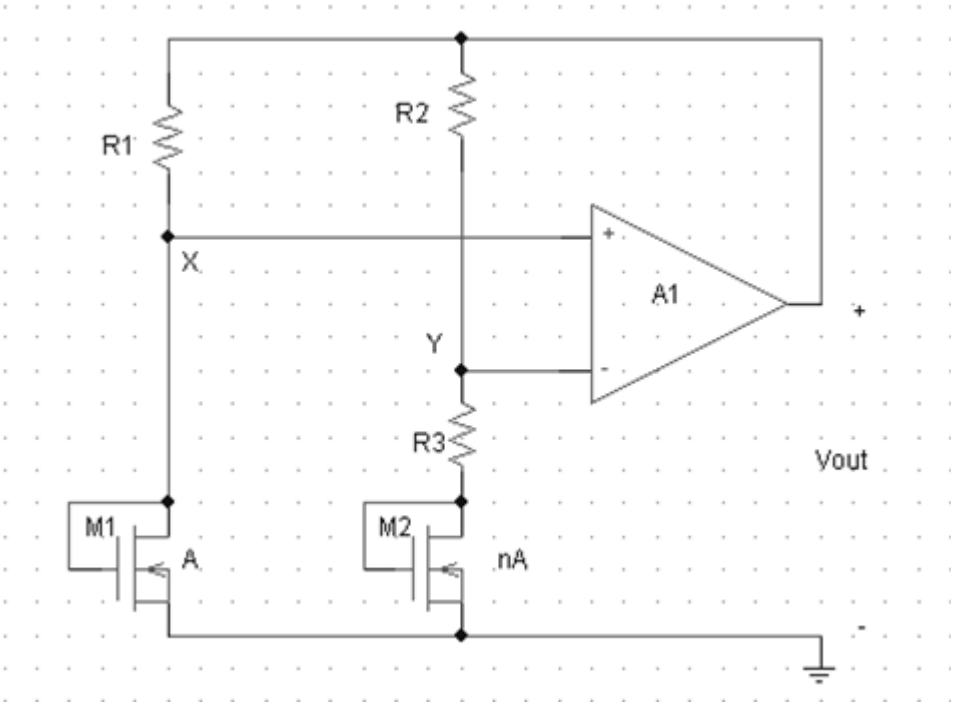

Fig. 1.8 Circuit of Fig. 1.3 Implemented with MOSFET

But the Op-amp output of Fig. 1.8 will not be temperature independent. Because, as the temperature varies the characteristics curve of the elements will shift and as a result there intersection will also shift. Since the intersecting point determines the Op-amp output, the output varies as the temperature varies.

However, in the case of the circuit of Fig. 1.6, by adjusting the value of the resistances it can be made such that the intersection point shifts vertically so that as the temperature varies, the input voltage at the intersection point remains same. That happens when we vary the resistance values according to equation (9). But this has not been yet accomplished for the circuit of Fig. 1.8 with NMOS. So the bandgap core must have BJTs.

In our arguments we stated that initially the output of the Op-amp must be non-zero other wise its output voltage will not build up. So, there must be a mechanism that will ensure that after the startup the output is non-zero and there is voltage buildup. If no startup is used then the output may remain at zero voltage indefinitely because the two curves also intersect at the zero voltage point. So, it is possible that the output will settle at that point unless pulled out of that degenerate point.

CHAPTER 2

CIRCUIT OPERATION

This chapter describes the operation of our circuit. Every part of our circuit will be discussed in detail. At the end of this chapter the complete schematic of the circuit will be presented. The circuit is drawn using software named COHESION DESIGNER.

2.1Basic Structure

The block diagram of the circuit is given below:

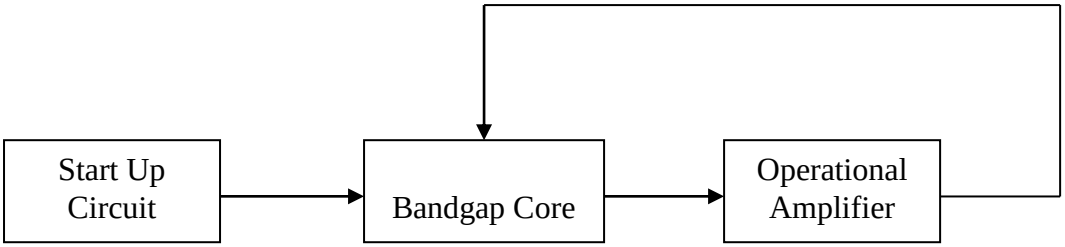

Fig. 2.1 Block Diagram of Bandgap Circuit

As we can see from the diagram the circuit consists of 3 parts:

1) Bandgap Core
2) Startup circuit
3) Operational Amplifier

Startup circuit is only used to start the operation of the circuit by injecting current into bandgap core. When the circuit reaches steady state, it turns off. Bandgap core provides the required reference voltage, which is insensitive to variation in temperature and supply voltage. Operational Amplifier is used to drive the bandgap core. Now each part will be discussed in detail.

2.1.1 Bandgap Core

This is the most important part of any bandgap circuit. This part produces reference voltage. The schematic of the circuit is given below:

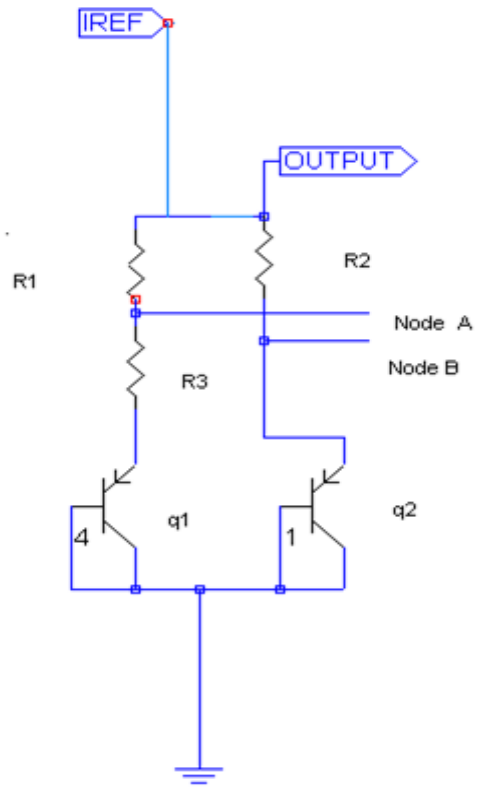

Fig. 2.2 Bandgap Core

Node A and Node B are actually input to the operational amplifier. Voltage of these two nodes is equal. IREF is a reference current source which is actually the output of OPAMP.R_1 R_2 and R_3 are nwell resistances. Two transistors are actually vertical inherent BJTs of CMOS process.

From the schematic of the circuit we can see that there are two branches in this core circuit. Initially current in branch1 (branch having R_1 and R_3) is higher than that of branch2 (branch having R_2).As discussed in previous chapters, at steady state current through each branch becomes equal. Therefore voltage of node A and node B becomes equal. Since voltages of node A and node B are equal, therefore the voltage across the resistor R_2 is

$$V_{R2} = I_2 \times R_2$$
$$= \frac{V_{BE2} - V_{BE1}}{R_3} \times R_2$$
$$= V_T \ln(n) \times \frac{R_2}{R_3}$$
$$= V_T \ln(4) \times \frac{R_2}{R_3}$$; [n = 4 for our circuit]

V_T is thermal voltage, whose expression is given as

$$V_T = \frac{K \times T}{q}$$

So V_T is directly proportional to absolute temperature (T).

VR2 is a positive TC voltage. And we know from the theory of BJT (discussed in previous chapters) Base emitter voltage of a BJT is conversely proportional to temperature, which is 1.94 mV/°C for the BJT's used in this circuit.

$$V_{out} = V_{R2} + V_{BE2}$$
$$= [V_T \ln(4) \times \frac{R_2}{R_3}] + V_{BE2}$$

Thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).

2.1.2 Startup Circuit

In the circuit of bandgap core, if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both branches. So we need to inject current in the bandgap core for proper operation of the circuit. Start up circuit does this job. This circuit also turns off when steady state is reached. A very simple start up circuit is used in bandgap circuit. Its schematic is given below:

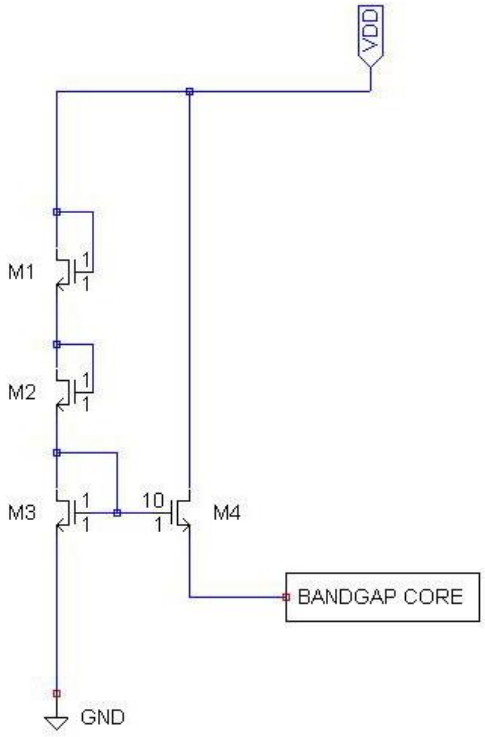

Fig. 2.3 Startup Network

During starting no current flows in bandgap circuit. Output voltage (which is also the source voltage of M4) is zero. So M4 is on. It is mirrored with M3. So drain current of M3 and M4 is equal. Thus current is injected into bandgap core. But as circuit reaches steady state, source voltage of M4 becomes equal to reference voltage (about 1.2V).Now since three diode connected MOS are in series, gate voltage of M4 becomes sufficiently low(due to drain source voltage drop in M1,M2,M3)so that it turns off.

2.1.3 Operational Amplifier

Operational Amplifier used on this circuit is basically a two stage differential amplifier. The main function of the operational amplifier is to drive the bandgap core. Operational Amplifier is designed in such a way that its output is insensitive to variation in supply. This helps to establish a reference voltage which is insensitive to supply. The schematic of OPAMP circuit is given below.

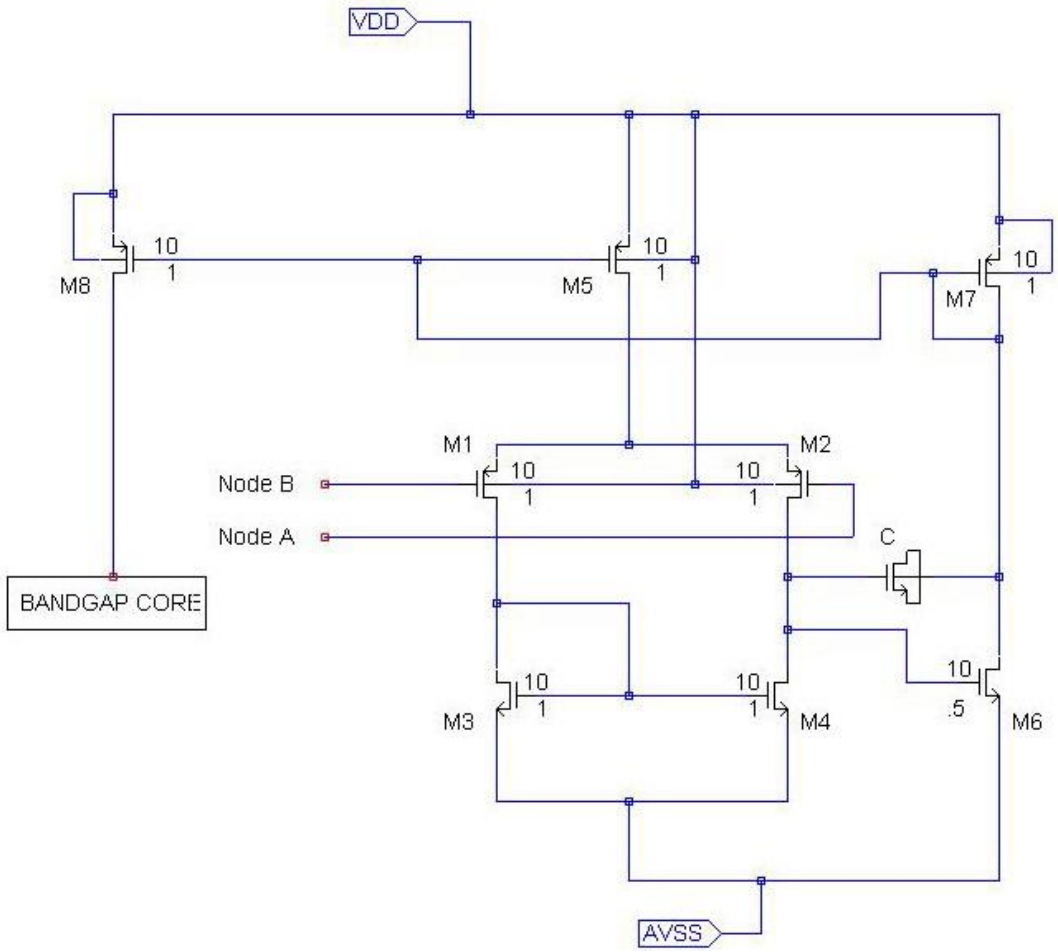

Fig. 2.4 Schematic of OPAMP

As we can see from the figure this is basically a two stage CMOS differential OPAMP. M1 and M2 are differential pair. M3 and M4 act as load. The current mirror formed by M5 and M8 supplies the differential pair with bias current. The second stage consists of M6, which is a common source amplifier actively loaded with the current source transistor M7. A capacitor C is included in the negative feedback path of the second stage. Its function is to enhance the Miller effect already present in M6 and thus provide the OPAMP with a dominant pole.

Ideally our operational amplifier should have infinite gain for proper function of bandgap core. Output current of operational amplifier drives the bandgap core. As differential input voltage of the operational amplifier is very small, small gain in amplifier will not produce enough current to drive the bandgap core. Transconductance of a MOSFET is not very high. So for proper function of bandgap core we need to increase the gain of the circuit. That's why a two stage operational amplifier has been used.

But in a two stage amplifier, there is more than one pole which tries to make the circuit unstable. To make sure that the circuit is stable, stability analysis of the op amp has to be done.

Another important aspect of OPAMP design is to produce a current which is insensitive to variation of V_{DD} (supply voltage).This is accomplished by driving the operational amplifier with its own output current. This is done by mirroring M5 and M7.This makes the output current of operational amplifier almost constant with respect to voltage.

2.2 Stability Analysis of the Operational Amplifier

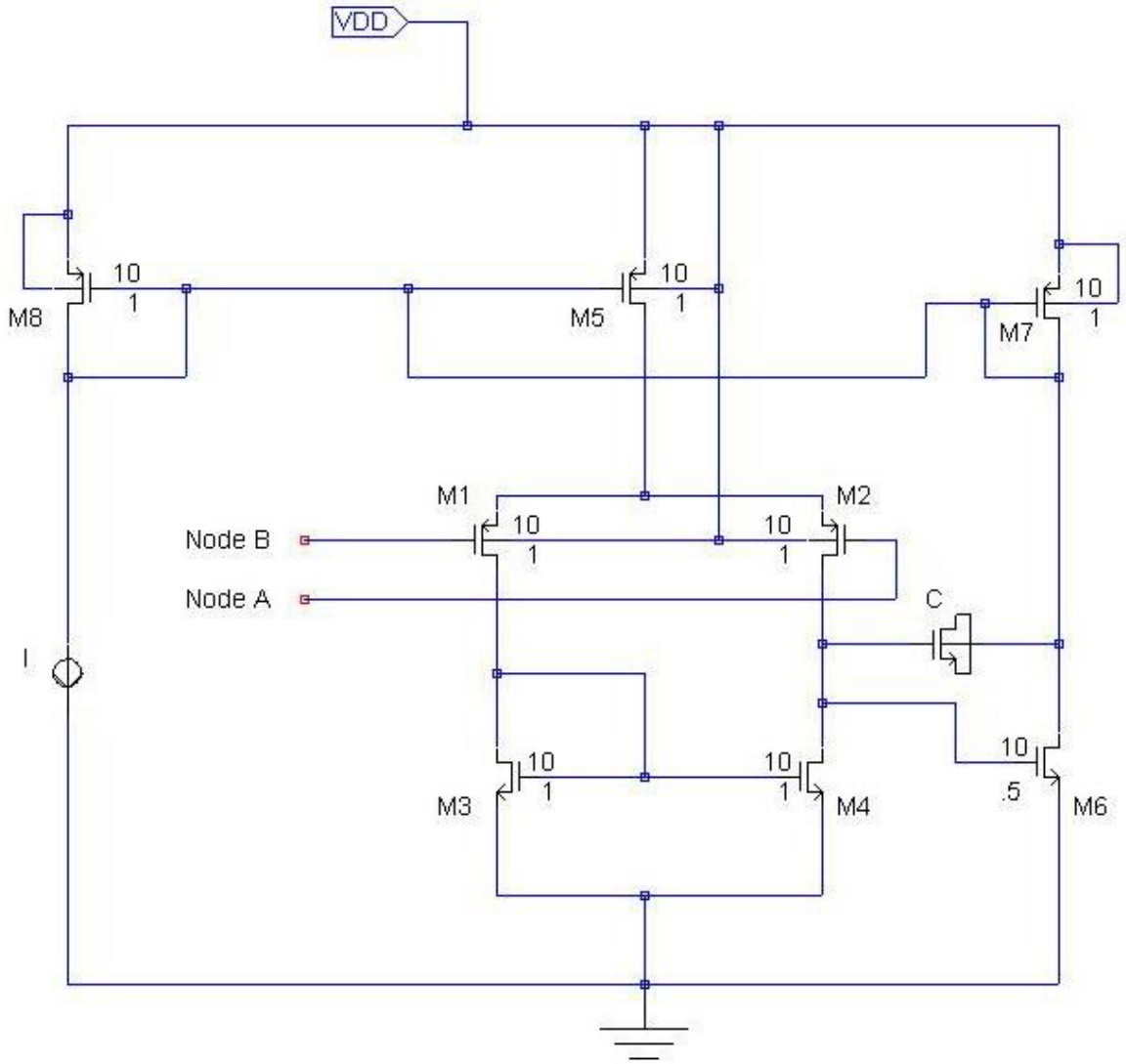

Fig. 2.5 Two-stage Amplifier

For stability analysis, we need to know gain margin and phase margin of the two stage op amp. Now we consider the simplified equivalent circuit shown in the following figure.

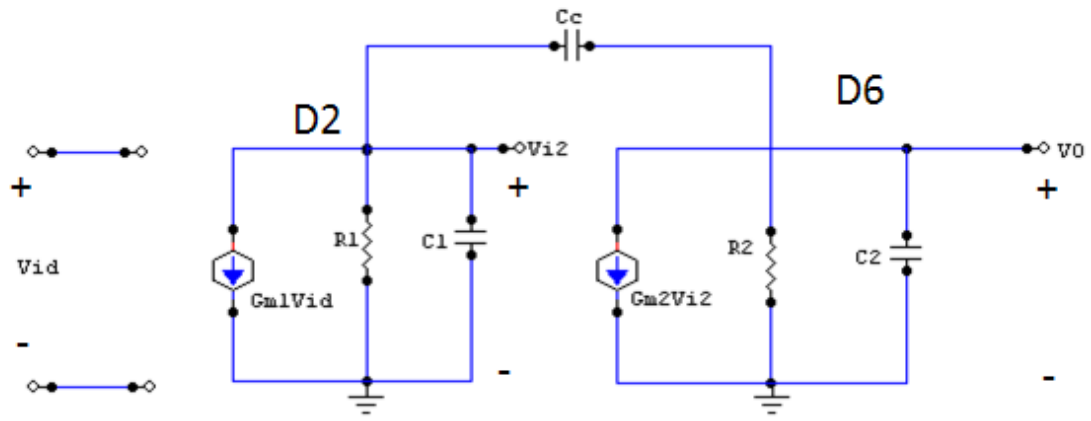

Fig. 2.6 Small Signal Equivalent Circuit of the Two Stage CMOS Op-Amp.

Here

Input stage transconductance, $G_{m1}= g_{m1}= g_{m2}$

Output resistance of the first stage, $R_1= r_{02} \| r_{04}$

Total capacitance at the interface between the first and the second stages C_1,

$$C_1= C_{gd4} +C_{db4} +C_{gd2} +C_{db2} +C_{gs6}$$

Transconductance of the second stage, $G_{m2} = g_{m6}$

Output resistance of the second stage, $R_2= r_{06} \| r_{07}$

Output node capacitance, $C_2 = C_{db6} +C_{gd7} +C_{db7} +C_L$

Where C_L is the load capacitance, which is usually much larger than that of transistors capacitances, hence C_2 is much larger than C_1. Finally we have neglected the capacitance C_{gd6}, because it is parallel to C_c and $C_c >> C_{gd6}$.

To determine the output voltage and hence the transfer function of the amplifier, first we have to find the node equation at the node D_2 and D_6.

$$G_{m1}V_{id} + (V_{i2}/R_1) + sC_1V_{i2} +sC_c(V_{i2}-V_0)=0$$

$$G_{m2}V_{i2} + (V_0/R_2) + sC_2V_0 + sC_c(V_0 - V_{i2})=0$$

Solving these two equations we find the transfer function A_v ,

$$\frac{V_0}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_c)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_c(C_1 + C_2)]R_1R_2}$$

Table 1: Values of some of the Level-1 MOSFET model parameters for 0.5µm CMOS process

	NMOS	PMOS
t_{ox}	9.5×10^{-9}	9.5×10^{-9}
μ_0	460	115
λ	0.1	0.2

Table 2: Values of width & length of the MOSFET's used in the amplifier

MOSFET	Width (µm)	Length(µm)	Multiplier
M1	1	1	1
M2	1	1	1
M3	1	1	1
M4	10	1	1
M5	10	1	1
M6	10	1	500
M7	10	1	1
M8	10	1	1

$\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m

$t_{ox} = 9.5 \times 10^{-9}$ m

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.63 \times 10^{-3}$ F/m^2

μ_n = 460 cm^2/V-s = 460×10^{-4} m^2/V-s

μ_p= 115 cm^2/V-s = 115×10^{-4} m^2/V-s

Let I = 60×10^{-6} A

For transistor M1, I_D= 30×10^{-6}A, W= 10µm, L=1µm

Now $I_D = \frac{1}{2}\ \mu n\ Cox\ (\frac{W}{L})Vov^2$

⇨ $30\times10^{-6} = \frac{1}{2} \times 460\times10^{-4} \times 3.63 \times 10^{-3} \times \frac{10\times10^{-6}}{1\times10^{-6}} \times Vov^2$

⇨ $Vov^2 = 0.0179662$

⇨ $Vov = 0.13404$ V

$g_{m1} = \frac{2I_D}{V_{ov}} = 447.76 \times10^{-6}$ mho

$G_{m1} = g_{m1} = g_{m2} = 447.76 \times10^{-6}$ mho

$r_0 = \frac{1}{\lambda I_D} = 333.33$ kΩ

$r_{02} = r_{04} = 333.33$ kΩ

$R_1 = r_{02} || r_{04} = 166.67$ kΩ

For transistor M6, $I_D = 60\times10^{-6}$A, W= 500×10μm, L=0.5μm

$I_D = \frac{1}{2}$ μp Cox $(\frac{W}{L})Vov^2$

⇨ $60\times10^{-6} = \frac{1}{2} \times 115 \times 10^{-4} \times 3.63 \times 10^{-3} (\frac{500\times10\times10^{-6}}{0.5\times10^{-6}}) \times Vov^2$

⇨ $Vov^2 = 2.87 \times 10^{-4}$

⇨ $Vov = 16.95 \times 10^{-3}$ V

$g_{m6} = \frac{2I_D}{V_{ov}} = 7.078 \times10^{-3}$ mho

$G_{m2} = g_{m6} = 7.078 \times10^{-3}$ mho

$r_0 = \frac{1}{\lambda I_D} = 83.33$ kΩ

$r_{06} = r_{07} = 83.33$ kΩ

$R_2 = r_{06} || r_{07} = 41.67$ kΩ

Let, $C_{gd} = 5 \times10^{-15}$ F $C_{db} = 5 \times10^{-15}$ F $C_{gs} = 20 \times10^{-15}$ F $C_L = 10 \times10^{-12}$ F $C = 1 \times10^{-9}$ F

$C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6} = 40 \times10^{-15}$ F

$C_1 = C_{db6} + C_{gd7} + C_{db7} + C_L = 10.015 \times10^{-12}$ F

$$\frac{V_0}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_c)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_c(C_1 + C_2)]R_1R_2}$$

Substituting the calculated values in the above equation, we obtain

$$\frac{V_0}{V_{id}} = \frac{22010.85 - 3.1098 \times 10^{-3}\mathrm{s}}{1 + \mathrm{s}[49.366 \times 10^{-3}] + s^2[6.9836 \times 10^{-11}]}$$

Using MATLAB we get bode plot, gain margin and phase margin as follows

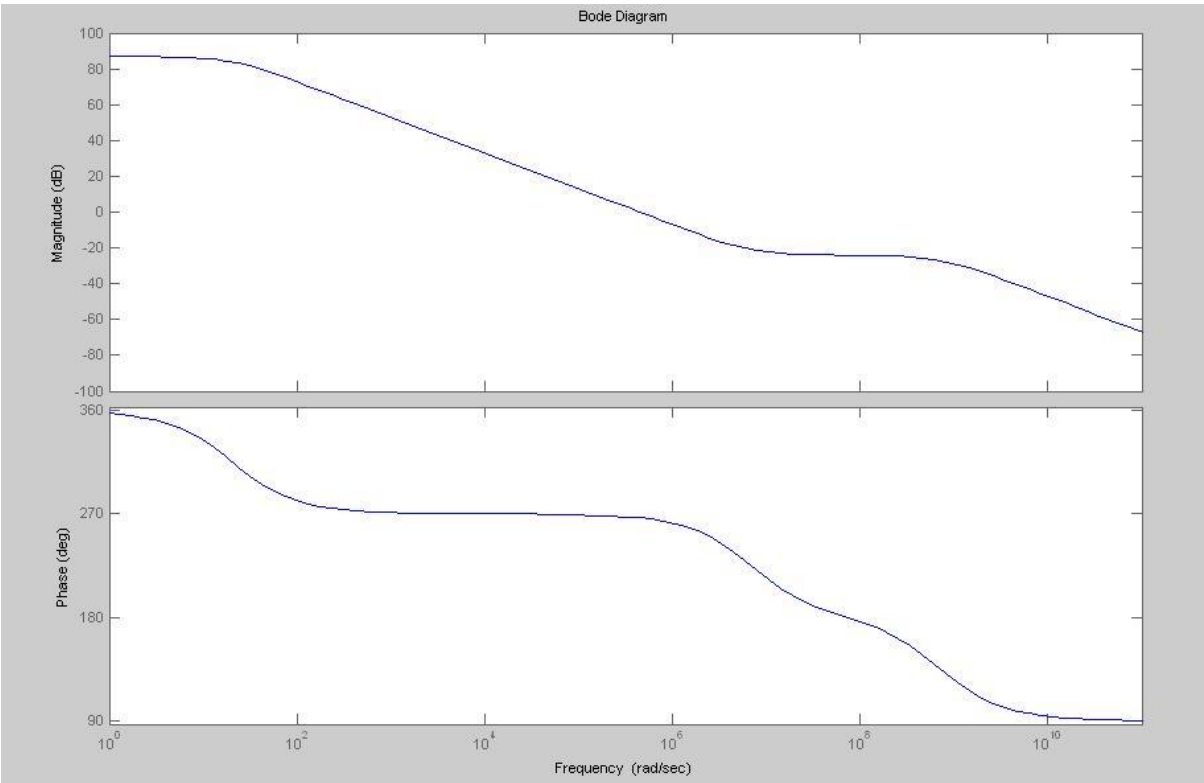

Fig. 2.7 Bode Plot

Gain Margin = 15.8743 dB

Phase Margin = 86.3547 deg

2.3 Schematic of Complete Circuit

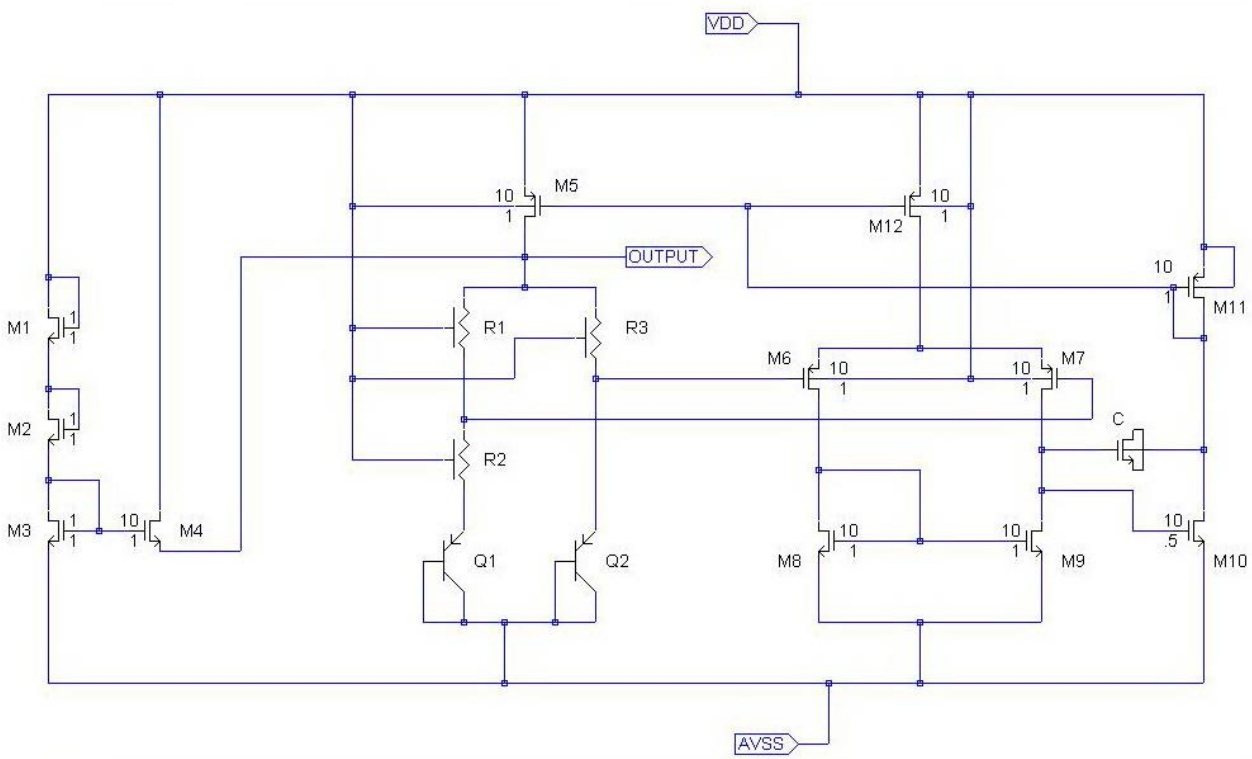

Fig. 2.8 Bandgap Reference Circuit

This is the schematic of complete circuit. All parts of this circuit were described in detail. We have used 0.5 micron process. All the resistances used in this circuit are n-well diffusion resistance. The BJT (bipolar junction transistor) used is the inherent BJT of a MOSFET. In this circuit V_{DD} denotes supply voltage, Output denotes output of circuit and AVSS denotes analog ground.

CHAPTER 3

ANALYSIS OF SIMULATION RESULTS

All the simulations were done using Hspice. The models of the device were used based on MXIC data. We used 0.5 micron process in our design. In this chapter we will give the result of our design.

3.1 Variation of Reference Voltage with respect to Temperature

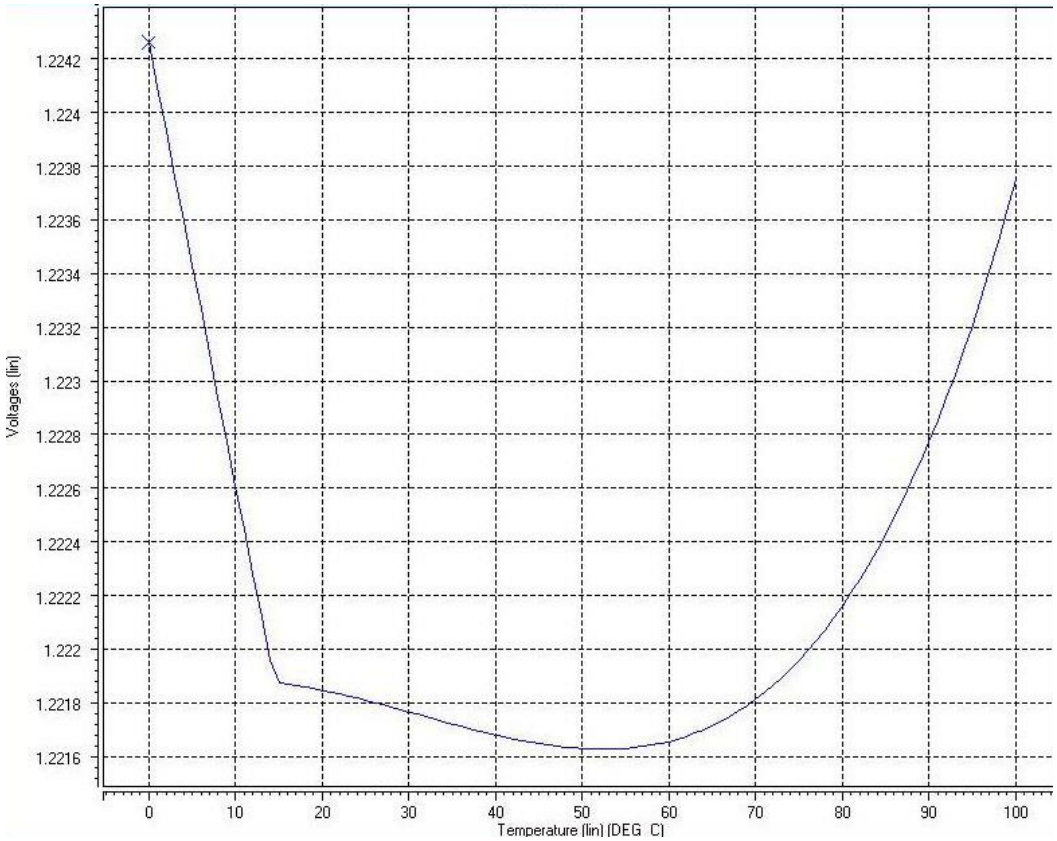

Fig. 3.1 Variation of Reference Voltage with respect to Temperature

As we see from wave shape, reference voltage is approximately 1.2218V at room temperature. And reference voltage almost remains constant from 20 to 70C.Total variation of reference voltage is about 2.6mv which is 0.213% of reference voltage. This same variation is 0.63% of reference voltage when the bandgap reference circuit is designed with a single stage amplifier [1].

3.2 Variation of Reference Voltage with respect to V_{DD}

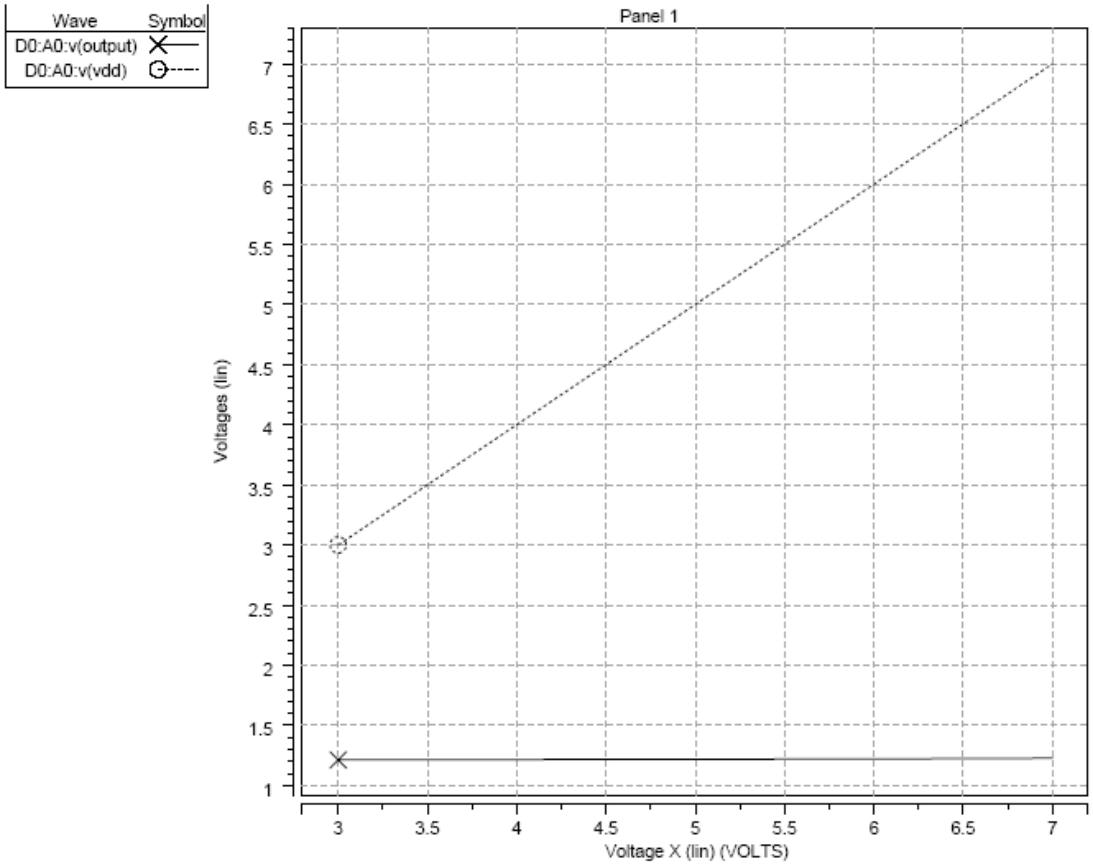

Fig. 3.2 Variation of Reference Voltage with respect to V_{DD}

As V_{DD} changes from 3V to 7V, the change in reference voltage is about 11mv, which is 0.275% with respect to change in V_{DD}. This same change in reference voltage is 0.35% with respect to change in V_{DD} when the bandgap reference circuit is designed with a single stage amplifier [1].

3.3 Variation of Reference Voltage with respect to Time

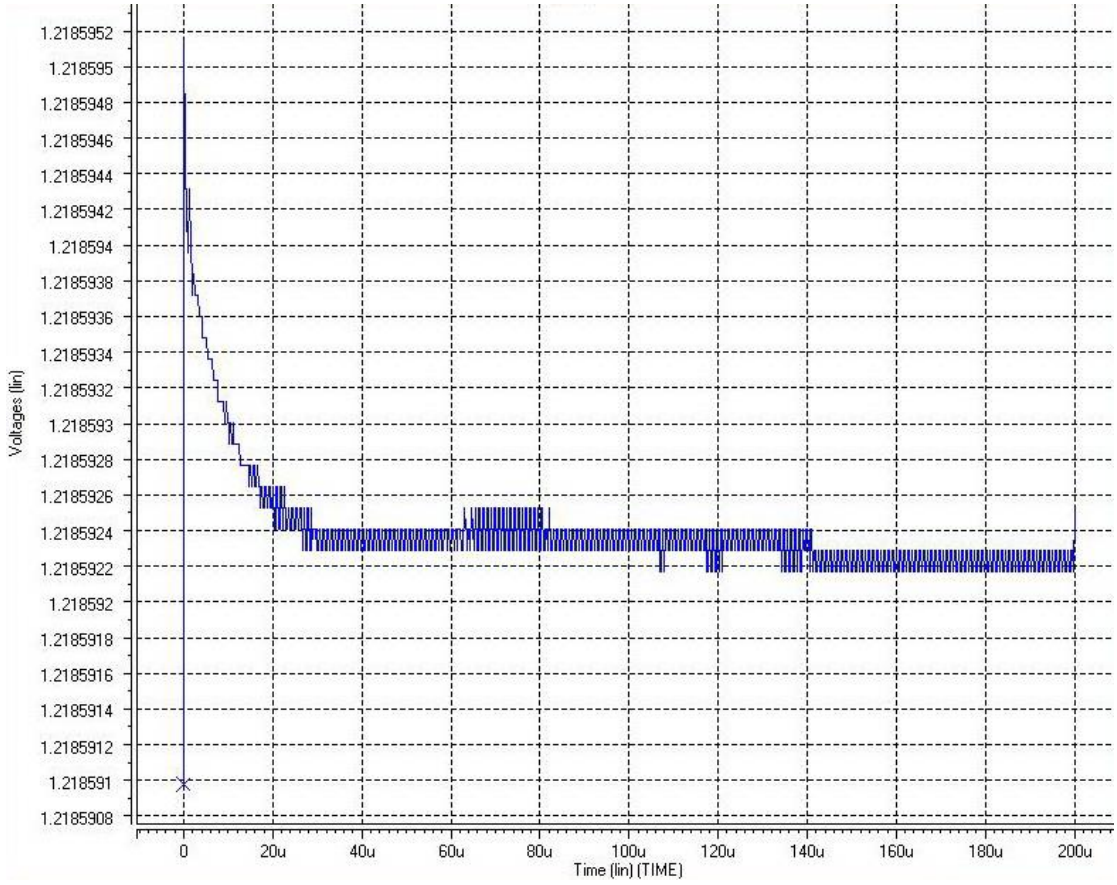

Fig. 3.3 Variation of Reference Voltage with respect to Time

From transient analysis it is observed that, reference voltage settles to fixed value after 25µs.Although there is oscillation after that, the amplitude of oscillation is in microvolt range and it can be neglected.

3.4 Variation of Reference Voltage with respect to Noise in Supply

Here we have assumed that noise voltage is a sine voltage having amplitude of 1V, frequency of 1Mega Hertz and damping factor of 10^5. Initially there is oscillation in reference voltage, but eventually reference voltage settles to steady state value.

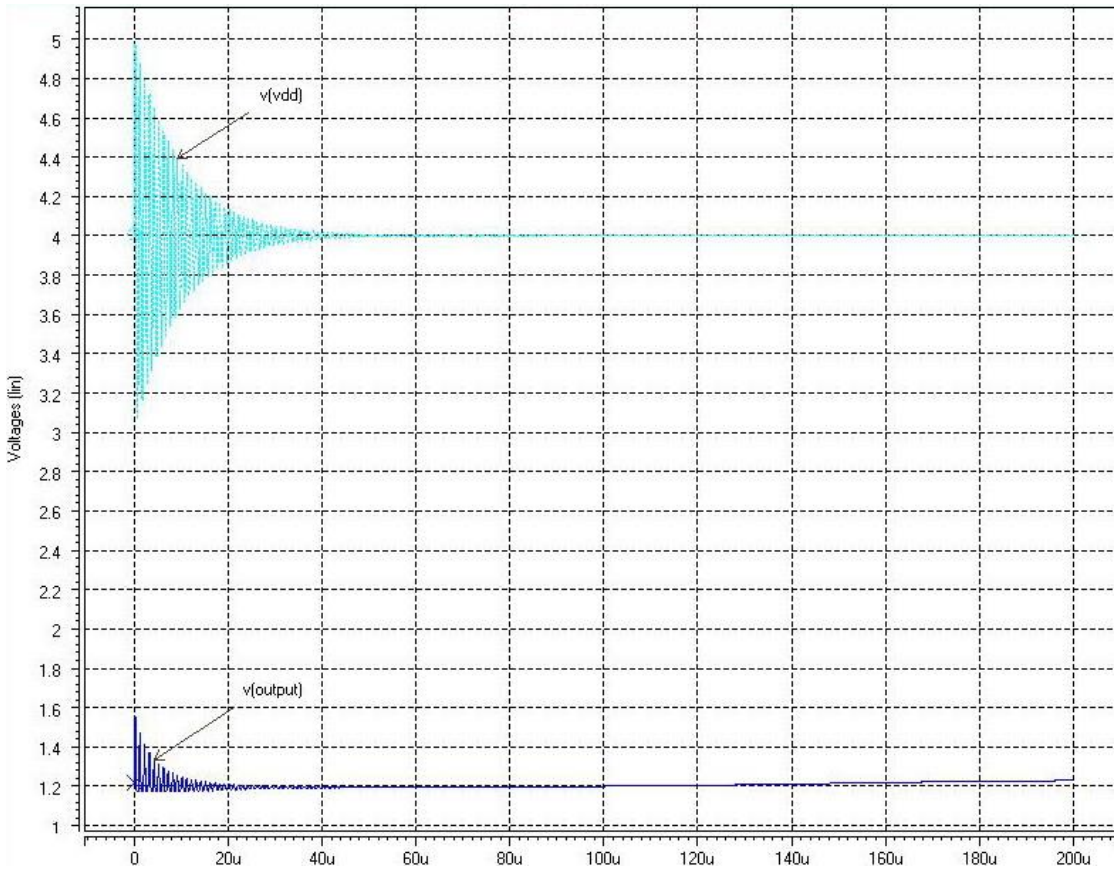

Fig. 3.4 Variation of Reference Voltage with respect to Supply Noise

CHAPTER 4

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

In this thesis we have designed a bandgap reference circuit in CMOS process. As a conclusion of this thesis key points of previous chapters are summarized. Also future works to be done in this thesis are discussed.

4.1 Summary

In this thesis we have designed a simple bandgap reference circuit in 0.5 micron CMOS process. The parasitic BJT of a CMOS process (pnp transistor between source, nwell and p substrate) is used in the bandgap core. Bandgap core produces a voltage that is insensitive to variation in temperature. This is achieved by summing a positive TC voltage and a negative TC voltage. In our circuit the variation of reference voltage is about 0.213% with respect to change in temperature which is better than the previously designed bandgap reference circuit (0.63%) using a single stage amplifier.

The operational amplifier used in our circuit is a two stage differential amplifier. The operational amplifier accomplishes two important tasks:

1) To drive the bandgap core.
2) To provide a voltage insensitive to variation in supply.

The variation of reference voltage is about 0.275% with respect to supply voltage which is better than the previously designed bandgap reference circuit (0.35%) using a single stage amplifier.

The bandgap reference circuit can support a zero current even when the power supply is on. So for proper operation we need to turn on the circuit. Therefore we have used a simple start-up circuit. When the circuit is turned on, this inverter circuit is turned off.

The main goal of our thesis is to design the circuit in CMOS process. This helps us to avoid BiCMOS process which is a little bit complicated and much more expensive than CMOS process.

4.2 Future Work

1) A layout of this circuit should be made.
2) We have used Hspice as our simulator. But CADENCE is a much powerful simulator. Simulating the circuit using CADENCE will give much more realistic result.
3) Changing the resistance of the bandgap core it is possible to design a reference circuit which shows satisfactory performance in the high temperature region.

BIBLIOGRAPHY

1. Wasim Hossain,Vashwar Tajdidur Rouf & Ryan Rakib, “CMOS Bandgap Circuit Design” Undergraduate Thesis, October 2007.
2. Philip E. Allen & Douglas R. Holberg, “CMOS Analog Circuit Design (2nd ed.)” Oxford University Press, 2002.
3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” Tata Mcgrow-Hill Edition, 2002.
4. Adel S. Sedra, Kenneth C. Smith, “Microelectronic Circuits (4th ed.)” Oxford University Press, 2007.
5. Richard C. Dorf & Robert H. Bishop, “Modern Control Systems (8th ed.)” Addison Wesley Longman Inc. 1998.
6. Brokaw, P., "A simple three-terminal IC bandgap reference", 'IEEE Journal of Solid-State Circuits', vol. 9, pp. 388 - 393, December 1974.
7. Widlar, R., "New Developments in IC Voltage Regulators", 'IEEE Journal of Solid-State Circuits', vol. 6, pp. 2 - 7, February 1971.
8. Banba, H., Shiga, H., Umezawa, A., Miyaba, T., Tanzawa, T., Atsumi, S., Sakui, K., "A CMOS bandgap reference circuit with sub-1-V operation", 'IEEE Journal of Solid-State Circuits', vol. 34, pp. 670 - 674, May 1999.
9. Cheng Jun, Chen Guican, “A CMOS Bandgap Reference Circuit”, ASIC, 2001.
10. Chunhua YAO, Boan LIU, and Yuwen XIA, “A 14-μA 3-ppm/°C CMOS Bandgap Voltage Reference”
11. Wendan Xu, Donglai Xu, Ian French, “A High Performance CMOS Bandgap Reference Circuit Design”, ‘IEEE Int. workshop VLSI Design & Video Tech. 2005’
12. Wang Zongmin, Zhu Xiaofei, Chen Lei, Zhang Dawei, Zhang Tieliang, “Low Voltage, High Performance Bandgap Reference in Standard CMOS Technology”, ‘IEEE Int. workshop VLSI Design & Video Tech. 2005’
13. Arne E. Buck, Charles L. McDonald, Stephen H. Lewis, T. R. Viswanathan, “A CMOS Bandgap Reference without Resistors”, ‘IEEE Journal of Solid State Circuits’, vol. 37, no.1, January 2002

14. Anne Johan Annema, “Low Power Bandgap Reference featuring DTMOST’s”, ‘IEEE Journal of Solid State Circuits’, vol.34, no.7, July 1999
15. Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui, “A CMOS Bandgap Reference Circuit with Sub-1V Operation”, ‘IEEE Journal of Solid State Circuits’, vol.34, no.5, May 1999
16. Savvas Koudounas, Julius Georgiou, “A Reduced Are, Low Power CMOS Bandgap Reference Circuit”
17. Han Wang, Qing Ye, “0.5V operational Transconductance amplifier for CMOS Bandgap Reference Circuit”
18. Andrea Pretelli, Anna Richelli, Luigi Colalongo, Zsolt M. Kovacs-Vajna, “Reduction of EMI Susceptibility in CMOS Bandgap Reference Circuits”, ‘IEEE Transactions on Electromagnetic Compatibility, vol. 48, no.4, November 2006
19. Hou-Ming Chen, Chih-Liang Huang and Robert C. Chang, “A New Temperature-Compensated CMOS Bandgap Reference Circuit for Portable Applications”
20. Ming-Dou Ker, Jung-Sheng Chen and Ching-Yun Chu, “A CMOS Bandgap Reference Circuit for SUB-1V Operation without using Extra Lowe Threshold Voltage Device”
21. Hongchin Lin, Wu-Chang and Yen-Tai Lin, “An Area-Efficient CMOS Bandgap Reference Circuit for Low Supply Voltages”

APPENDIX A: HSPICE NETLIST

Netlist for the Simulation of Variation of Reference Voltage with respect to Temperature

```
*startup circuit
m1 1 1 2 gnd nch l=1u w=1u
m2 2 2 3 gnd nch l=1u w=1u
m3 3 3 gnd gnd nch l=1u w=1u
m4 1 3 output gnd nch l=1u w=10u
*bandgap core
r1 output 5 rnw r=57.642k w=1u l=59u
r2 5 6 rnw r=4.999k w=1u l=5.117u
r3 output 7 rnw r=57.643k w=1u l=59u
q1 gnd gnd 6 qpnp1x m=4
q2 gnd gnd 7 qpnp1x m=1
*op amp
m5 output 11 1 1 pch l=1u w=10u
m6 9 7 8 1 pch l=1u w=10u
m7 10 5 8 1 pch l=1u w=10u
m8 9 9 gnd gnd nch l=1u w=10u
m9 10 9 gnd gnd nch l=1u w=10u
m10 11 10 gnd gnd nch l=0.5u w=10u m=500
m11 11 11 1 1 pch l=1u w=10u
m12 8 11 1 1 pch l=1u w=10u
c1 10 11 cpinw c=1n

vdd 1 gnd 5

.dc temp 0 100 1          *for variation of reference voltage with respect to temperature
.option list post nomod
.op
```

```
.LIB 'c:/model/process/PROCESS_A/m5v3/BIP.txt' subbip
.LIB 'c:/model/process/PROCESS_A/m5v3/05Passive.txt' R_TYP
.LIB 'c:/model/process/PROCESS_A/m5v3/05Passive.txt' C_TYP
.LIB 'c:/model/process/PROCESS_A/m5v3/05logic.txt' TT
.end
```

Input File for the Simulation of Variation of Reference Voltage with respect to Temperature

```
*startup circuit
m1 1 1 2 gnd nch l=1u w=1u
m2 2 2 3 gnd nch l=1u w=1u
m3 3 3 gnd gnd nch l=1u w=1u
m4 1 3 output gnd nch l=1u w=10u
*bandgap core
r1 output 5 rnw r=57.642k w=1u l=59u
r2 5 6 rnw r=4.999k w=1u l=5.117u
r3 output 7 rnw r=57.643k w=1u l=59u
q1 gnd gnd 6 qpnp1x m=4
q2 gnd gnd 7 qpnp1x m=1
*op amp
m5 output 11 1 1 pch l=1u w=10u
m6 9 7 8 1 pch l=1u w=10u
m7 10 5 8 1 pch l=1u w=10u
m8 9 9 gnd gnd nch l=1u w=10u
m9 10 9 gnd gnd nch l=1u w=10u
m10 11 10 gnd gnd nch l=0.5u w=10u m=500
m11 11 11 1 1 pch l=1u w=10u
m12 8 11 1 1 pch l=1u w=10u
c1 10 11 cpinw c=1n
```

```
vdd 1 gnd 5

.dc vdd 3 7 0.5              *for variation of reference voltage with respect to vdd
.temp 30
.option list post nomod
.op

.LIB 'c:/model/process/PROCESS_A/m5v3/BIP.txt' subbip
.LIB 'c:/model/process/PROCESS_A/m5v3/05Passive.txt' R_TYP
.LIB 'c:/model/process/PROCESS_A/m5v3/05Passive.txt' C_TYP
.LIB 'c:/model/process/PROCESS_A/m5v3/05logic.txt' TT

.end
```

Input File for the Simulation of Variation of Reference Voltage with respect to Temperature

```
*startup circuit
m1 1 1 2 gnd nch l=1u w=1u
m2 2 2 3 gnd nch l=1u w=1u
m3 3 3 gnd gnd nch l=1u w=1u
m4 1 3 output gnd nch l=1u w=10u
*bandgap core
r1 output 5 rnw r=57.642k w=1u l=59u
r2 5 6 rnw r=4.999k w=1u l=5.117u
r3 output 7 rnw r=57.643k w=1u l=59u
q1 gnd gnd 6 qpnp1x m=4
q2 gnd gnd 7 qpnp1x m=1
*op amp
m5 output 11 1 1 pch l=1u w=10u
m6 9 7 8 1 pch l=1u w=10u
```

```
m7 10 5 8 1 pch l=1u w=10u
m8 9 9 gnd gnd nch l=1u w=10u
m9 10 9 gnd gnd nch l=1u w=10u
m10 11 10 gnd gnd nch l=0.5u w=10u m=500
m11 11 11 1 1 pch l=1u w=10u
m12 8 11 1 1 pch l=1u w=10u
c1 10 11 cpinw c=1n

vdd 1 gnd 5                    *for variation of reference voltage with respect to time

.temp 30
.options  reltol=1e-6 gmindc=1e-12
.option list post nomod captab
.op
.tran 100n 200u
.print tran v(output)

.LIB 'c:\model\process\PROCESS_A\m5v3\BIP.txt' subbip
.LIB 'c:\model\process\PROCESS_A\m5v3\05Passive.txt' R_TYP
.LIB 'c:\model\process\PROCESS_A\m5v3\05Passive.txt' C_TYP
.LIB 'c:\model\process\PROCESS_A\m5v3\05logic.txt' TT

.end
```

Input File for the Simulation of Variation of Reference Voltage with respect to Temperature

```
*startup circuit
m1 1 1 2 gnd nch l=1u w=1u
m2 2 2 3 gnd nch l=1u w=1u
m3 3 3 gnd gnd nch l=1u w=1u
m4 1 3 output gnd nch l=1u w=10u
```

```
*bandgap core
r1 output 5 rnw r=57.642k w=1u l=59u
r2 5 6 rnw r=4.999k w=1u l=5.117u
r3 output 7 rnw r=57.643k w=1u l=59u
q1 gnd gnd 6 qpnp1x m=4
q2 gnd gnd 7 qpnp1x m=1
*op amp
m5 output 11 1 1 pch l=1u w=10u
m6 9 7 8 1 pch l=1u w=10u
m7 10 5 8 1 pch l=1u w=10u
m8 9 9 gnd gnd nch l=1u w=10u
m9 10 9 gnd gnd nch l=1u w=10u
m10 11 10 gnd gnd nch l=0.5u w=10u m=500
m11 11 11 1 1 pch l=1u w=10u
m12 8 11 1 1 pch l=1u w=10u
c1 10 11 cpinw c=1n

vdd 1 gnd sin(4 1 1MEG 0 1e5)     *for variation of reference voltage with respect to noise in
                                  supply

.temp 30
.options  reltol=1e-6 gmindc=1e-12
.option list post nomod captab
.op
.tran 100n 200u
.print tran v(output)

.LIB 'c:\model\process\PROCESS_A\m5v3\BIP.txt' subbip
.LIB 'c:\model\process\PROCESS_A\m5v3\05Passive.txt' R_TYP
.LIB 'c:\model\process\PROCESS_A\m5v3\05Passive.txt' C_TYP
.LIB 'c:\model\process\PROCESS_A\m5v3\05logic.txt' TT

.end
```