Design of a telescopic fully-differential OTA

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***Abstract*— This paper deals with the design of a low power fully differential telescopic operational transconductance amplifier to meet the required specifications. This circuit can be used for various low power applications. A comprehensive circuit designing and methodology approach analysis is performed and shown. The functionality of the proposed circuit is verified through simulations in Cadence ADE Virtuoso environment using 0.18μm CMOS process model parameters. The performance evaluation is performed and compared with analytical values to determine the correctness of circuit. The performance is also compared with target design specifications and all the specifications are met with a good margin.**

***Index Terms*— Biasing, Common mode feedback (CMFB), Operational Transconductance amplifier (OTA), Telescopic architecture.**

I. Introduction

The operational transconductance amplifier (OTA) is the block with the highest power consumption in analog integrated circuits in many applications. Low power consumption is becoming more important in handset devices, so it is a challenge to design a low power OTA. There is a tradeoff between speed, power, and gain for an OTA design because usually these parameters are contradicting parameters. There are three kinds of OTAs: two stage OTAs, folded cascode OTAs, and telescopic OTAs. The telescopic amplifier consumes the least power compared with the other two amplifiers, so it is widely used in low power consumption applications [1][2].

Besides low power applications, OTA is the core module of the sample and hold circuit. The intrinsic MOS transistor gain is limited as transistors dimension is scaling down and operating voltage is reducing. Designing high-gain and high-speed operational amplifier is becoming increasingly challenging. [3][4]. The main bottleneck is that there is a tradeoff between speed and gain, because high dc gain demands a multistage design with long-channel devices, a low bias current levels; whereas the high-speed demands single stage design, short-channel devices, a high bias current levels. But there have been several approaches to resolve this conflict, gain-boosting technique is one of these approaches to solve this problem in the condition that the auxiliary amplifier is designed reasonably, otherwise, the introduction of zero-pole deteriorate settling performances of operational amplifier, even though it does not noticeably affect the frequency response. In addition, the design of common-mode feedback circuit has always been a difficulty in designing operational amplifier,

In this paper, a two-stage telescopic cascade OTA is designed employed common mode feedback which is a good solution to the output common-mode level shifting problem as well as stability of the common mode output voltage. The target is to design an operational Transconductance amplifier which can meet the required design specifications.

This paper is organized as follows. Telescopic OTA circuit design is described in section II. Section III presents the design methodology approach and major tradeoff considerations. Section IV describes the analysis of important design parameters. Section V gives the simulation results to verify the functionality of the designed circuit. The performance of the circuit is described by Section VI. The work is concluded in section VII.

II. Circuit Design and its Description

This section provides the description of the designed OTA. Compared with single-ended output operational amplifier, fully differential amplifier employs two-stage topology, which has a lot of advantages, for example no influence of common mode noise, more high linearity and reducing even harmonic interference, so we employ the two-stages fully differential telescopic cascode structure [5][6]. The first stage uses the telescopic structure with cascade stages amplifier which ensures the main high gain as to achieve specifications required. However, there are five MOS transistors from the power to the ground, and then they limit the output swing, so the second stage employs common source topology to obtain high output swing [7]. And in order to ensure amplifier have a good frequency characteristics, Miller compensation capacitor and nulling resistor are set between first-stage and second stage, the common-mode feedback circuit for every stage are designed to stabilize the common mode output voltage. The following sub-sections provide description on each of these.

A. Telescopic two-stage OTA

Fig. 1. shows the fully differential double stage telescopic cascade architecture based OTA. The input stage deploys NMOS transistors and the first stage comprises of 5 and use markup styles. The node voltages and current in all the

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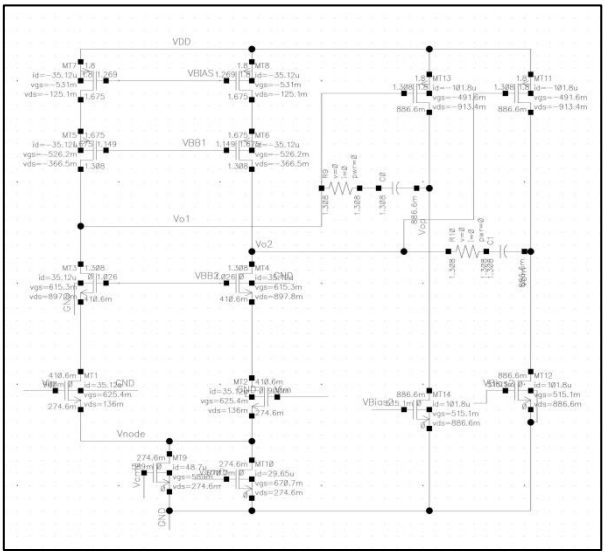

Fig. 1. Telescopic OTA architecture

branches are marked. The transistors *MT1* and *MT2* form the input stage of telescopic OTA. Transistors *MT2-MT6* are deployed as cascade stages to amplify the gain of first stage and increase the output impedance to shift dominant pole at lower frequency. Transistors *MT7* and *MT8* are the active PMOS loads. The tail current is passed from transistors *MT9* and *MT10*, which is common feedback controlled to stabilize the stage 2 output common mode voltage. The stage employs common source PMOS transistors *MT11*, *MT13* and NMOS transistors *MT12* and *MT14* serving as active loads. The PMOS input stage is chosen since; the first stage has 3 NMOS transistors to ground and 2 PMOS transistors. So, it is difficult to maintain voltages close to 0.6V-0.7V at the output of first stage. Hence, PMOS input stage 2 is chosen to ensure that input common mode range is high. The miller capacitance and nulling resistors are added to obtain optimum frequency response.

B. Common Mode Feedback Loop

The common mode feedback loop is designed to stabilize the common mode output voltage. The reference voltage of 0.9V is obtained by voltage divider circuit. The differential PMOS pair is deployed which adjusts the current based on the voltage difference between the two branches [8]-[10]. Accordingly, the current is fed to the the tail transistor *MT10*. Fig. 2 shows the common mode feedback loop system. The common mode loop gain is set by transistors *MT16* and *MT18*. The total current is drawn through transistor *MT15* and is divided based on differential voltages. Transistors *MT17* and *MT19* forms the current mirror.

C. Biasing Circuit

The biasing circuit is shown in Fig. 3. The transistors *MT20* is connected with ideal grounded current source and is used as

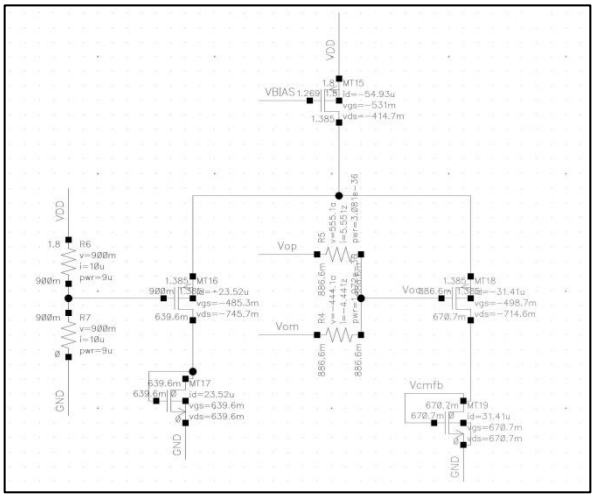

Fig. 2. CMFB loop

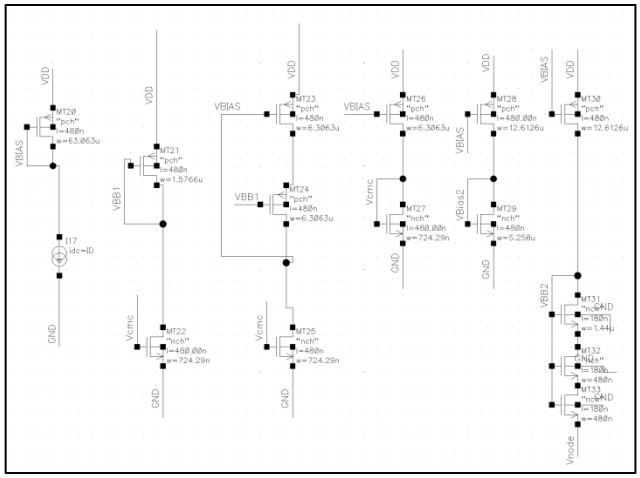

Fig. 3. Biasing Circuit

current mirror for biasing transistors *MT21*, *MT23*, *MT26*, *MT28* and *MT30*. The transistors MT21-MT25 are deployed to bias node voltage *VBB1* which ensures minimum voltage difference between transistors *MT5-MT7* and *MT6-MT8* to drive them in saturation region. The transistor *MT27* forms the current mirror with the tail transistor to bias. The transistors MT28 and MT29 are deployed to bias second stage active load transistors *MT12* and *MT14*. To maintain minimum voltage difference of V_T+2V_{ov}, the transistors *MT30-MT33* is deployed which ensures reliable saturation region operation.

III. DESIGN METHODOLOGY

This section describes the design methodology and approach adopted to design fully differential telescopic OTA. The authors have followed a systematic approach to design the circuit. The automated MATLAB utilities are developed for evaluating parameters using g_m/i_d methodology. Also, various QA checks are incorporated to ensure that no contradicting assumptions. The utility also determines major design tradeoffs related to design specification to ensure optimum

circuit design and serve as good reference point. This section is divided into 3 sub-sections, each discussing about the design approach, automated utilities and checkers, and major tradeoffs being taken into consideration.

A. Design Approach

The approach involves evaluation of major circuit parameters using g_m/i_d methodology. The authors have coded the main equations in MATLAB environment to eliminate any calculation errors. Also, this reduces design effort to lot of extent by providing a good starting point. The flow chart of design approach is shown by Fig.4. The circuit parameters are calculated as a function of stage 1 input current. The approach involves 3 main stages – evaluation, checker and tradeoffs. At the end of execution, a summary is obtained which proved to be very helpful. Once, the device parameters are decided, the circuit simulation is performed and sizing is tweaked to further improve the performance. The common efficient circuit design approaches are adopted as well.

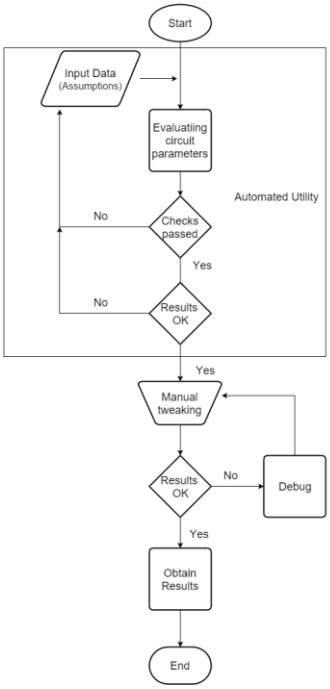

Fig. 4. Design approach flowchart

B. Automated Utilities & QA Checkers

The automated utility is developed in MATLAB environment to ease the design process by eliminating any calculation errors and saving design effort and time. The main features include accurate calculation of widths and lengths based on biasing conditions, checks to ensure that required specifications are met and the assumptions considered for biasing are met. In the approach, to ensure proper biasing and high power efficiency, the transistors are assumed to bias at low over-drive voltages and accordingly expressions are obtained using long channel and g_m/i_d approach. The results are sweeped across range of capacitance values to determine the sweet spot. But, the authors have taken this automation as a good reference point and the circuit fine optimization is done based on simulation results.

C. Major Design tradeoffs consideration

The circuit is designed keeping in consideration the design tradeoffs. Table I lists down the major design decisions being taken into consideration.

TABLE I
DESIGN DECISIONS AND TRADEOFFS

Decision	Reason
Telescopic architecture	Power and output swing tradeoff
PMOS second stage	To improve input common mode range
CMFB loop	Common mode stable and power tradeoff
2 stage design	To achieve high output swing
Fully differential	Output swing and power tradeoff
Stage 2 current	Slewing rate
Miller cap + nulling res	To increase the phase margin
Choice of C_c	Noise, speed and power tradeoff
Choice of C_L	Slew, speed and noise tradeoff
Choice of C_1 and C_2	Speed and noise tradeoff
CMFB loop current	Stability and CMFB loop gain
Choice of R_Z	Phase margin and power tradeoff
Summing with resistors	Gain and power tradeoff
Biasing circuit	Power and performance tradeoff

IV. DESIGN ANALYSIS

In this section, the analysis of major design parameters is performed to analyze the circuit performance.

A. Gain Analysis

The open loop gain of a telescopic cascade two stage OTA is product of gain of both the stages and is given by (1).

$$OverallGain = Gain_{stage1} * Gain_{stage2} \tag{1}$$

The stage 1 and stage 2 gains are given by (2) and (3) respectively. The values of $g_m r_n$, $g_m r_p$, and other required parameters are calculated using g_m/i_d methodology.

$$Gain_{stage1} = g_{m1} * \left(\left(r_{n1} * \left(g_{m3} r_{n3} \right) \right) \| \left(r_{p7} * \left(g_{m5} r_{p5} \right) \right) \right) = 450.9 \tag{2}$$

$$Gain_{stage2} = g_{m11} * \left(r_{p11} \| r_{n12} \right) = 50.7 \tag{3}$$

$$OverallGain = 450.9 * 50.7 = 87.18dB \tag{4}$$

The transistors of the second stage are biased in such a way to maximize the output swing. The g_m/i_d of transistors in telescopic stage and second stage are kept high, in range of 15-20 to save power by biasing them in weak overdrive region.

B. Frequency Analysis

The frequency analysis is performed to determine the closed loop bandwidth, phase margin and stability of system. The values of C_1 and C_2 as per specifications handout are kept as 0.5pf. The feedback factor is given by (5).

$$\beta = \frac{C_2}{C_1 + C_2 + C_{gg1}} = \frac{0.5p}{0.5p + 0.5p + 18.47f} = 0.491 \tag{5}$$

where $C_{gg1} = W_1 L_1 C_{OX} = 18.47\,fF$ (6)

The closed loop bandwidth is evaluated by (7). The dominant pole is less than 1KHz and non-dominant pole sits at frequency around 125MHz, evaluated in (8). The overall phase margin of system is given by (9).

$$f_c = \frac{\beta g_{m1}}{2\pi C_C} = \frac{0.491 * 641u}{2\pi * 1.3pf} = 30.53MHz \tag{7}$$

(8)

$$f_{p2} = \frac{g_{m2}}{2\pi * \left(C_{gg2} + (C_L + (1-\beta)C_2) + \frac{C_{gg2}(C_L + (1-\beta)C_2)}{C_C} \right)} = 125.7MHz$$

$$PM = \tan^{-1}\left(\frac{f_{p2}}{f_c}\right) = \tan^{-1}\left(\frac{125.7}{30.53}\right) = 76.43^o \tag{9}$$

C. Transient Analysis

The transient analysis is performed to determine the settling time, static error and dynamic error of the system. The loop gain of the OTA is expressed by (10).

$$Loopgain(T_o) = \beta(openloopDCgain) = 0.491 * 22860.63 = 81dB \tag{10}$$

The static error is inverse of the loop gain and is expressed by (11). The settling time is also calculated for 0.08% dynamic settling error time and is expressed by (12).

$$StaticError = \frac{1}{Loopgain(T_o)} = 0.00491\% \tag{11}$$

$$t_s = \frac{-1}{w_c} \ln\left(\xi_{dtotal} \left(1 - \beta \frac{C_2}{C_2 + C_c} \right) \right) = 37.98ns \tag{12}$$

D. Noise Analysis

The noise analysis is performed to determine the noise due to first and second stage. The value of γ is kept as 0.67. The other remaining parameters are determined using g_m/i_d methodology. The noise at single ended output is given by (13). The integrated noise for fully differential OTA will be twice of single ended configuration. The output rms noise voltage is expressed by (14).

$$v_{ntot}^2 = \frac{\gamma}{\beta}\left(\frac{kT}{C_C}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \right) + \left(\frac{kT}{C_{Ltot}}\left(1 + \gamma\left(1 + \frac{g_{m5}}{g_{m7}}\right)\right) \right) = 1.5473e-8 \tag{13}$$

$$v_{rms} = \sqrt{2 * v_{ntot}^2} = 175.78uV \tag{14}$$

V. Simulation Results

This section presents the simulation results of the designed telescopic OTA employing CMFB. The simulations are performed using 0.18µm CMOS process parameters in Cadence Virtuoso ADE environment. The supply voltage V_{DD} is 1.8V. As per the design specifications, the value of C_1 and C_2 are kept equal, both at 0.5pf. The load capacitor value is set at 1.2pf, which is higher than 1pf as per the specification. The miller capacitance C_c is set at 1.3pf and nulling resistor R_z is kept at 0.47kΩ, which is greater than $1/g_{m2}$. The transistors aspect ratios are listed in Table II.

TABLE II
ASPECT RATIO OF MOSFETS IN OTA

MOSFET	*W(µm)/L(µm)*
MT1, MT2	*7.2µm/0.18 µm*
MT3, MT4	*10.2µm/0.18 µm*
MT5, MT6, MT7, MT8, MT20	*63.063µm/0.48µm*
MT9	*9.6µm/0.48µm*
MT10, MT17, MT19	*2.4µm/0.48µm*
MT11, MT13	*360.8µm/0.18µm*
MT12, MT14	*57.84µm/0.48µm*
MT15	*90µm/0.48µm*
MT16, MT18	*100µm/0.18µm*
MT21	*1.576µm/0.48µm*
MT22, MT25, MT27	*0.724µm/0.48µm*
MT23, MT24, MT26	*6.306µm/0.48µm*
MT28, MT30	*12.613µm/0.48µm*
MT29	*5.258µm/0.48µm*
MT31	*1.44µm/0.18µmm*
MT32, MT33	*0.48µm/0.18µm*

The following sub-sections illustrate the simulation results obtained in DC, AC, stability, transient, and noise analysis.

A. DC Analysis

The dc gain and offset analysis is performed and differential voltage V_d is swept for the complete output swing range. A 1000 point fine parametric sweep is performed to obtain input-referred offset V_{offset}, differential-mode gain A_{DM}) and output swing. The procedure is repeated for range of input common mode voltages V_{CM}. Fig. 5. shows the output range and 3dB gain plot with the offset voltage. The offset voltage is 1.856pV and the A_{DM} come out to be 86.61dB. The output swing from the analysis comes out to be [-1.357, 1.357]. The input common mode range is plotted in Fig. 6. The power dissipation of design is also evaluated by connecting no signal to input and observing the current from V_{DD} power rail.

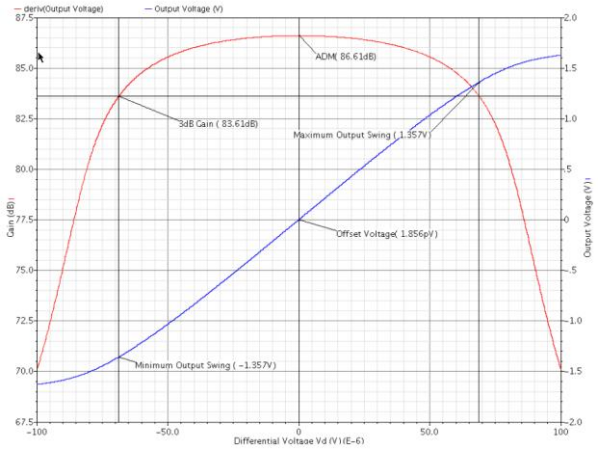

Fig. 5. Open loop DC gain and output swing

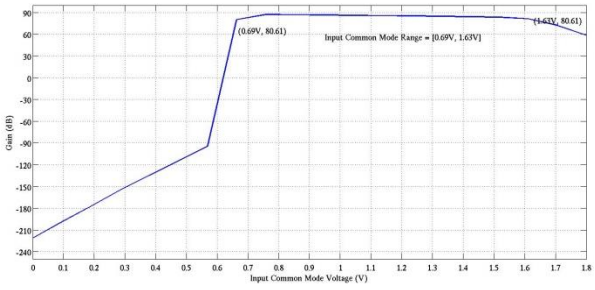

Fig. 6. Input Common-mode range

B. *AC Analysis*

The AC analysis is performed to observe the CMRR and PSRR response of the OTA. The CMRR value is obtained by A_{DM} - A_{CM}. A_{DM} is evaluated from DC analysis and A_{CM} is calculated from AC analysis by calculating the ac magnitude at 1Hz. Similarly, PSRR is obtained by evaluating A_{DM} - A_{VDD} where A_{VDD} is obtained by calculating AC gain at 1Hz. The values of CMRR and PSRR come out to be 110.45dB and 92.17dB respectively. Fig. 7. and Fig. 8. show the CMRR and PSRR plots as function of frequency.

C. *Stability and Frequency Analysis*

The stability analysis is performed for the OTA in closed loop. Due to input configuration, signal is passed from a high pass filter and extra pole and zero is introduced which can be ignored. Fig. 9. shows the phase and loop gain plot. The loop gain of the OTA is 80.32dB and phase margin is 76.80^{o}. The non-dominant pole is at 126.80MHz. The closed loop bandwidth or closed loop unity gain frequency is 29.71MHz.

D. *Transient Analysis*

The transient analysis is performed to meet the settling time, dynamic and static error specification. Fig. 10. shows the transient response of the output going up. The zoomed version of the plot is shown in Fig. 11. Similarly, the plots are shown for output going down and shown in Fig. 12. and Fig. 13. Since the loop gain is quite high, the static error comes out to be very low, 0.005% whereas dynamic error comes out to be 0.08% at settling time of 39.01ns.

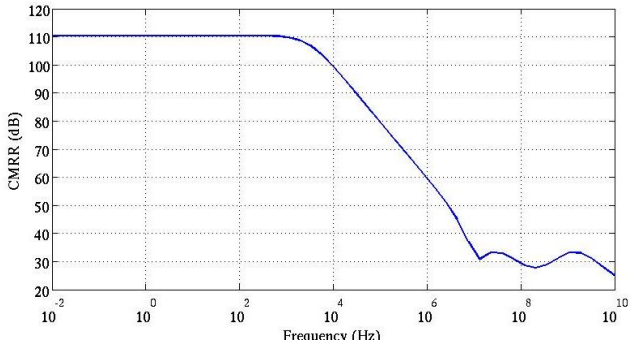

Fig. 7. Common mode rejection ratio

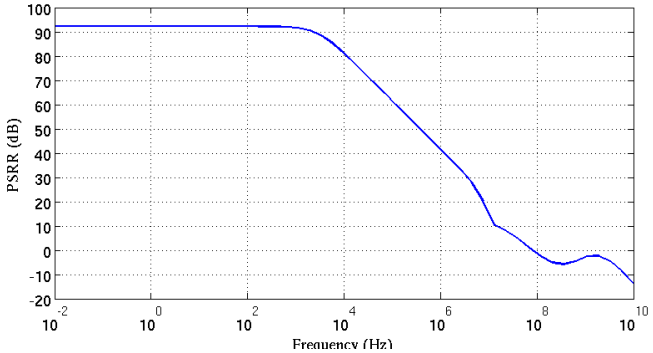

Fig. 8. Power Supply rejection ratio

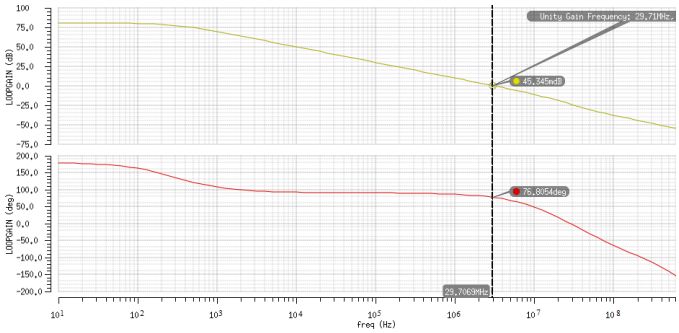

Fig. 9. Magnitude and Phase response

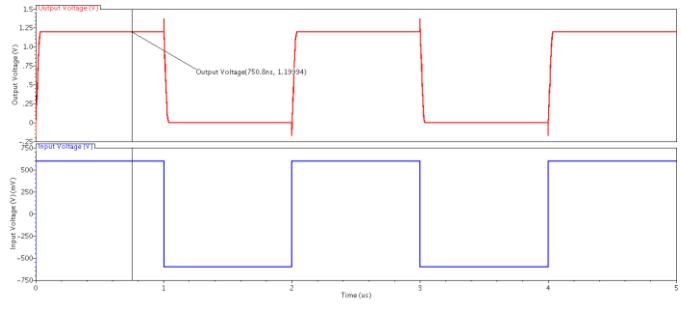

Fig. 10. Settling Time going up

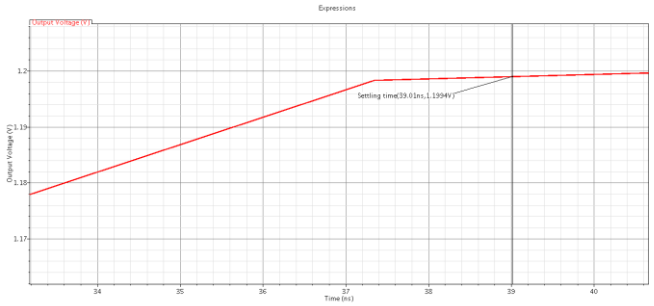

Fig. 11. Zoomed plot of settling time going up

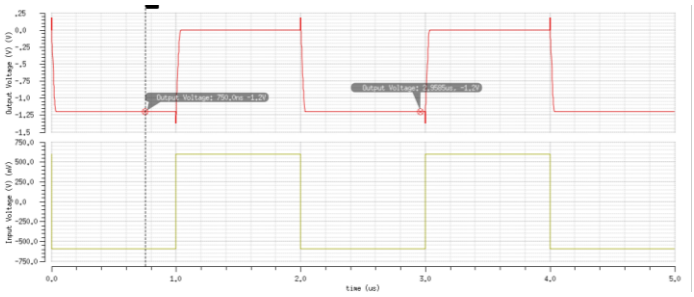

Fig. 12. Settling Time Going down

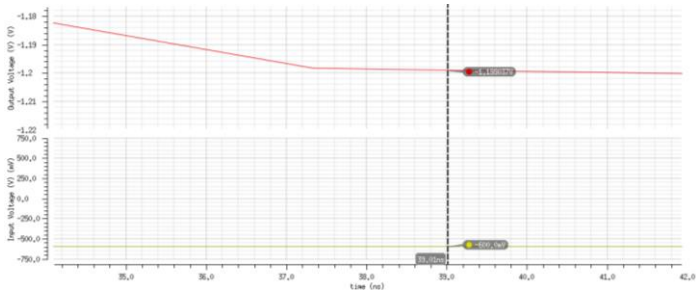

Fig. 13. Zoomed plot of settling time going down

E. Noise Analysis

The noise analysis is performed to calculate the integrated noise for the fully differential OTA. The integrated noise comes out to be 3.108e-8 V^2 for frequency range of 1KHz-10GHz. The output rms value of noise calculated from the integrated noise comes out to be 176.12µV.

VI. Performance Evaluation

The performance of the designed circuit is presented in this section. The simulated values obtained in section IV is compared with the simulated values obtained in section V. The values are compared with the simulated values and % error is calculated to prove that simulated results match closely with the calculated values. Table III lists the comparison of major design parameters. The results obtained from the simulation are also compared with target specifications, and are summarized in Table IV. All the specifications are met with a good margin while optimizing the power to the optimum level.

TABLE III
Analytical vs Simulated Characteristics of OTA

Characteristics	Calculated Value	Simulated Value	Error (%)
OTA open-loop DC gain	87.18dB	86.61dB	0.65%
Closed loop bandwidth	30.53MHz	29.71MHz	2.68%
Loop Gain	81.18dB	80.32dB	0.98%
Phase Margin	76.43°	76.80°	0.48%
Static settling error	0.00492%	0.005%	0.20%
Settling Time	37.98ns	39.01ns	2.72%
Total output noise (rms)	175.78µ	176.12µ	0.19%

TABLE IV
Performance Characteristics of OTA

Characteristics		Target Specification	Result
Capacitive load ($C_1 = C_2$, $C_L \geq$ 1pF)			$C_1 = C_2$ = 0.50pf, C_L = 1.20pf, C_c = 1.3pf
OTA open-loop DC small-signal gain			86.61dB
Static settling error		≤ 0.1%	0.005%
Dynamic settling error		≤ 0.1%	0.08%
Input referred offset		< 10 µV	1.86pV
Minimum output swing		[0.3V, 1.5V]	[-1.36V, 1.36V]
Input common-mode range			[0.69V, 1.63V]
Closed-loop unity gain frequency			29.71MHz
Phase margin		> 45°	76.80°
Settling Time	Up	< 40ns	39.01ns
	Down	< 40ns	39.01ns
CMRR at DC		> 60dB	110.45dB
PSRR at DC		> 60dB	92.17dB
Total output noise (rms value)		≤ 200µV	176.12µV
Total power consumption		Minimize	733.10µW

The capacitor values are kept in range to meet the optimum performance. The open loop DC small signal gain of OTA comes out to be 86.61dB. Due to high loop gain, the static settling error value comes out to much lesser than the target value of 0.1%. Since the configuration is fully differential, the input offset comes out to be 1.86pV and meets the specification by large margin. The output range also becomes double and comes out to be ±1.357V. The input common mode range for this architecture comes out to be [0.69V, 1.63V]. The closed loop unity gain frequency comes out to be 29.71MHz with a low settling time of 39.01ns, lower than the target specification. The circuit design is quite stable and phase margin comes out to be 76.25°. The output noise rms value for both differential outputs comes out to be 176.12µV, which is 12% lesser than the target value. The circuit is having high common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) with values of 110.45dB and 92.17dB respectively, making it suitable to use at front end of any circuit to suppress common mode and power supply noise. Besides meeting all the target specifications with a good margin, the circuit power consumption is minimized and comes out to be 733.10µW. All these specifications, i.e. low power, low noise, high gain and input common mode range, high CMRR, PSRR, phase margin makes this circuit a good fit for various applications like sensor nodes, pipelined ADCs, signal conditioning etc.

VII. Conclusion

A low power fully differential telescopic operational Transconductance amplifier employing CMFB loop is designed to meet the required specifications. The comprehensive circuit design analysis is performed and design methodology is presented. The simulation results are included to verify the correctness of the design and to quantify the error with the calculated values. The performance evaluation is performed to prove that the target specifications are met by a good margin. Thus, this circuit can be used in various applications such as sensor nodes, pipelined ADCs, signal conditioning etc.

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