Bandgap Design

Introduction

- One of the essential building blocks of many analog circuits is a voltage reference, which should exhibit little dependence on supply and process parameters and a well-defined dependence on temperature.

- Temperature dependence: -

1- Positive temperature coefficient (+ve TC): Proportional to absolute temperature (PTAT).

2- Negative temperature coefficient (-ve TC): Complementary to absolute temperature (CTAT).

3- Temperature independent (Zero-TC): ZTAT = PTAT + CTAT.

- If we achieve a temperature independent reference it will also be process independent.

- Applications: Voltage regulators, ADCs and DACs, Biasing of amplifiers, Common-mode (CM) level of fully-differential circuits, ...etc.

Band-gap Reference

- A reference voltage is generated by adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants.

- For example, for two voltages v1 and v2 that vary in opposite directions with temperature, choose a1 and a2 such that: -

$$a1(dv1/dT) + a2(dv2/dT) = 0$$

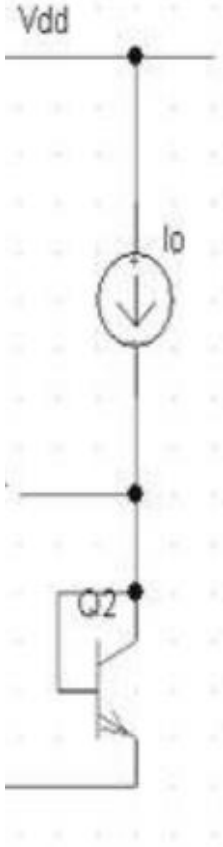
obtaining a reference voltage, VREF = a1.v1 + a2.v2 with zero TC.

- We must now identify two voltages that have positive and negative TCs. Among various device parameters in semiconductor technologies, the characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative TCs.

CTAT Voltage

- The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a pn-junction diode exhibits a negative TC.

$$I_C = I_S e^{\frac{|V_{BE}|}{V_T}} \rightarrow |V_{BE}| = V_T \ln \frac{I_C}{I_S}$$



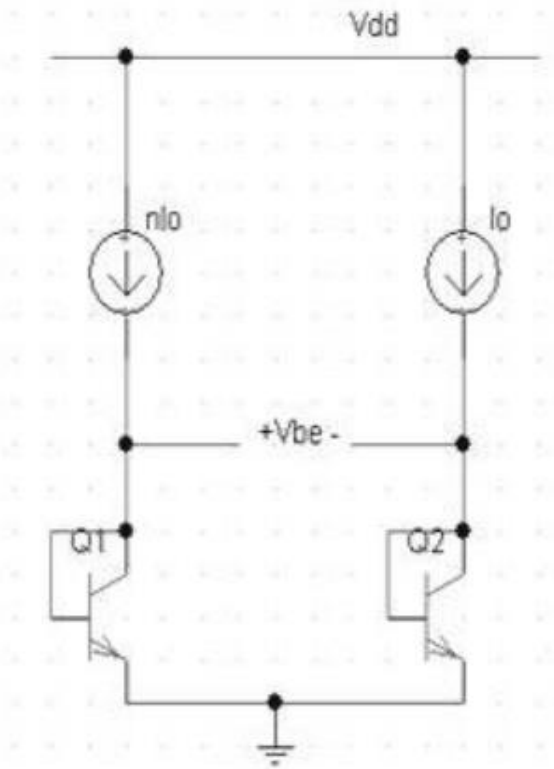
❑ It can be shown that Vbe = const. − b1 T → CTAT

- Is is a strong function of temperature.
- b1 from simulations: Usually b1 ≈ 1.5 − 2 mV/K.

PTAT Voltage

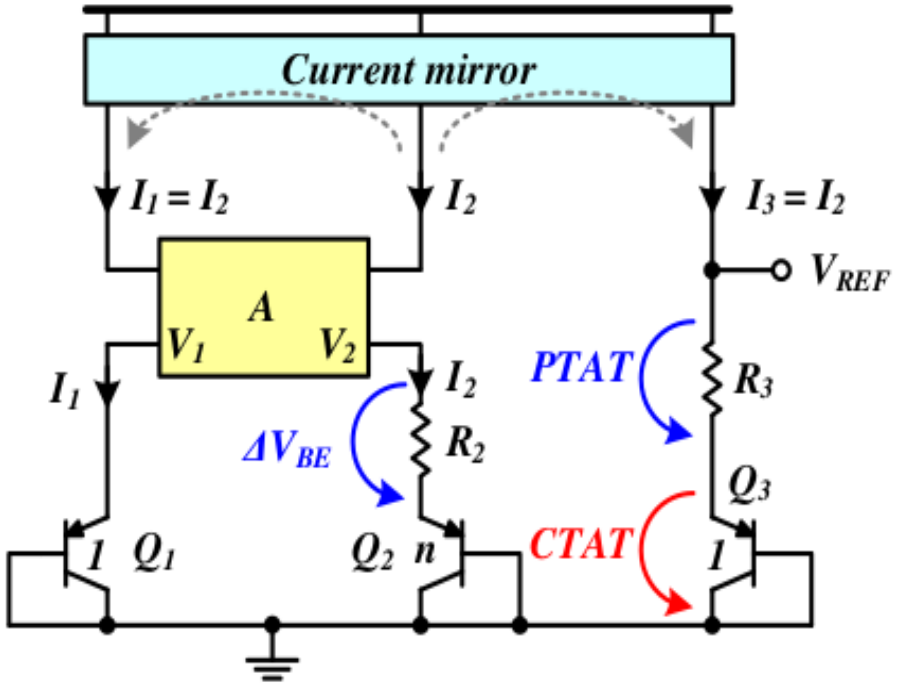
- If two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature.

- $|V_{BE1}| \approx V_T \ln \frac{I_1}{I_S}$ and $|V_{BE2}| \approx V_T \ln \frac{I_2/n}{I_S} = V_T \ln \frac{I_2}{I_S} - V_T \ln n$
- $\Delta V_{BE} = |V_{BE1}| - |V_{BE2}| = V_T \ln n = \frac{kT}{q} \ln n \quad \propto T \rightarrow$ PTAT!



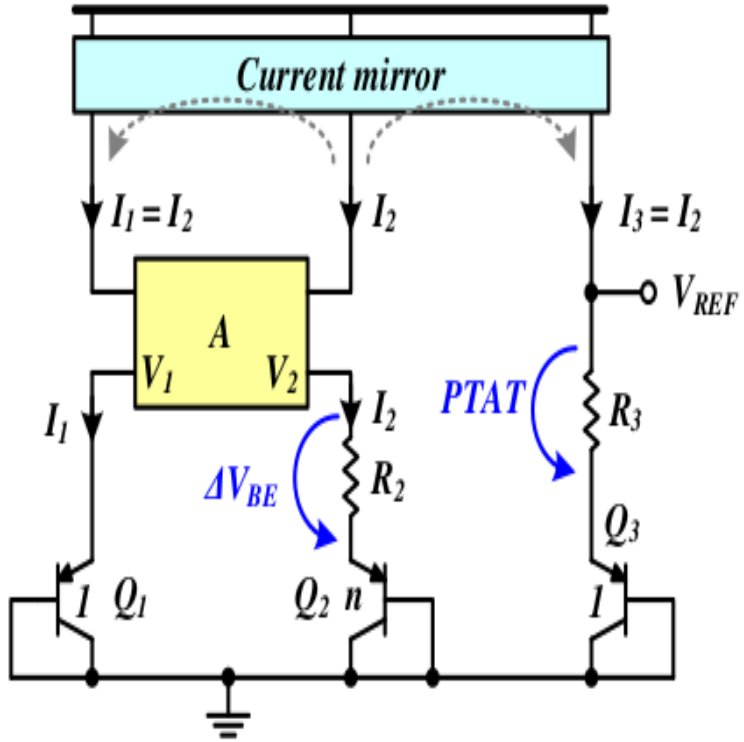
Basic Band-gap Reference

- Adding a PTAT and CTAT in one circuit will produce a ZTAT voltage reference as shown in figure:
- The A-block is a circuit that makes V1 = V2 .
- The current mirror copies I2 to I1 and I3 .



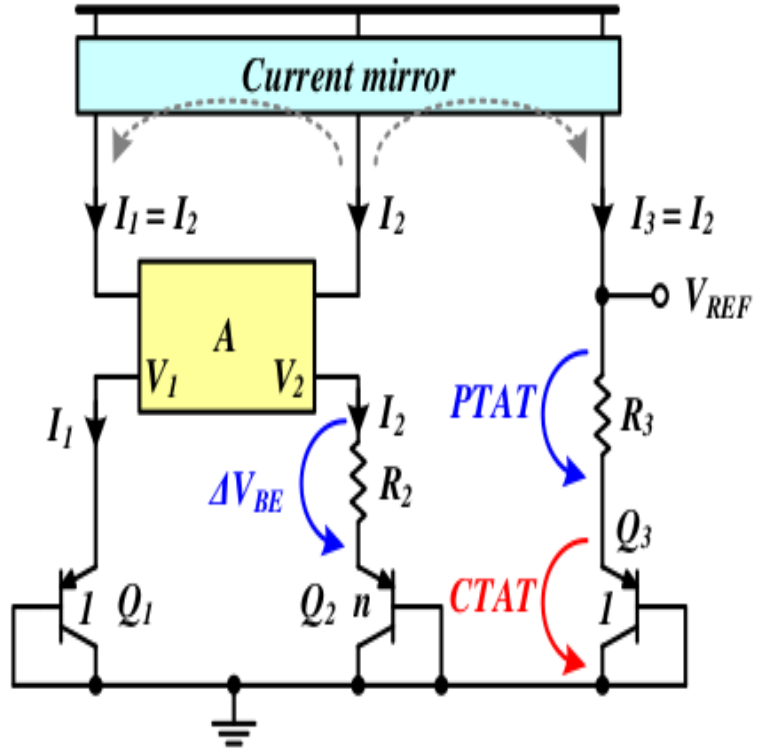
The PTAT Component

- $\Delta V_{BE} = |V_{BE1}| - |V_{BE2}| = V_T \ln n = \frac{kT}{q} \ln n \quad \propto T \rightarrow$ PTAT
- $I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{kT}{q} \ln n \cdot \frac{1}{R_2} \quad \propto T \rightarrow$ PTAT
- $V_{R_3} = I_3 R_3 = \Delta V_{BE} \cdot \frac{R_3}{R_2} = V_T \ln n \cdot \frac{R_3}{R_2} = a_1 T \quad \propto T \rightarrow$ PTAT
- $a_1 = \frac{k}{q} \ln n \cdot \frac{R_3}{R_2} \approx 0.086 \ln n \cdot \frac{R_3}{R_2}\ mV/K$



The CTAT Component

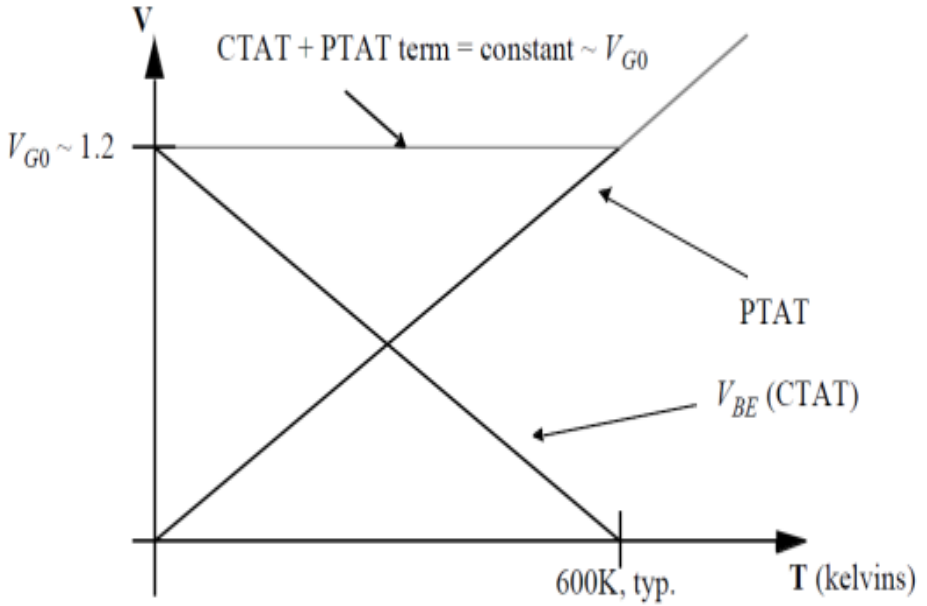
- It can be shown that $|V_{BE}| = V_T \ln\frac{I_C}{I_S} \approx V_{G0} - b_1 T$ → CTAT
  - I_S is a strong function of temperature.
  - $|V_{BE}|$ is CTAT even if I_C itself is PTAT!
- All "simple" analytical models are inaccurate (and complicated).
  - Get b_1 from simulations: Usually $b_1 \approx 1.5 - 2\ mV/K$.



The ZTAT Reference Voltage

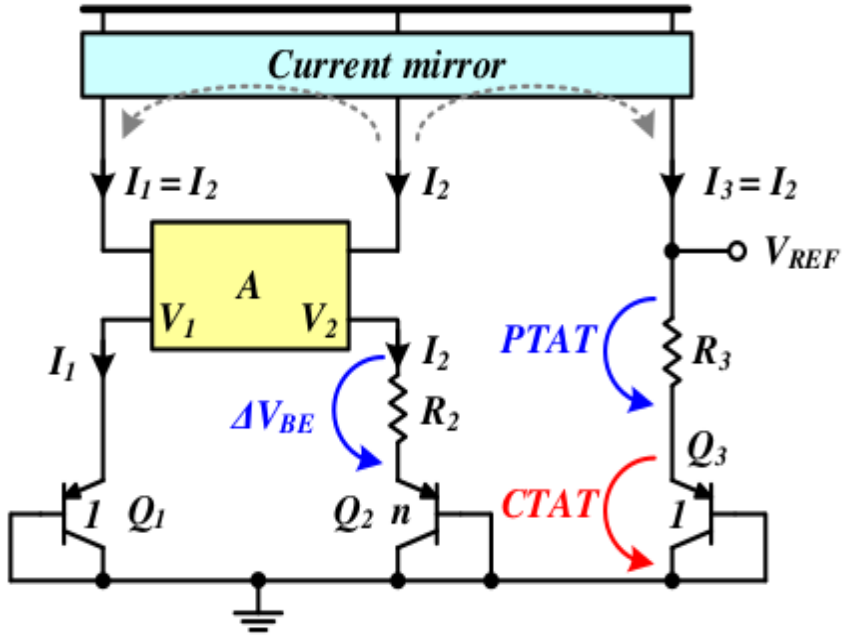
- $V_{R_3} = I_3 R_3 = \Delta V_{BE} \cdot \frac{R_3}{R_2} = V_T \ln n \cdot \frac{R_3}{R_2} = a_1 T$ → PTAT
- $|V_{BE}| = V_T \ln \frac{I_C}{I_S} \approx V_{G0} - b_1 T$ → CTAT
- $V_{REF} = \Delta V_{BE} \cdot \frac{R_3}{R_2} + |V_{BE3}| = a_1 T + V_{G0} - b_1 T \approx V_{G0}$
- $V_{REF} = PTAT + CTAT = ZTAT \approx V_{G0}$

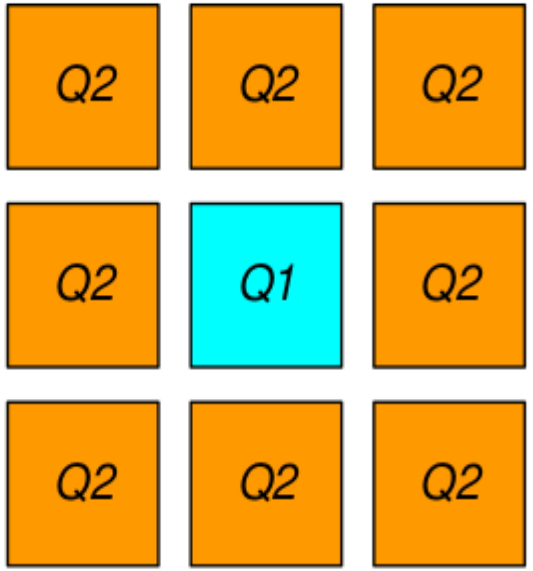
$V_{G0} = E_{g0}/q$ $\approx 1.2\ V$ is the bandgap voltage (energy) of Si extrapolated at absolute zero Kelvin



The number of BJT's used

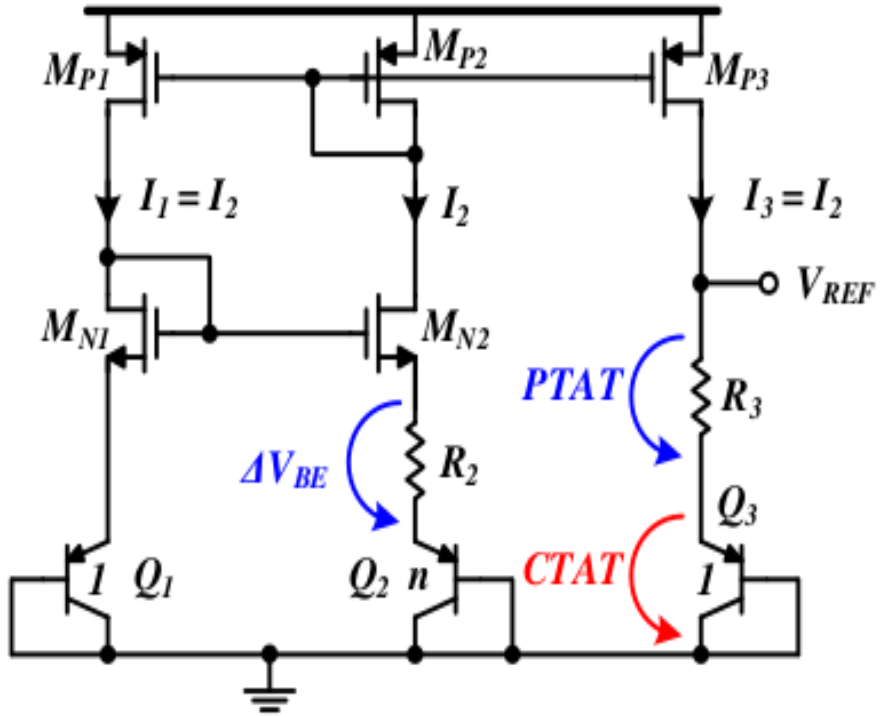
- Due to layout considerations, two values of n are usually used.
  - $n = 8$
  - $n = 24$





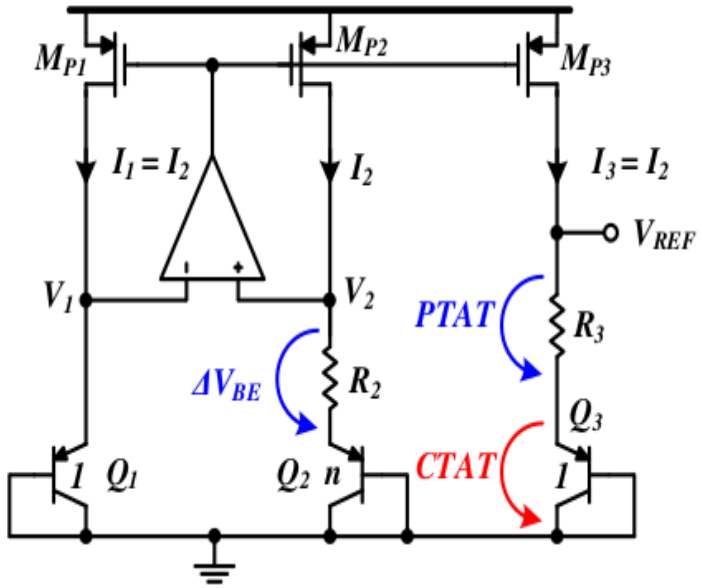
Band-gap Reference Topologies
1- Current mirror based

- Current mirror: M_{P1-3}
- A-block: $M_{N1,2}$ → Same current → Same V_{GS}
- Choice of L and W
  - Large L ($> 1\mu m$) is usually used: Reduce CLM and flicker noise.



Band-gap Reference Topologies
2- Op-amp based

- The op-amp keeps V_1 and V_2 at the same voltage.
- The op-amp can be implemented as a simple 5T OTA.
  - Folded cascode may be used if wide input range is required.
- Bias the op-amp using a constant-gm circuit.
  - Or use the BGR itself to bias it (self-biased)!

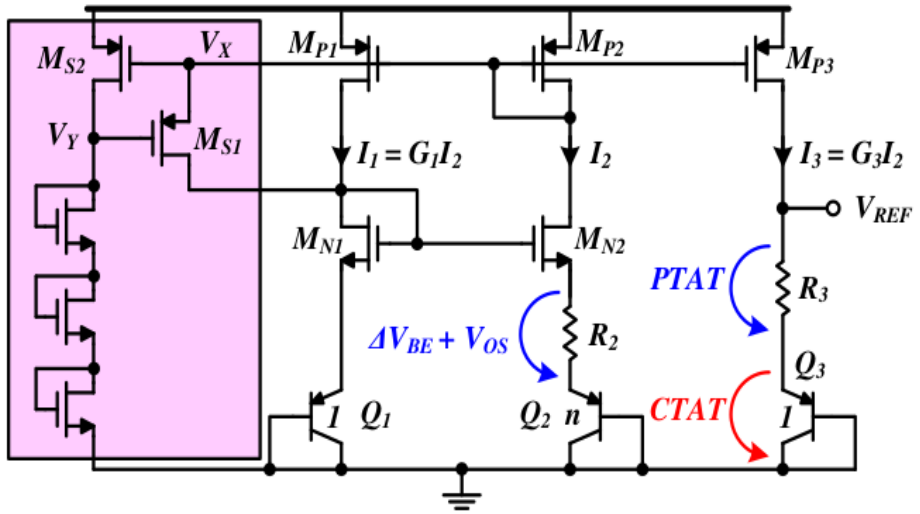


The start-up Problem

- In the circuit of bandgap, if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both branches. So it is needed to inject current in the bandgap core for proper operation of the circuit. Start-up circuit does this job. This circuit also turns off when steady state is reached.

Operation of start-up circuit

- Startup problem means $V_X = V_{DD}$ and $V_Y = 0$.
  - M_{S1} will turn on charging the gates of $M_{N1,2}$.
  - $Q_{1,2}$ will turn on and the BGR starts.
  - V_Y will increase turning off M_{S1} and driving M_{S2} in linear region.



Band-gap Curvature

- PTAT and CTAT are **not perfectly linear.**
  - They both have convex upward curvature → Curvatures add!
- If expressed mathematically:

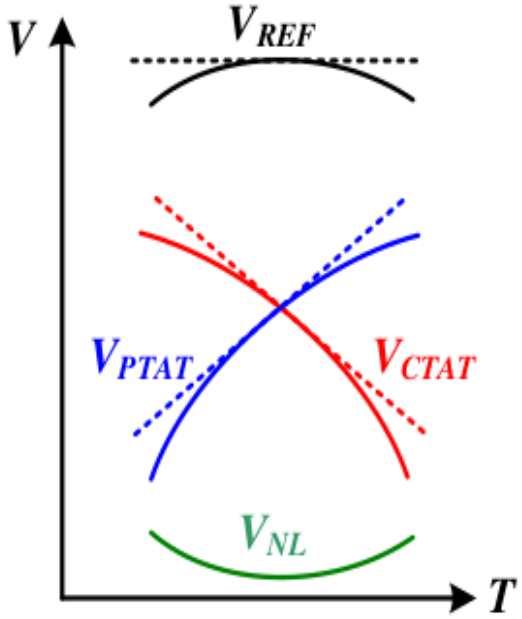
$$V_{PTAT} \approx a_1 T - a_2 T^2$$

$$V_{CTAT} \approx V_{G0} - b_1 T - b_2 T^2$$

$$V_{REF} \approx V_{G0} + (a_1 - b_1)T - (a_2 + b_2)T^2$$

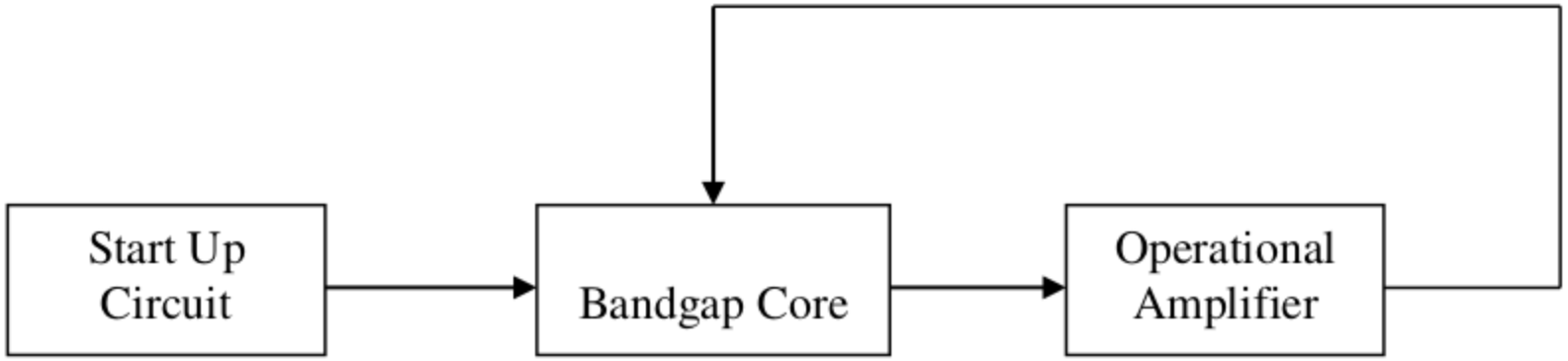
- We can set $a_1 = b_1$
- But a_2 and b_2 add (convex upward)

$$V_{REF} \approx V_{G0} - (a_2 + b_2)T^2$$

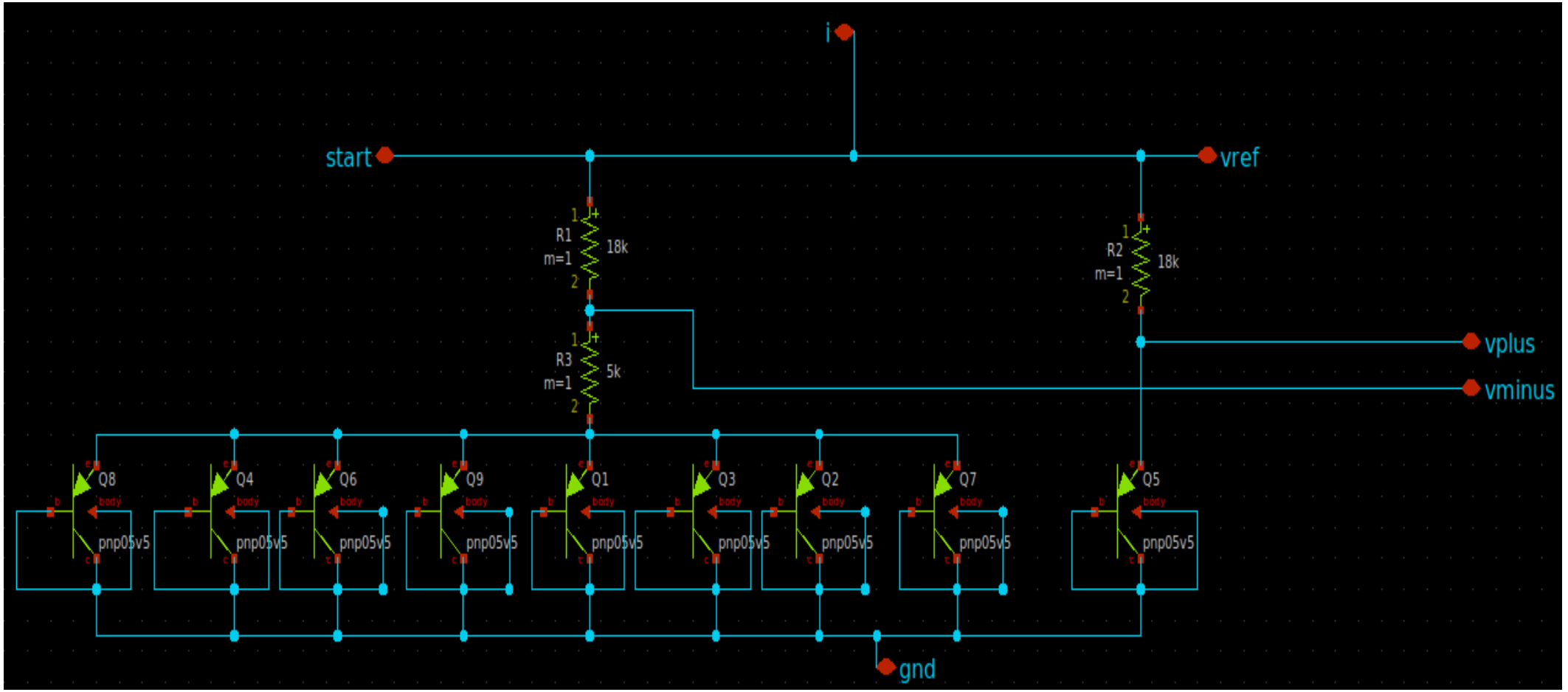


Proposed Band-gap Design

The block diagram of the circuit is given below:



Proposed Band-gap Design
1.1- Band-gap core schematic



Proposed Band-gap Design
1.2- Band-gap core analysis

- $VR2 = I2 \times R2$

  $= ((VBE2 - VBE1) / R3) \times R2$

  $= VT \ln(n) \times (R2 / R3)$

  $= VT \ln(8) \times (R2/R3)$

  Where: [n = 8 for our circuit] and $VT=KT/q$.

- VR2 is a positive TC which is 1.94 mV/°C for the BJT's used in this circuit.

- Vout =Vref= VR2 + VBE2, thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).

Proposed Band-gap Design
1.2- Band-gap core analysis

Vref = a1 VR2 + a2 VBE = const. => dVref/dT = a1 dVR2/dT + a2 dVBE/dT = 0

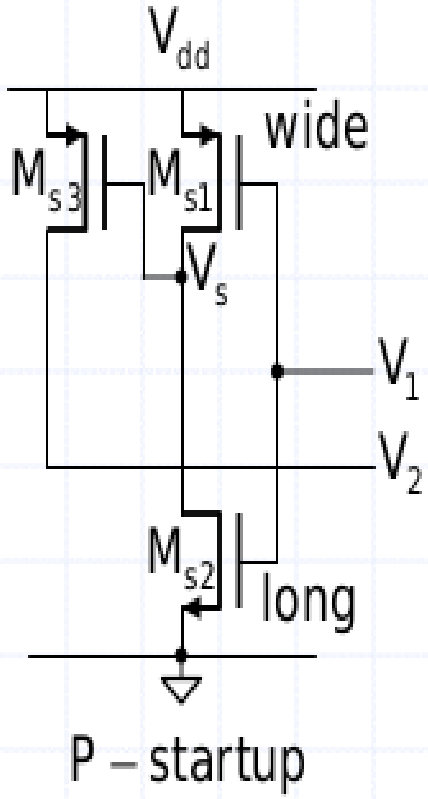
So a1(85uv/k) - a2(1.6mv/k) = 0

Since CTAT slope is greater than PTAT slope we will make a2=1 and vary a1 to make PTAT slope increasing to reach CTAT slope:

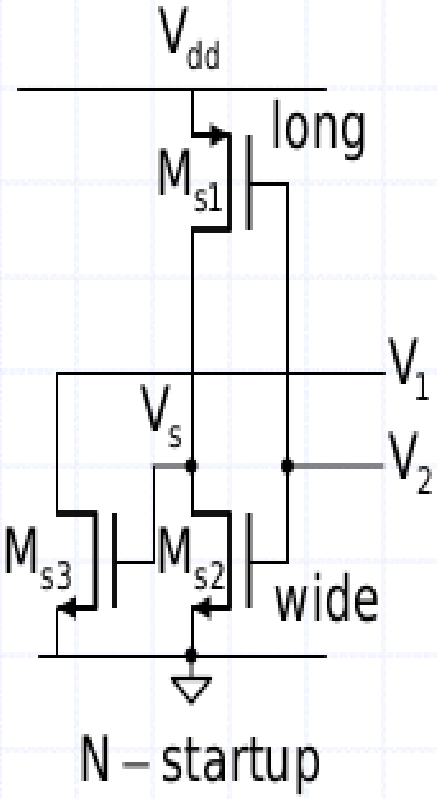
So a1=1.6m/85u => a1=19 = (R2/R1)*ln(8)

Let I=30uA then R1=VTln(8)/I = 2k ohm and R2= a1R1/ln(8) = 18k

Proposed Band-gap Design
2.1 - Start-up Circuit schemes

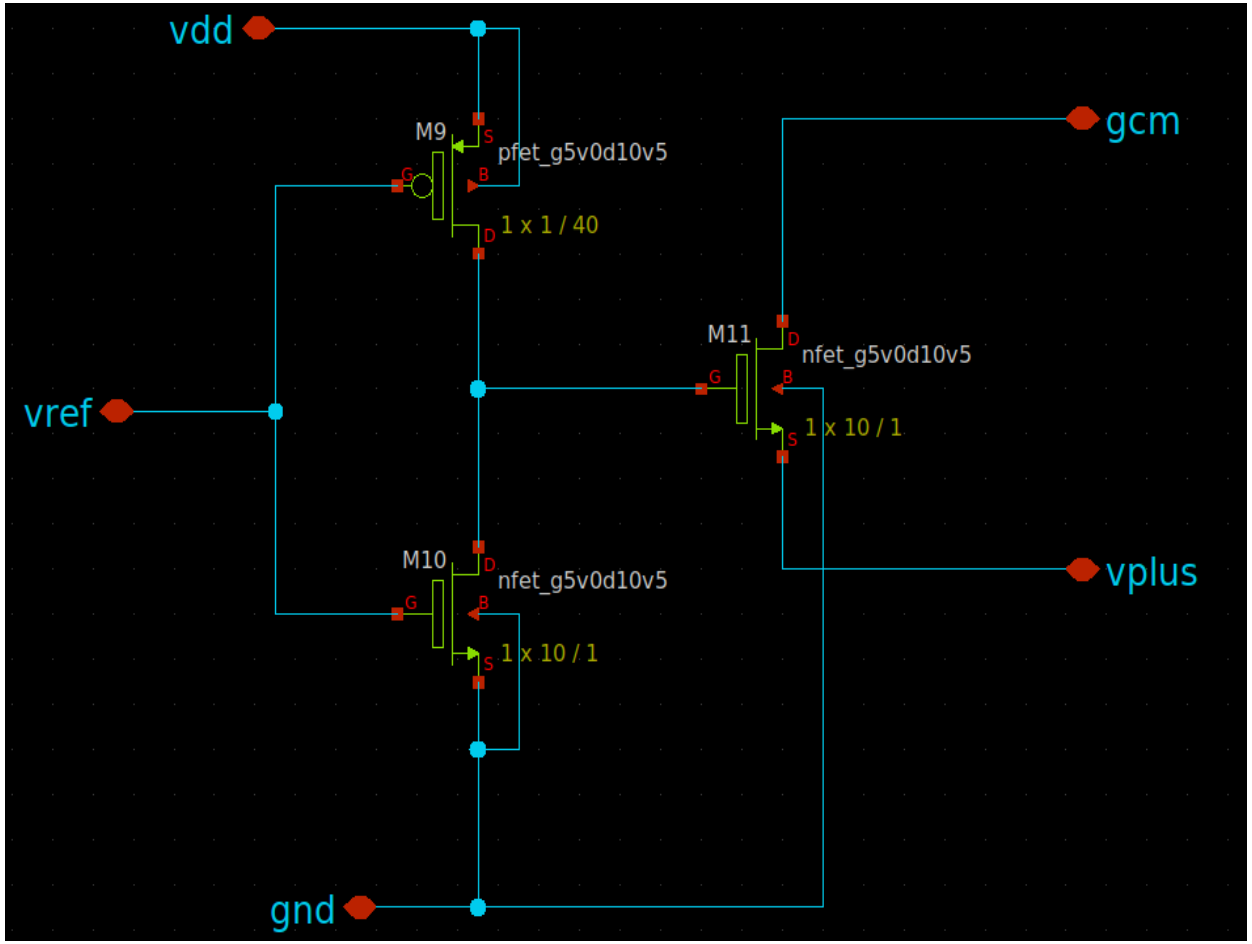


P – startup



N – startup

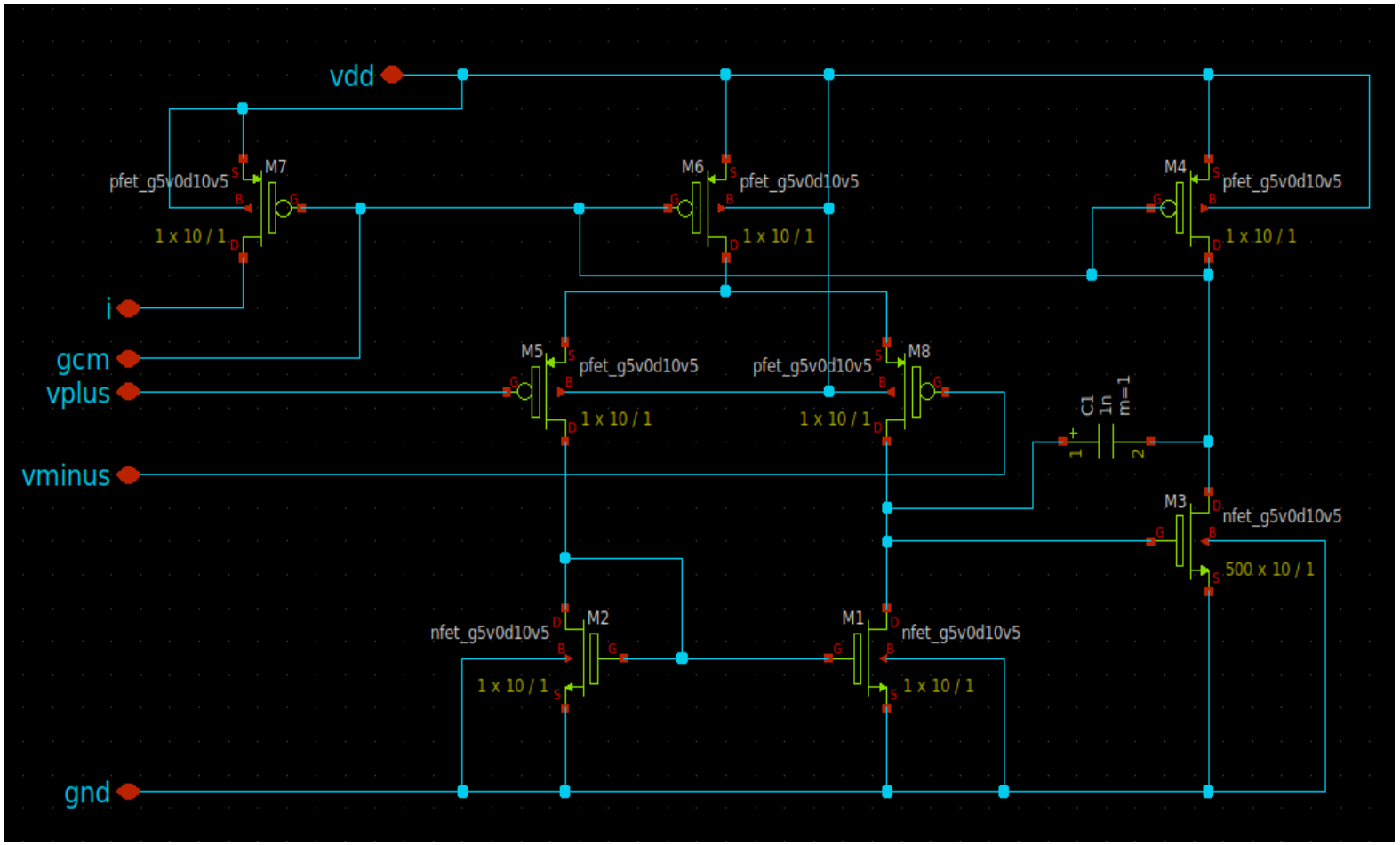
Proposed Band-gap Design
2.2- Start-up Circuit schematic



Proposed Band-gap Design
2.3- Start-up Circuit operation

- At first Vref = 0 but M9 will be ON so there is current will flow in M9 and also in M10 so M11 will turn ON and it will pull down the voltage at current mirror gate down from Vdd and v+ of the op-amp will increase (so Vref no longer be zero) and when it reaches a value close to vdd then M11,M10,M9 will be OFF and at this moment the role of start-up circuit will be ended.

Proposed Band-gap Design
3.1- OTA schematic



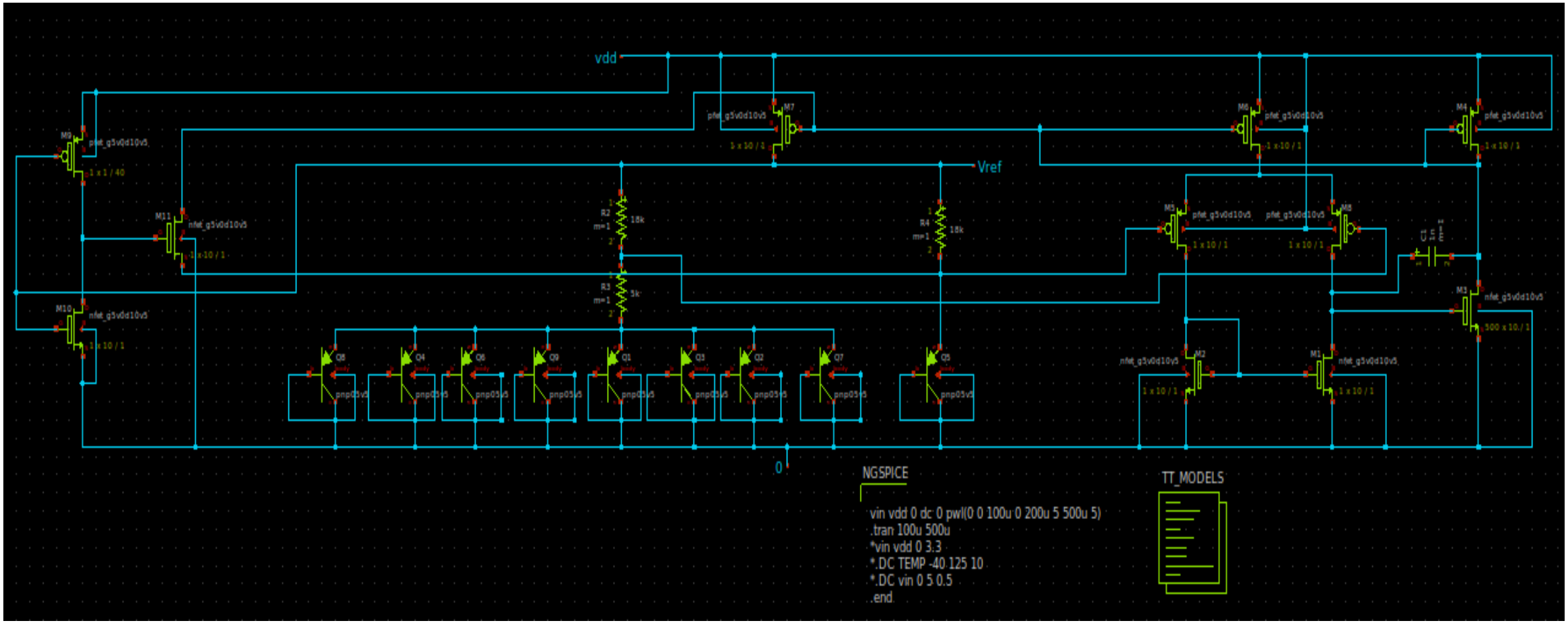
Proposed Band-gap Design
3.2- OTA Properties

- Ideally our operational amplifier should have infinite gain for proper function of bandgap core. So for proper function of bandgap core we need to increase the gain of the circuit. That's why a two stage operational amplifier has been used.

- But in a two stage amplifier, there is more than one pole which tries to make the circuit unstable. To make sure that the circuit is stable, stability analysis of the op amp has to be done.

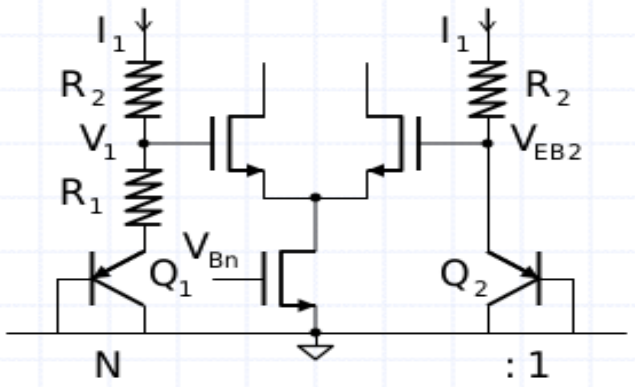
- Another important aspect of OPAMP design is to produce a current which is insensitive to variation of VDD (supply voltage), this is accomplished by driving the operational amplifier with its own output current(self-biased), this makes the output current of operational amplifier almost constant with respect to voltage.

Proposed Band-gap Design Complete circuit



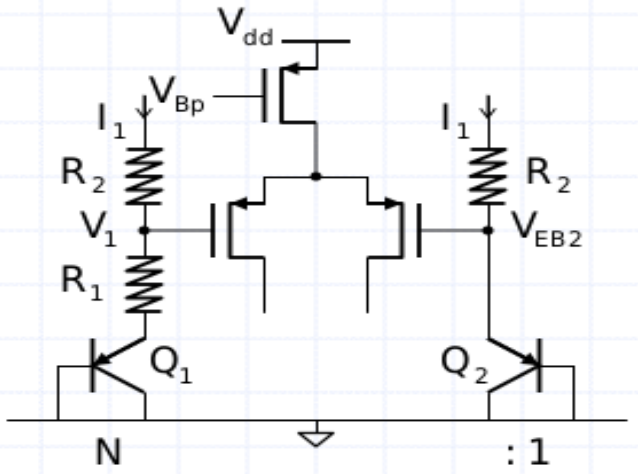
Choosing input stage of OTA

Let the gate overdrive voltage be $V_{gsn}-V_{tn} = |V_{gsp}|-|V_{tp}| = V_{ov}$.



For NMOS input, we need
$V_{EB2} > V_{tn} + 2V_{ov}$

V_{EB2} ranges from 0.5V to 0.7V
$\Rightarrow V_{tn} < 0.2V$
$\Rightarrow$ too tough to be satisfied

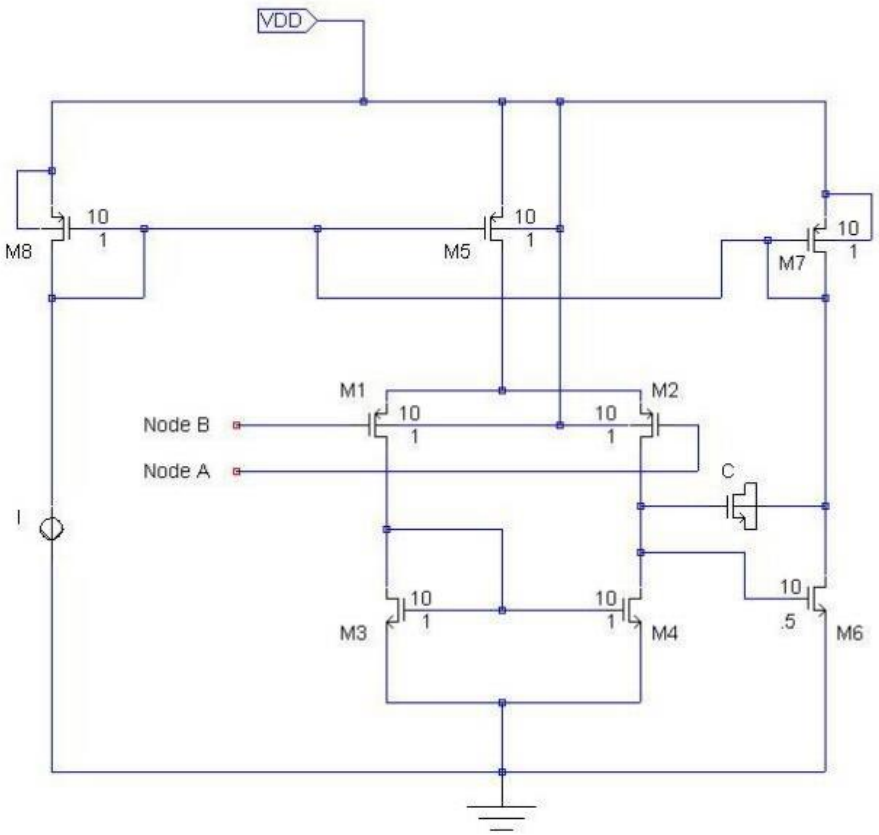


For PMOS input, we need
$V_{dd} > V_{EB2} + |V_{tp}| + 2V_{ov}$

For V_{EB}=0.64V, $|V_{tp}|$=0.44V, V_{ov}=0.15V
$\Rightarrow V_{dd}(min) = 1.38V.$

Analysis of the Op-amp

MOSFET	Width (µm)	Length(µm)	Multiplier
M1	1	1	1
M2	1	1	1
M3	1	1	1
M4	10	1	1
M5	10	1	1
M6	10	1	500
M7	10	1	1
M8	10	1	1



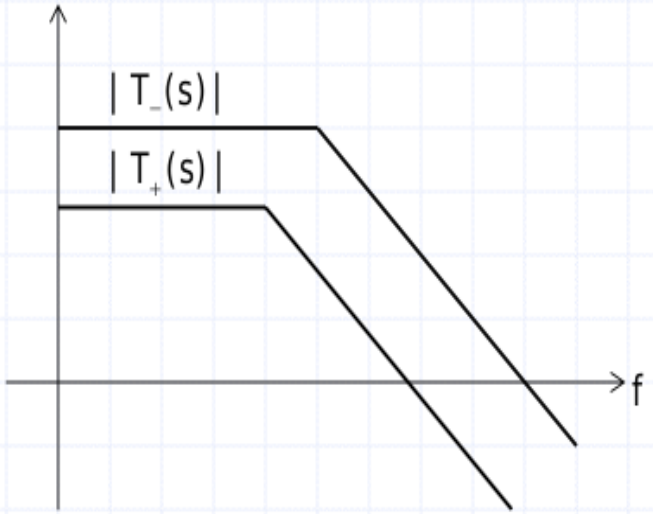
Stability of Bandgap

Negative feedback loop:

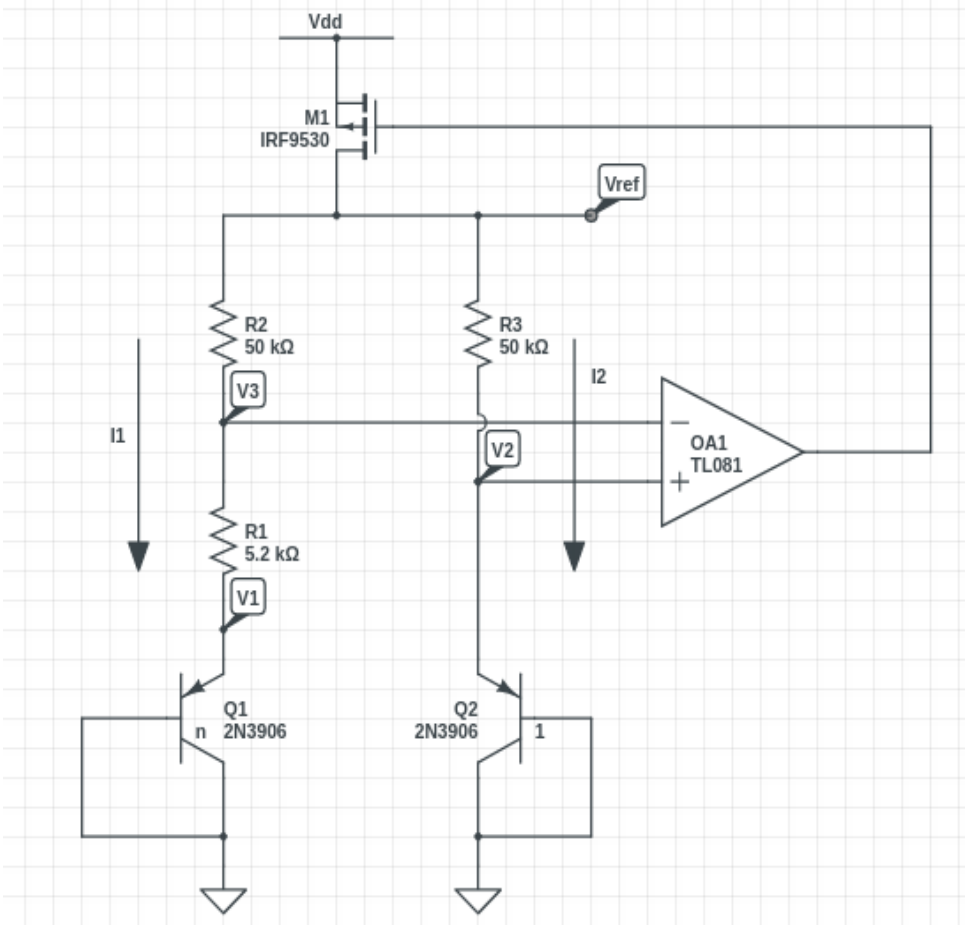
$$T_{-} = \frac{1 + g_{m1}R_1}{1 + g_{m1}(R_1 + R_2)} \times A(s)$$

Positive feedback loop:

$$T_{+} = \frac{-1}{1 + g_{m1}R_2} \times A(s)$$

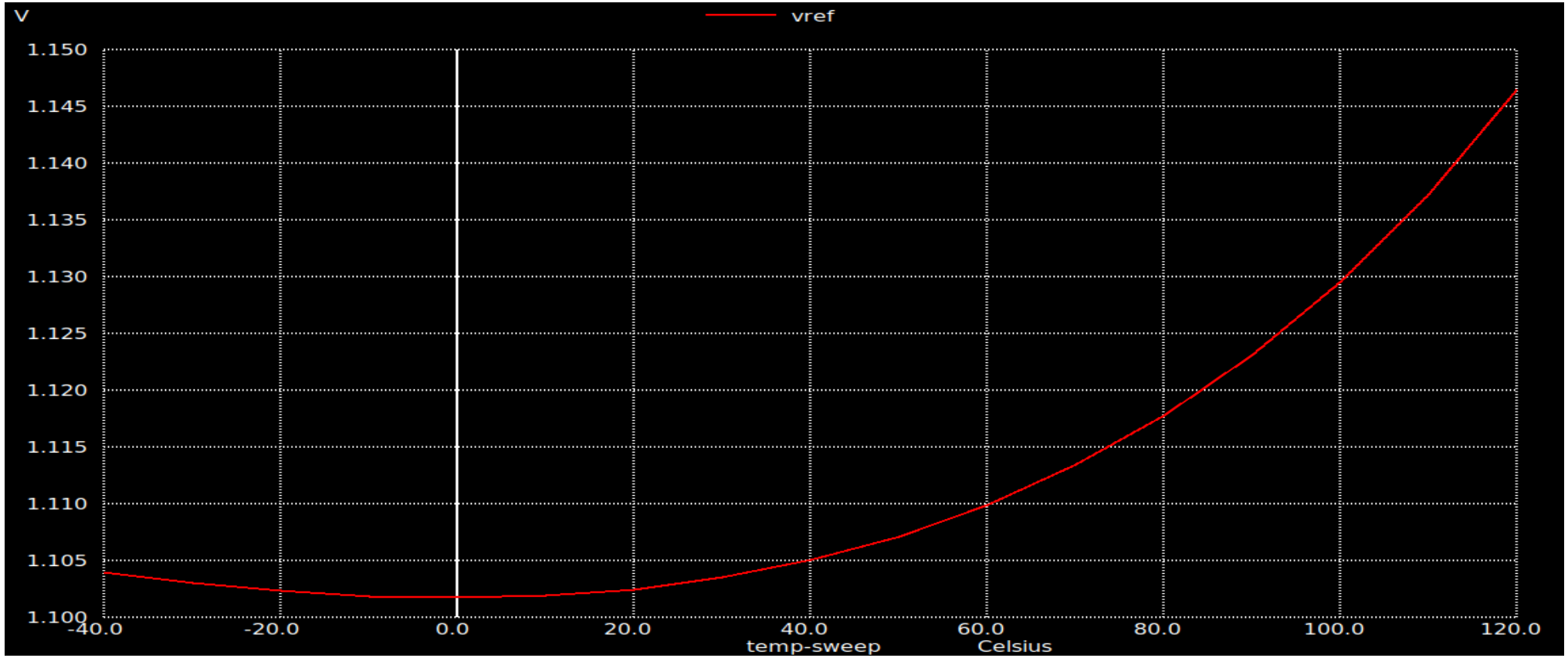


For stability, we need $|T_{-}| > |T_{+}|$, and this criterion is satisfied by the above two relations.



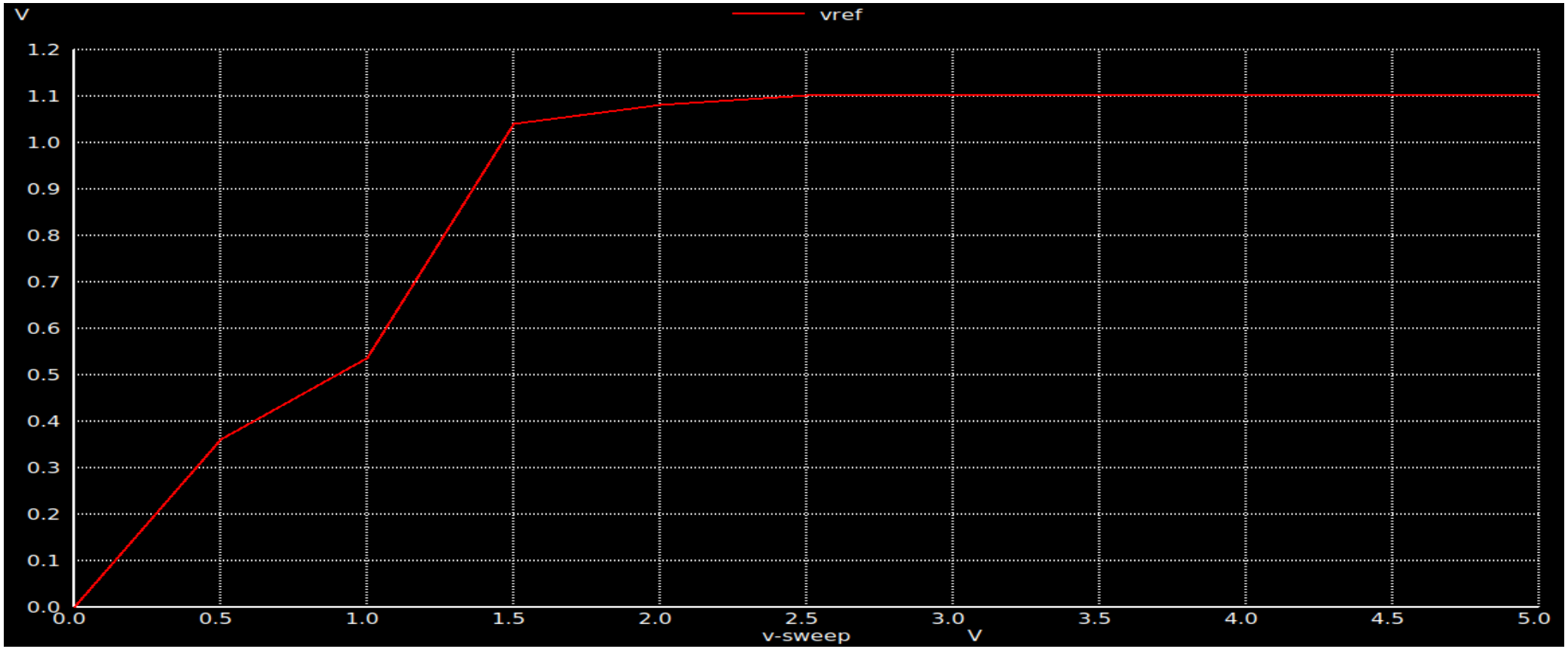
Simulation of Bandgap 3.3v
1- DC sweep vs Temperature

- Vdd = 3.3v and the temperature was swept from –40 to 120 c



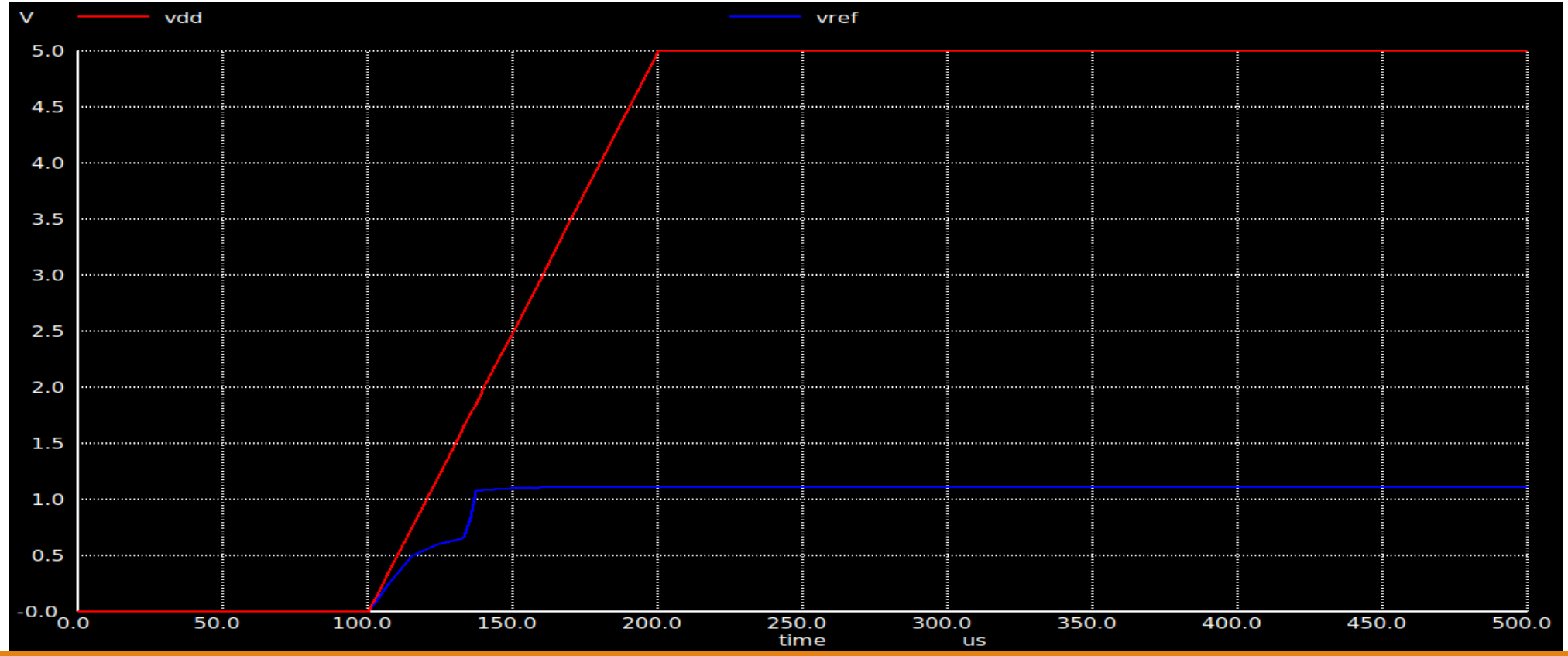
Simulation of Bandgap 3.3v
2- DC sweep vs Supply voltage

- VDD was swept from 0 to 5v



Simulation of Bandgap 3.3v
3- Transient Analysis

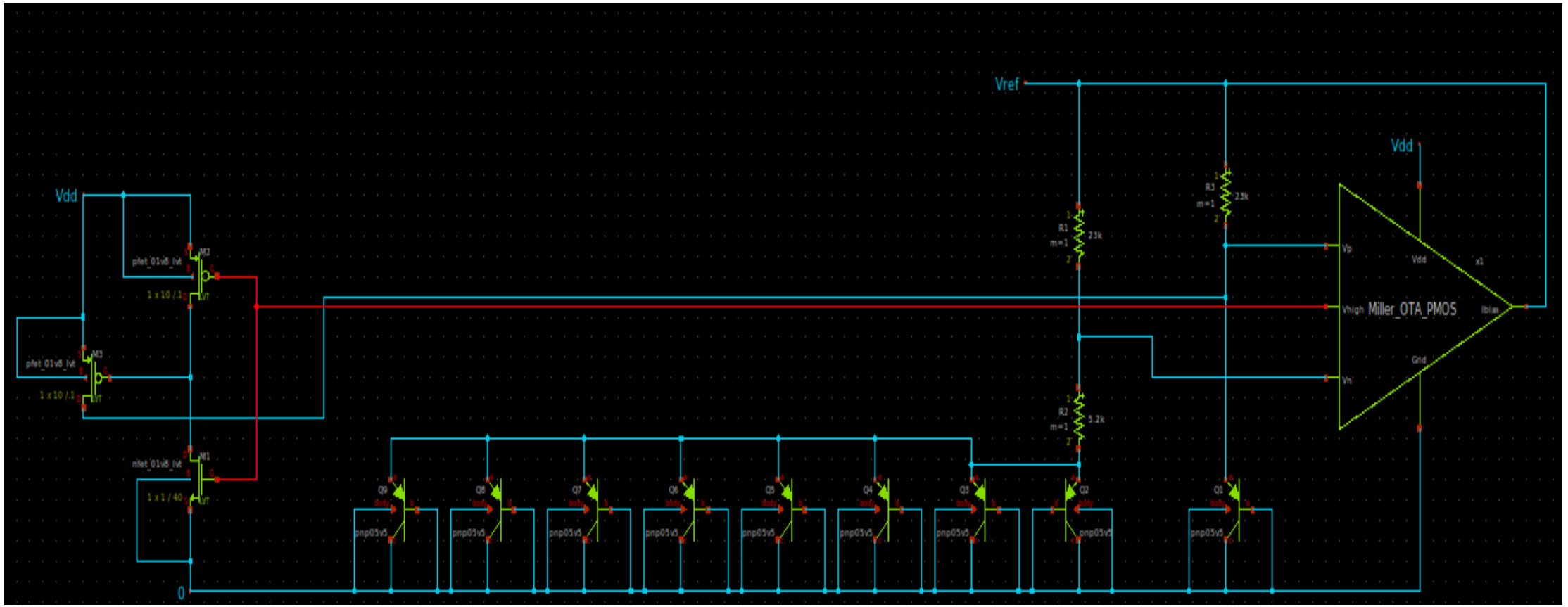
- A step voltage from 0 to 5v volt used with 100 us rise time



SPICE Netlist

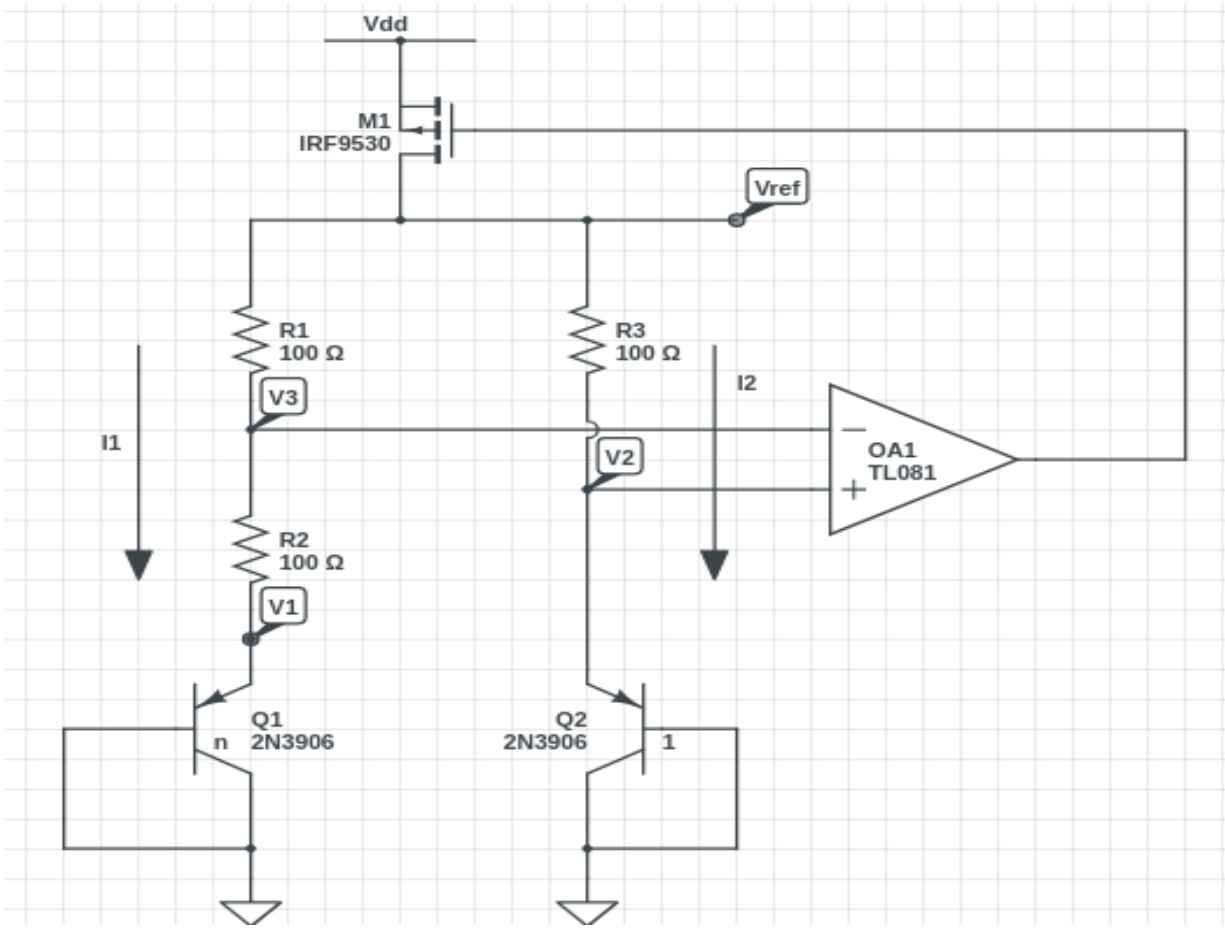
```
NGSPICE


*vin vdd 0 dc 0 pwl(0 0 100u 0 200u 5 500u 5)
*.tran 100u 500u
vin vdd 0 3.3
.DC TEMP -40 125 10
*.DC vin 0 5 0.5
.end
```

Design of BGR using 1.8v supply

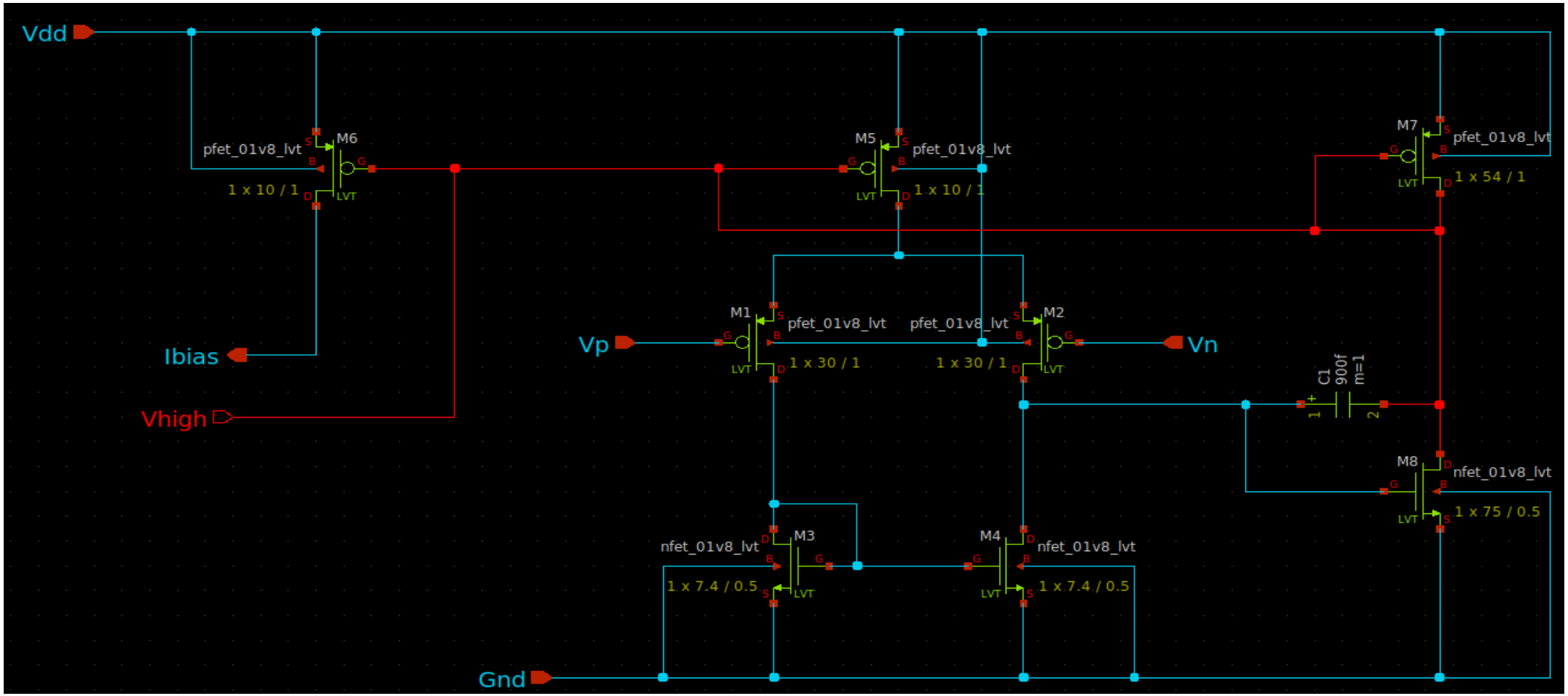


Analysis of BGR circuit

I2 = Io exp(v2/vt) , I1 = n * Io exp(v1/vt)
So v1-v2 = vt ln(I1/nI2)
I1=I2
v3 = I1*R2 + v1 = v2
Vref = I1 * R1 + v3 and Vref = I2* R3 + v2
I1=I2=(v2-v1)/R2 so I1=vt/r2 ln(n)
Vref = vt*(R3/R2)*ln(n) + v2 = 1.2v
Vref = -------PTAT--------- + CTAT = 1.2v
Using I1=I2= 10 µA , n=8
From above equation R2=5.2kΩ
R3=R1=50kΩ



OTA schematic



Analysis of OTA

- Two stage miller OTA used with the following specs:-

DC gain = 60 dB , GBW = 30 MHZ , Phase margin >= 60 deg , ICMR = 0.8v : 1.6v

Slew rate = 20v / microsec , C load = 2pf , Vdd = 1.8v

- Miller cap Cc >= 0.22 to achieve PM >= 60 deg so Cc = 800fF

- from Slew rate equation : SR = I5 / Cc we get I5 = 20 microAmp

- from GBW eauation: GBW = gm1 / 2πCc we get gm1 then (W/L) of m1,m2

- from ICMR+ equation : we get (W/L) of m3,m4

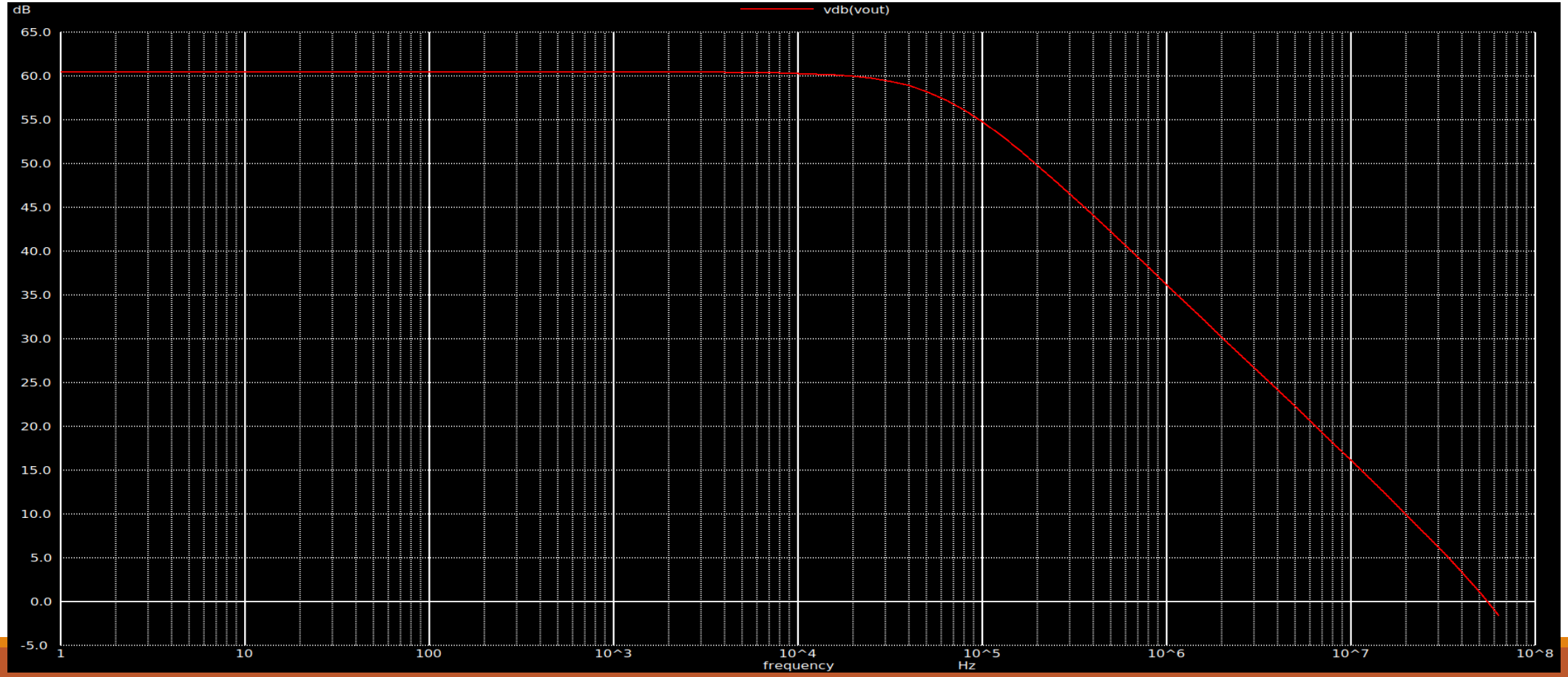
- from ICMR- eqatution : we get (W/L) of m5,m6

- from phase margin condition : we get (W/L) of m8

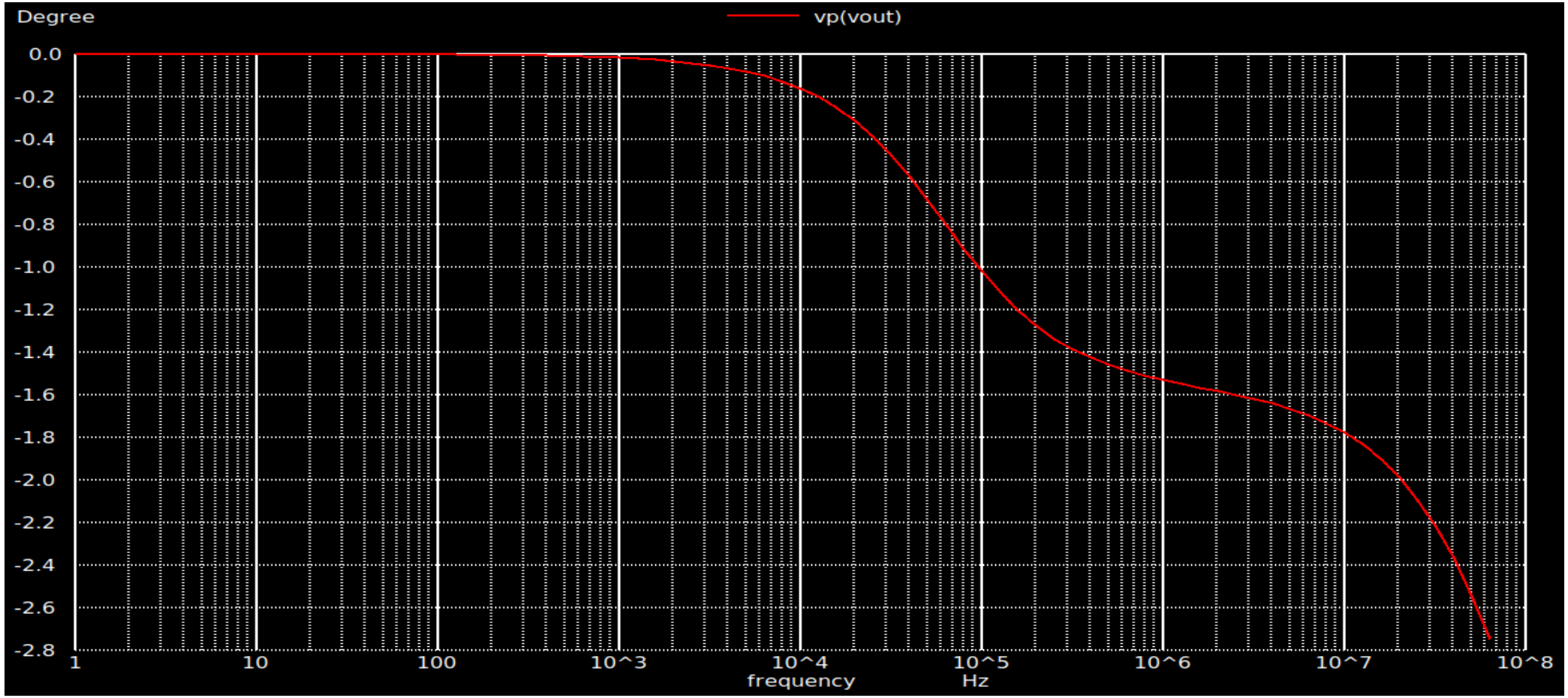
-from current mirror relation between m5,m7 we get (W/L) of m7

OTA simulation
1- AC analysis

Gain > 60 db , GBW = 60 MHZ , PM = 97 deg

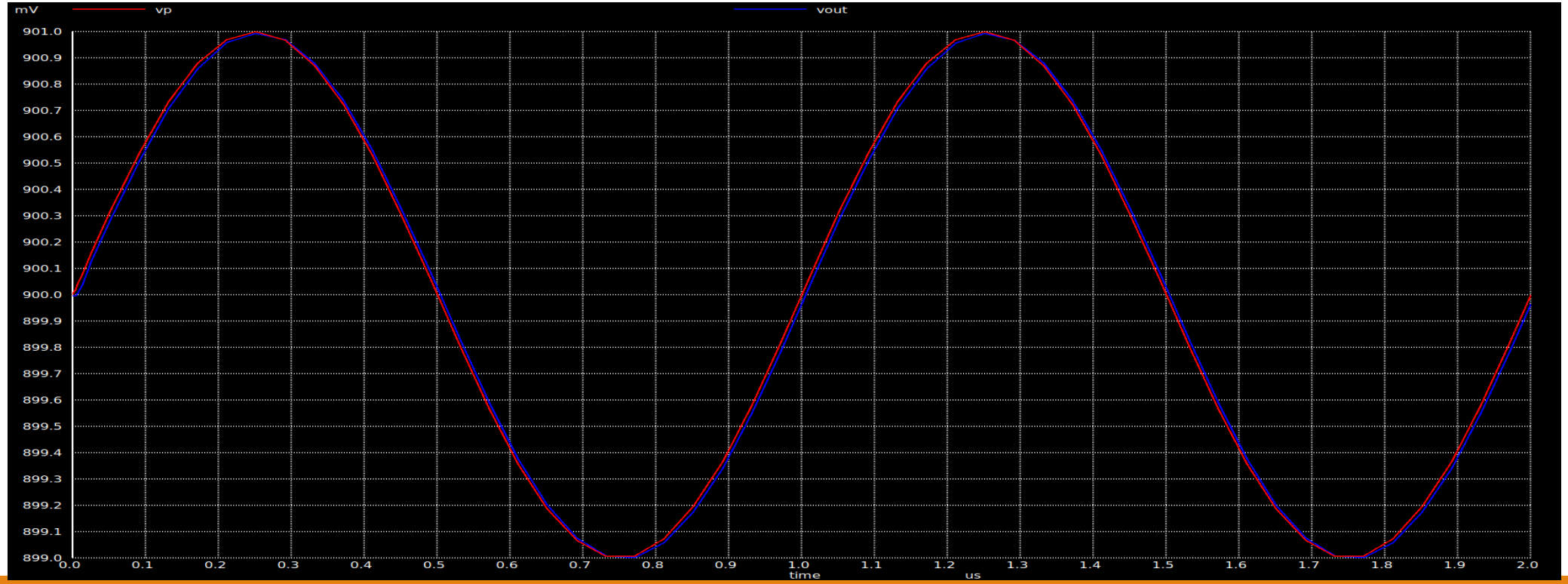


OTA Simulation:
1- AC Analysis



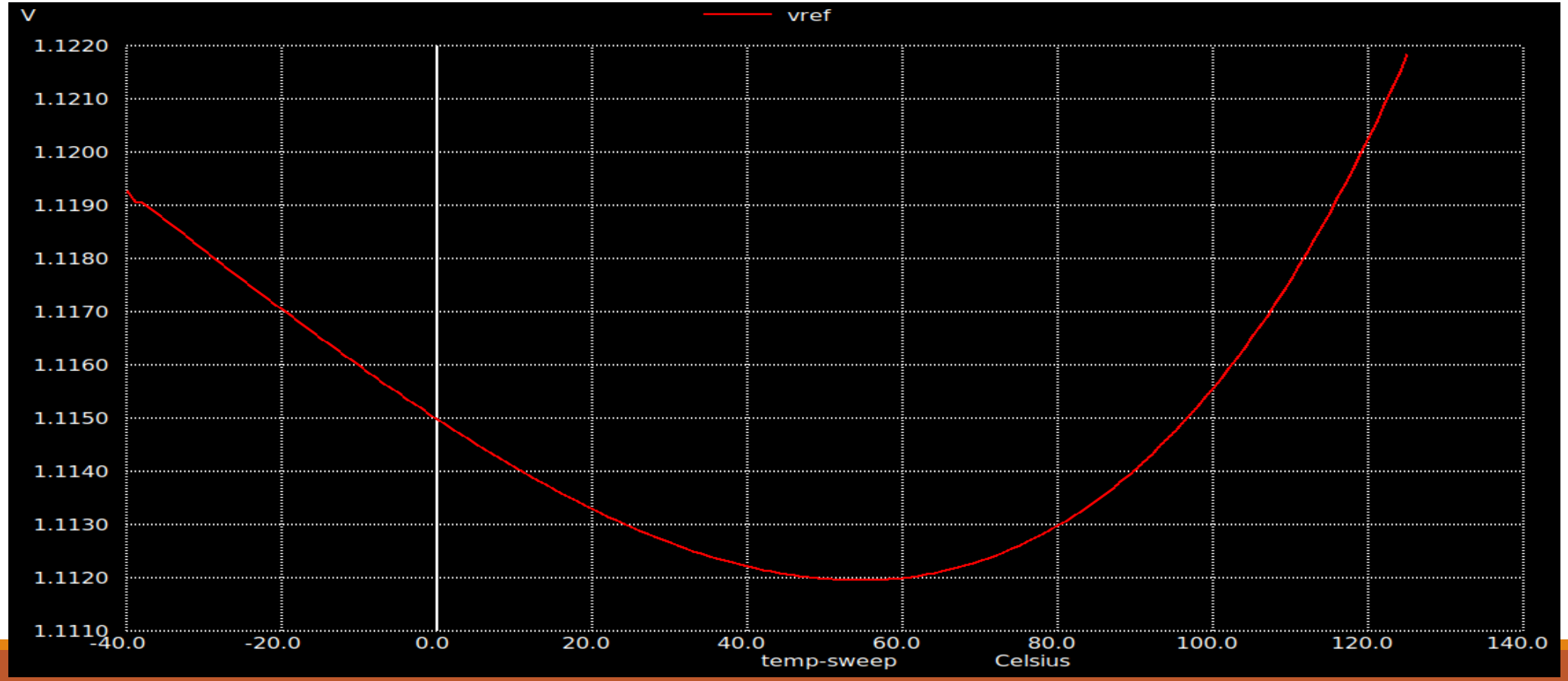
OTA Simulation
2- Transient Analysis

- I put the OTA in a feedback as a buffer and run transient simulation with input 1mv AC and 0.9v DC and the output is equal to the input as seen below:



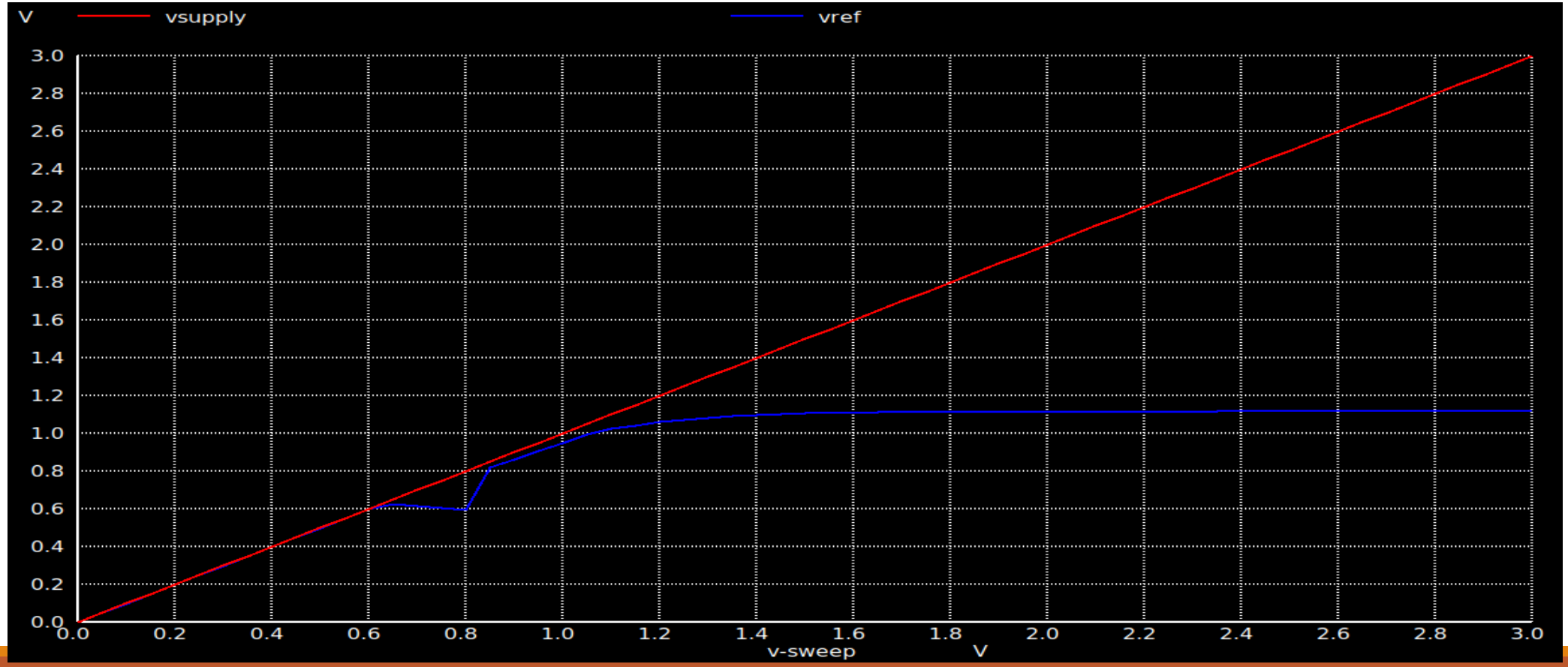
Simulation of Bandgap 1.8v
1- DC sweep vs Temperature

Using Vdd=1.8v and the temperature was swept from –40 to 125 deg and output is 1.11



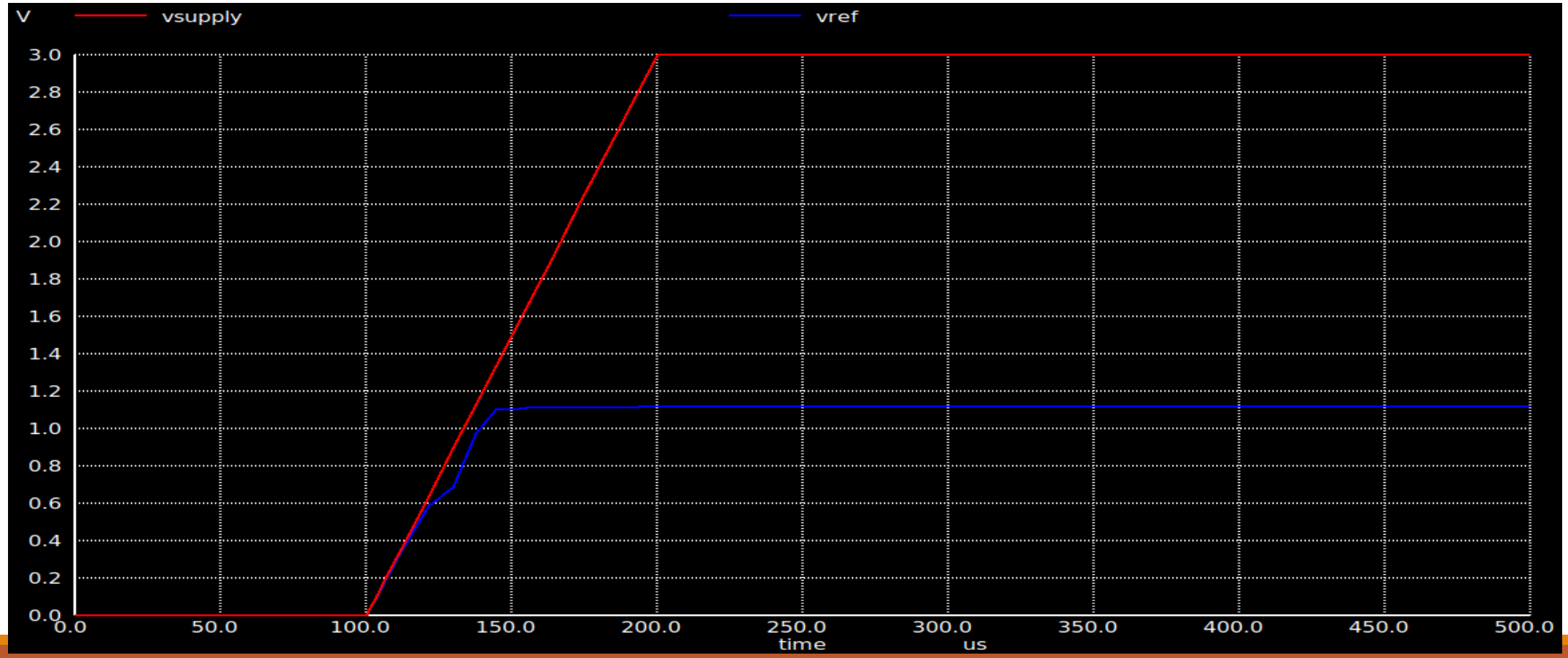
Simulation of Bandgap 1.8v
2- DC sweep vs Supply voltage

- VDD was swept from 0 to 3v and the output is 1.1v



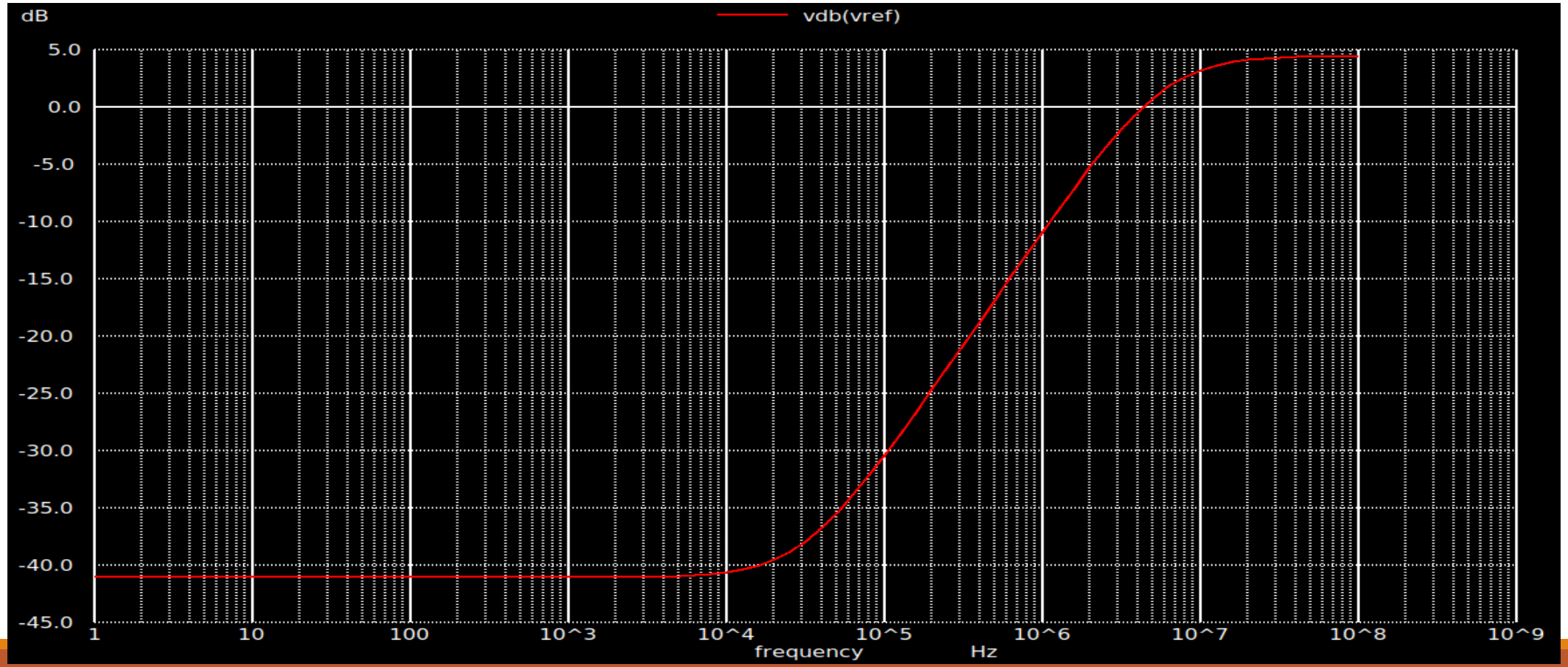
Simulation of Bandgap 1.8v
3- Transient Analysis

- A step voltage from 0 to 3v volt used with 100 us rise time and the output is 1.1v



Simulation of Bandgap 1.8v
4- PSRR Analysis

- PSRR = -40 dB from 1Hz to 16 KHZ



SPICE Netlist

NGSPICE

```
*vin Vdd 0 1.8
*.DC TEMP -40 125 1
*.DC vin 0 3 0.05
*vin Vdd 0 dc 0 pwl(0 0 100u 0 200u 3 500u 3)
*.tran 100u 500u
vin vdd 0 DC 1.8 AC 1
.ac dec 10 1 100MEG
.end
```

References

1- https://www.youtube.com/watch?v=wJz6claEGa0list=PLK2eyR1C9gjp5tk5j7eTYU_Th4IL_H83T

2- https://www.researchgate.net/publication/275341924_Design_of_a_Simple_CMOS_Bandgap_Reference

3- https://drive.google.com/drive/folders/1OWcbg8f48_ilr8jptdFEA3nbNeQyD0Hi

4- https://www.youtube.com/watch?v=F2fCmRKGoCY&list=PLK2eyR1C9gjoBp61ZDvz6Zdd_6Hu7vZTz