IC Design of Power Management Circuits (IV)

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Part IV

Bandgap References

Content (1)

Bandgap Reference Fundamentals:
PTAT Loop, V_{PTAT}, V_{BE}, V_{BG}, V_{REF}
Tempco, Line and Load Regulation, PSR
Positive and Negative Feedback Loops, Stability
Symmetrical Matching in Bipolar and CMOS Transistors

Simplest Bandgap References:

Basic BGR: Basic Bandgap Reference	in [Meijer 76]
Basic SM BGR: Basic Symmetrically Matched BGR	[industry]
PCS BGR: Peak Current Source BGR	[Cheng 05]

Classic Bandgap References:

Widlar BGR	[Widlar 71]
Brokaw BGR	[Brokaw 74]

in [Meijer 76]: referenced, but not proposed, in [Meijer 76].
[industry]: circuit not published but used in the industry.

Content (2)

CMOS Bandgap References with Op Amp:

Vertical PNPs for CMOS BGRs	[Song 83]
OP BGR: Op Amp Based BGR	[Kuijk 73]
CM BGR: Op Amp Based BGR with Current Mirror	[Gregorian 81]
FR BGR: BGR with Folded Resistors	[Neuteboom97]
SFR BGR: BGR with Symmetrical Folded Resistors	[Banba 99]
FRD BGR: BGR with Folded Resistor Dividers	[Leung 02]

CMOS Bandgap References without Op Amp:

4T BGR: BGR with 4T Current-Voltage Mirror (CVM)	in [Gray 01]
4T SM BGR: BGR with 4T SM CVM	[industry]
8T SM BGR: BGR with 8T SM CVM	[Lam 09]

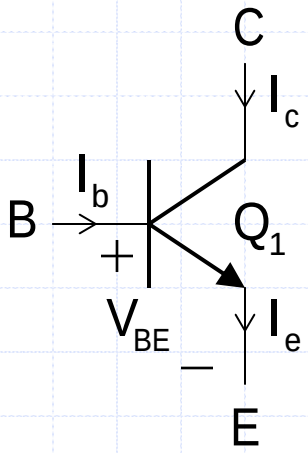
Design Issues:

Start Up
Trimming
Organization of References in IC System

I-V Characteristic of NPN

The I-V characteristic of a short-base npn transistor is [Sze 81]

$$I_c = I_s\left(e^{V_{BE}/nV_T} - 1\right)$$
$$= qn_i^2 A \frac{D_n}{N_A W_B}\left(e^{V_{BE}/nV_T} - 1\right)$$



where I_c: collector current
I_s: reverse saturation current
V_{BE}: base-emitter voltage
V_T: thermal voltage = kT/q
k: Boltzmann's constant (=1.38x10^{-23} J/K)
T: absolute temperature (Kelvin, K)
q: electronic charge (=1.6x10^{-19} C)
n: non-ideality factor
n_i: intrinsic carrier concentration
A: area of base
D_n: diffusion constant of electron (minority carrier) in the base
N_A: donor (majority carrier) doping concentration in the base
W_B: effective base width (to replace diffusion length)

Temperature Dependence of I-V Curve

We investigate the temperature dependence of the transistor. With Einstein's relation:

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q}$$

we have

$$I_s = C_1 T n_i^2 \bar{\mu}_n$$
$$n_i^2 = C_2 T^3 e^{-V_{Go}/nV_T}$$
$$\mu_n = C_3 T^{-\eta}$$

and gives

$$I_s = C T^{\gamma} e^{-V_{Go}/nV_T} \qquad (C = C_1 C_2 C_3,\ \gamma = 4 - \eta)$$

where μ_n: (average, effective) mobility of electron
V_{Go}: silicon bandgap voltage at 0K (=-273°C) [Gray 01] gives V_{Go}=1.205V with no explanation; while [Sze 81] gives V_{Go}=1.17V, and V_G(300k)=1.11V using experimental data.

Temperature Dependence of V_{BE}

The temperature dependence of the collector current is quite complicated but could be expressed as [Gray 01]

$$I_c = DT^{\chi}$$

and gives

$$V_{BE} = nV_T \ln\left(\frac{I_c}{I_s}\right)$$

$$= nV_T \ln\left(\frac{DT^{\chi}}{CT^{\gamma}e^{-V_{Go}/nV_T}}\right)$$

$$= V_{Go} - nV_T \ln\left(ET^{\gamma-\chi}\right) \qquad (E = C/D)$$

$$= V_{Go} - nV_T[(\gamma-\chi)\ln(T) + \ln(E)]$$

Note: (1) V_{BE} is lower than V_{Go}

(2) Temperature coefficient (TC) of V_{BE} ($\partial V_{BE}/\partial T$) is negative

Realizing V_{REF}

The thermal voltage at T = 300K (27°C) is

$$V_T = \frac{kT}{q} = \frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}} = 25.88\text{mV}$$

The TC of V_T at 300K is positive:

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} = \frac{V_T}{T}$$
$$= +86.25\times10^{-6}\ \text{V}/^{\circ}\text{C}$$

From previous page, we learn that TC of V_{BE} is negative. If we design a circuit with a voltage proportional to V_T, then we have

$$V_{REF} = V_{BE} + MV_T$$
$$= V_{Go} - nV_T(\gamma-\chi)\ln(T) + V_T[M - n\ln(E)]$$

We need to determine the condition for V_{REF} to have zero TC.

Condition for Zero-TC of V_{REF}

The condition for zero TC of V_{REF} at a predefined temperature T_o is

$$\left.\frac{dV_{REF}}{dT}\right|_{T_o} = 0$$

$$\Rightarrow \quad -nV_{T_o}(\gamma-\chi)\frac{1}{T_o} - \frac{nV_{T_o}(\gamma-\chi)}{T_o}\ln(T_o) + \frac{V_{T_o}}{T_o}[M - n\ln(E)] = 0$$

$$\Rightarrow \quad M - n\ln(E) = n(\gamma-\chi)[1+\ln(T_o)]$$

$$\therefore \quad V_{REF} = V_{Go} + nV_T(\gamma-\chi)\left(1-\ln\left(\frac{T}{T_o}\right)\right)$$

As the reference voltage is close to V_{Go}, so it is labeled the bandgap reference voltage:

$$V_{BG} = V_{BE} + MV_T$$

$$= V_{Go} + nV_T(\gamma-\chi)\left(1-\ln\left(\frac{T}{T_o}\right)\right)$$

Temperature Dependence of V_{BG}

For $T = T_o + \Delta T$ and $\ln(1+\delta) \approx \delta - \frac{1}{2}\delta^2$, we have

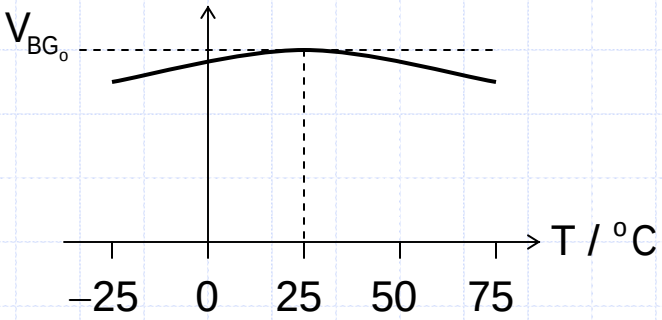
$$V_T = V_{T_o}\left(1 + \frac{\Delta T}{T_o}\right)$$

$$\ln\left(\frac{T}{T_o}\right) = \ln\left(1 + \frac{\Delta T}{T_o}\right) \approx \frac{\Delta T}{T_o} - \frac{1}{2}\frac{\Delta T^2}{T_o^2}$$

then

$$V_{BG} = V_{Go} + nV_{T_o}(\gamma - \chi)\left(1 - \frac{1}{2}\frac{\Delta T^2}{T_o^2}\right)$$

Hence, V_{BG} peaks at $V_{BGo} = V_{BG}(T_o)$, and $V_{BG}(T) < V_{BG}(T_o)$:



Direct Design of V_{BG}

A direct consideration of a zero-TC voltage reference without resorting to semiconductor physics is to recognize that

$$\frac{dV_{BE}}{dT} = -2\text{mV} / {}^{o}\text{C} \sim -2.2\text{mV} / {}^{o}\text{C}$$

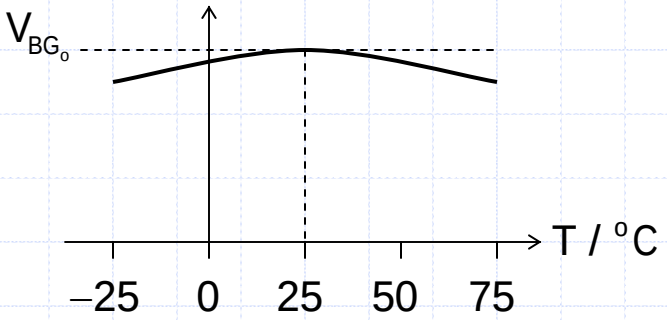
while the thermal voltage has a positive TC:

$$\frac{dV_T}{dT} = \frac{k}{q} = \frac{V_T}{T} = +86.25\mu\text{V} / {}^{o}\text{C}$$

The bandgap voltage is then generated by

$$V_{BG} = V_{BE} + MV_T$$

with M = 23.2 for dV_{BE}/dT = -2mV/^{o}C.



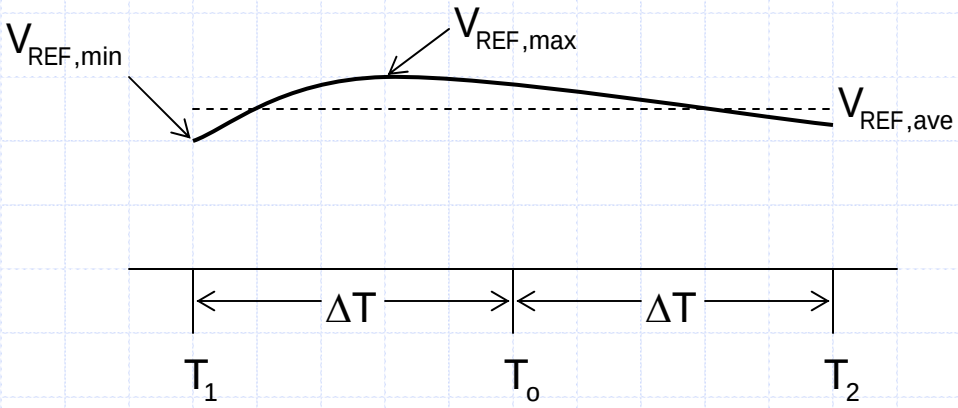
TC of Voltage References

The IC industry defines TC of V_{REF} as:

$$TC = \frac{|V_{REF,max} - V_{REF,min}|}{T_2 - T_1} \quad \text{in mV / }^{o}\text{C}$$

$$= \frac{|V_{REF,max} - V_{REF,min}| / V_{REF,ave}}{T_2 - T_1} \quad \text{in ppm / }^{o}\text{C}$$

Moreover, due to simulation and fabrication variations, the measured zero TC point may not be at exactly the midpoint of the temperature range:



TC of BGR

For the ideal I-V curve with the temperature range of $2\Delta T$, the TC of V_{BG} is given by

$$TC = \frac{1}{2} n V_{T_o} (\gamma - \chi) \frac{\Delta T^2}{T_o^{\,2}} \frac{1}{2\Delta T}$$

Let $n(\gamma - \chi) = 2$, and $T_o = 300K$ (27^oC), then

$$V_{BG} = 1.205 + 2 \times 25.88m \approx 1.26V$$

If the temperature range is from 250K (-23^oC) to 350K (77^oC), then $T_o = 300K$ (27^oC), $\Delta T = 50^oC$, $T_2 - T_1 = 100^oC$, and

$$TC = \frac{1}{2} \times 2 \times 25.88m \times \frac{50^2}{300^2} \times \frac{1}{100}$$

$$\approx 7.2\mu V / {}^oC$$

$$\approx 6ppm / {}^oC$$

In actual design, the TC figures would be (much) worse.

Line Regulation

Line regulation is the change of V_{REF} w.r.t. the change in V_{dd}:

$$\text{line reg.} = \frac{\Delta V_{REF}}{\Delta V_{dd}} \quad \text{in mV / V}$$

$$= \frac{\Delta V_{REF} / V_{REF}}{\Delta V_{dd}} \quad \text{in \% / V}$$

Transistor circuits are non-linear circuits for large signal changes, and hand analysis is impossible. It could be obtained by simulation. In datasheets, line regulation is usually measured:

- Find V_{dd}(min) such that the voltage reference is barely operative
- Measure points range from V_{dd}(min)+0.2V to V_{dd}(max)
- Compute line regulation

Power Supply Rejection

For a good voltage reference (also for bandgap reference and linear regulator), the output voltage should be a weak function w.r.t. the supply voltage. Hence, a small signal parameter, the power supply rejection, gives good indication of line regulation.

Power supply rejection (PSR) is the small signal change of V_{BG} w.r.t. the small signal change in V_{dd}.

In transfer function form: $$PSR = \frac{v_{bg}}{v_{dd}}$$

In dB: $$PSR = 20 \times \log \left| \frac{v_{dd}}{v_{bg}} \right|$$

Usually $|v_{bg}/v_{dd}| < 1$, but we customarily give a positive PSR in dB.

Note: Line reg. $\approx$ PSR $\times \Delta V_{dd}$

Load Regulation and Output Impedance

Load regulation is the change of V_{REF} w.r.t. the change in I_o:

$$\text{load reg.} = \frac{\Delta V_{REF}}{\Delta I_o} \qquad \text{in mV / mA}$$

$$= \frac{\Delta V_{REF} / V_{REF}}{\Delta I_o} \qquad \text{in \% / mA}$$

In datasheets, load regulation is usually measured. Moreover, many BGRs cannot drive resistive loads, and load regulation is not included.

In the small signal limit, load regulation is the output impedance:

$$R_{o(REF)} = \frac{dV_{REF}}{dI_o} \qquad \text{in } \Omega$$

Stability inferred from Line and Load Transients

For a feedback system, stability is usually determined by computing or measuring the loop gain and the gain and phase margins.

For a circuit, and especially an integrated circuit, however, due to loading effect and that loop-breaking points may not be accessible, stability is inferred by simulating or measuring the line transient and/or load transient.

If the circuit is stable and has adequate phase margin, line and load transients will show first order responses.

If the circuit is stable but has a phase margin less than 70^{o}, line and load transients will show minor ringing.

If the circuit is unstable, line and load transient will show serious ringing/oscillation.

Voltage References Criteria

A good voltage reference should have:

(1) Low TC over a wide range of temperature
(2) Low line regulation and good power supply rejection (PSR)
(3) Good stability

Other considerations:

(1) Low load regulation (if applicable)
(2) Minimum V_{dd} for operation
(3) Consume little power
(4) Small area for resistors
(5) Small area for compensation capacitor (if applicable)
(6) Low noise
(7) Long term stability

PTAT Current Generator

A commonly used PTAT (proportional to absolute temperature) current generator is discussed in [Kessel 71] as shown below. Now,

$$V_{BE1} = V_T \ln \frac{I_1}{N I_s} \qquad V_{BE2} = V_T \ln \frac{I_2}{I_s}$$

Ignore early effect, then

$$I_2 = I_1$$

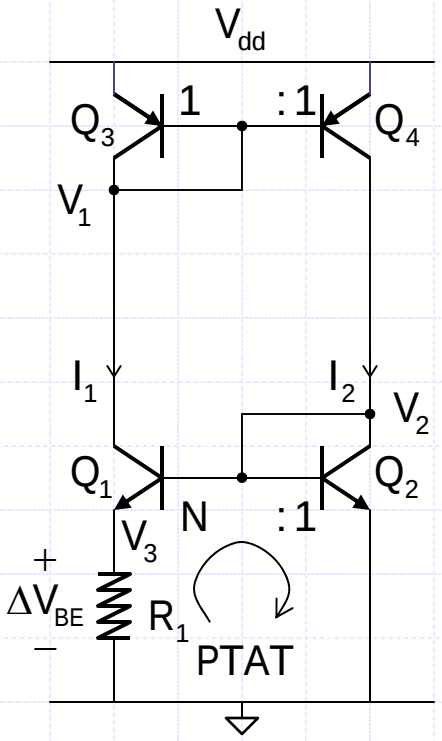
and

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln(N)$$

I_1 (and I_2) is a PTAT current:

$$I_1 = \frac{V_T}{R_1} \ln(N)$$

(If TC of R is smaller than TC of V_T.)



Basic BGR: Schematic

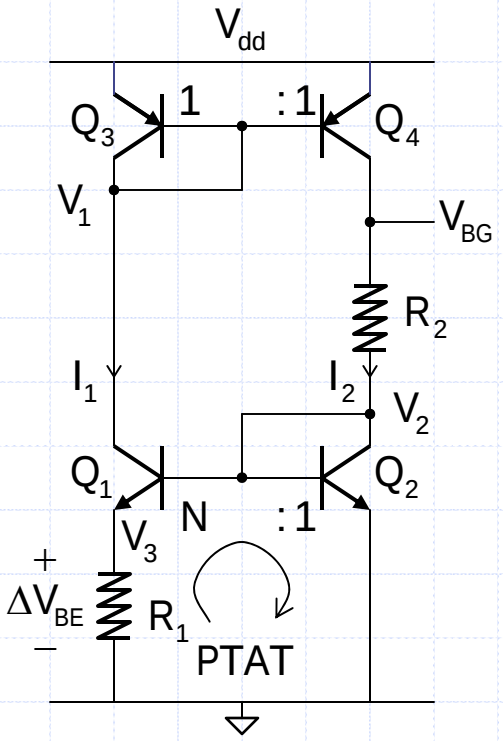
The simplest bandgap reference (BGR) consists of 4 transistors and 2 resistors. Positive TC is generated by the PTAT circuit consists of Q_1, R_1 and Q_2 (n=1 and large β) [Meijer 76]*. The reference voltage is

$$V_{BG} = V_{BE2} + I_2 R_2$$

$$= V_{BE2} + \frac{R_2}{R_1} \ln(N) V_T$$

Clearly, V_{BE2} has a –ve TC, and V_T has a +ve TC. Note that the TCs of R_1 and R_2 cancel each other. Also, the basic BGR, and all other BGRs, requires a start-up circuit (to be discussed later).

*The basic BGR is referenced, not proposed, in [Meijer 76].



Basic BGR: Zero TC Condition

To achieve zero TC for V_{BG} at T_o, we set

$$\left.\frac{dV_{BG}}{dT}\right|_{T_o} = 0 \Rightarrow \frac{dV_{BE2}}{dT} + \frac{R_2}{R_1}\ln(N)\frac{V_{T_o}}{T_o} = 0$$

R_1 and R_2 has the same TC, and $(R_2/R_1)\times\ln(N)$ is independent of temp. In practice, TC of V_{BE2} is obtained by characterizing the process, and

$$\frac{dV_{BE}}{dT} \approx -2mV/^oC \quad \text{to} \quad -2.2mV/^oC$$

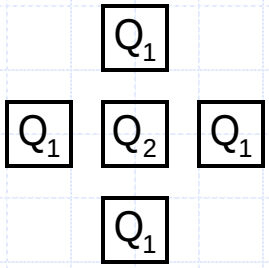
The transistor ratio N is usually taken as 4 or 8, and I_1 is determined by the application, usually ranges from 10μA to 100μA. Let TC of V_{BE} be -2mV/^{o}C (from measurement), and T_o=300K, then

$$\frac{R_2}{R_1}\ln(N) = \frac{2m\times T_o}{V_T} = \frac{2m\times q}{k} = \frac{3.2\times10^{-22}}{1.38\times10^{-23}} \approx 23.2$$

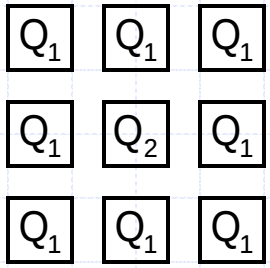
Basic BGR: Matching Consideration

Common centroid layout for Q_1 and Q_2 for better matching:

$Q_1:Q_2 = 4:1$



$Q_1:Q_2 = 8:1$



Take N=8, $\Delta V_{BE} = V_T \ln(N) = 53.8\text{mV}$ at T=300K. For $I_1 = 5\mu\text{A}$,

$$R_1 = \frac{V_T}{I_1}\ln(N) = 10.76\text{k}\Omega$$

$$R_2 = \frac{2m \times T_o \times R_1}{V_T \ln(N)} = 2m \times T_o \times I_1 = 120\text{k}\Omega$$

N.B. Some designs use N > 100 to generate a large ΔV_{BE} for better (lower) sensitivity due to process variations.

Process and Simulation

Process: TSMC 0.18μ deep n-well CMOS

NMOS: V_{tn}=0.44V

PMOS: $|V_{tp}|$=–0.44V

npn: V_{BE}(4.7μA)=0.70V

pnp: V_{EB}(4.7μA)=0.64V

Conditions: N=8, $I_1 \approx 4.6\mu A$ @25°C, R_1=10.8kΩ, R_2=91.6kΩ

Notes:

(1) All voltage references in this talk are simulated using the same 0.18μ CMOS process that also supports bipolar transistors.

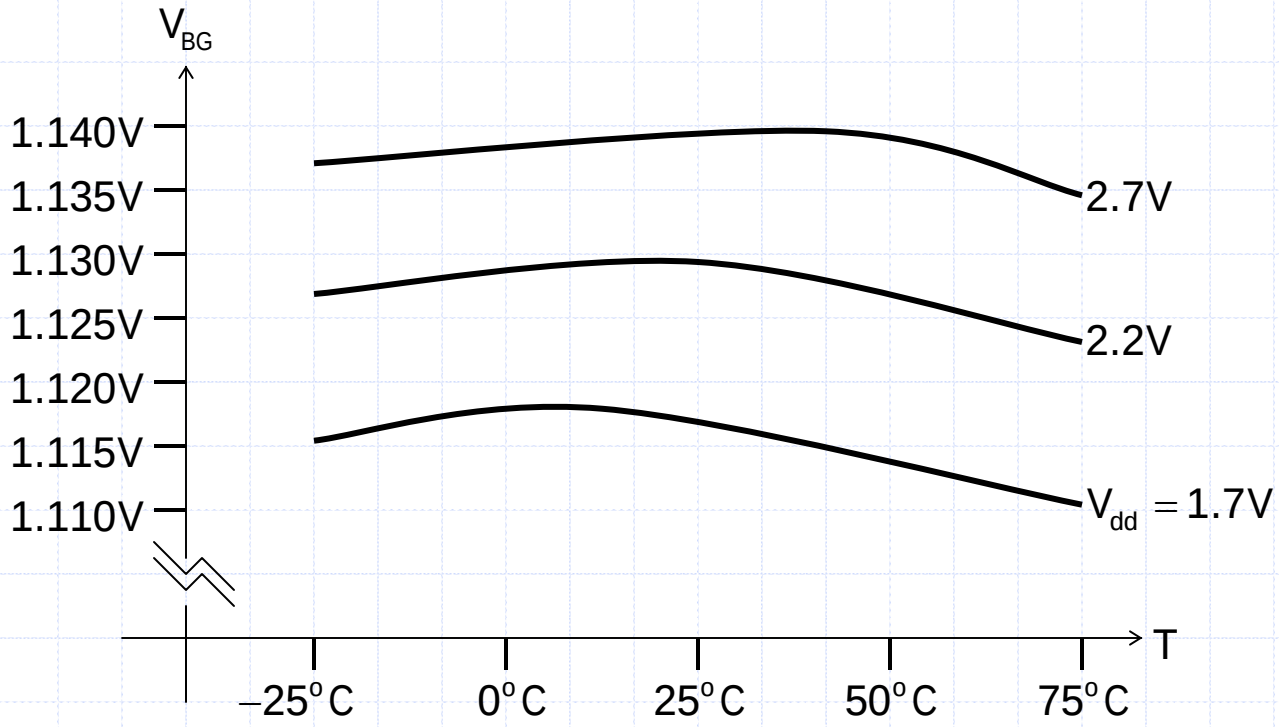
(2) With N=8, R_2 should be $11.16 \times R_1$ = 120.5kΩ, but as the non-ideality factor $n \neq 1$, R_2 needed is smaller.

(3) Current mirrors are simulated using PMOS transistors.

(4) I thank Mr. Chenchang Zhan for assisting in all Spice simulations.

Basic BGR: TC + Line Reg. Simulation

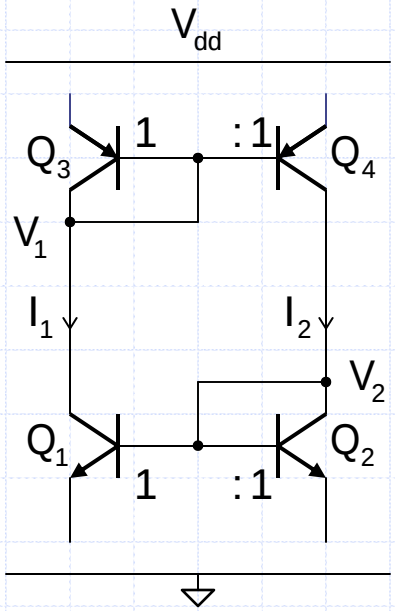
Instead of cutting and pasting the simulation results, they are redrawn using PowerPoint as shown below. Note that line regulation causes a larger error than the temperature dependence.



Cross-Biased 4T Cell

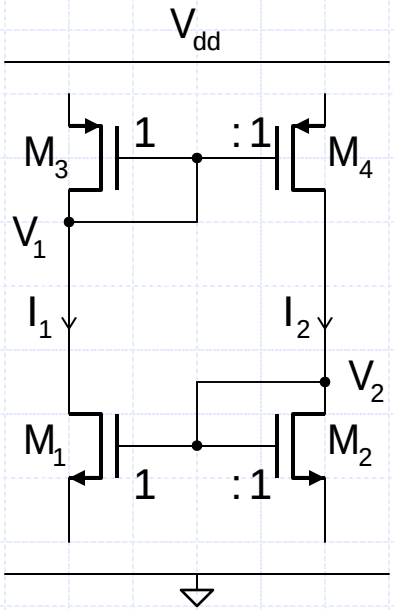
The loop gain of the basic BGR is independent of R_2. Moreover, for N = 1 and $R_1 = 0\Omega$, T = -1, and the circuit oscillates.

Although the circuit oscillates, this cross-biased 4T cell, when properly connected, can be considered as a current mirror as well as a voltage mirror: current conveyer [Smith 68], or current-voltage mirror (CVM) [Lam 08]. More on this later.



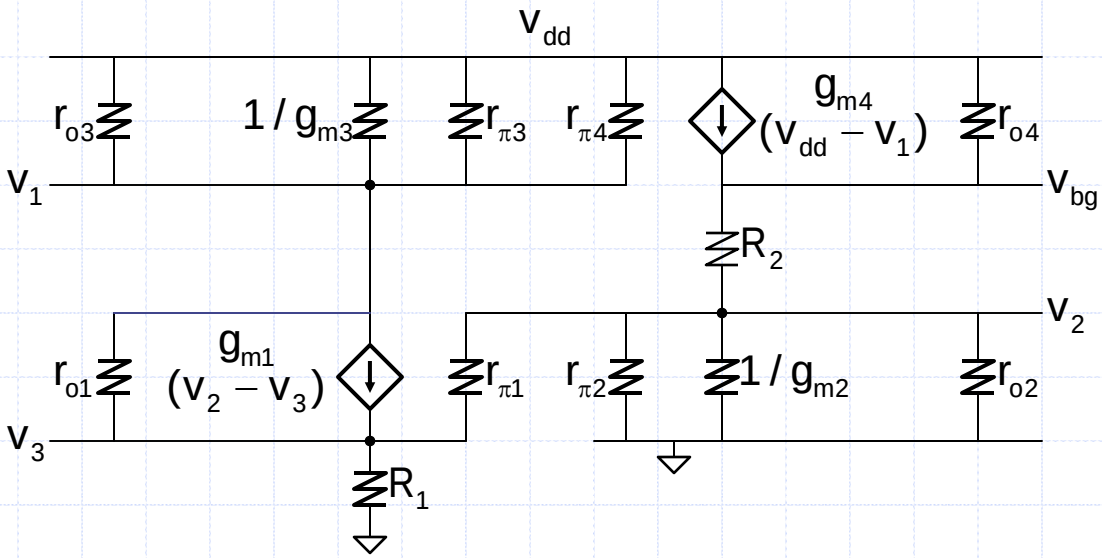
UNSTABLE by themselves!

But could be useful if properly connected.



Basic BGR: PSR Analysis

Small signal model for computing PSR of the basic BGR:

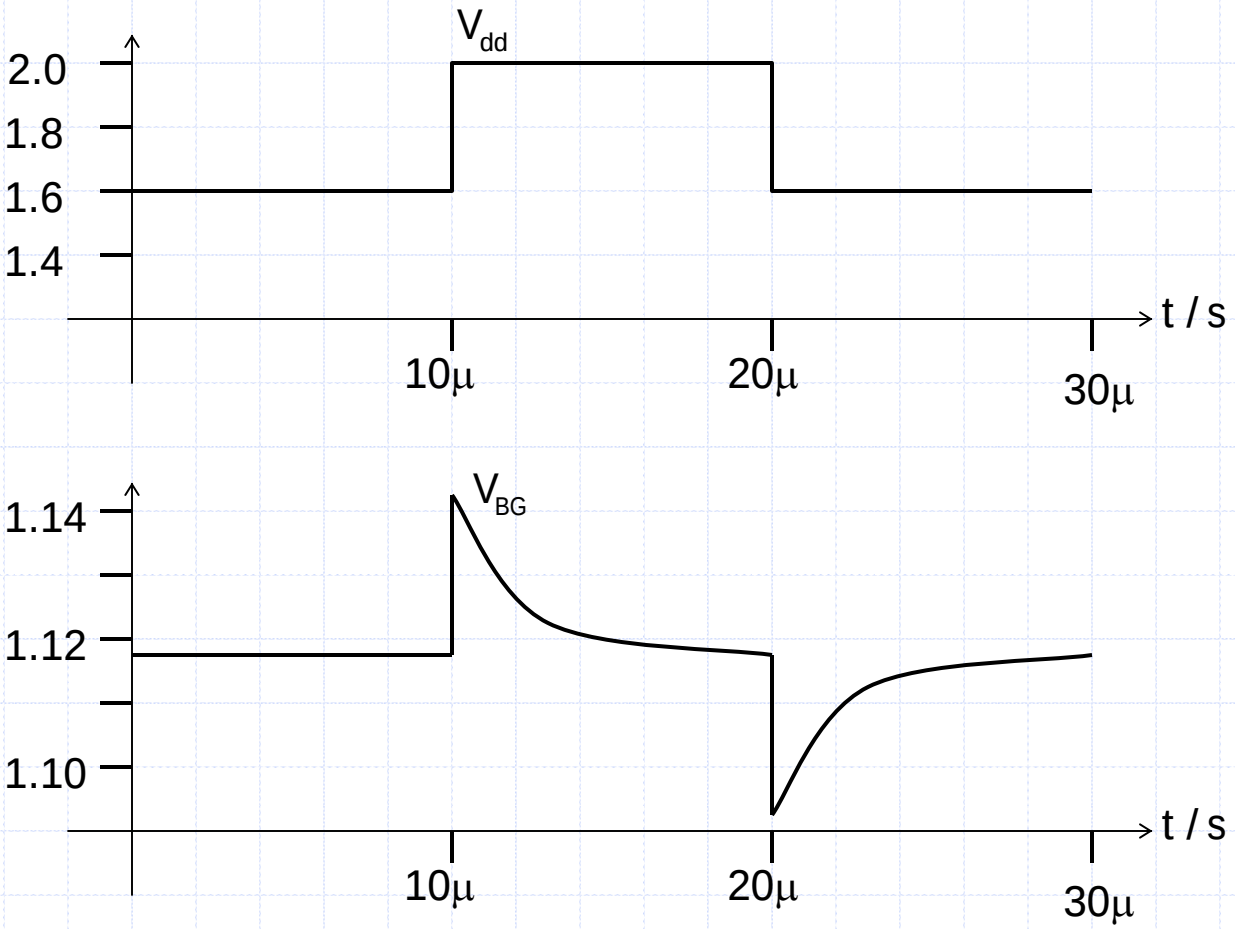


The computation is not trivial, but using appropriate approximations, it could be shown that, for $r_{on}=r_{o1,2}$, $r_{op}=r_{o3,4}$,

$$PSR = \frac{v_{bg}}{v_{dd}} = \left(1+\frac{R_2}{R_1}\ln(N)\right)\left(\frac{r_{on}}{r_{op}+r_{on}}+\frac{1}{\ln(N)}\right)\frac{1}{g_m(r_{op}\,||\,r_{on})}$$

Basic BGR: Line Transient

Assume on-chip application such that C_{Load}=10pF. The basic BGR is stable with a larger C_{Load}.



Basic BGR: Performance Summary

Parameter	Computation	Simulation BSIM 3 (β_n=20)	Simulation Level 1 (β_n=80)
R_2 (R_1=10.8kΩ)	120.5kΩ	91.6kΩ	108.3kΩ
$V_{dd}(min)=V_{BG}+0.2V$	1.45V	1.5V	1.5V
V_{BG} (V_{dd}=1.7V)		1.118V	1.118V
TC	6ppm/^{o}C	49ppm/^{o}C	8ppm/^{o}C
Loop gain	-0.324	-0.349	-0.324
PSR	32.7dB	33.6dB	32.4dB
Line regulation	23mV/V	22mV/V	25mV/V

N.B.

(1) R_2 is smaller than computed because n (ideality factor) is not 1.

(2) BSIM3 simulation using parasitic Q_1 and Q_2 gives a much larger TC than predicted in pp.13. By substituting Q_1 and Q_2 with Level 1 npn with β_n=80, TC simulation is close to prediction.

Symmetrical Matching of Bipolar Transistors

When a pair of bipolar transistors Q_1 and Q_2 of the same type are matched, the area ratio is designed to be the same as the intended current ratio. However, their collector-emitter voltages may be different and their collector currents are different due to early effect.

If Q_1 and Q_2 are forced (by an additional circuit) to have essentially the same V_C, V_B and V_E, then they are called symmetrically matched (SM) [Lam 07b].

High performance BGRs inevitably employ symmetrical matching to improve PSR, although not explicitly stated [Brokaw 74].

Basic SM BGR

For the basic BGR, line regulation and PSR could be improved by reducing the early effect of Q_1 and Q_2. The Q_5 and Q_6 branch is added, forcing Q_1 and Q_2 to be symmetrically matched. By adding R_2 at the collector of Q_3, Q_3 and Q_4 are symmetrically matched.

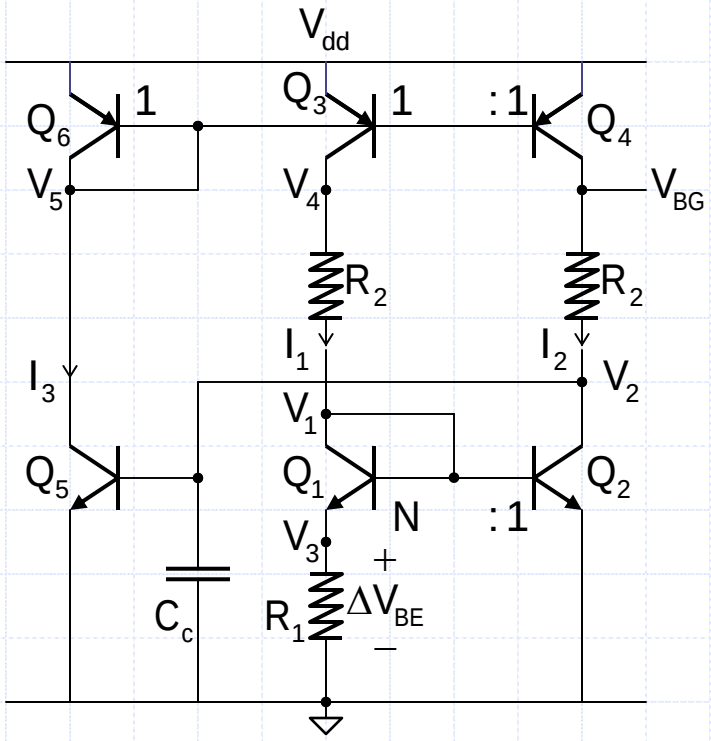
The reference voltage is

$$V_{BG} = V_{BE5} + \frac{R_2}{R_1} \ln(N) V_T$$

The loop gain at breaking at V_2 is

$$T = -\frac{v_{2o}}{v_{2i}} = \ln(N) \times g_m (r_{op} \,||\, r_{on})$$

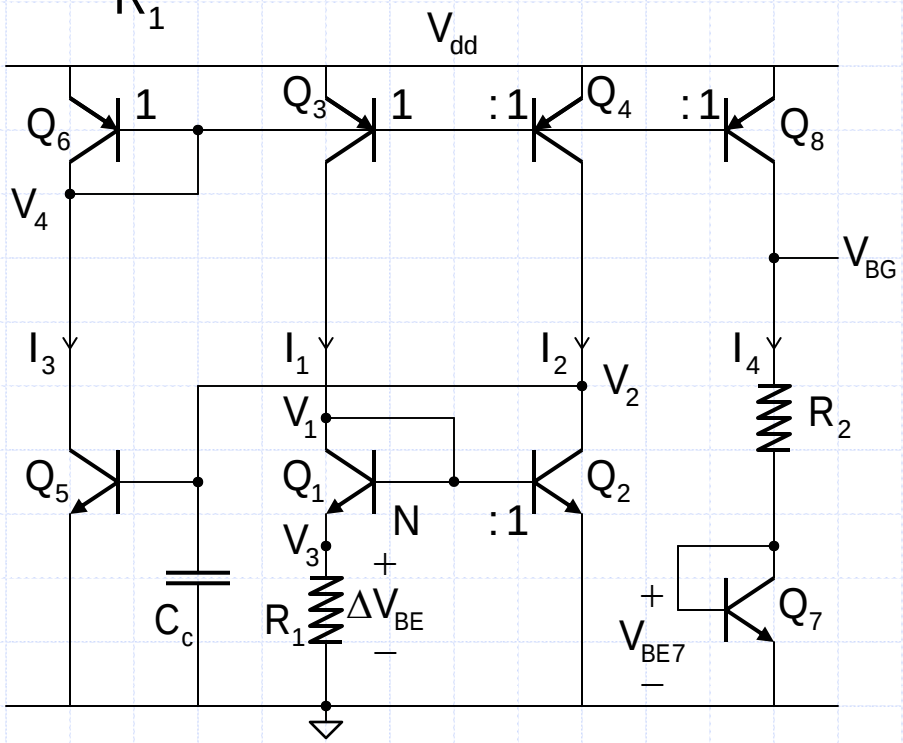
where all transistors have the same transconductance g_m, all npn have the same r_{on}, and all pnp have the same r_{op}. This T is –ve feedback.



Basic SM BGR (2)

To save a large R_2, a fourth branch (Q_7 and Q_8) could be added, and

$$V_{BG} = V_{BE7} + \frac{R_2}{R_1} \ln(N) V_T$$



N.B. Both basic SM BGRs are used in the industry but not discussed in the literature.

Basic SM BGR: Performance Summary

Parameter	Computation	Simulation BSIM 3 (β_n=20)	Simulation Level 1 (β_n=80)
R_2 (R_1=10.8kΩ)	120.5kΩ	115.4kΩ	105.7kΩ
V_{dd}(min)	1.45V	1.5V	1.3V
V_{BG} (V_{dd}=1.7V)		1.3305V	1.3305V
TC	6ppm/^{o}C	13.3ppm/^{o}C	5.9ppm/^{o}C
Loop gain	64.5dB	60.9dB	64.1dB
PSR		69dB	60dB
Line regulation		-0.36mV/V	-0.83mV/V

N.B. TC performance of the basic SM BGR is closer to prediction even for BSIM3 simulation using parasitic Q_1 and Q_2.

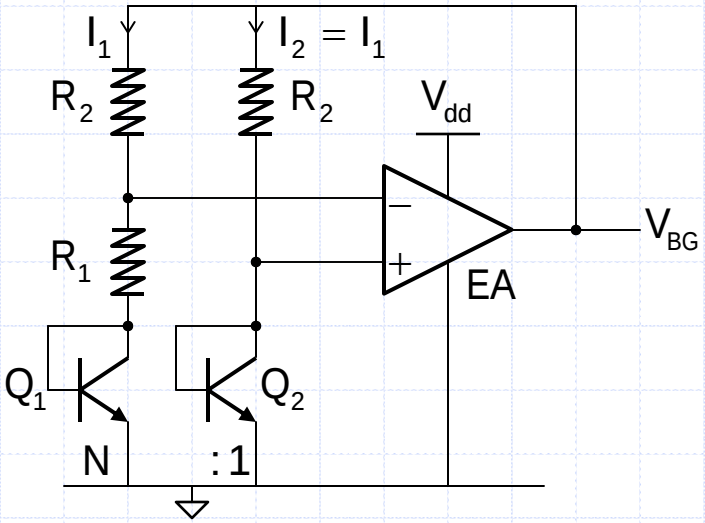
Op-Amp Based BGR (OP BGR)

The op-amp based bandgap was first discussed in [Kuijk 73] using Widlar current source [Widlar 65] with $I_1 \neq I_2$. For $I_1 = I_2$, Q_1 and Q_2 will have different sizes (N:1). The op-amp A(s) forces $I_1 = I_2$, and I_1 is a PTAT current:

$$V_{BE2} - V_{BE1} = V_T \ln(N) = I_1 R_1$$

$$V_{BG} = V_{BE2} + I_1 R_2$$

$$= V_{BE2} + \frac{R_2}{R_1} \ln(N) V_T$$

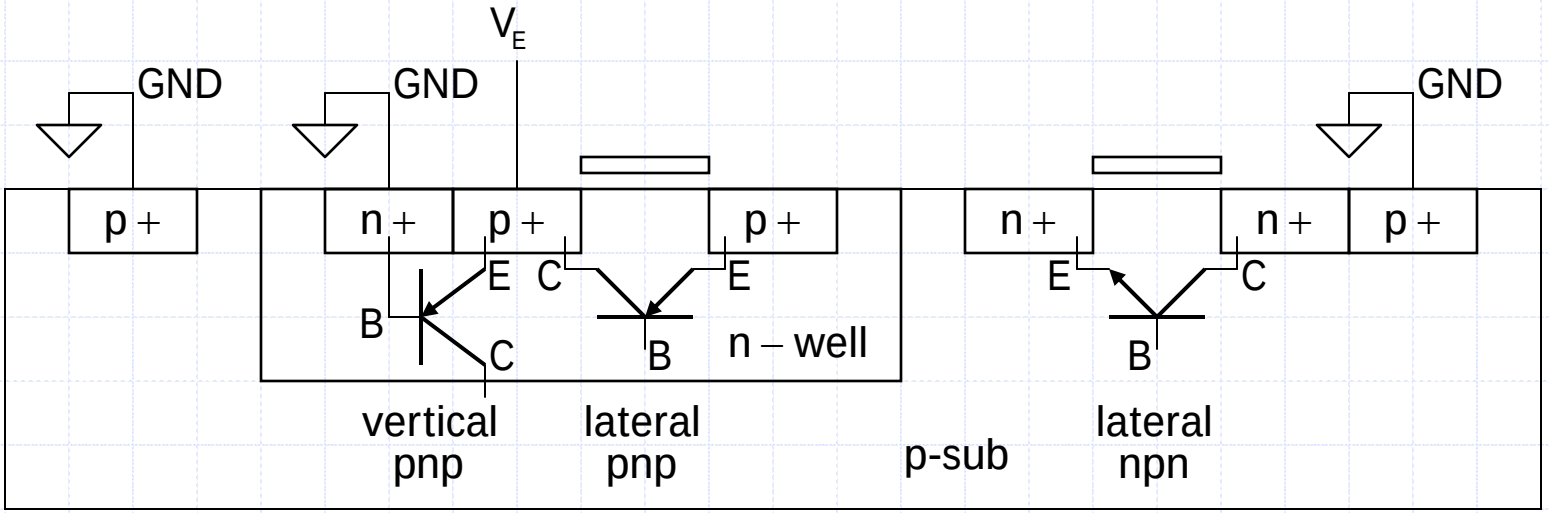


This V_{BG} relation is the same as that of the basic BGR. However, the total resistance is

$$R_T = R_1 + 2R_2.$$

BJTs in Digital CMOS Process

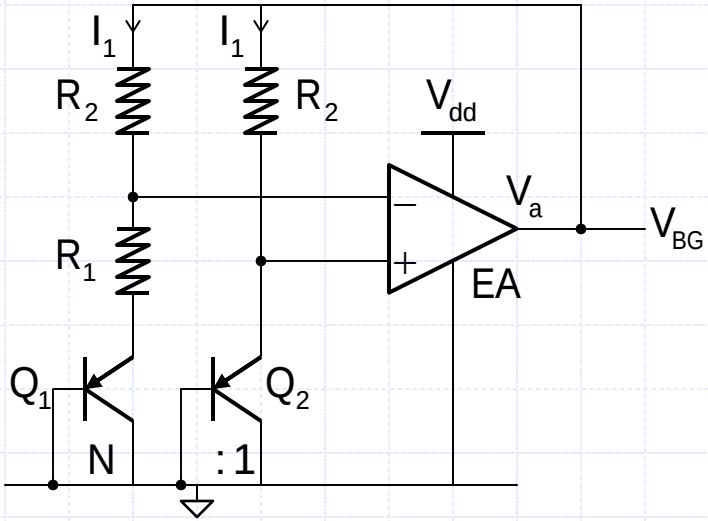
In a digital CMOS n-well process, parasitic lateral pnp, lateral npn and vertical pnp transistors could be identified. Vertical pnp transistors are more commonly used for their lower base resistance than lateral transistors. However, the collector, which is the p-sub, is restricted to be connected to ground.

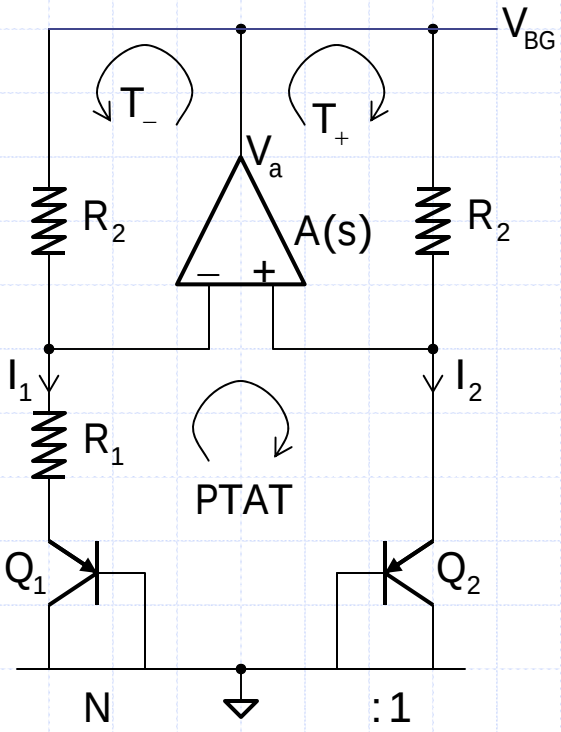


Parasitic vertical pnp transistors were used in [Song 83].

Op-Amp Based BGR (OP BGR)

For a standard CMOS digital process, BGR usually uses parasitic vertical pnp transistors. By drawing the CMOS op-amp based BGR (OP BGR) as shown on the right, two feedback loops, one negative and one positive, can easily be identified.





This BGR can drive resistive load if EA is properly designed.

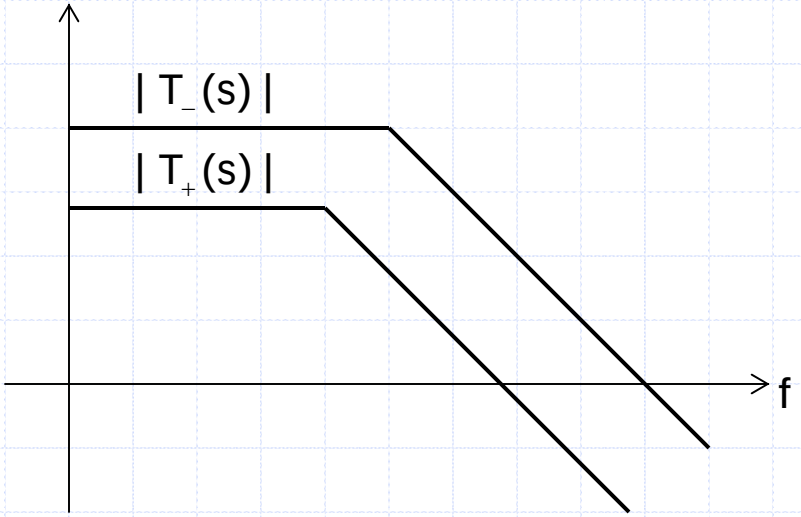
OP BGR: –ve and +ve Feedback Loops

Negative feedback loop:

$$T_{-} = \frac{1 + g_{m1}R_1}{1 + g_{m1}(R_1 + R_2)} \times A(s)$$

Positive feedback loop:

$$T_{+} = \frac{-1}{1 + g_{m1}R_2} \times A(s)$$



For stability, we need $|T_{-}| > |T_{+}|$, and this criterion is satisfied by the above two relations.

The above T_{-} and T_{+} ignore parasitic capacitors of the transistors and resistors. By accounting for all parasitics, we require $|T_{-}(j\omega)| > |T_{+}(j\omega)|$ for all frequencies.

OP BGR: System Loop Gain

By breaking the loop at the output of the op-amp V_a, the system loop gain T(s) is given by

$$T = T_- - T_+$$

$$= \left(\frac{1 + g_{m1} R_1}{1 + g_{m1}(R_1 + R_2)} - \frac{1}{1 + g_{m1} R_2} \right) \times A(s)$$

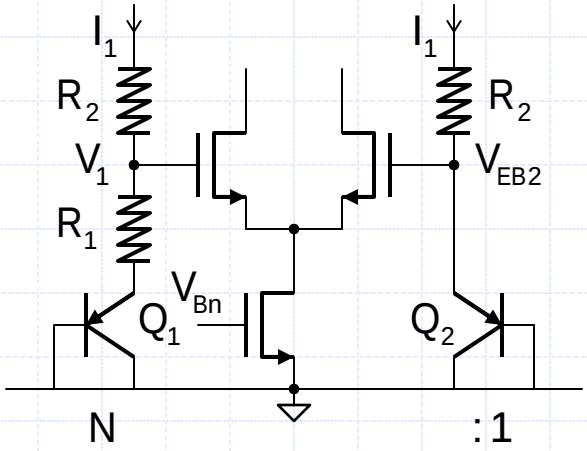
Stability of a system is determined by the system loop gain, however, parasitic capacitors complicate the loop gain expression, and may not be too useful in compensation consideration:

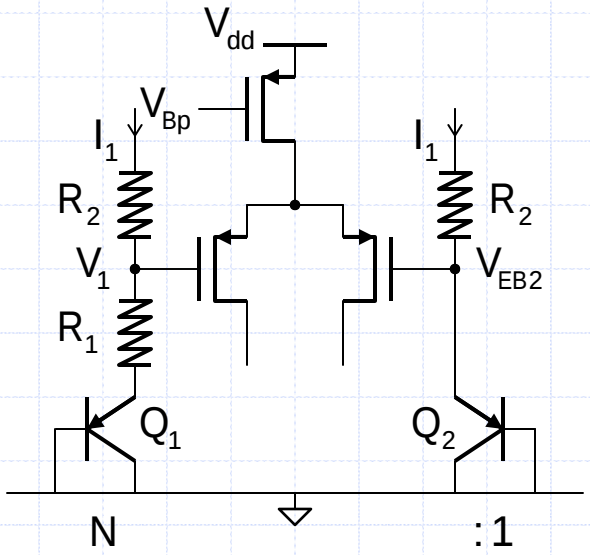
$\Rightarrow$ Considering $T_-(s)$ and $T_+(s)$ for stability is more direct.

An example is shown in designing the current-mirror (CM) BGR.

OP BGR: Input Stage

Let the gate overdrive voltage be $V_{gsn}-V_{tn} = |V_{gsp}|-|V_{tp}| = V_{ov}$.





For NMOS input, we need

$V_{EB2} > V_{tn} + 2V_{ov}$

V_{EB2} ranges from 0.5V to 0.7V

$\Rightarrow V_{tn} < 0.2V$

$\Rightarrow$ too tough to be satisfied

For PMOS input, we need

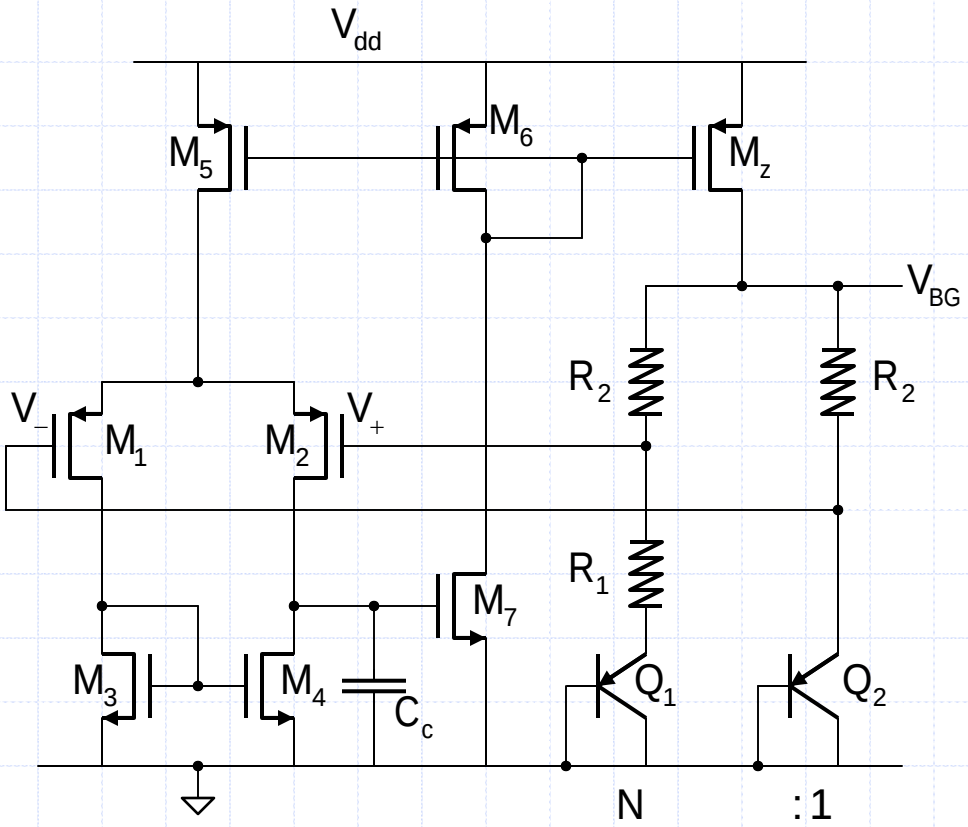
$V_{dd} > V_{EB2} + |V_{tp}| + 2V_{ov}$

For V_{EB}=0.64V, $|V_{tp}|$=0.44V, V_{ov}=0.15V

$\Rightarrow V_{dd}(min) = 1.38V.$

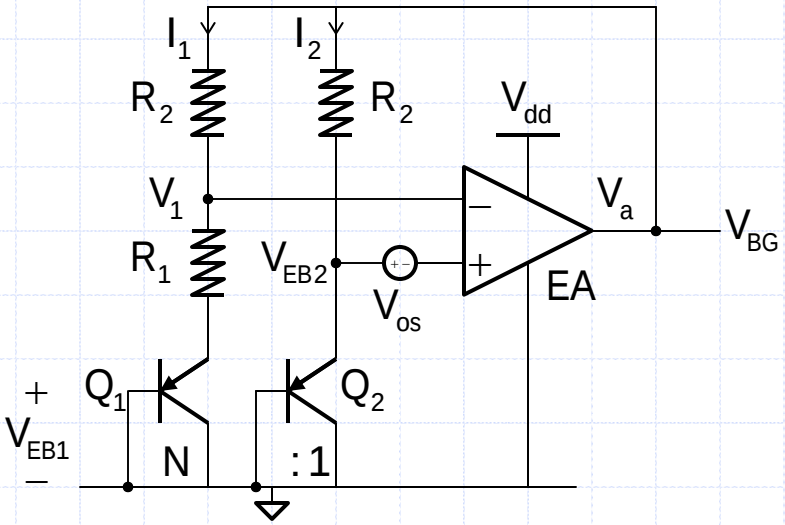
OP BGR: Example

The OP BGR could be implemented by a 2-stage op-amp with a self-biasing scheme, and it resembles the CM BGR to be discussed in terms of feedback connections. Note that a start-up circuit is needed.



OP BGR: Offset Error

For a bipolar op-amp, the offset voltage could be as low as 1mV, while for a CMOS op-amp, the offset voltage could be a few mV.



By accounting for V_{os}, it can be shown that [Song 83]

$$V_{BG} = V_{EB2} + \frac{R_2}{R_1}\ln(N)V_T - \left(1 + \frac{R_2}{R_1}\right)V_{os}$$

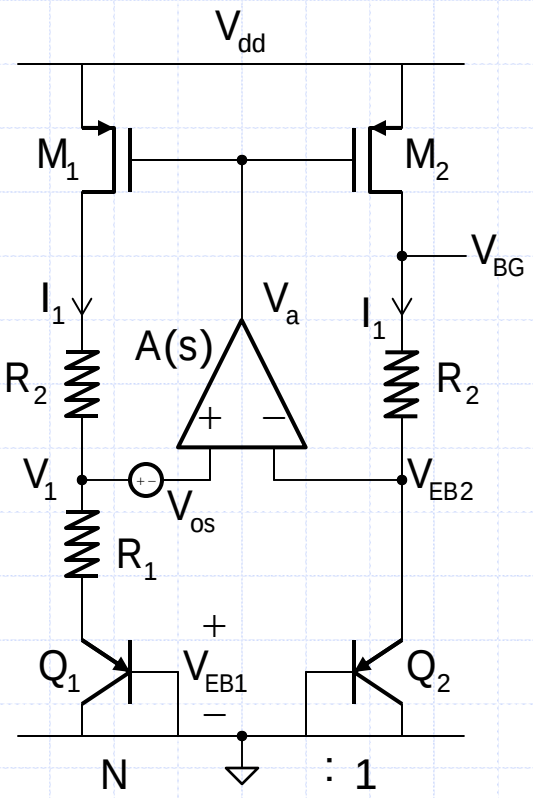
CM BGR: Offset Error

The op amp may drive a current mirror instead of the resistors directly [Gregorian 81]. The BGR is thus called the current-mirror BGR (CM BGR). The current mirror forces the drain currents of M_1 and M_2 to be equal, and

$$V_{BG} = V_{EB2} + \frac{R_2}{R_1}\ln(N) \times V_T + \frac{R_2}{R_1} \times V_{os}$$

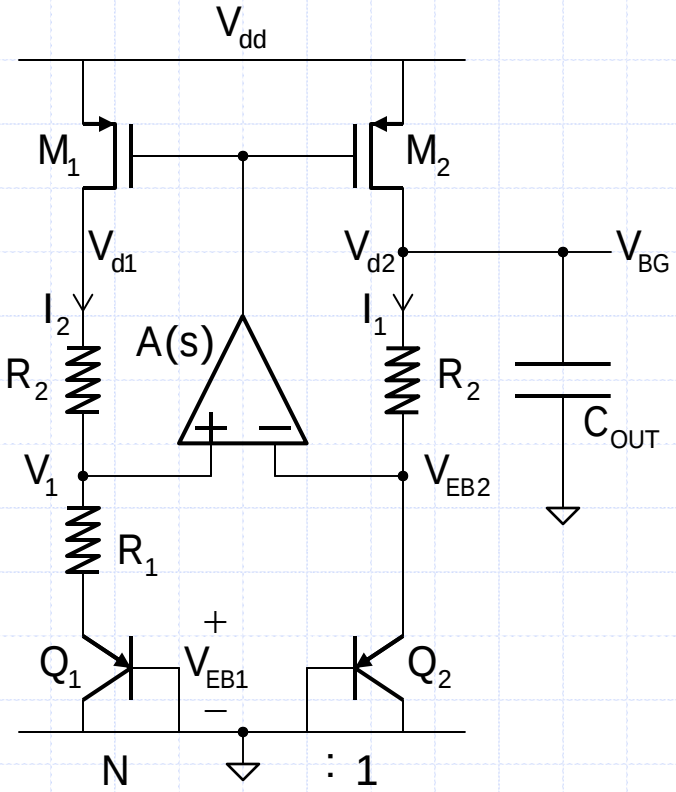
Hence, the effect due to V_{os} is smaller and opposite to that of the OP BGR.

In principle, R_2 at M_1 may be eliminated to save a resistor, but channel length modulation of M_1 and M_2 affects accuracy.



T_+ and T_- of CM BGR

Note that V_{d1} and V_{d2} generate the same reference voltage, but the reference output should be taken at V_{d2}, because with the filtering capacitor C_{OUT}, the positive feedback loop then has an even lower gain at high frequencies, satisfying $|T_-(j\omega)| > |T_+(j\omega)|$.



With a PMOS input stage, and

$V_{EB2} = 0.64V$

$|V_{tp}| = 0.44V$

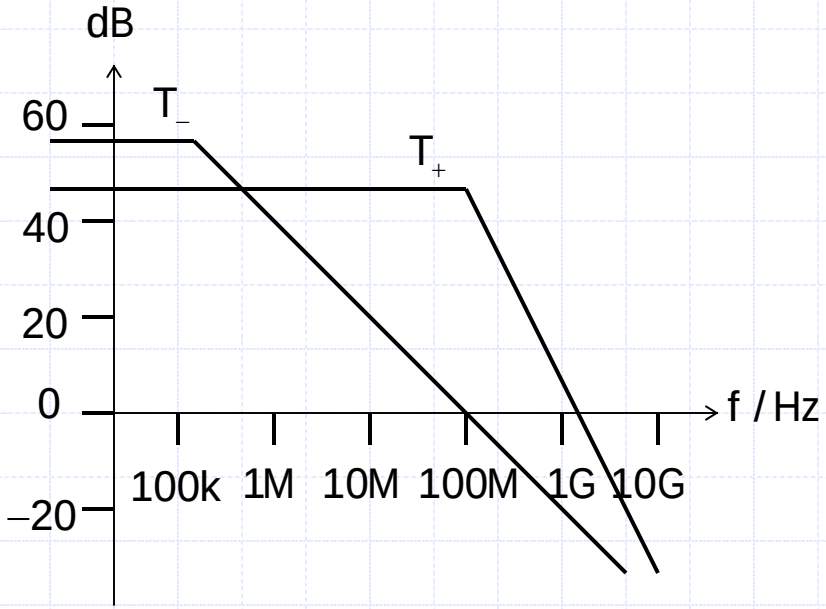
$V_{ov} = 0.15V$

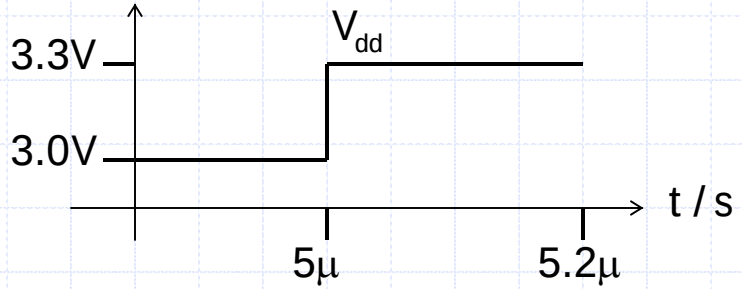
The minimum V_{dd} is thus

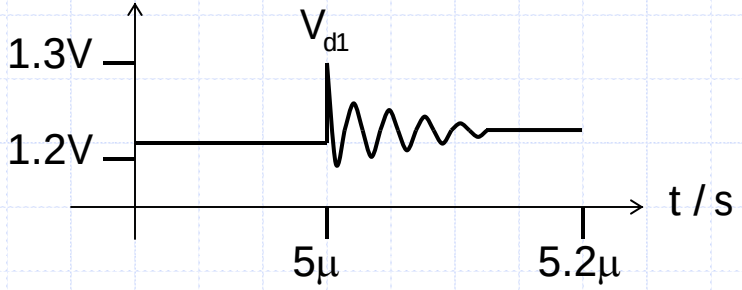
$V_{dd}(min) = V_{BE2} + |V_{tp}| + 2V_{ov} = 1.38V$

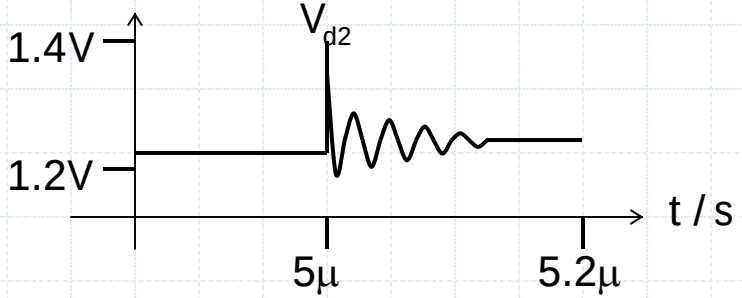
CM BGR: Line Transient with cap. at V_{d1}

If C_{OUT} is connected at V_{d1}, then $|T_+(j\omega)| > |T_-(j\omega)|$ at high frequencies, making the BGR unstable.



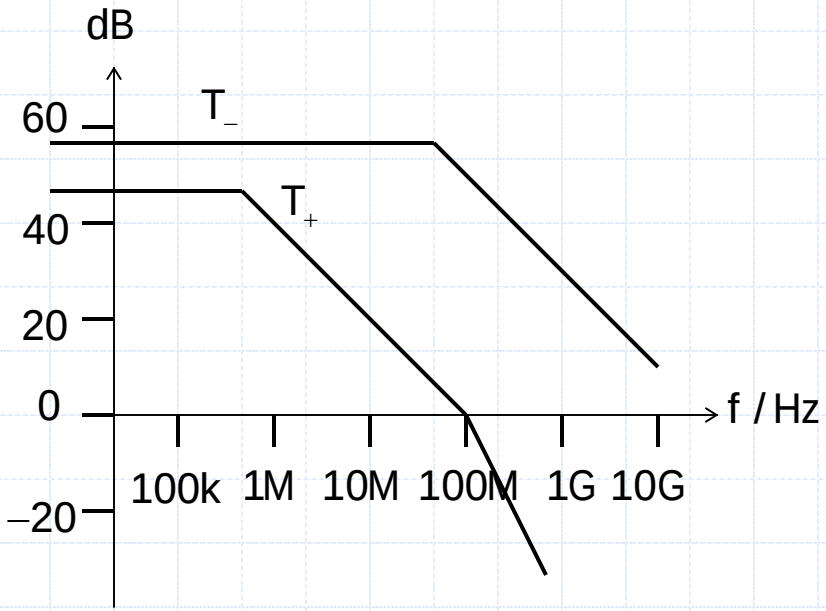


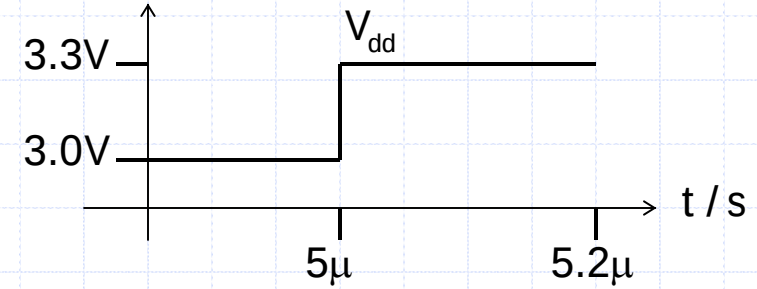


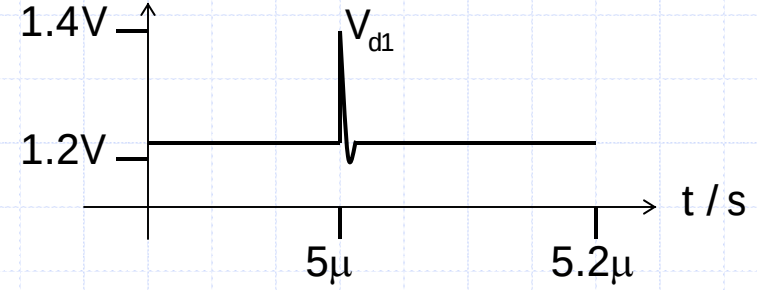


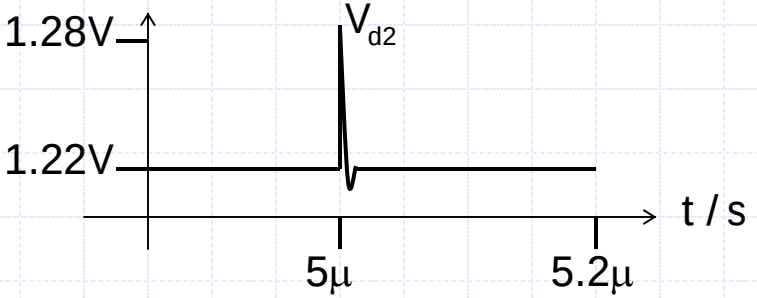
CM BGR: Line Transient with cap. at V_{d2}

If C_{OUT} is connected at V_{d2}, then $|T_+(j\omega)| < |T_-(j\omega)|$ for all frequencies, and the BGR is stable.



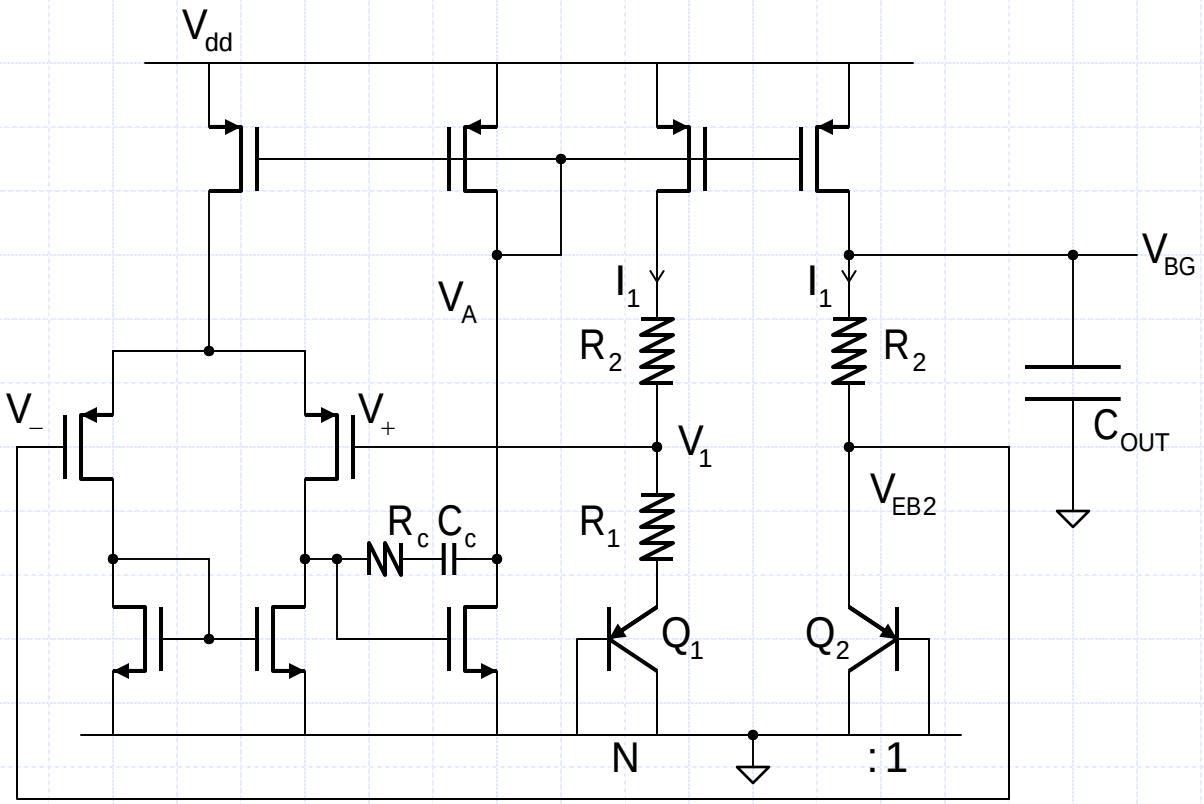






CM BGR with PMOS Input

A 2-stage op amp could be used, and biased by the PTAT circuit.



CM BGR: Performance Summary

Parameter	Computation	Simulation BSIM 3
R_1	12kΩ	12kΩ
R_2	133.9kΩ	123.1kΩ
R_T	279.8kΩ	258.2kΩ
I_{pnp}	4.75μA	4.75μA
I_{op}	9.5μA	9.5μA
I_{total}	19μA	19μA
C_c		200fF
V_{dd}(min)	1.38V	1.5V
V_{BG} (V_{dd}=1.7V)		1.2757V
TC	6ppm/^{o}C	7.26ppm/^{o}C
PSR		79dB
Line regulation		+0.12mV/V

BGR with Folded Resistor: FR BGR

In [Neuteboom 97], the resistors R_2 is folded down to decrease the requirement of V_{dd}, using a special process. With $I_1=I_2=I_3$:

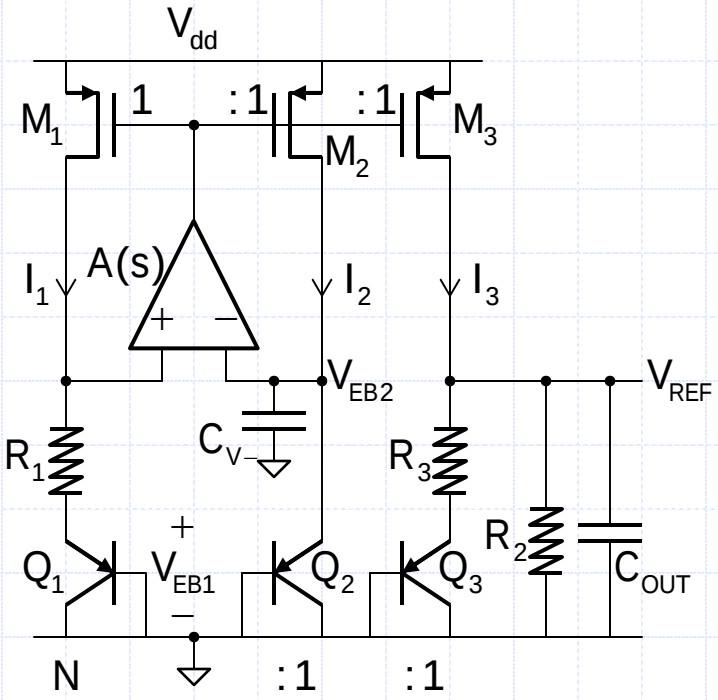
$$I_3 = \frac{V_T \ln(N)}{R_1} = \frac{V_{REF}}{R_2} + \frac{V_{REF} - V_{EB3}}{R_3}$$

$$\Rightarrow \quad \frac{V_{REF}}{R_2} + \frac{V_{REF}}{R_3} = \frac{V_{EB3}}{R_3} + \frac{V_T \ln(N)}{R_1}$$

$$\Rightarrow \quad V_{REF} = \frac{R_2}{R_2 + R_3}\left(V_{EB3} + \frac{R_3}{R_1} \ln(N) V_T \right)$$

For $R_2 = R_3$, then $R_T = R_1 + 2R_2$, and

$$V_{REF} = \frac{1}{2}\left(V_{EB3} + \frac{R_2}{R_1} \ln(N) V_T \right)$$



Using a normal process, $V_{dd(min)}$ is still $V_{EB2}+|V_{tp}|+2V_{ov}$.

BGR with Symmetrical Folded Resistors: SFR BGR

In [Banba 99], both branches of R_2 are folded down to generate a zero-TC current I_3. With $I_1=I_2=I_3$:

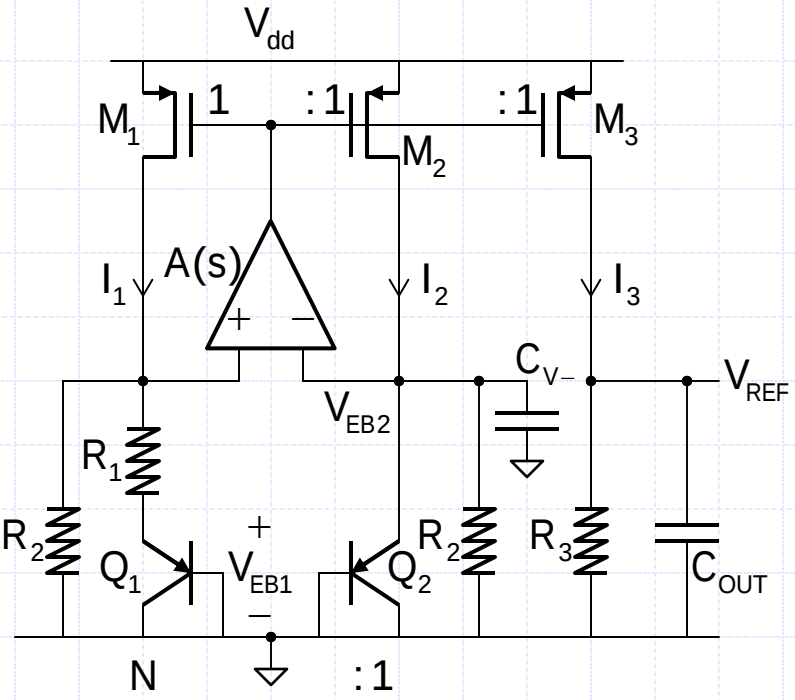
$$I_1 = \frac{V_{EB2}}{R_2} + I_{R_1}$$

$$\Rightarrow \quad I_1 = \frac{V_{EB2}}{R_2} + \frac{V_T \ln(N)}{R_1}$$

$$\Rightarrow \quad V_{REF} = \frac{R_3}{R_2}\left(V_{EB2} + \frac{R_2}{R_1}\ln(N) V_T \right)$$

For $R_3 = R_2/2$, $R_T = R_1 + 2½R_2$, and

$$V_{REF} = \frac{1}{2}\left(V_{EB2} + \frac{R_2}{R_1}\ln(N) V_T \right)$$



FR BGR and SFR BGR with Sub-1V Operation

In [Neuteboom 97], the 0.8μ process has $|V_{tp}|$=-0.7V and V_{tn}=0.5V. Due to low V_{tn}, the op amp has an NMOS input stage, and

$$V_{dd}(min) = V_{REF} + V_{ov}$$

For V_{REF}=670mV, the BGR works at V_{dd}=0.9V or lower.

In [Banba 99], the 0.4μ n-well process has $|V_{tp}|$=-1V, V_{tn}=0.7V, and native NMOS with $V_{tn(native)}$=-0.2V. The op amp uses a native NMOS input stage, and

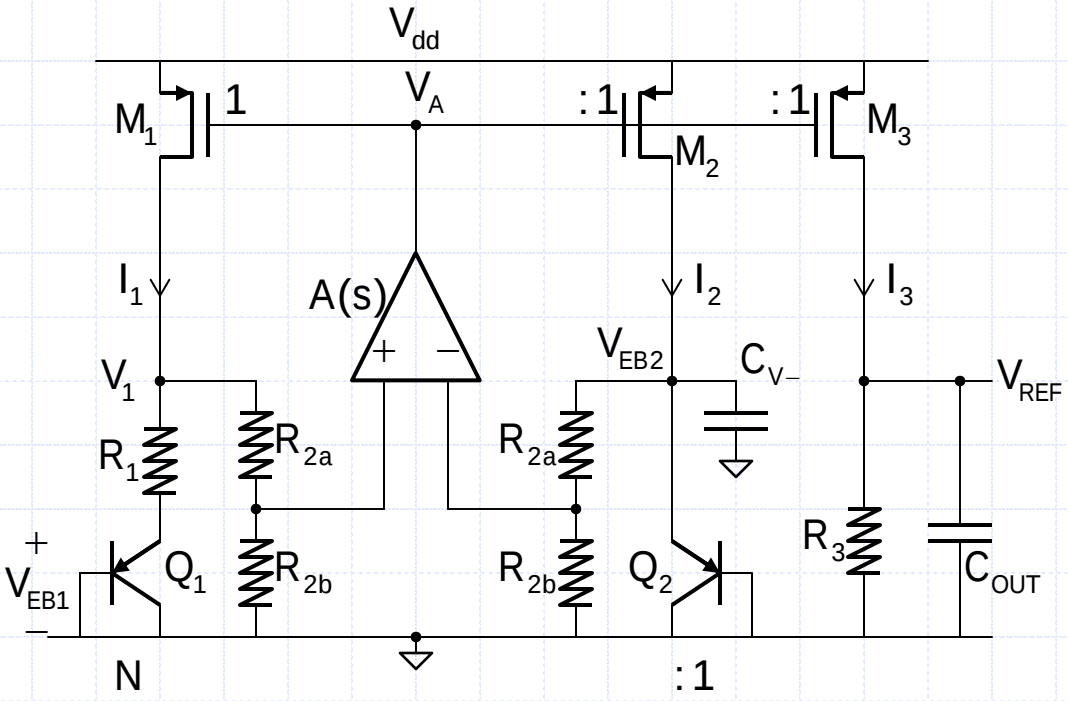
$$V_{dd}(min) = V_{REF} + V_{ov}$$

For V_{REF}=515mV, the simulated lowest V_{dd} is 0.84V. However, all measurements in [Banba 99] used V_{dd} are larger than 2.4V.

BGR with Folded Resistor Dividers: FRD BGR

By using resistor dividers for R_2 in [Banba 99], the V_{dd} requirement can truly be reduced [Leung 02], without using low V_{tn} for NMOS. With $b = R_{2b}/(R_{2a}+R_{2b})$, then

$$V_{dd}(\min) = bV_{EB2} + |V_{tp}| + 2V_{ov}$$



SFR/FRD BGR: Performance Summary

Parameter	SFR BGR	FDR BGR
R_1	25kΩ	25kΩ
R_2	269.4kΩ	268.5kΩ (b=0.6)
R_3	126kΩ	125.5kΩ
R_T	689.8kΩ	687.5kΩ
I_{pnp}	4.75μA	4.75μA
C_{VBE2}	5pF	5pF
C_c / R_c	60fF / 12kΩ	60fF / 12kΩ
I_{total}	24.25μA	24.25μA
V_{dd}(min)	1.4V	1.2V
V_{BG}	0.6015V	0.6003V
TC	4.32ppm/^{o}C (V_{dd}=1.8V)	6.1ppm/^{o}C (V_{dd}=1.5V)
PSR	84.7dB	96.5dB
Line reg.	-0.12mV/V	-0.12mV/V

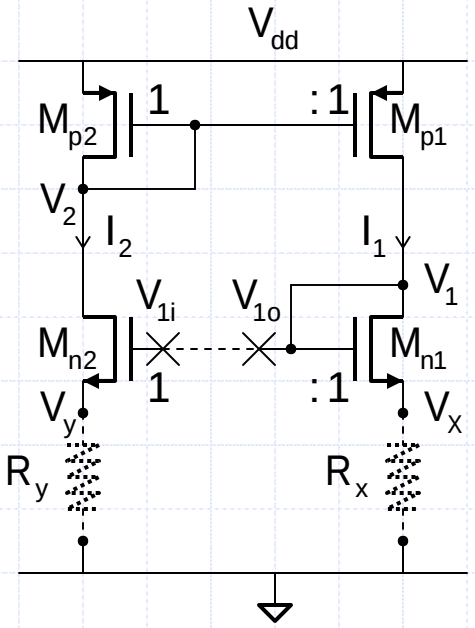
Cross-Biased 4T Cell

PTAT loop is realized by forcing $V_{EB1}+I_1R_1$ $(=V_y)$ = V_{EB2} $(=V_x)$. The previous BGRs use an op-amp, but we may use a "voltage mirror" instead. The cross-biased 4T cell with the PMOS side connected to V_{dd} is such a voltage mirror.

A positive feedback loop is identified and the diode-connection must be at R_x with $R_x<R_y$ to maintain stability.

The loop gain is

$$T = -\frac{V_{1o}}{V_{1i}} = -\frac{1+g_{mn}R_x}{1+g_{mn}R_y}$$



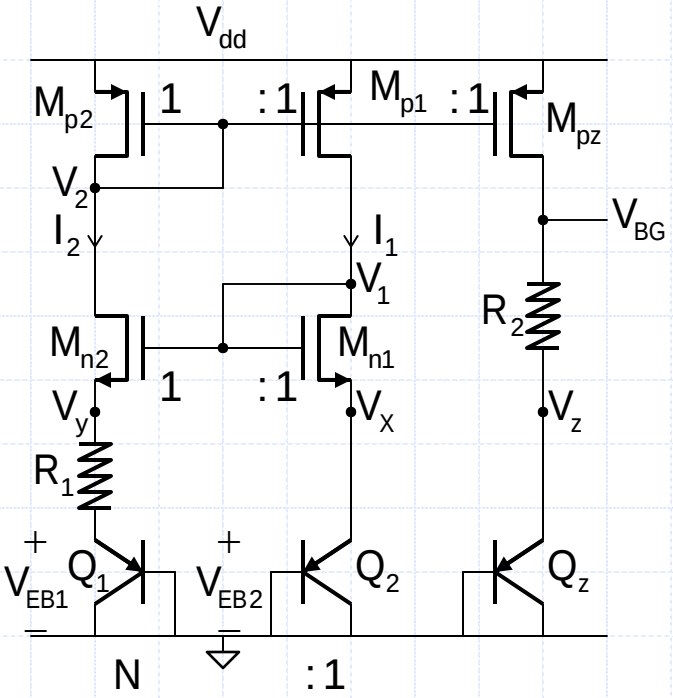
BGR with 4T Current-Voltage Mirror

The 4T current-voltage mirror (CVM) forces $V_y=V_x$, and Q_1, R_1 and Q_2 forms a PTAT loop with

$$I_1 = I_2 = \frac{V_T}{R_1}\ln(N)$$

The reference voltage is thus

$$V_{BG} = V_{EBZ} + \frac{R_2}{R_1}\ln(N) \times V_T$$



The loop gain of the 4T BGR is

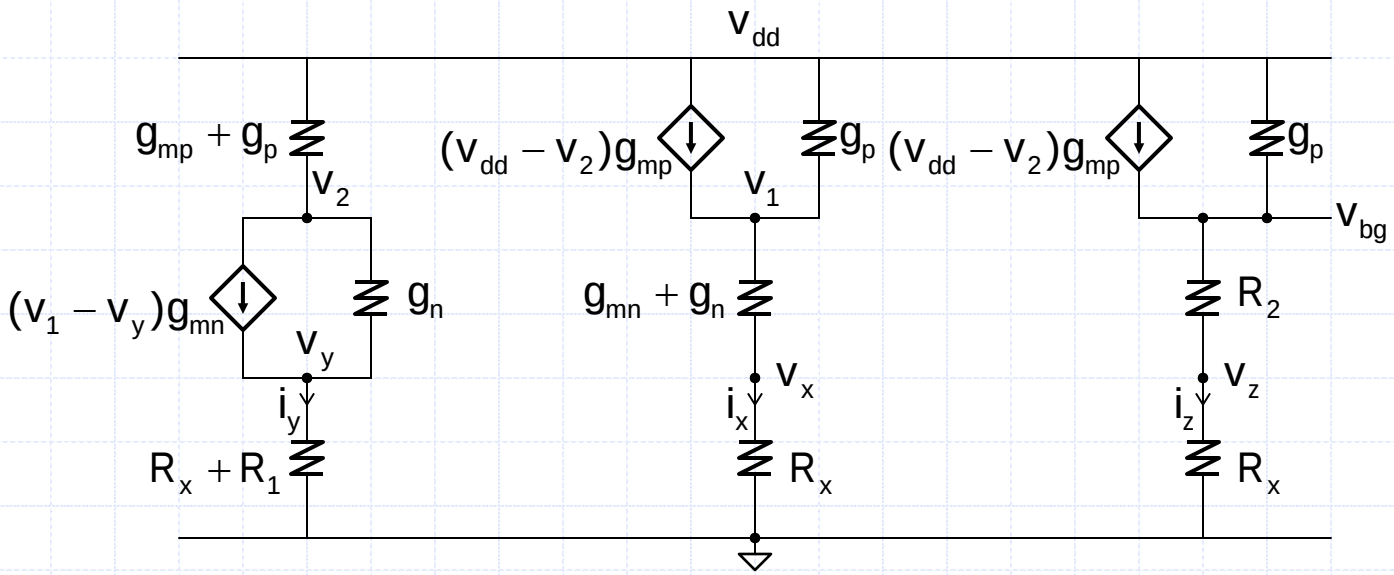
$$T = -\frac{V_{1o}}{V_{1i}} = -\frac{1+g_{mn}R_x}{1+g_{mn}(R_1+R_x)}$$

where $R_x=1/g_{mq}$, with g_{mq} the transconductance of all pnp transistors, and

$$V_{dd(min)} = V_{EB2}+V_{tn}+2V_{ov}$$

4T BGR: PSR Analysis

Small signal model for computing PSR of the 4T BGR:

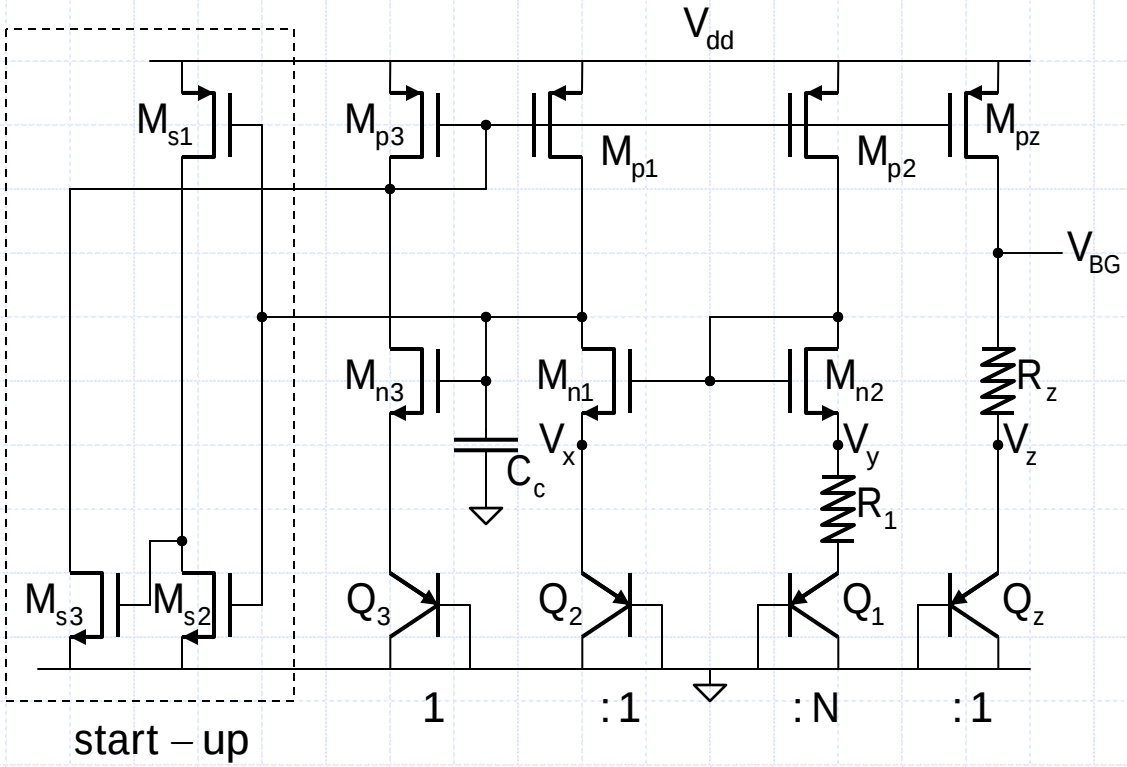


With appropriate approximation, and $r_{dsp}=1/g_p$, $r_{dsn}=1/g_n$, we arrive at

$$PSR=\frac{V_{bg}}{V_{dd}}=\frac{1+r_{dsp}/r_{dsn}+g_{mn}(R_x+R_1)}{g_{mn}R_1}\frac{(R_x+R_2)}{r_{dsp}}$$

4T SM BGR

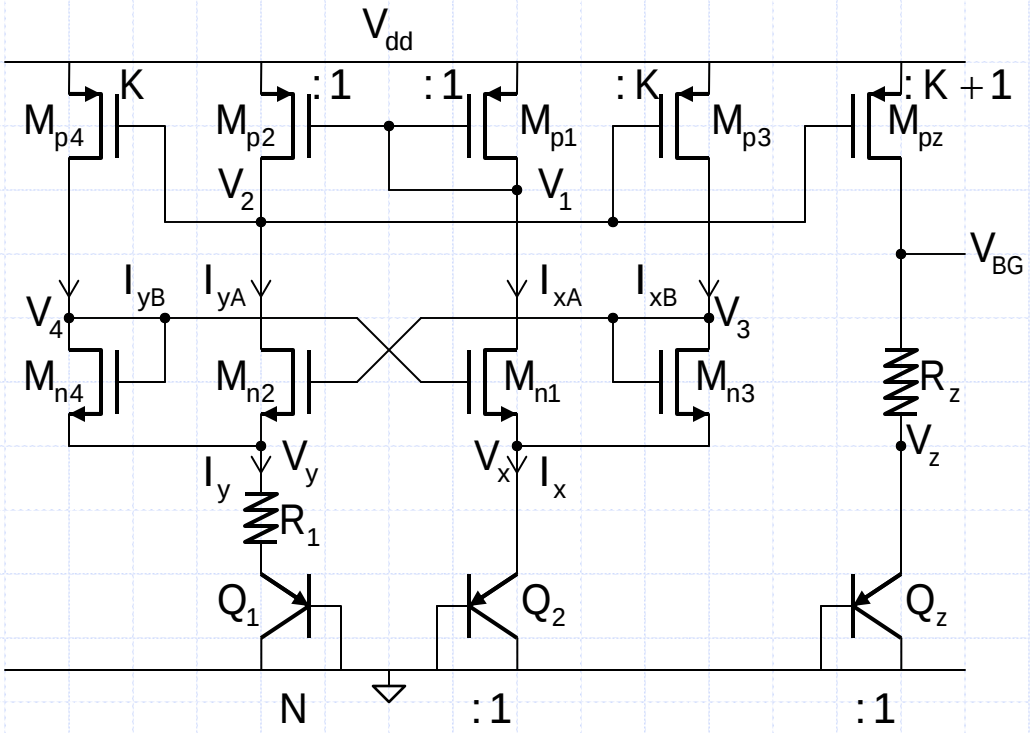
By adding the M_{n3} and M_{p3} branch, M_{n1} and M_{n2} are symmetrically matched. The diode-connection of NMOS is at Q_1 rather than at Q_2 to give negative feedback, and C_c is added for compensation [industry].



[industry]: circuit not published but used in the industry.

8T SM BGR

Another way to achieve symmetrical matching is to use an 8T SM CVM [Taylor 99]. A modified version is shown below [Lam 08]. For stability, we require K>1, and a suggested value is K=4.



8T SM BGR: Operation

When the PTAT loop is activated, the current I_X flows in Q_2 is equal to $I_{XA}+I_{XB}$.

The W/L ratio of M_{p1} and M_{p3} is 1:K, and I_{XB} is approximately equal to $K \times I_{XA}$ (M_{p1} and M_{p3} are not symmetrically matched).

To provide the correct gate drive for M_{p3}, the feedback action of the SM CVM drives V_2 to be essentially equal to V_1, such that the X branch is symmetrically matched to the Y branch.

Now, with V_{SG} of M_{p1} being equal to V_{SG} of M_{p2}, M_{p1} is then symmetrically matched to M_{p2}.

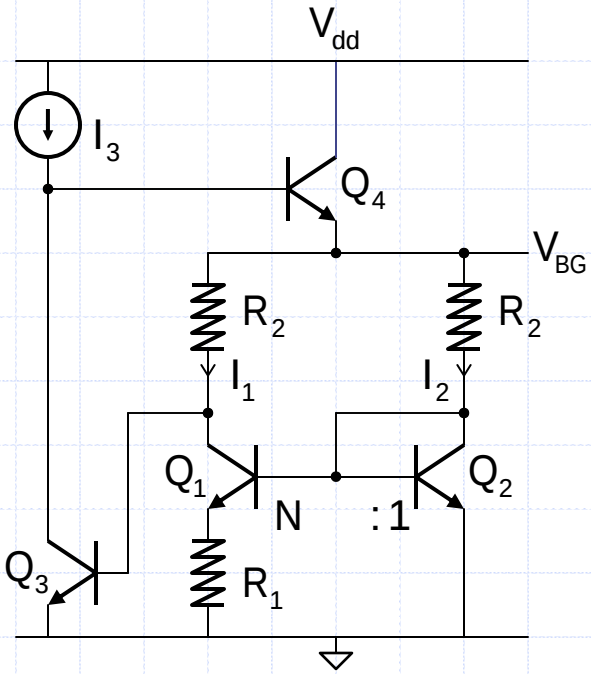
Arguing in a similar fashion, we conclude that all transistor pairs (M_{n1}, M_{n2}), (M_{p1}, M_{p2}), (M_{n3}, M_{n4}) and (M_{p3}, M_{p4}) are symmetrically matched and thus $V_Y=V_X$.

4T/8T BGRs: Performance Summary

Parameter	4T BGR	4T SM BGR	8T SM BGR
R_1	12kΩ	12kΩ	12kΩ
R_2 (R_1=12kΩ)	113.3kΩ	123.9kΩ	124.1kΩ
I_{pnp}	4.5μA	4.5μA	4.5μA
C_c	-	5pF	-
pnp	N+2	N+3	N+2
I_{total}	13.5μA	18μA	13.5μA
V_{dd}(min)	1.7V	1.8V	1.8V
V_{BG} (V_{dd}=2V)	1.2142V	1.2815V	1.2701V
TC	11.9ppm/°C	5.44ppm/°C	6.1ppm/°C
PSR	20dB	50.3dB	44.1dB
Line reg.	42.1mV/V	-4.9mV/V	-5.8mV/V

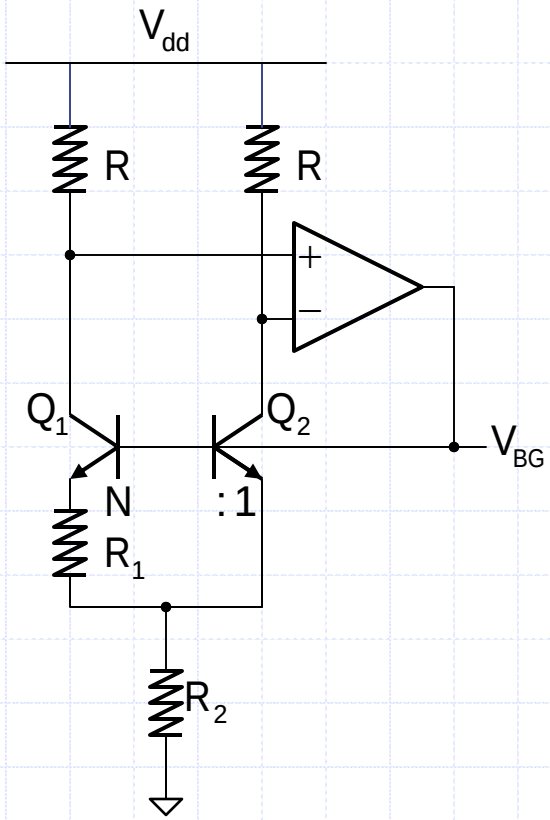
Modified Widlar BGR

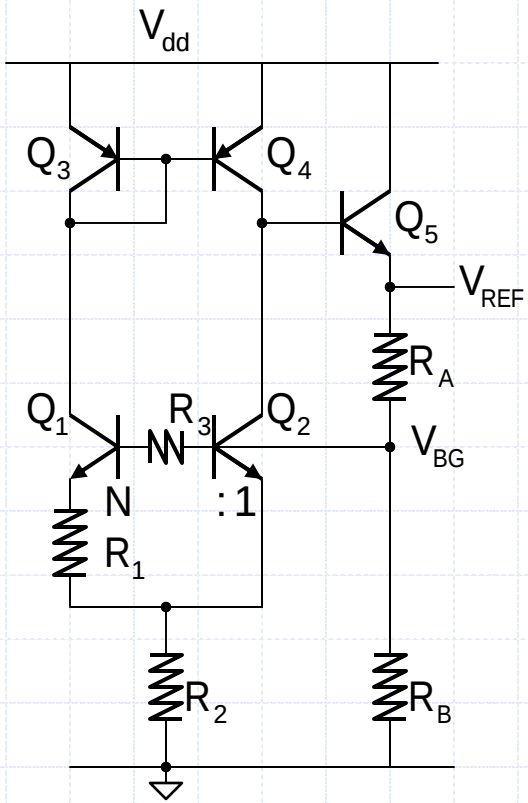
Widlar's original BGR [Widlar 71] has minor matching difficulties. A modified version with better matching is shown below [Gilbert 96].



Brokaw BGR (1)

The Brokaw BGR is a popular topology for BJT process [Brokaw 74], and its CMOS variant is discussed in [Vittoz 79].





To compensate for base current error, set

$$R_3 = \frac{R_1}{R_2}\frac{R_A R_B}{R_A + R_B}$$

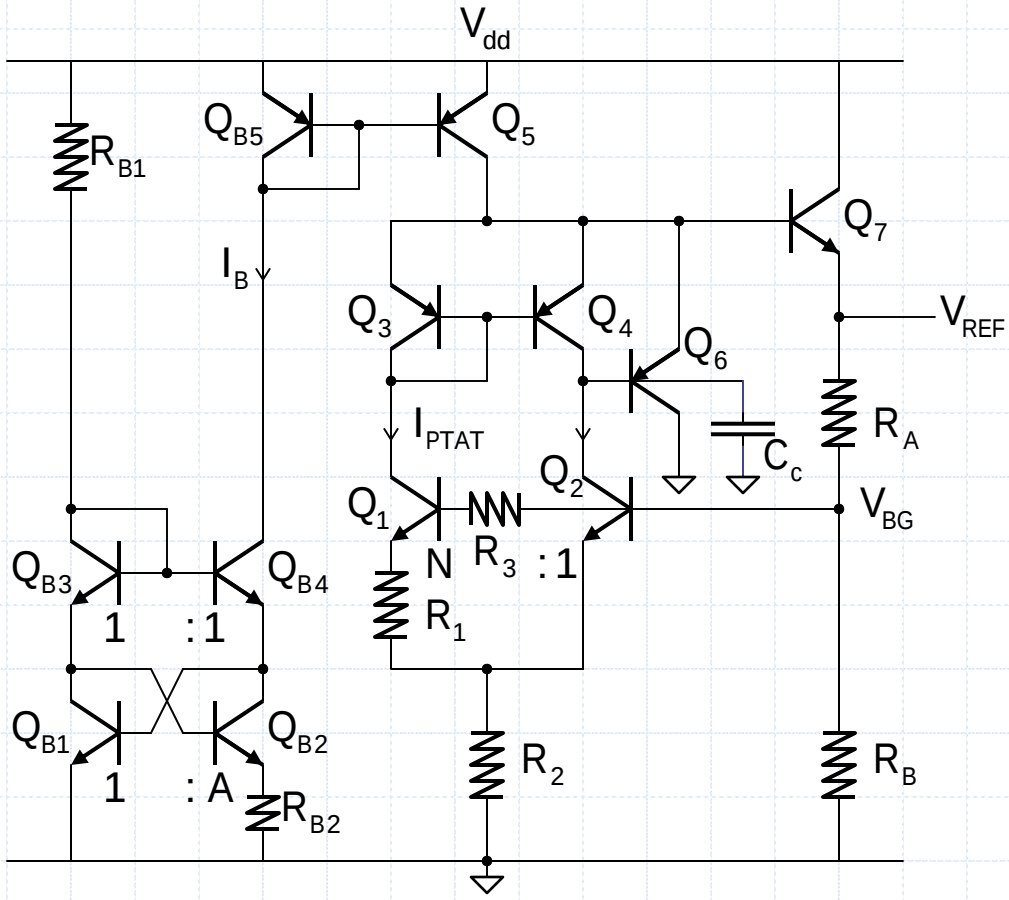
$$V_{BG} = V_{BE2} + 2\frac{R_2}{R_1}\ln(N)V_T$$

$$V_{REF} = \left(1 + \frac{R_A}{R_B}\right)V_{BG}$$

Brokaw BGR (2)

To achieve symmetrical matching between Q_3 and Q_4, Q_6 is added [Brokaw 74].

Q_{B1}, Q_{B2} and R_{B2} forms a PTAT loop to produce I_B, a PTAT current. Q_{B3} and Q_{B4} are used to minimize base current error. I_B is at least 3 times of I_{PTAT}, to supply enough base current to Q_7 to drive resistive load.



Start-Up Consideration

The basic BGR has two stable operation points:

(1) Normal mode with $V_{BG} \approx 1.2V$; and

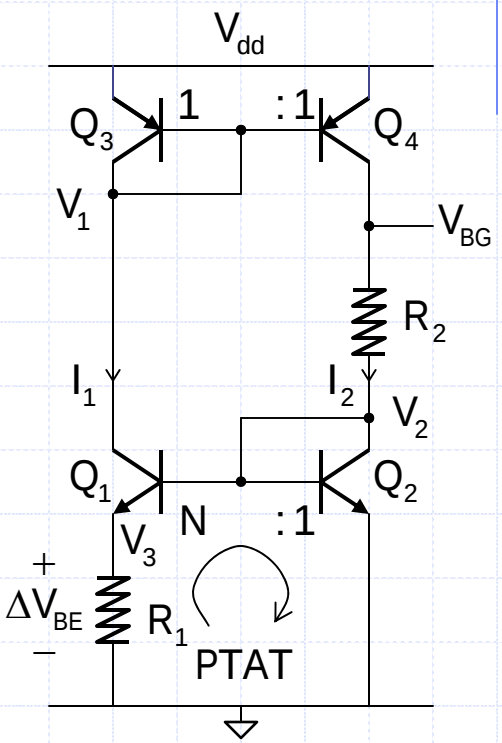
(2) Shutdown mode with $V_1 = V_{dd}$ and $V_2 = 0$.

A start-up circuit should

(1) automatically steer the BGR from the shutdown mode to the normal mode;

(2) disconnect from the BGR when it is working in the normal mode; and

(3) consume very little power.

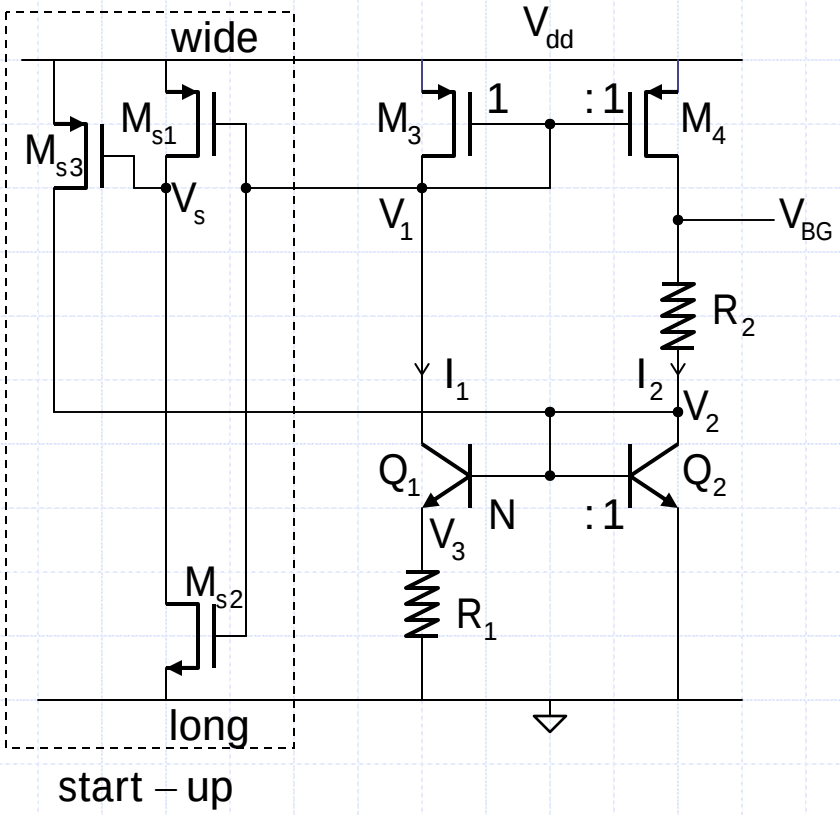


Basic BGR with CMOS Start-Up

Consider the 0.18μ CMOS process that supports bipolar transistors.

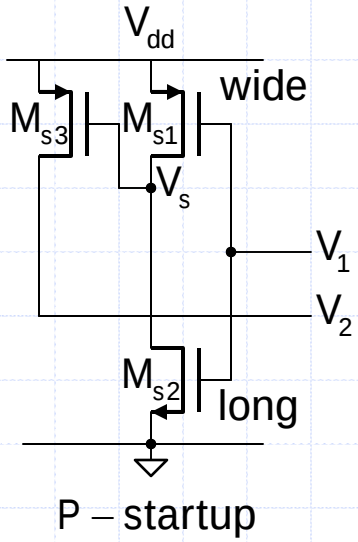
When BGR is shut down, $V_1 = V_{dd}$, M_{s1} is off and M_{s2} is on, such that V_s is low, turning on M_{s3} that pumps current to Q_2. Q_1 mirrors current to turn on M_3, and M_4 mirrors current and the BGR works properly.

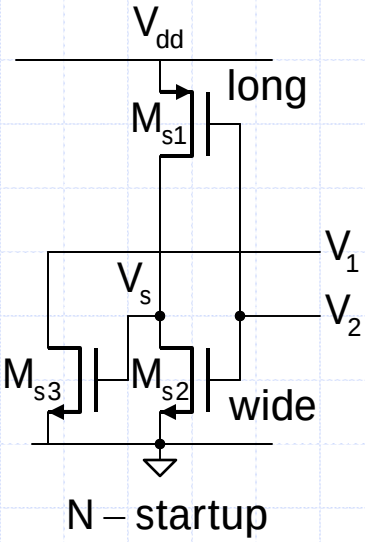
M_{s1} should be turned on hard by V_1, trying to source large current that puts itself into the linear region with a very small V_{sd1}, such that M_{s3} is shut off and isolated from the BGR.



CMOS Start-Up Schemes

A start-up circuit is used to jumpstart the main circuit, and V_1 and V_2 are the normal operating voltages of the main circuit. The basic BGR may only use the P-startup circuit. Note that V_2 is only 0.6V (at 27^{o}C) and may be too low to turn on M_{s2} of the N-startup circuit.





Both the P-startup and the N-startup circuits consume quiescent current, and M_{s2}(P-startup) and M_{s1}(N-startup) should be made long.

Trimming for Zero-TC

Consider the Brokaw BGR. The simulated BGR has zero-TC, giving, say, V_{BG}=1.263V at 25^{o}C, and R_A and R_B are adjusted to give, say, V_{REF}=2.50V. Due to inaccurate modeling and process variations, the fabricated BGR will have a different V_{REF} and large TC.

A very accurate V_{REF} will need to trim for both zero-TC and accurate initial value. The zero-TC point is determined by R_1:R_2, while the initial accuracy of V_{REF} (at room temp.) is determined by R_A:R_B.

Trimming individual BGR for zero-TC is too time consuming. In practice, the zero-TC point is determined by fabricating and measuring the BGRs a few times using the same vendor and process. After finding the “optimal” ratio of R_1:R_2, this is then fixed for mass production and individual BGR will only be trimmed for initial accuracy.

Trimming for Initial Accuracy

For V_{REF}=2.50V±1% over T and V_{dd}, the initial accuracy should be V_{REF} = 2.50V±0.25% by trimming R_B. The LSB of 0.25% is 6.25mV, and for 4-bit trimming, the trimming range is ≈±50mV.

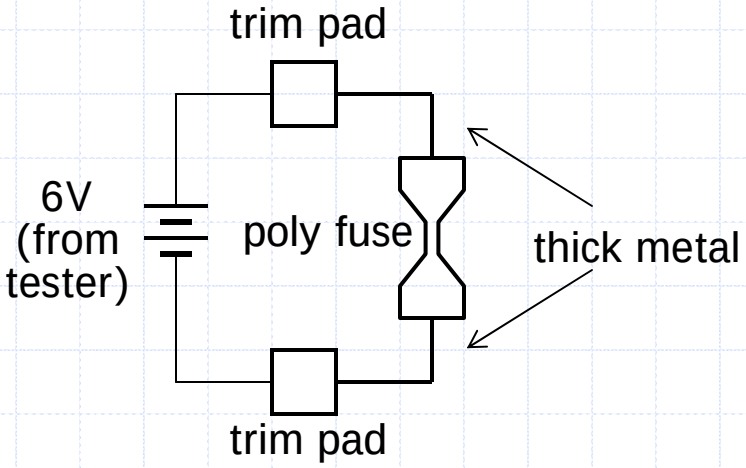
Let I_{REF}=5μA, such that R_A=247.4kΩ and R_B=252.6kΩ±10kΩ. R_B is divided into R_{B1}=242.6kΩ and R_{B2}=18.75kΩ. R_{B2} consists of 4 smaller resistors of 1.25kΩ (LSB), 2.5kΩ, 5kΩ and 10kΩ (MSB) that are connected in parallel with poly fuses (≈100Ω).

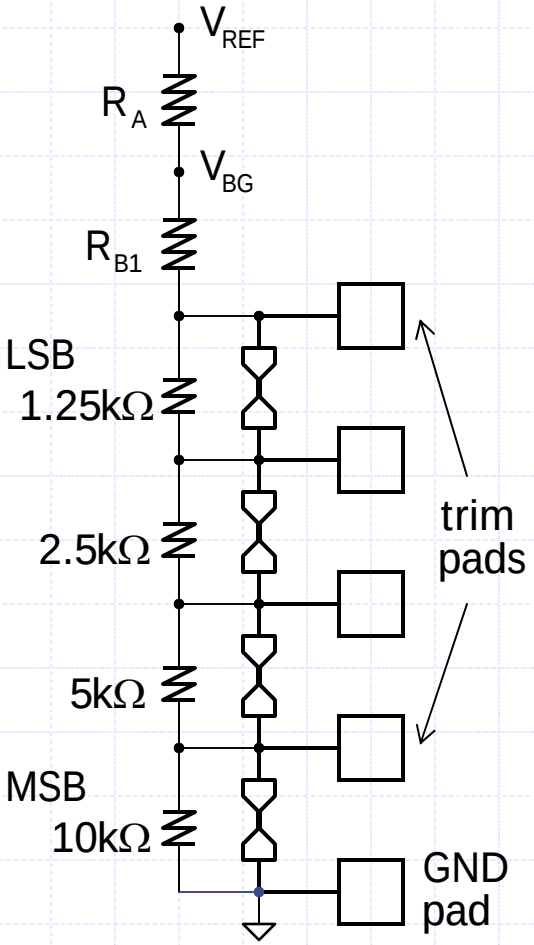
If the fabricated BGR behaves as designed, only 1 fuse (MSB fuse) is needed to be blown open. Otherwise, the BGR could still be trimmed up and down +43.75mV/-50mV.

Trimming Circuit

Trimming is usually done during wafer testing. A poly fuse of around 100Ω needs 60mA to be blown open.

For $R_{LSB} >> R_{poly}$: blow fuse to trim up.

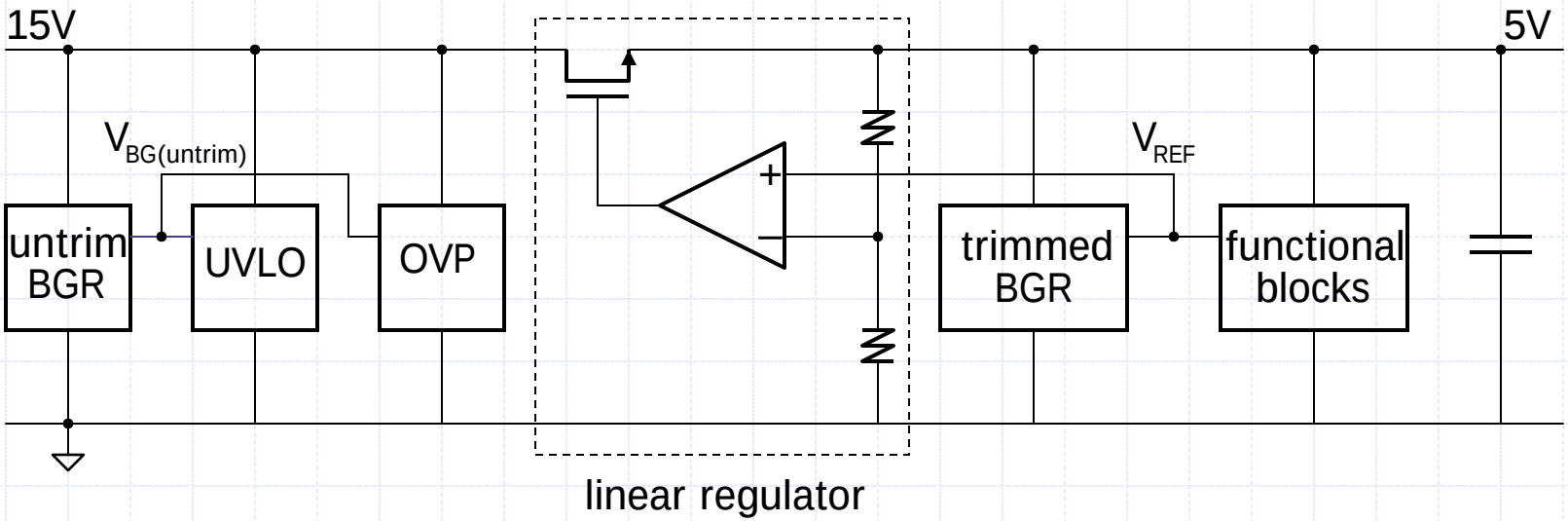




Organization of BGRs in IC Systems

For a low-voltage system, e.g., V_{dd}=5V, there is usually only one trimmed voltage reference.

For a system with V_{dd}=15V, there are usually two voltage references, one trimmed for accuracy, and a second one untrimmed and could work at very low voltage for start-up, UVLO (under voltage lockout) and OVP (over voltage protection).



References: Books / Thesis

Books / Book Chapters / Thesis:

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IC Design of Power Management Circuits (V)

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International Symposium on Integrated Circuits
Singapore, Dec. 14, 2009

Part V

Development of Integrated Charge Pumps

Foreword

The first AC-DC switched-capacitor power converters (charge pumps) were invented in the 1930's, while DC-DC charge pumps found many applications in recent years. After seventy years of research and development, the study is still not systematic and not standardized. My study on AC-DC and DC-DC charge pumps suggests the following four areas of attention:

- Analysis
- Topology
- Gate Control
- Regulation

A comprehensive review of the development of charge pumps would definitely include the works from all over the world. However, due to limited time, I could only concentrate on the research efforts at HKUST, and in particular, my own research. I hope I could write up a better account in the future.

Content

AC-DC and DC-DC Charge Pumps
Step-Up, Step-Down, and Inverting Charge Pumps
Single-Branch and Dual-Branch Charge Pumps

Linear (Dickson) Charge Pumps
Fibonacci (Ueno) Charge Pumps
Exponential Charge Pumps
2N-X Charge Pumps

2-Phase Charge Pumps
- Gate Control Strategies
- ANTZ Topological Tree

Multi-Phase Charge Pumps

Regulated Charge Pumps

Switched-Capacitor Power Converters

Qn.

What is a switched-capacitor power converter (SCPC)?

Ans:

An SCPC converts an input power source to an output voltage that supplies power to a load, with power transfer components that consists of only switches and capacitors.

Currently, there are more step-up SCPCs than step-down SCPCs, and hence an SCPC is better known as a Charge Pump (QP).

Classification of Charge Pumps

A major classification of charge pumps is according to input:

AC-DC charge pumps
DC-DC charge pumps

In this talk, the focus is on DC-DC charge pumps. In particular, integrated step-up charge pumps.

Classifications of DC-DC Charge Pumps

According to output vs input (with $V_s > 0$):

- $V_o > V_s$: step-up charge pumps
- $V_o < V_s$: step-down charge pumps
- $V_o < 0$: inverting charge pumps

According to conversion ratio:

- Linear charge pumps (Dickson charge pumps)
- Fibonacci charge pumps (Ueno charge pumps)
- Exponential charge pumps (2^N charge pumps)
- 2N-X charge pumps

According to ripple-reduction:

- Single-branch charge pumps
- Dual-branch charge pumps

According to phases:

- 2-phase charge pumps
- Multi-phase charge pumps

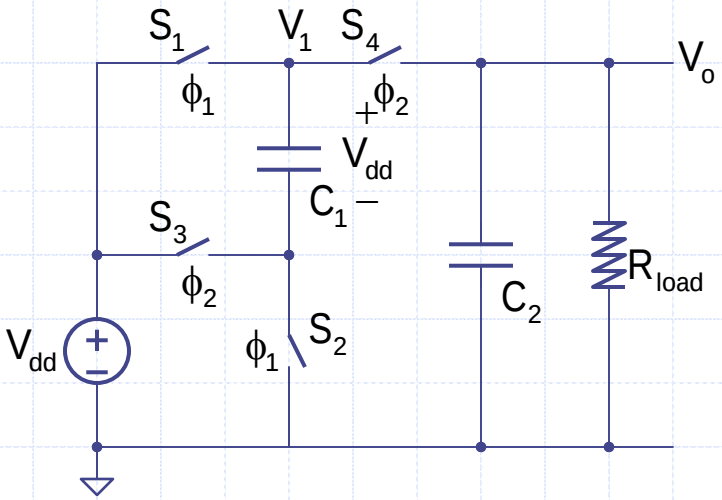
Step-Up Charge Pump

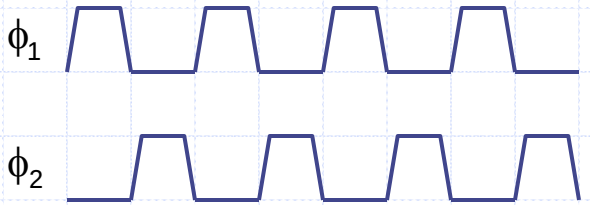
A voltage doubler (2X charge pump) is shown below.

Clock phases ϕ_1 and ϕ_2 are non-overlapping with appropriate voltages to switch on and off the switches completely.

When ϕ_1=1, C_1 is charged to V_{dd}.

When ϕ_2=1, C_1 sits on top of V_{dd}, and charges V_1 towards $2V_{dd}$.



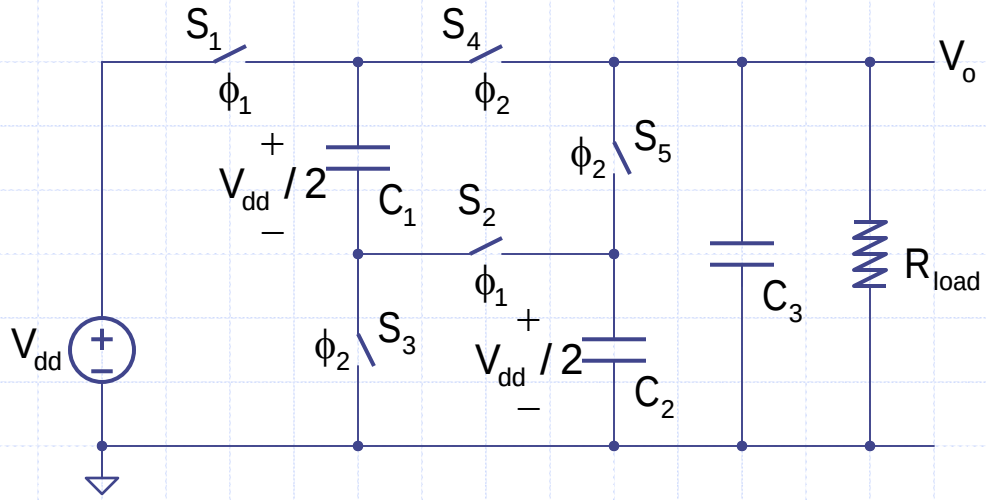


Step-Down Charge Pump

A voltage divider (divided by 2) is shown below.

When ϕ_1=1, C_1 and C_2 are charged in series to $V_{dd}/2$.

When ϕ_2=1, C_1 and C_2 are connected in parallel to charge V_o towards $V_{dd}/2$.

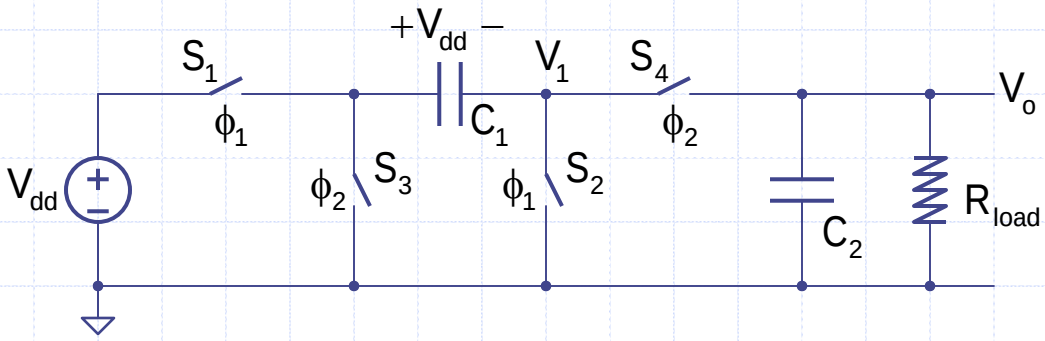


Inverting Charge Pump

An inverting charge pump is obtained by charging a capacitor in one direction and discharging it in the reverse direction.

When ϕ_1=1, C_1 is charged to V_{dd}.

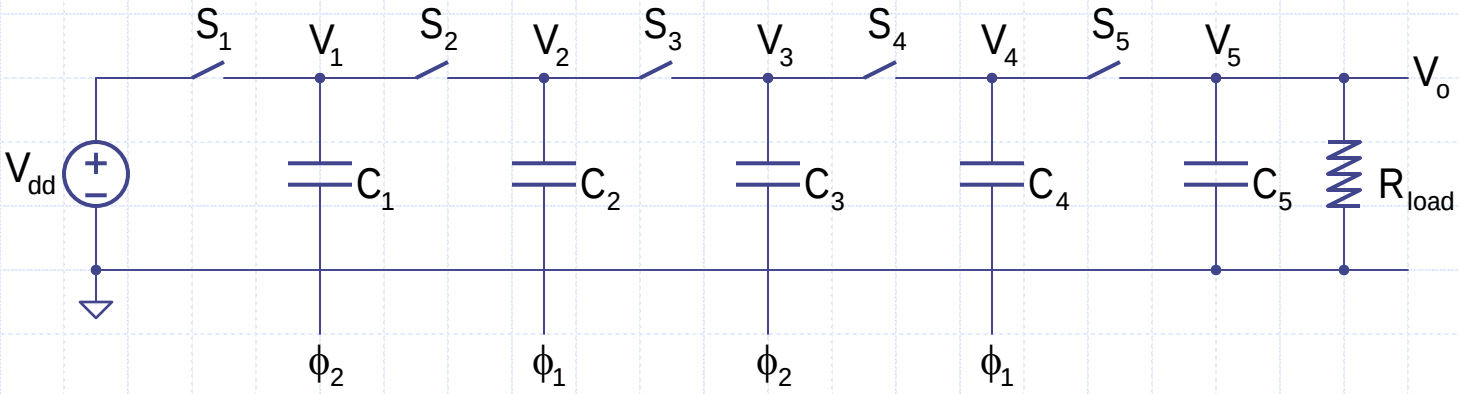
When ϕ_2=1, the “positive” plate of C_1 is connected to ground, and the “negative” plate charges V_o towards $-V_{dd}$.



Linear Charge Pump

Principle of operation (with ideal switches):
ϕ_1=1, (ϕ_2=0), C_1 is charged to V_{dd}.
ϕ_2=1, top of C_1 (V_1) is pushed to $2V_{dd}$, charging C_2 to $2V_{dd}$.
ϕ_1=1 again, top of C_2 (V_2) pushed to $2V_{dd}$, charging C_3 to $3V_{dd}$.
Similarly, V_o=V_5 is then $5V_{dd}$.

For N flying capacitors, the conversion ratio M = V_o/V_{dd} is N+1, and a linear charge pump (LQP) is obtained.

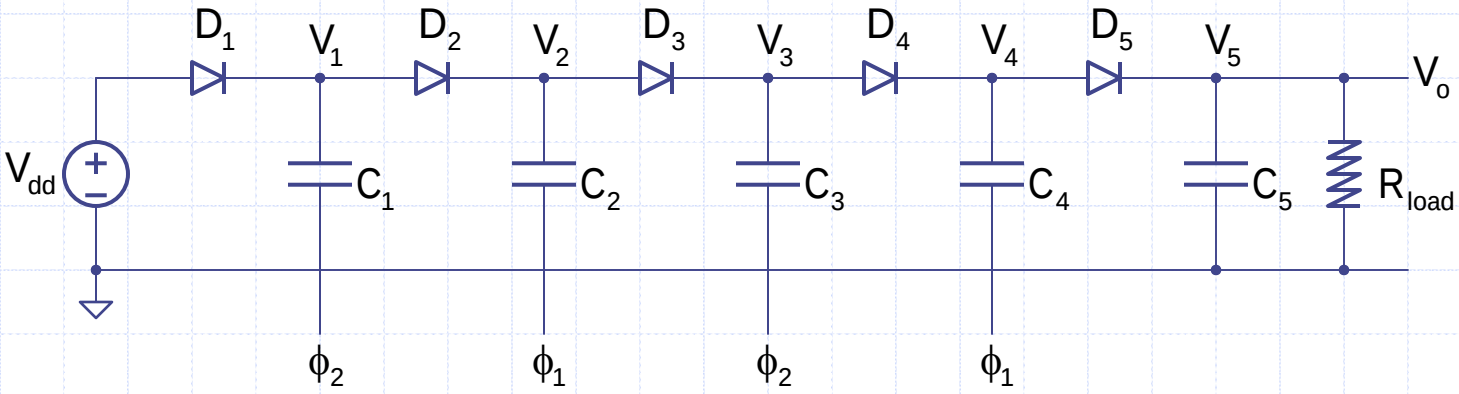


Dickson Charge Pump

The first integrated charge pump is a linear charge pump presented in [Dickson 76], and is commonly known as Dickson charge pump.

Accounting for the diode drop V_d:

$$V_o = (N+1)\times(V_{dd} - V_d).$$

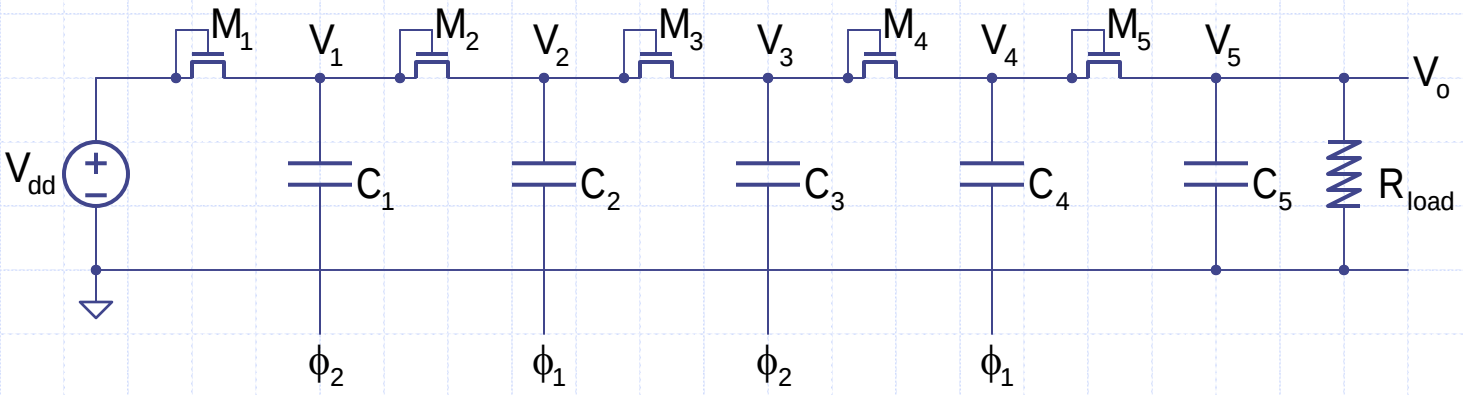


LQP with Diode-Connected Transistors

In [Dickson 76], in fact, diode-connected transistors are used, and

$$V_o = (N+1)\times(V_{dd} - V_{tn(k)}).$$

For an n-well process, the p substrate (p-sub) has to be connected to GND, and high stage switches M_k (k>1) have body effect, and $V_{tn(k+1)} > V_{tn(k)}$. Eventually, $V_{tn(k)} > V_{dd}$, and adding more stages could not increase the conversion ratio.

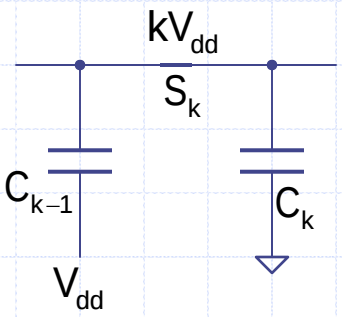


ON and OFF Conditions of a MOSFET

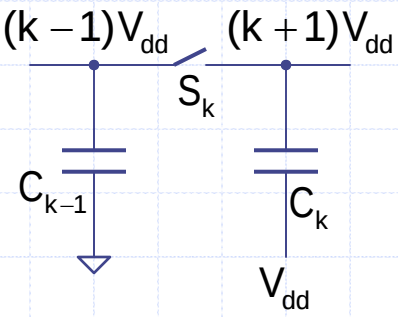
Qn. Can we design a charge pump with no loss due to V_d or V_{tn}?

Ans. Surely we can, but first we need to determine the conditions for turning on and off an MOS (power) switch completely [Su 05].

ON



OFF



Assume $V_{dd} > V_{tn}$, $|V_{tp}|$, and let V_{gk} be the gate voltage of S_k.

S_k is NMOS: turned on if $V_{gk} > (k+1)V_{dd}$; turned off if $V_{gk} < (k–1)V_{dd}$.

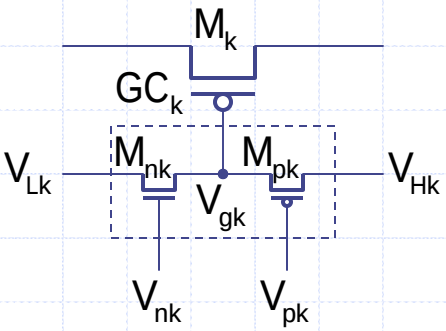
S_k is PMOS: turned on if $V_{gk} < (k–1)V_{dd}$; turned off if $V_{gk} > (k+1)V_{dd}$.

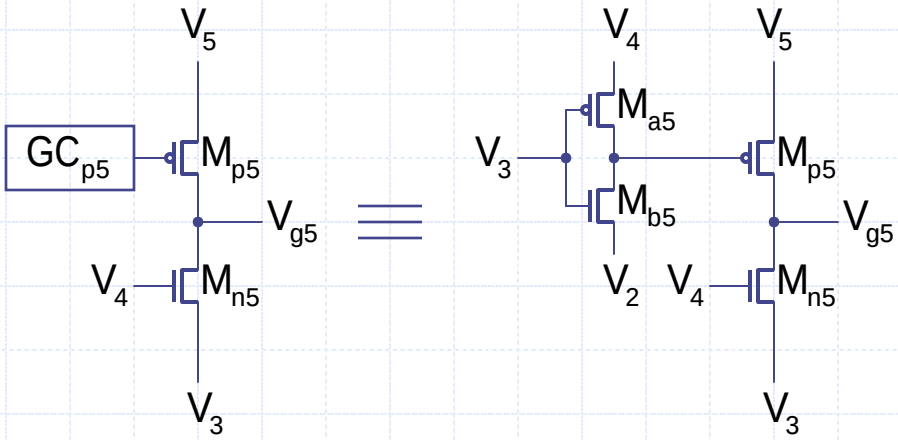
Gate Control Schemes

In [Su 05], a systematic study of gate control for both NMOS and PMOS power switches is presented. For the 5X LQP, S_5 has to be PMOS, and gate control circuits for PMOS are shown below.

First-level gate control: uses a PN pair to control the gate of M_k.

Second-level gate control: treats M_{pk} (or M_{nk}) as M_k, and generates GC_{pk} to drive M_k with a larger gate drive.





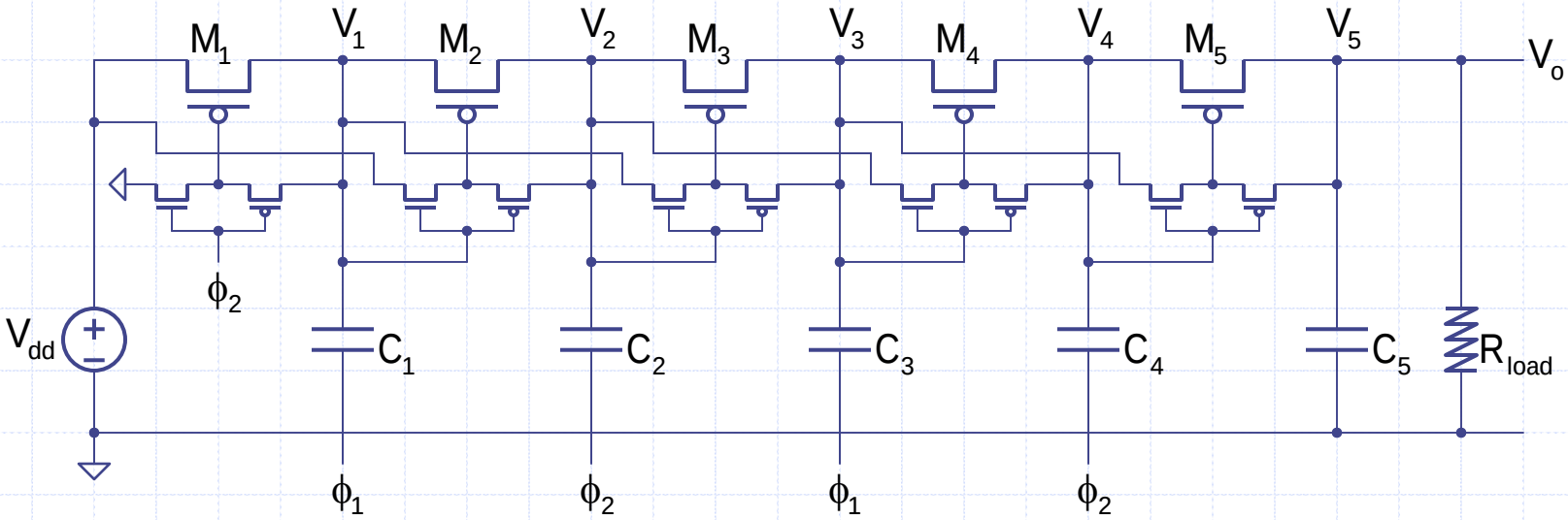
Gate Control Candidates

	(V_{Hk}, V_{pk})	(V_{nk}, V_{Lk})
GC_1	**(V_1, ϕ_2)**, (V_1, V_{dd}), (V_3, V_2), (V_5, V_4)	(V_{dd}, ϕ_1), (ϕ_2, ϕ_1), **$(\phi_2, 0)$**
GC_2	**(V_2, V_1)**, (V_4, V_3)	**(V_1, V_{dd})**, (V_1, ϕ_2), (V_{dd}, ϕ_2), (ϕ_1, ϕ_2), $(\phi_1, 0)$
GC_3	**(V_3, V_2)**, (V_5, V_4)	**(V_2, V_1)**, (V_{dd}, ϕ_1), (ϕ_2, ϕ_1), $(\phi_2, 0)$
GC_4	**(V_4, V_3)**	**(V_3, V_2)**, (V_1, V_{dd}), (V_1, ϕ_2), (V_{dd}, ϕ_2), (ϕ_1, ϕ_2), $(\phi_1, 0)$
GC_5	**(V_5, V_4)**	**(V_4, V_3)**, (V_2, V_1), (V_{dd}, ϕ_1), (ϕ_2, ϕ_1), $(\phi_2, 0)$

5X LQP w/o Drop Loss

The first LQP that completely eliminates (diode) drop loss is [Cheng 03] using the boldfaced options in the previous page. Only simulation was provided.

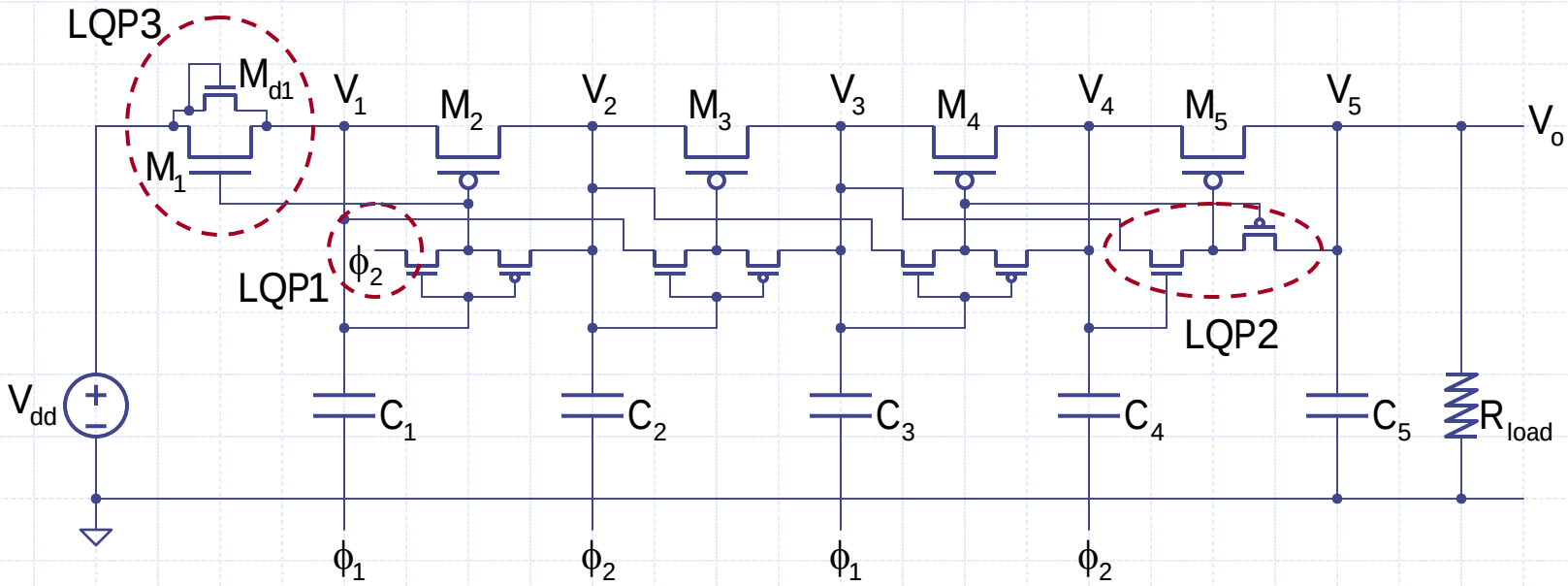
Implementation and measurement were finally realized in [Su 05] using the concept of first-level gate control. We labeled it LQP0.



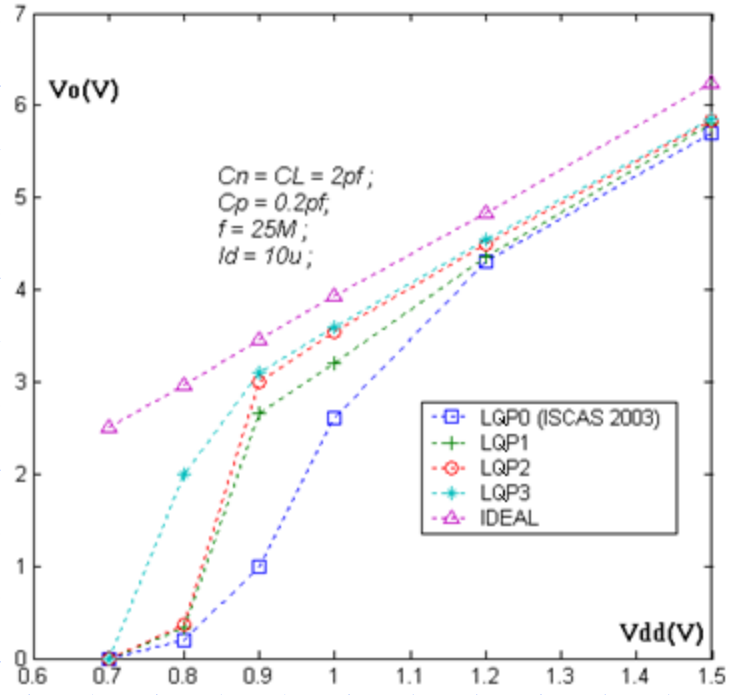
Improved 5X LQPs

The efficiency of LQP0 could be improved by increasing the gate drives of some transistors to $2V_{dd}$:

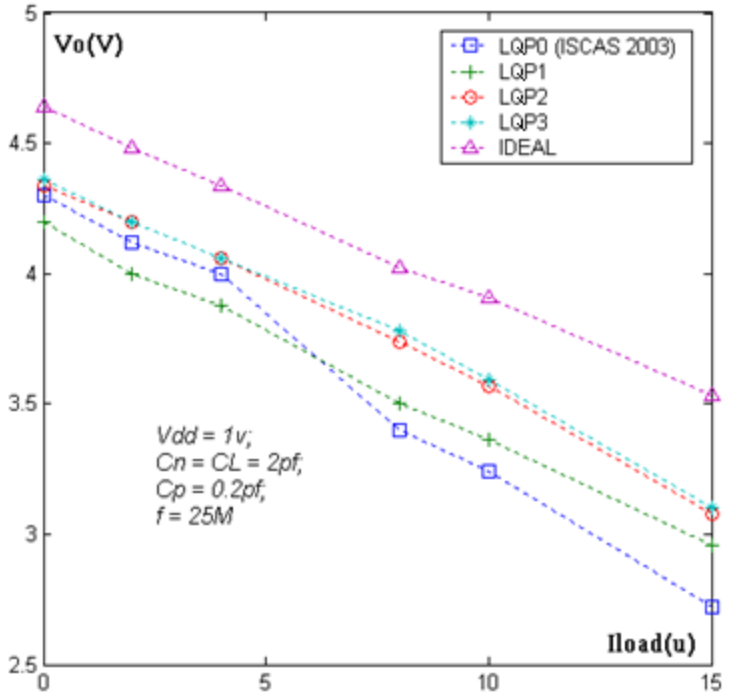
- LQP1: connect V_{L2} to ϕ_2 so gate drive of M_2 is $2V_{dd}$
- LQP2: second-level gate control for M_5
- LQP3: change M_1 to NMOS, but need M_{d1} for startup



Performance Comparison of 5X LQPs



V_o vs V_{dd} for ideal and practical QPs

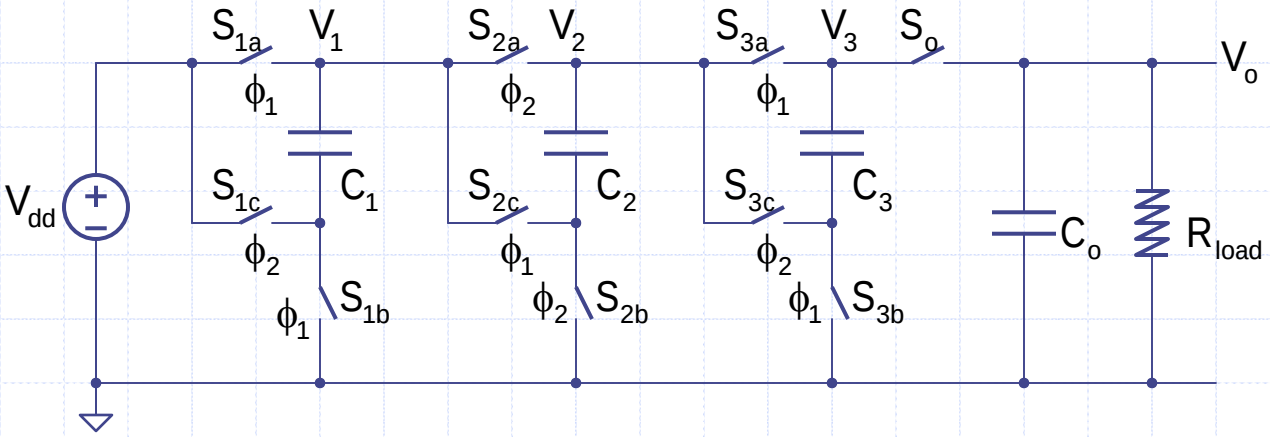


V_o vs I_{load} for ideal and practical QPs

Fibonacci Charge Pump

In [Ueno 91], a 2-phase charge pump is suggested that could realize a conversion ratio of 2, 3, 5, 8, 13, etc. that are Fibonacci numbers, and it could be referred as a Fibonacci charge pump (FQP).

In [Makowski 97], it is shown, using graph theoretical concepts, that an FQP achieves the largest conversion ratio using the fewest capacitors among all 2-phase charge pumps.



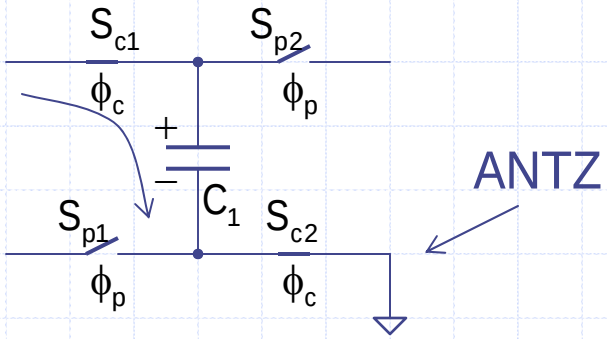
ANTZ Principle

Qn: How many 2-phase charge pumps could be realized given a specified number of flying capacitors?

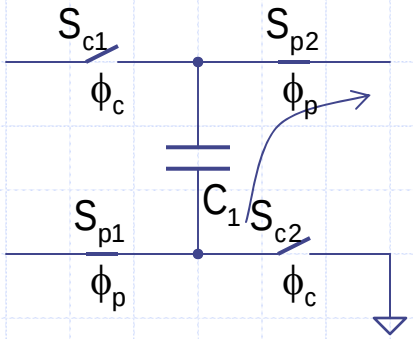
Ans: To answer the above question, we need to formulate a systematic construction of charge pumps, the ANTZ principle: All Negative Terminals are connected to Zero (GND) during the charging phase [Su 07].

It should be noted that all published charge pumps are abided by the ANTZ principle, and hence it is not a restrictive requirement.

Charging Phase

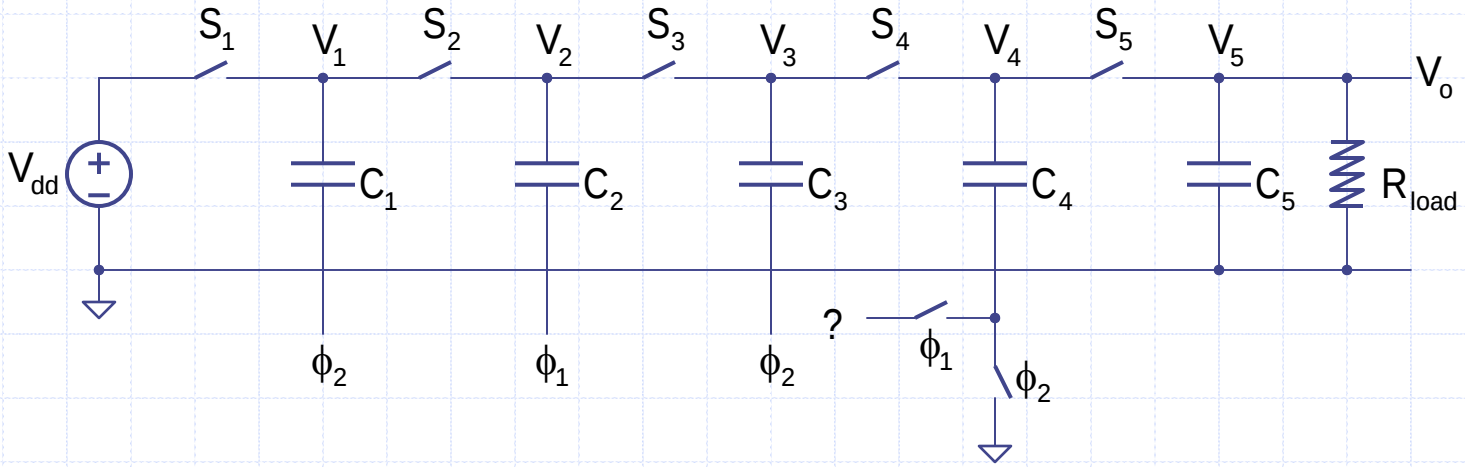


Pumping Phase

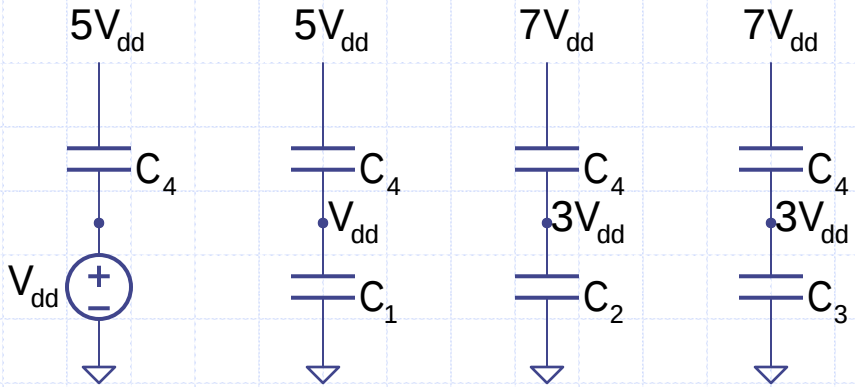


Charging and Pumping Scenarios

Consider a charge pump structure:



After C_4 is charged to $4V_{dd}$ in ϕ_2, it may be connected differently in ϕ_1:



ANTZ Tree Construction (1)

Voltage Vector: $\mathbf{V_p}(C_x)$ = (V_p of C_x in ϕ_1, V_p of C_x in ϕ_2), with V_p the potential of the positive terminal of C_x.

For the LQP in pp. 10, $\mathbf{V_p}(C_3) = (3V_{dd}, 4V_{dd}) = (3, 4)$ for short.

Construct the ANTZ tree using voltage vectors.

Level 0: No capacitor but only V_{dd}

$\mathbf{V_p}(V_{dd}) = (1, 1)$

Level 1: 1 capacitor C_1

$\mathbf{V_p}(C_1) = (1, 2)$ or $(2, 1)$

Eliminate redundancy and the final assignment is

$\mathbf{V_p}(C_1) = (1, 2)$

ANTZ Tree Construction (2)

Level 2: C_1 and C_2

To avoid redundancy, C_2 should not assume (1, 2).

C_2 charged in $\phi_1 \Rightarrow$ has to be connected in series with C_1 and V_{dd} in ϕ_2, and gives (1, 3).

C_2 charged in $\phi_2 \Rightarrow$ (1) charged to V_{dd} by source and gives (2, 1)
(2) charged to $2V_{dd}$ by C_1, and gives (3, 2)

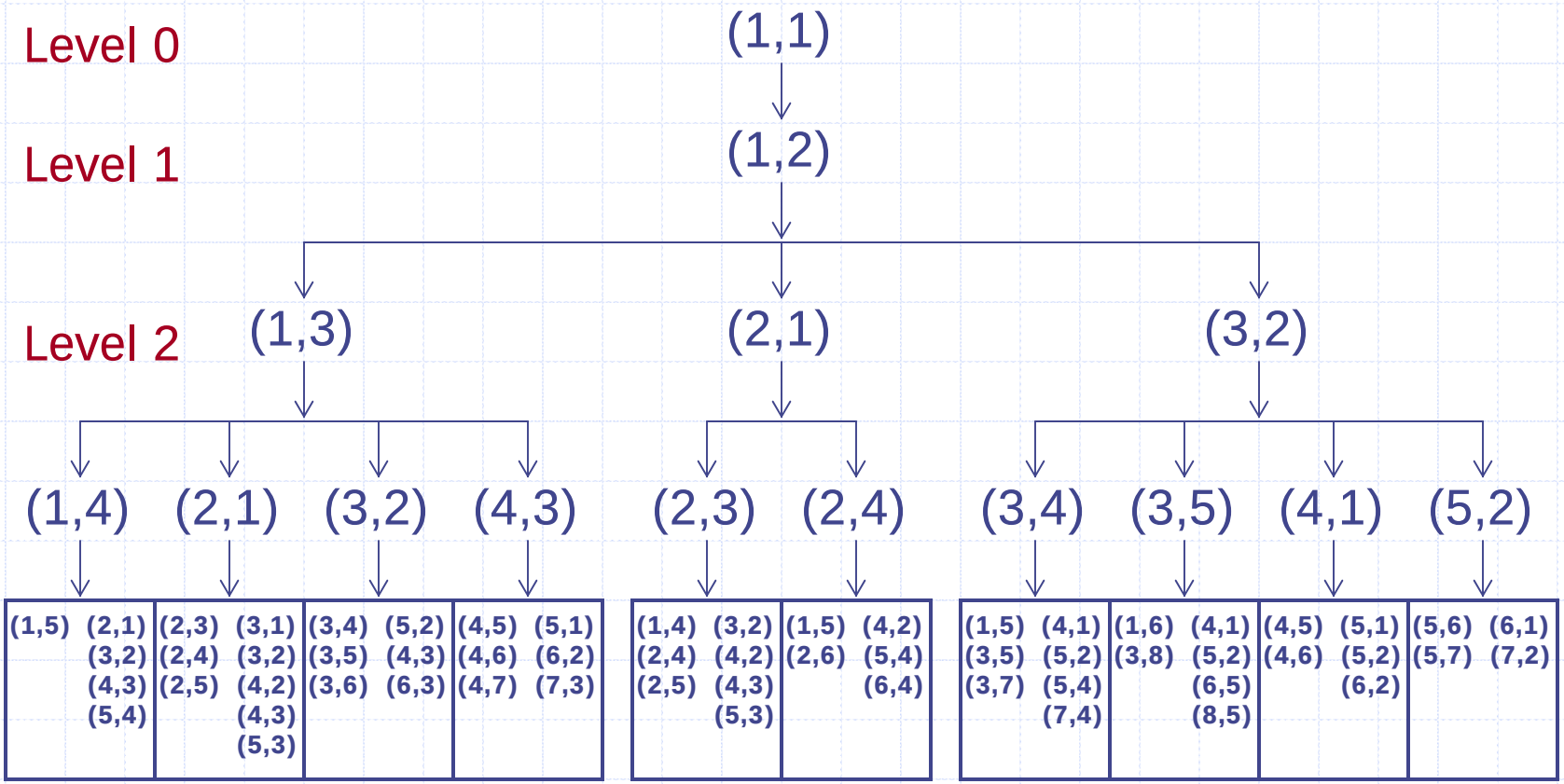
Hence, we have the following vector paths (starting from Level 1):

$(1, 2) \rightarrow (1, 3)$
$(1, 2) \rightarrow (2, 1)$
$(1, 2) \rightarrow (3, 2)$

Level 3 and Level 4 are constructed in a similarly fashion.

4-Capacitor ANTZ Tree

The 4-capacitor ANTZ tree has 59 configurations.



Charge Pumps from ANTZ Tree

5X Heap Charge Pump [Mihara 95]:

$(1, 2) \rightarrow (1, 3) \rightarrow (1, 4) \rightarrow (1, 5)$

3X Dual-Branch Charge Pump [Pellinconi 03]:

$(1, 2) \rightarrow (2, 1) \rightarrow (2, 3) \rightarrow (3, 2)$

2nX or 2^nX (Exponential) Charge Pump (n=2) [Ying 03], [Ki 08]:

$(1, 2) \rightarrow (2, 1) \rightarrow (2, 4) \rightarrow (4, 2)$

5X Linear Charge Pump [Dickson 76]:

$(1, 2) \rightarrow (3, 2) \rightarrow (3, 4) \rightarrow (5, 4)$

8X Fibonacci Charge Pump [Ueno 91]:

$(1, 2) \rightarrow (3, 2) \rightarrow (3, 5) \rightarrow (8, 5)$

New 8X FQP [Su 07]:

$(1, 2) \rightarrow (3, 2) \rightarrow (3, 5) \rightarrow (3, 8)$

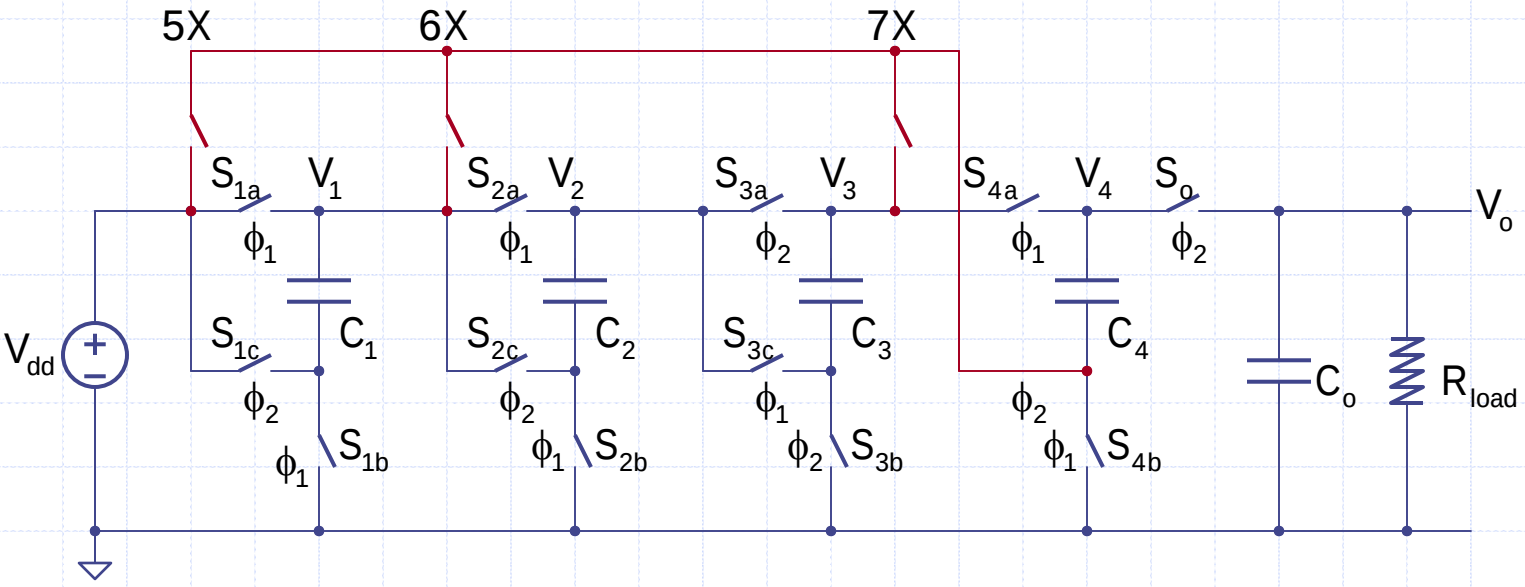
Variable Conversion Ratio

Qn: What is the advantage of identifying all possible topologies?

Ans: The ANTZ tree helps to design charge pumps with a variable conversion ratio, by observing that adjacent topologies only differ by one connection.

For example, consider the vector paths:

$(1, 2) \rightarrow (1, 3) \rightarrow (4, 3) \rightarrow (4, 5)$ / $(4, 6)$ / $(4, 7)$

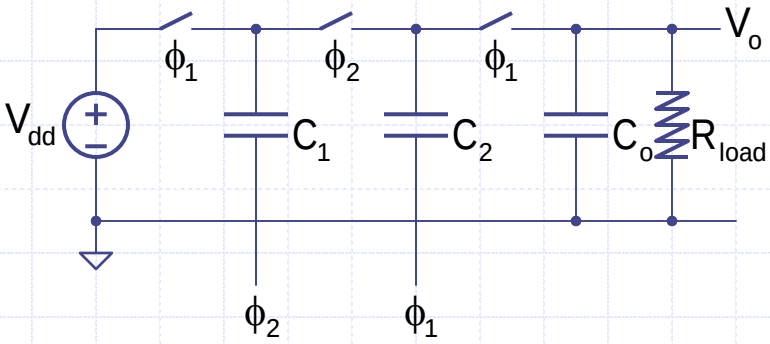


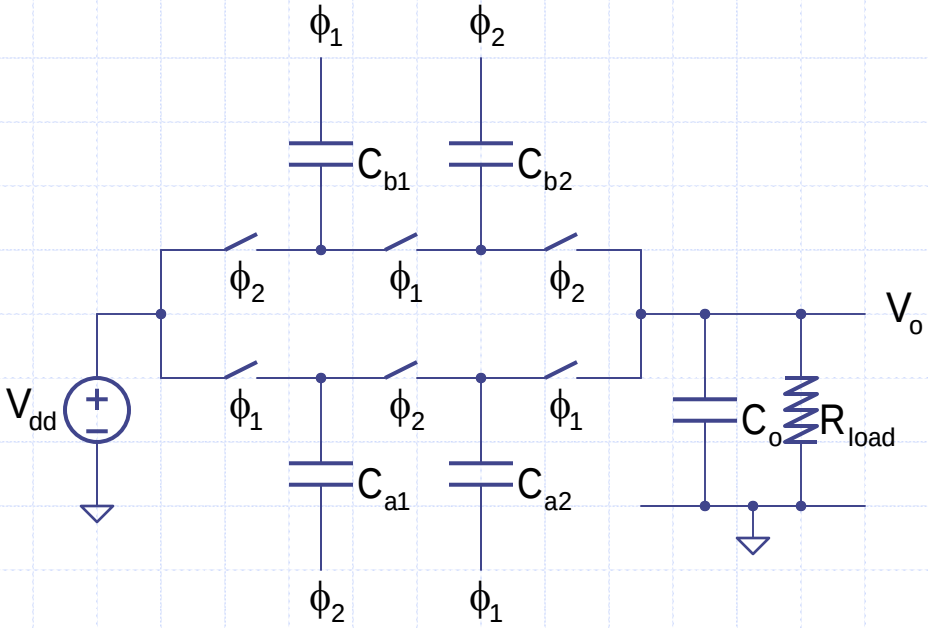
Dual-Branch Charge Pumps

Using the same total capacitance, a dual-branch charge pump is more efficient than a single-branch charge pump [Ki 05]:

$$C_{ak} = C_{bk} = C_k/2$$

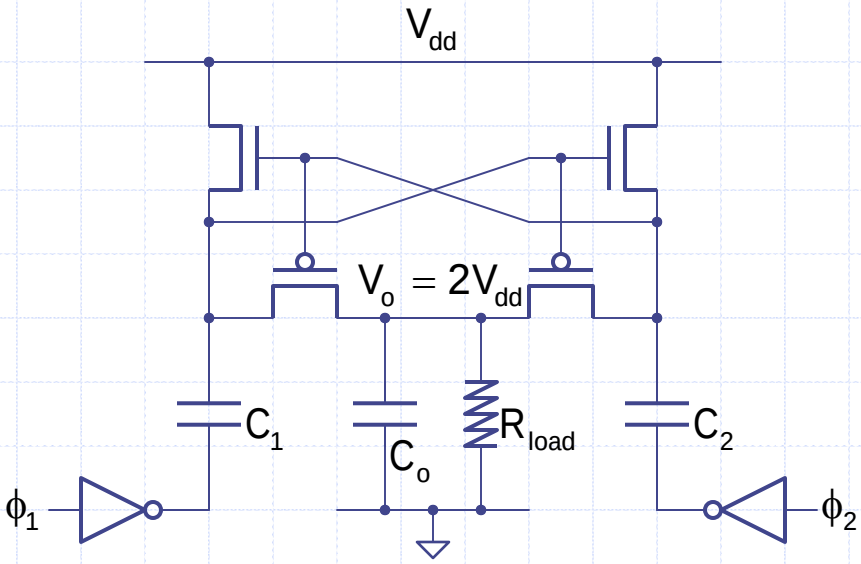
Hence, dual-branch charge pumps are more suitable for on-chip implementation.



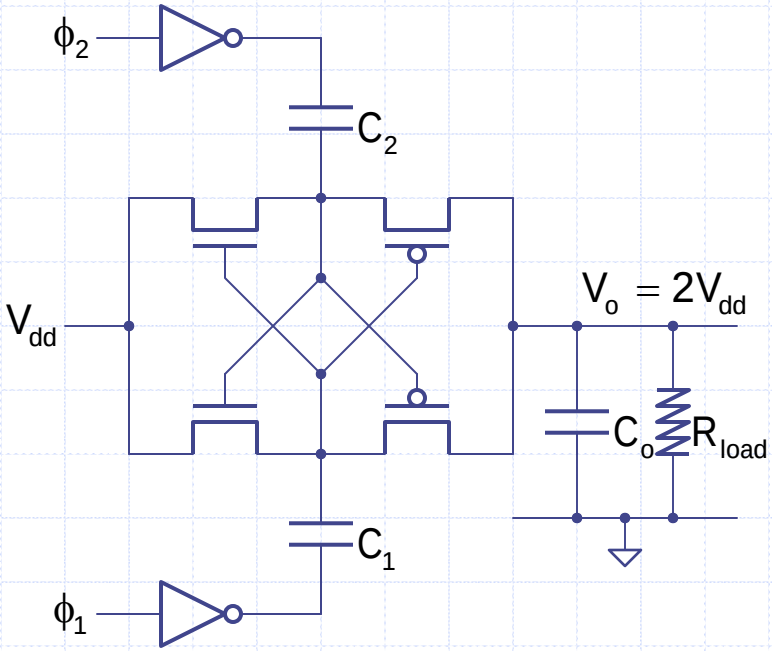


Cross-Coupled Voltage Doublers

Dual-branch charge pumps could make use of the opposite branch for gate drives, and typical examples are cross-coupled voltage doublers such as [Nakagome 91] and [Favrat 98] (they are equivalent).



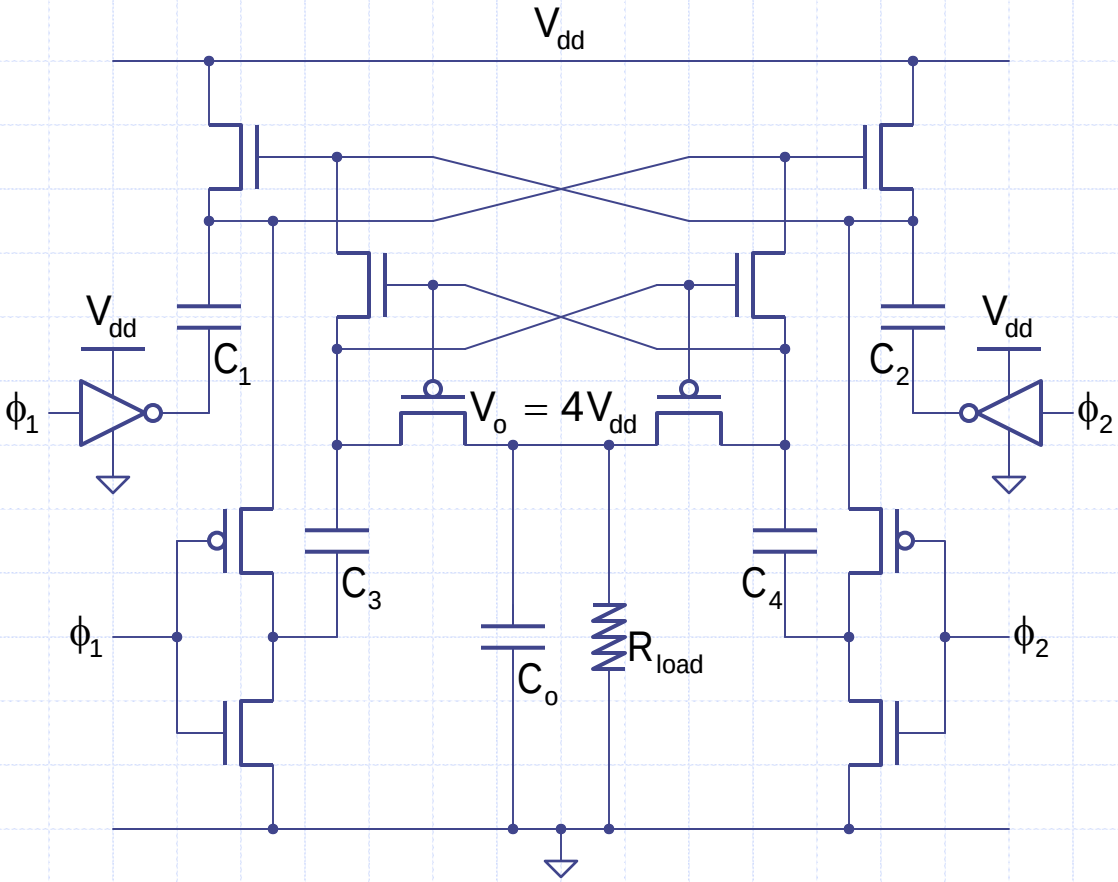
[Nakagome 91]



[Favrat 98]

Component-Efficient 2N-X Charge Pumps

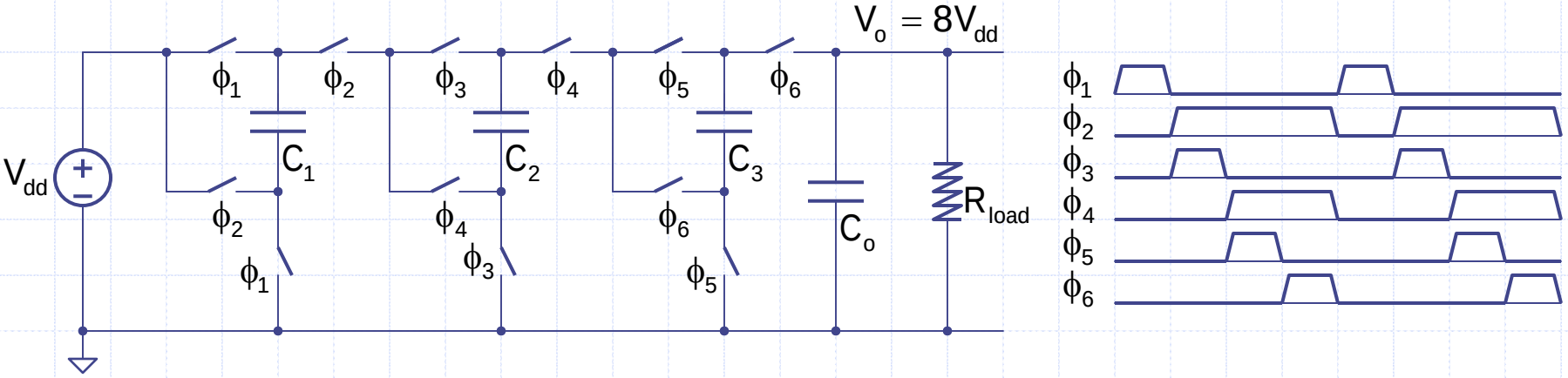
A 4X charge pump could be constructed by cascading two 2X cross-coupled doublers, using 16 power switches. [Ying 02] suggests a 4X cross-coupled charge pump using only 14 power switches.



2N-Phase Exponential Charge Pump

Qn. Is it possible to design an exponential ($2^N X$) charge pump?

Ans. Yes, [Starzyk 01] suggests a consecutive charging scheme that uses a 2N-phase clock: C_1 is charged in ϕ_1, hold for a long ϕ_2, within which C_2 is charged in ϕ_3 and for a shorter ϕ_4, but long enough for C_3 to charge in ϕ_5 and pump in ϕ_6.

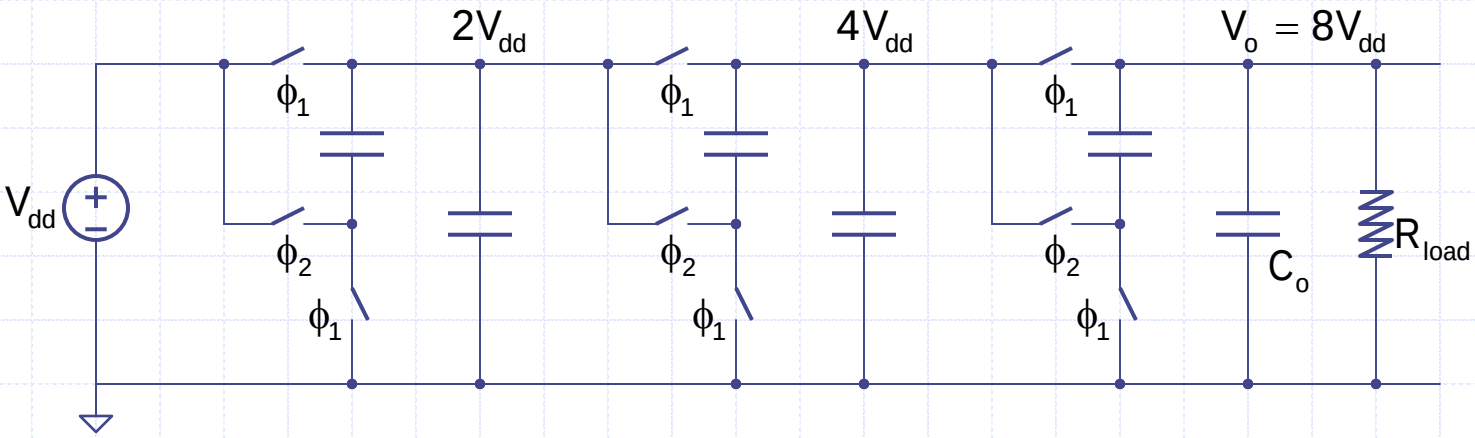


EQP with Cascade Doublers

A straightforward way is to cascade voltage doublers [Chang 04]. However,

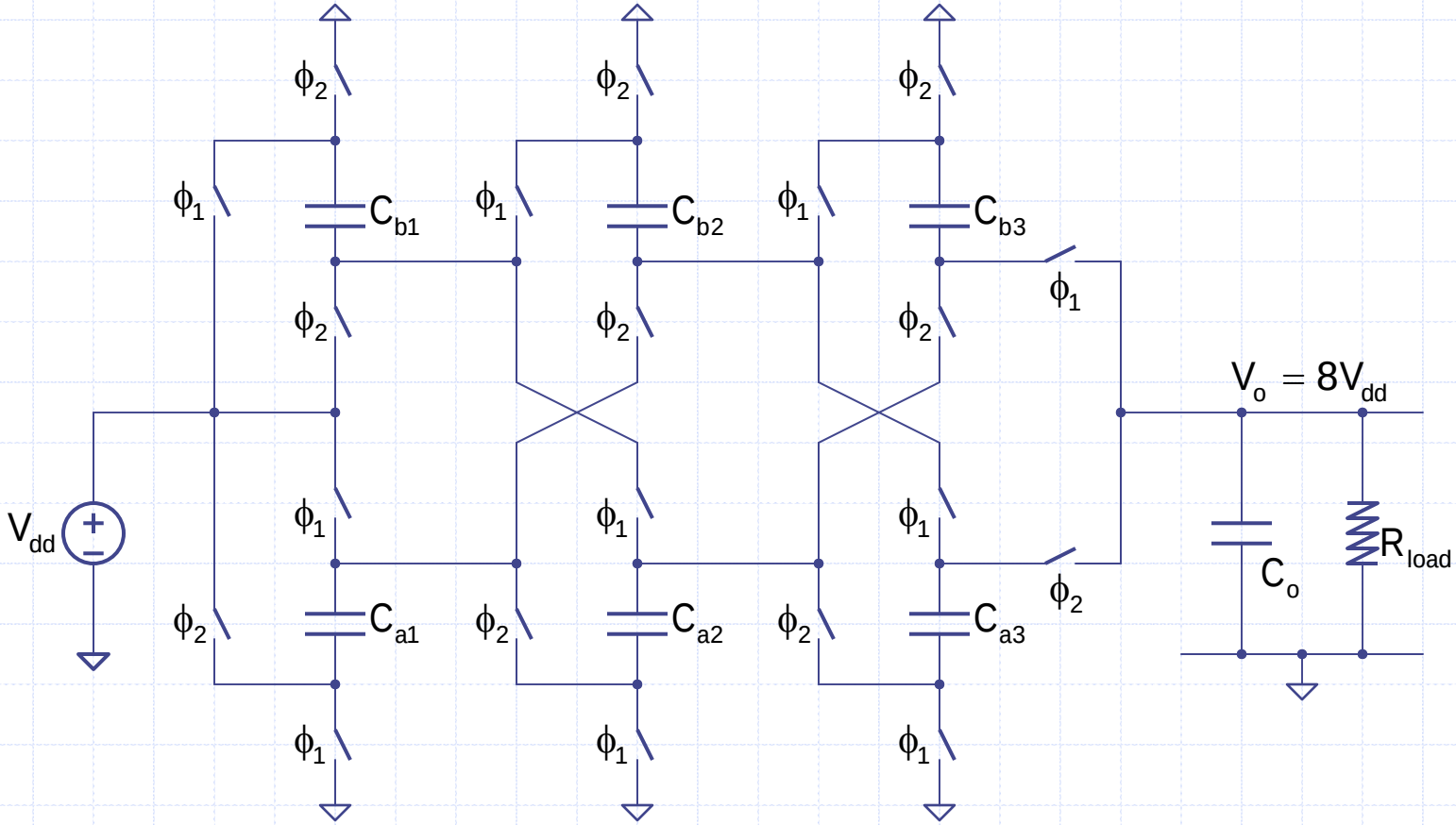
(1) an N-stage charge pump needs 2N capacitors; and

(2) single-branch structure needs a larger total area than a dual-branch structure for the same efficiency.



Cross-Coupled EQP

[Ki 08] suggests a cross-coupled dual-branch exponential charge pump: C_{a1} is charged to V_{dd} in ϕ_1, pumped in ϕ_2, and pushes up C_{a2} by $2V_{dd}$ and charges C_{b2} to $2V_{dd}$ at the same time.



Properties of Cross-Coupled EQP

Advantages:

(1) Only a 2-phase clock is needed, and gate drive is simpler because dual branch operation provides node voltages to drive the other branch.

(2) Dual branch operation charges the output in both phases, reducing the ripple, or equivalently, enhancing the efficiency as compared to single branch charge pumps.

Disadvantages:

(1) Need 2N capacitors, and may not be good if off-chip capacitors are used.
(2) Using cross-biased nodes for gate drives results in reversion loss.

Multi-Phase Charge Pumps

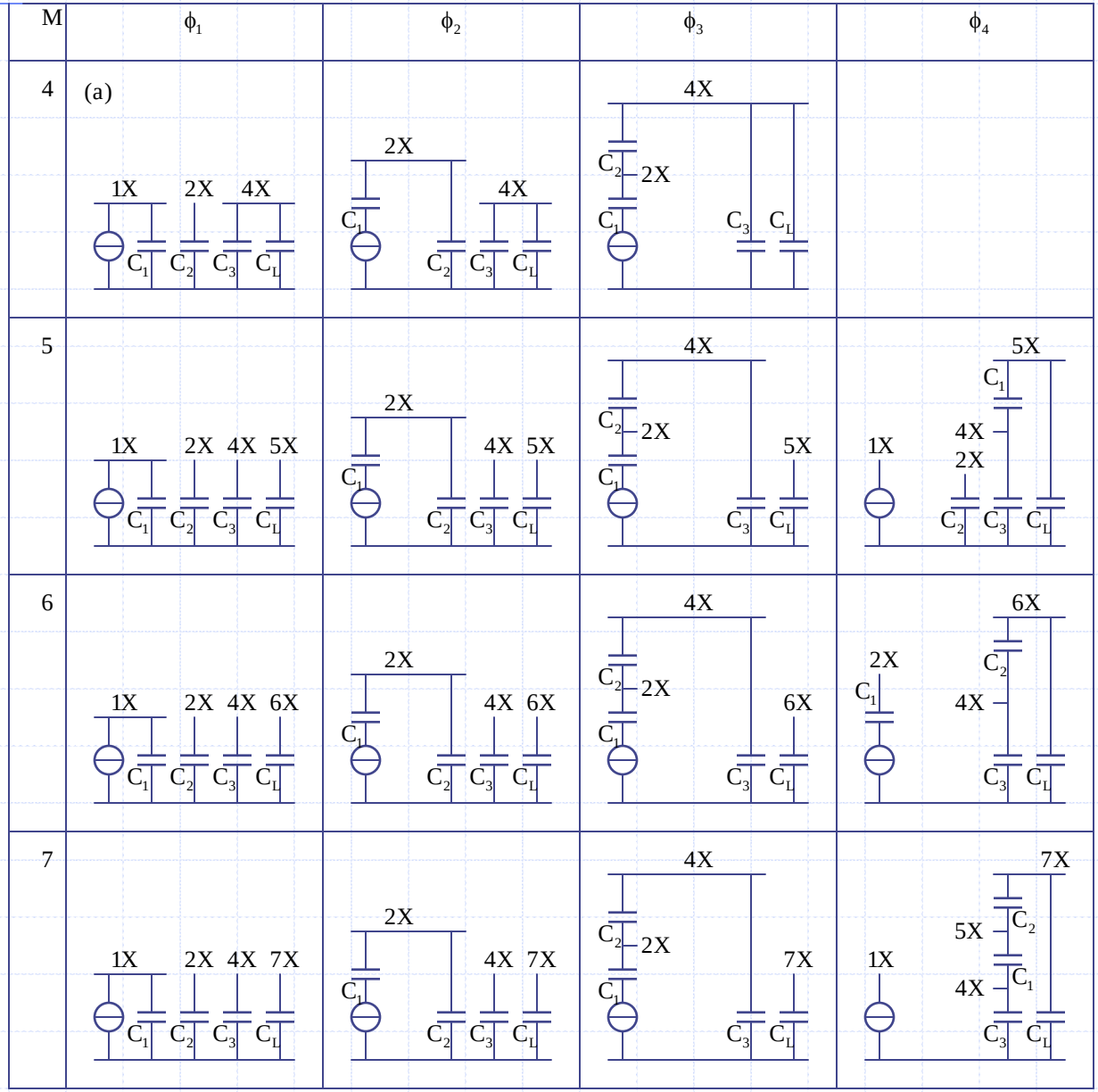
Qn. Is it possible to design an exponential ($2^N X$) charge pump using only N flying capacitors but using fewer than 2N phases?

Ans. Yes, [Su 08b] suggests a systematic strategy to design multi-phase charge pumps, observing the one voltage criteria.

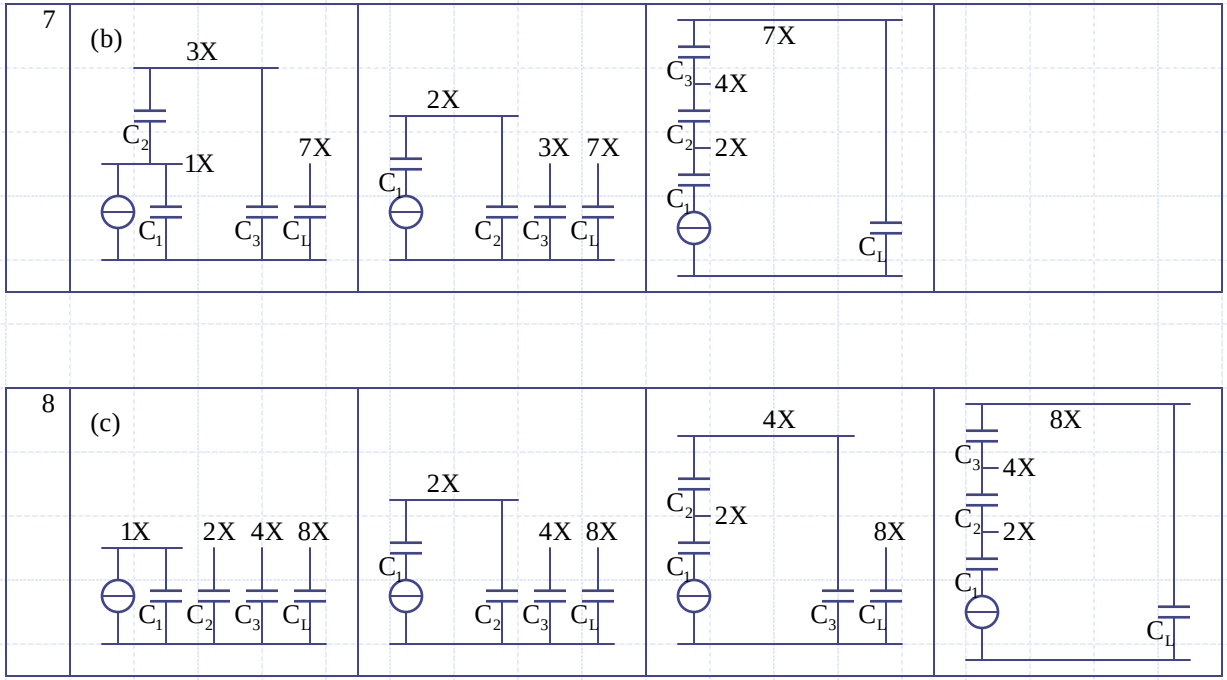
One voltage criteria: Each capacitor should be charged to only one voltage value that is a multiple of V_{dd} for all charging phases, and in the discharging phases, the lowering of the capacitor voltage is mainly due to the load current.

With the one voltage criteria, we demonstrate that a $2^N X$ charge pump could be realized using N flying capacitors and only N+1 phases.

3/4-Phase QPs with 3 Flying Capacitors



Multi-Phase 7X and 8X Charge Pumps

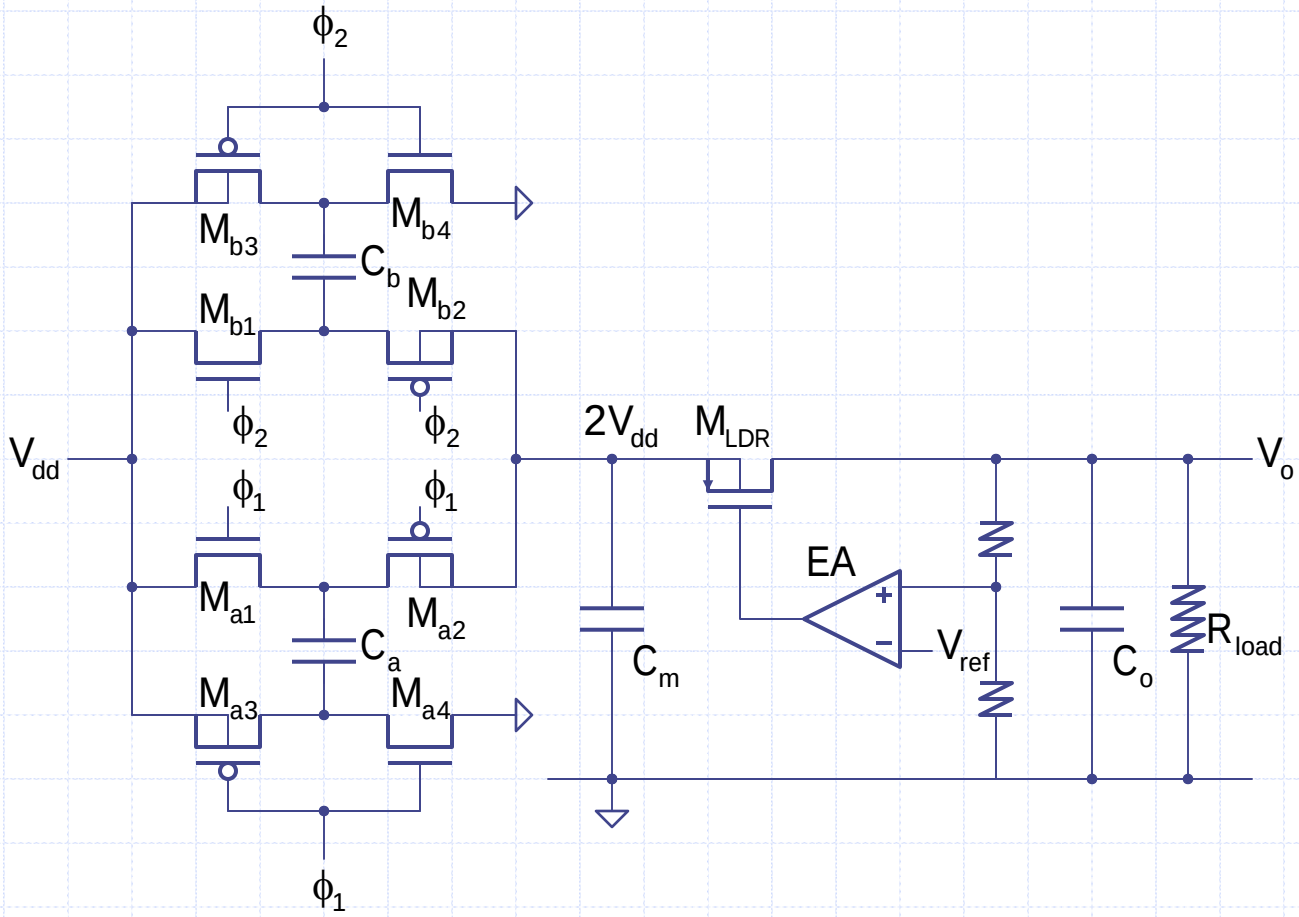


Comparison of Exponential Charge Pumps

	Linear QP	Cascade 2X's	X-coupled EQP	Multi-phase
Caps	2^N	2N	2N+1	N
Clock	2-phase	2N-phase	2-phase	(N+1)-phase
Speed	very slow	fast	fast	medium
	single-branch	single-branch	dual-branch cross-coupled	single-branch
Area	large	medium	low	low
Eff.	poor	good	good	medium

Voltage Doubler + LDR

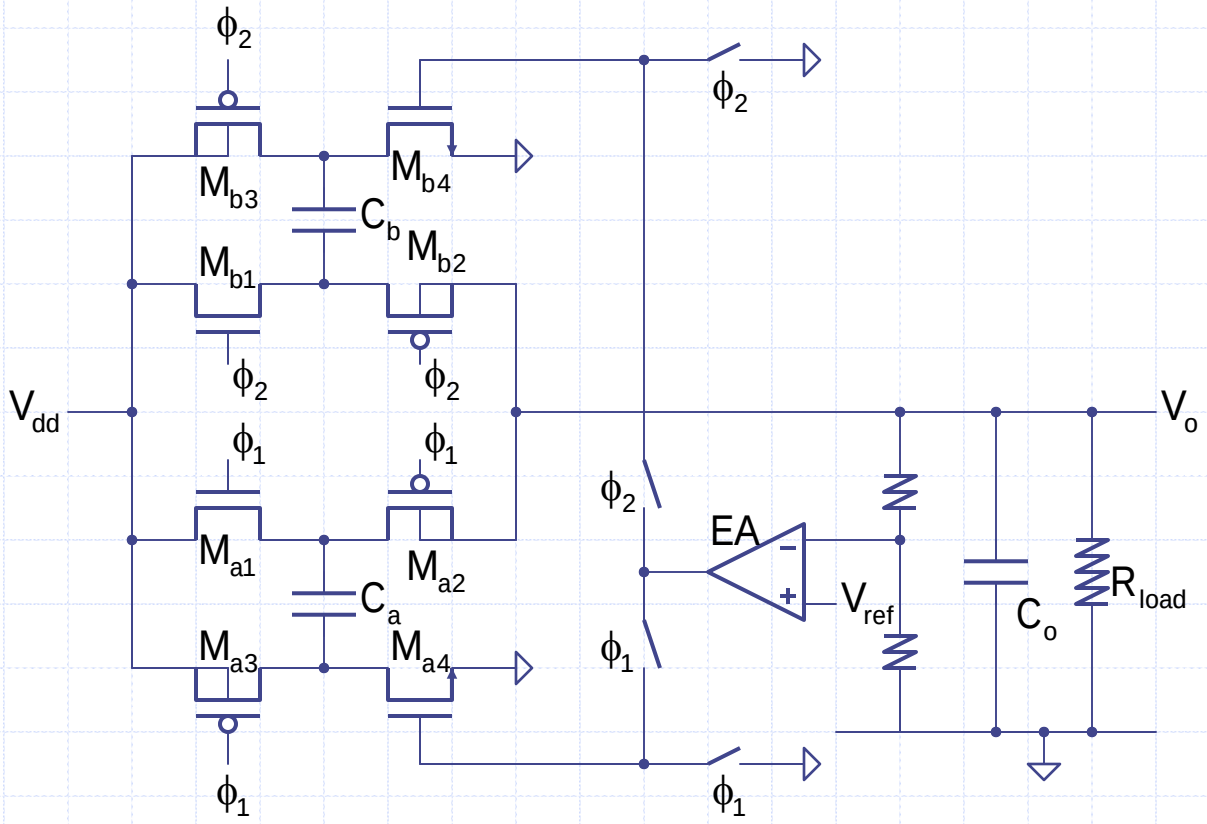
To achieve a regulated output voltage, a straightforward method is to cascade the charge pump with a low dropout regulator (LDR) to achieve a regulated charge pump (RQP).



RQP with Quasi Switches

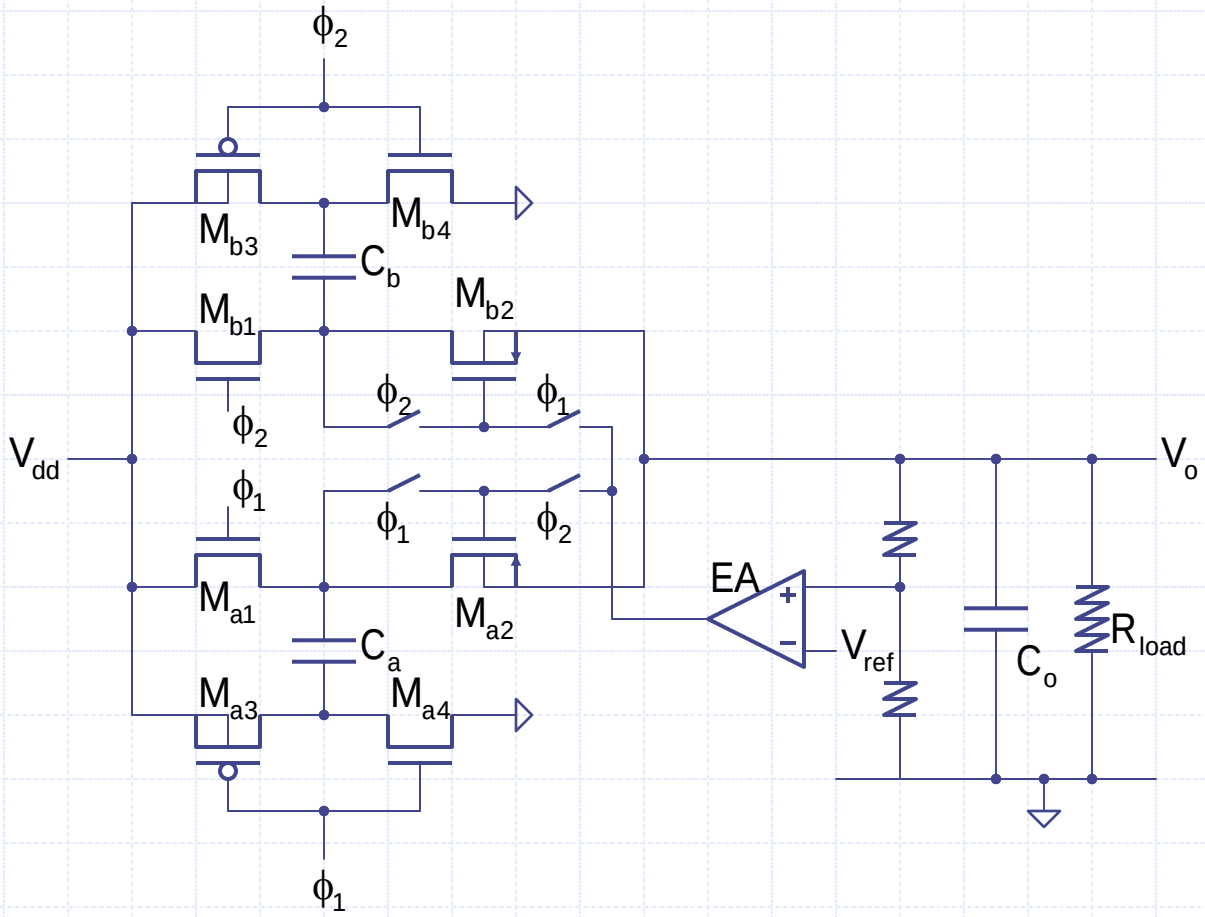
In [Chung 98], the switches M_{a4} and M_{b4} are turned into controlled current sources (resistors), coined quasi switches, and charges C_a and C_b to V_1 ([Chung 98] uses only single-branch) such that

$$V_o = V_{dd} + V_1$$



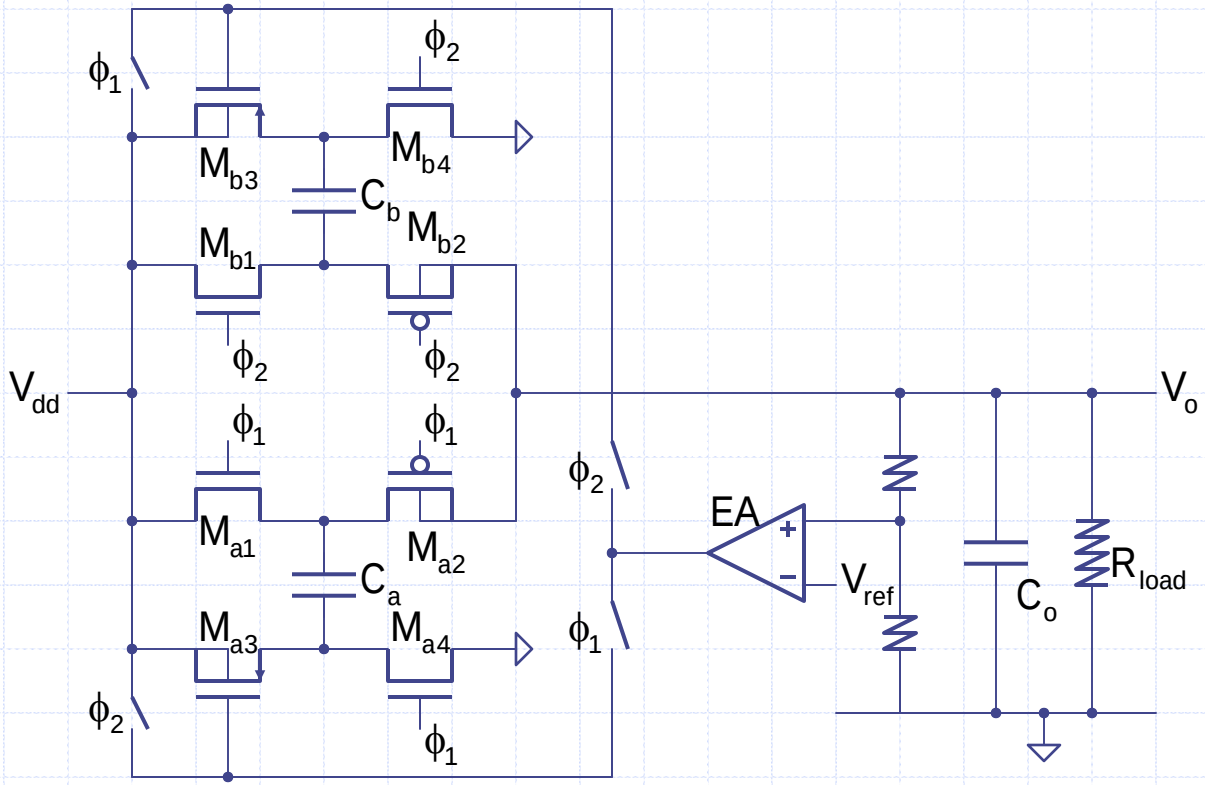
Switching Low Dropout Regulator

The RQP with quasi-switches cannot achieve in-phase regulation, and the best is to combine M_{a2} (M_{b2}) with M_{LDR}, and the scheme is coined switching low dropout regulator (SLDR) [Chen 01].



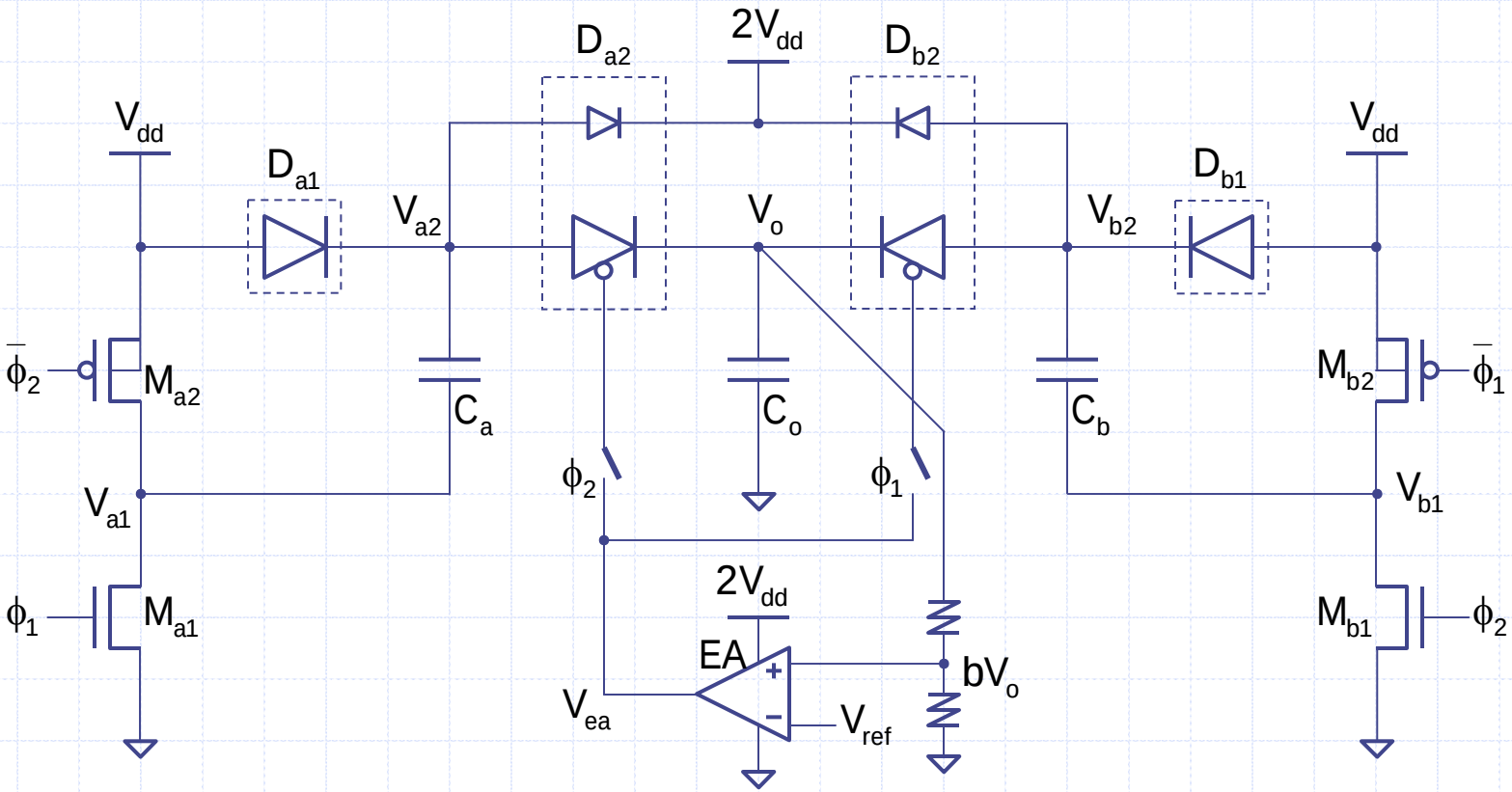
RQP with Pseudo-Continuous Regulation

An alternative way to achieve in-phase regulation is to incorporate M_{LDR} into M_{a3} (M_{b3}), and the scheme is coined pseudo-continuous regulation [Lee 05].



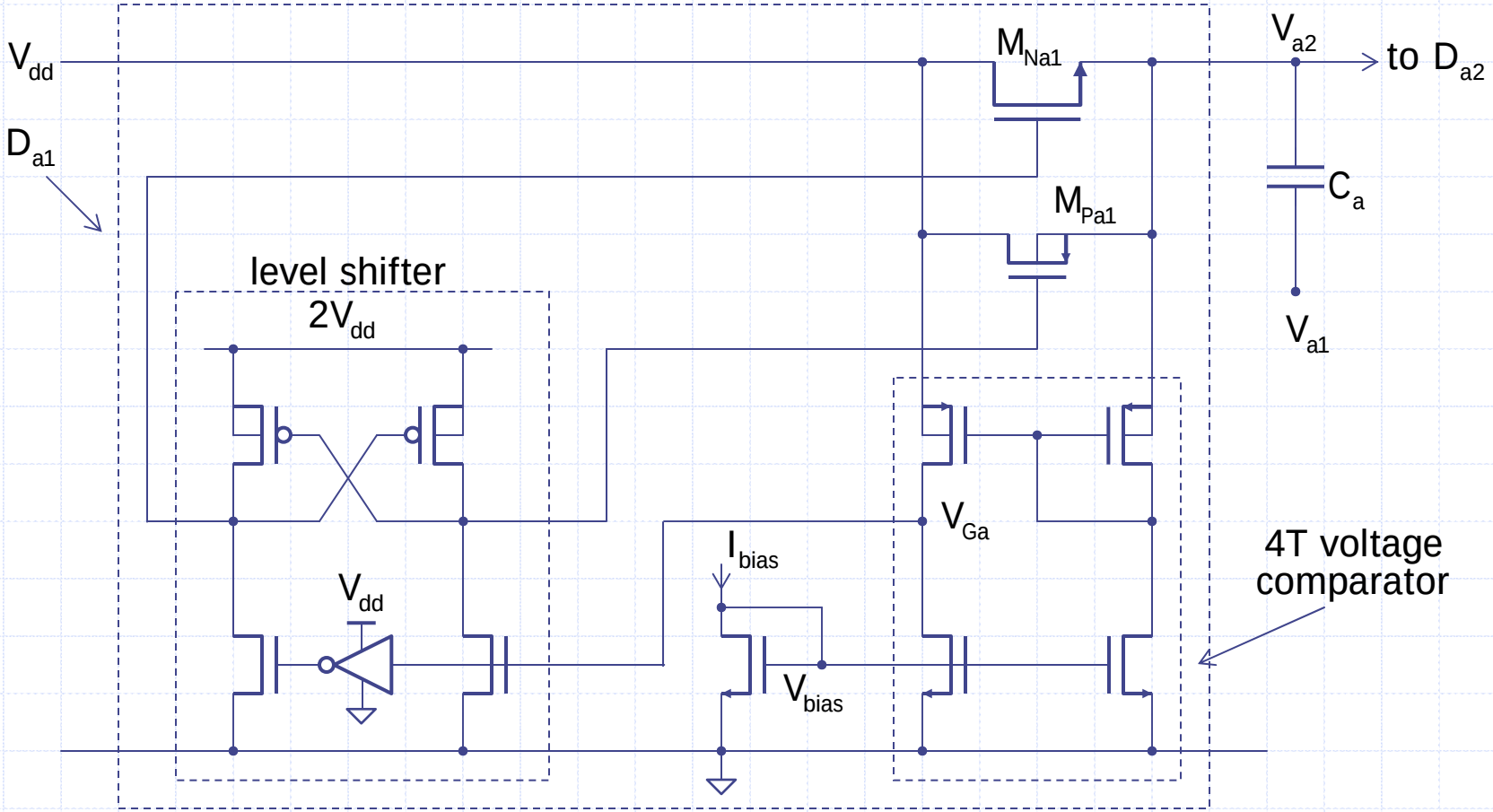
RQP with Active Diodes

An alternative way of implementing the switching LDR is to use active diodes, i. e., using MOS transistors with control to replace the diodes [Lam 06a].



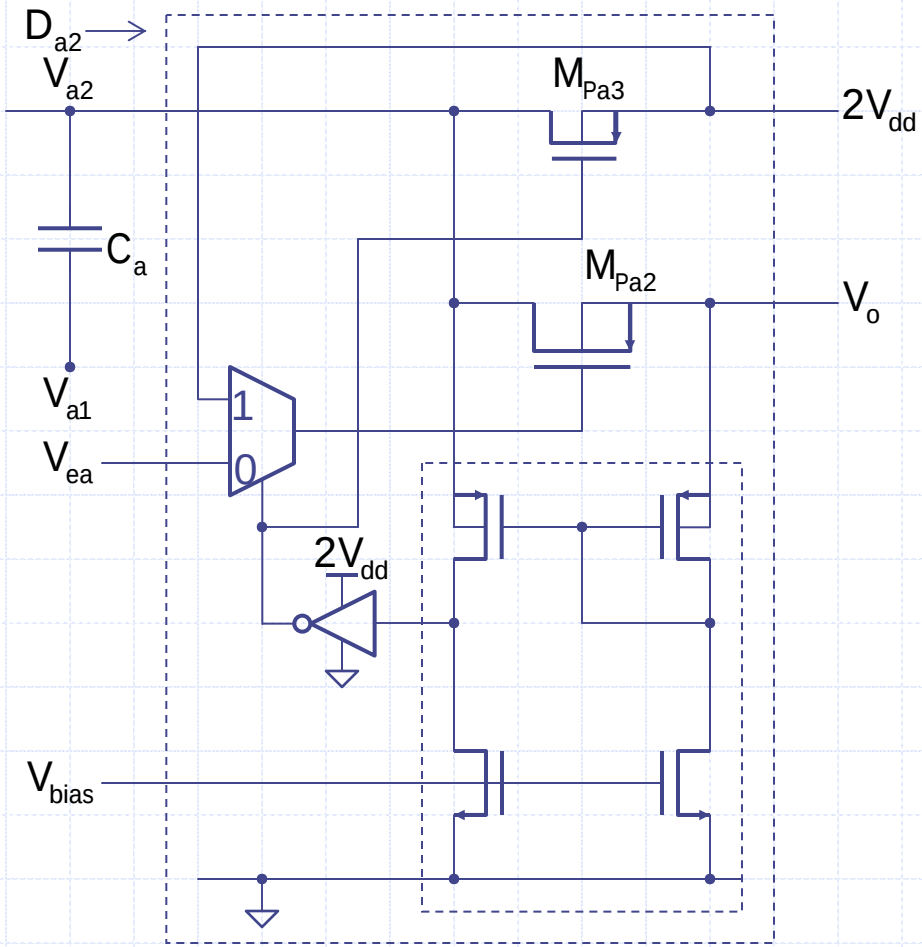
Implementation of D_{a1}

An active diode is an MOS switch with a differential common gate comparator and level shifter [Lam 06a].



Implementation of D_{a2}

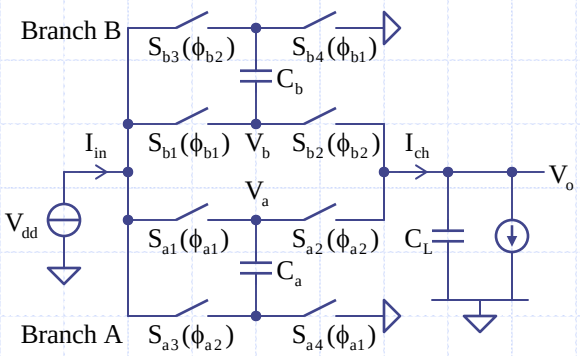
Active diode D_{a2} (D_{b2}) also serves as the pass transistor of the LDR.

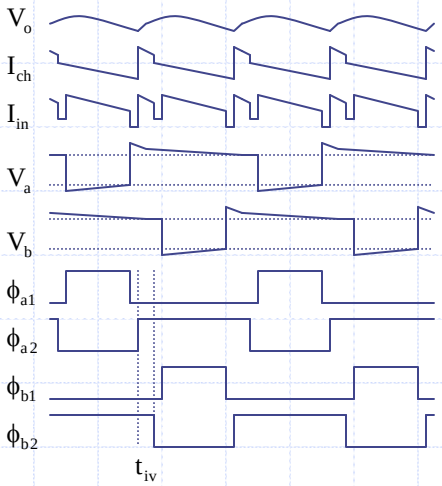


RQP with Continuous Output Regulation (1)

To achieve (in-phase) continuous output regulation, a 4-phase clock with interleaving control is proposed [Su 09].

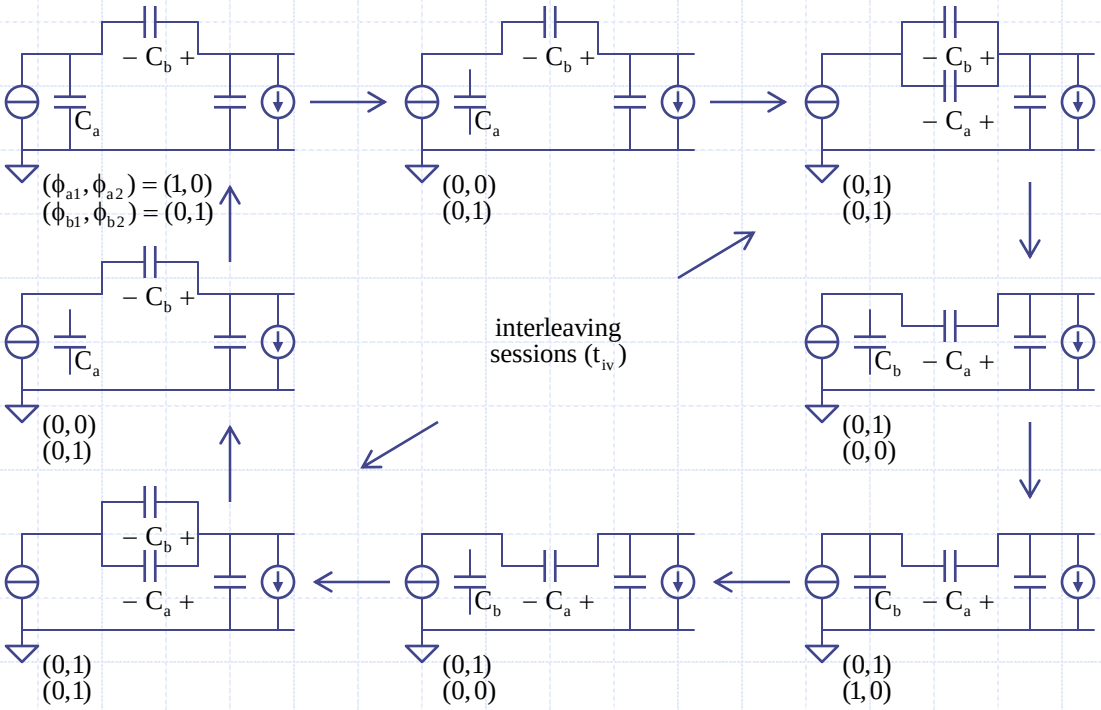
Voltage doubler with 4-phase interleaving clock:





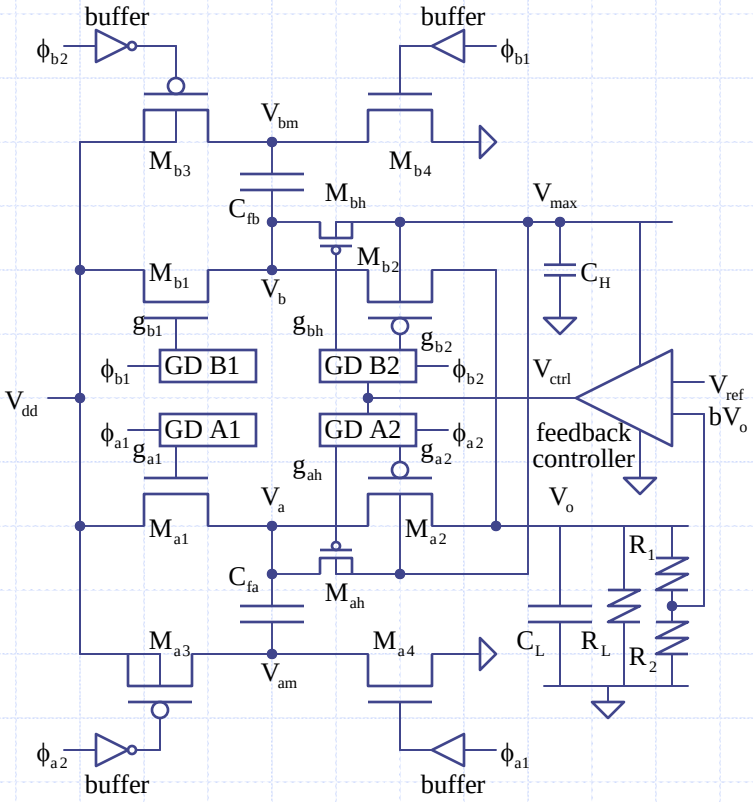
RQP with Continuous Output Regulation (2)

The interleaving scenario:



RQP with Continuous Output Regulation (3)

The LDR architecture:



Remarks

A systematic study of charge pumps should cover analysis, topology, gate control and regulation. This talk only covers snapshots on topology, gate control and regulation.

The talk centered on the research activities at HKUST. The attached reference section only mentions those papers (in chronological order) that are directly useful for the discussion:

[BLUE] Papers from other institutions
[RED] HKUST papers (Ki's research group)
[PINK] HKUST papers (Mok's and Tsui's research groups)

The reference section tabulates all publications since the setup of the Integrated Power Electronics Lab. in 1995 up to Sept. 2009, and topics such as analysis, AC-DC charge pumps, energy harvesting applications, etc., are not covered in this talk due to limited time.

References: Analysis, Gate Control

Analysis

[Dickson 76] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE J. of Solid State Circ., pp.374-378, June 1976.

[Makowski 97] M. S. Makowski, "Realizability conditions and bounds on synthesis of switched-capacitor dc-dc voltage multiplier circuits," IEEE Trans. on Circ. & Syst. I, pp. 684-691, Aug. 1997.

[Ki 05] W. H. Ki, F. Su and C. Y. Tsui, "Charge redistribution loss consideration in optimal charge pump design," IEEE Int'l. Symp. on Circ. & Syst., pp.1895-1898, May 2005.

Gate Control

[Cheng 03] K. H. Cheng, C. Y. Chang and C. H. Wei, "A CMOS charge pump for sub-2.0V operation," IEEE Int'l Symp. on Circ. & Syst., pp.V-89 – V-92, 2003.

[Lee 05] H. Lee and P. Mok, "Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler," IEEE J. of Solid-State Circ., pp.1136–1146, May 2005.

[Su 05] F. Su, W. H. Ki and C.Y. Tsui, "Gate control strategies for high efficiency charge pumps", IEEE Int'l. Symp. on Circ. & Syst., pp.1907-1910, May 2005.

[Su 06] F. Su, W. H. Ki and C. Y. Tsui, "High efficiency cross-coupled doubler with no reversion loss," IEEE Int'l. Symp. on Ckts. & Sys., pp.2761-2764, May 2006.

References: Topology (1)

[Dickson 76] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE J. of Solid State Circ., pp.374-378, June 1976.

[Nakagome 91] Y. Nakagome et al., "An experimental 1.5-V 64-Mb DRAM," IEEE J. of Solid-States Circ., pp. 465-472, March 1991.

[Ueno 91] F. Ueno et. al., "Emergency power supply for small computer systems," IEEE Int. Symp. Circ. & Syst.., 1991, pp. 1065–1068.

[Mihara 95] M. Mihara, Y. Terada and M. Yamada, "Negative heap pump for low voltage operation flash memory," IEEE VLSI Symp. on Circ., 1995, pp. 75–76.

[Favrat 98] P. Favrat, P. Deval and M. J. Declercq, "A high efficiency CMOS voltage doubler," IEEE J. of Solid-States Circ., March 1998, pp.410-416.

[Starzyk 01] J. A. Starzyk, Y. W. Jan and F. Qiu, “A DC-DC charge pump design based on voltage doublers,” IEEE Trans. on Circ. & Syst., pp.350-359, March 2001.

[Ying 02] T. R. Ying, W. H. Ki and M. Chan, "Area-efficient CMOS integrated charge pumps," IEEE Int'l. Symp. on Circ. & Syst., Scottsdale, USA, pp.III.831-III.834, May, 2002.

[Cheng 03] K. H. Cheng, C. Y. Chang and C. H. Wei, "A CMOS charge pump for sub-2.0V operation," IEEE Int'l Symp. on Circ. & Syst., pp.V-89 – V-92, 2003.

References: Topology (2)

[Pelliconi 03] R. Pelliconi et. al., "Power efficient charge pump in deep submicron standard CMOS technology," IEEE J. Solid-State Circ., pp. 1068–1071, Jun. 2003.

[Ying 03] T. R. Ying, W. H. Ki and M. Chan, "Area-efficient CMOS charge pumps for LCD drivers," IEEE J. of Solid-State Circ., pp.1721-1725, Oct. 2003.

[Chang 04] L. K. Chang and C. H. Hu, “An exponential-folds design of a charge pump styled DC/DC converter,” IEEE Power Elec. Specialists Conf., pp.516-520, June 2004.

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IC Design of Power Management Circuits (VI)

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Part VI

Introduction to Low Dropout Regulators

Content

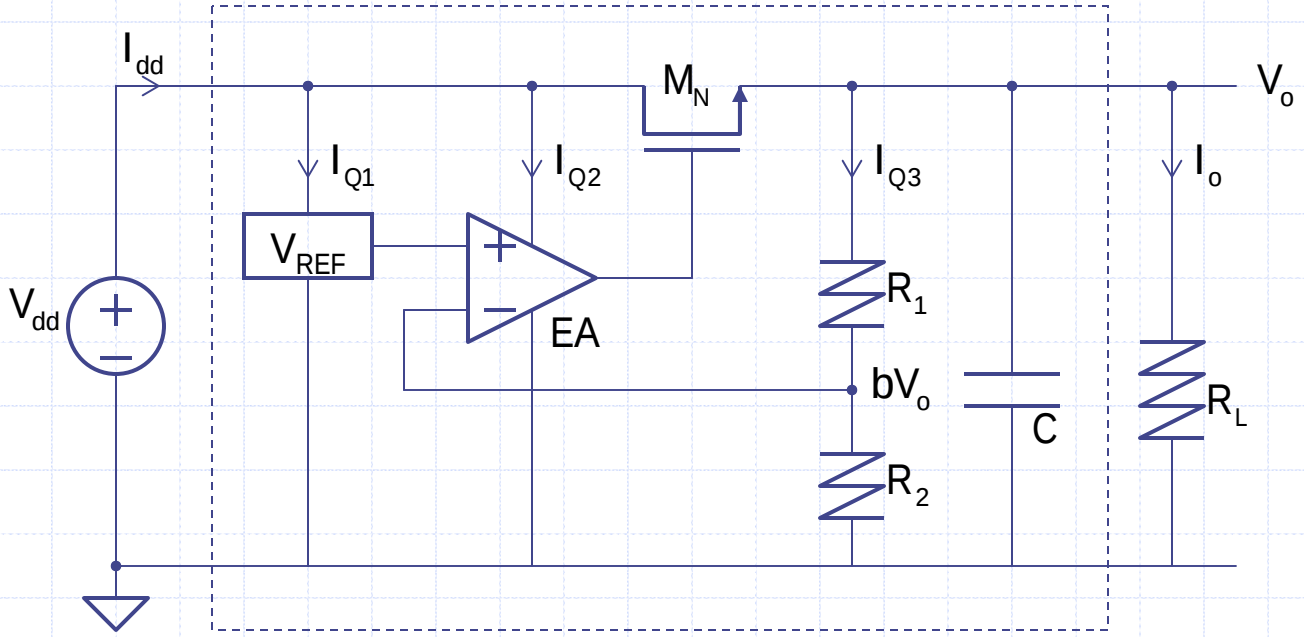
Generic Linear Regulator

Low Dropout Regulator

Simple Low Dropout Regulator

Generic Linear Regulator

A linear regulator consists of a pass transistor inserted between the input supply voltage V_{dd} and the required output voltage V_o, and a feedback circuit for controlling the voltage drop across the pass transistor such that V_o is kept constant. In CMOS design, the pass transistor could be an NMOS or a PMOS transistor.



Linear Regulator

Dropout Voltage of Linear Regulator

One important parameter of a linear regulator is the dropout voltage (V_{DO}) that is defined as the minimum voltage difference between V_{dd} and V_o such that the regulator still performs satisfactorily as a linear regulator:

$$V_{DO} = \min[V_{dd} - V_o]$$

As V_o is usually fixed, we have

$$V_{DO} = V_{ddmin} - V_o$$

For the linear regulator in the previous page, the high output swing of the error amplifier EA is $V_{dd}-V_{ov}$, and $V_{gsN} = V_{tn}+V_{ov}$ (V_{ov} is the gate overdrive voltage of all transistors), and V_{ddmin} is computed as

$$V_{ddmin} = V_o + V_{gsN} + V_{ov}$$
$$= V_o + V_{tn} + 2V_{ov}$$

Efficiency of Linear Regulator

Another important parameter is the efficiency that is obtained as

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o I_o}{V_{dd} I_{dd}} = \frac{V_o}{V_{dd}} \frac{I_o}{I_o + I_Q} \approx \frac{V_o}{V_{dd}}$$

and

$$\eta_{max} \approx \frac{V_o}{V_{ddmin}} = \frac{V_o}{V_o + V_{tn} + 2V_{ov}}$$

For example, if V_o=1.8V, V_{tn}=0.8V, V_{ov}=0.2V, then the maximum efficiency is only 60%.

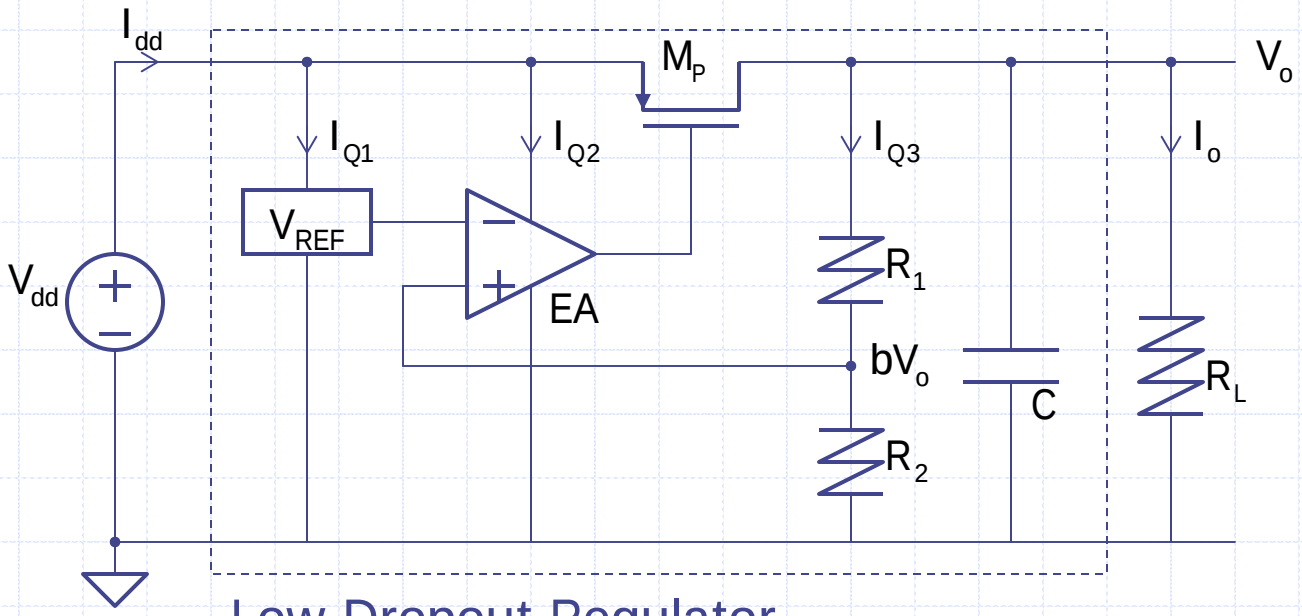
It is desirable to have a low V_{DO} such that the efficiency is still satisfactory even when the battery is drained very low.

Low Dropout Regulator

Low dropout regulators (LDRs) could be achieved by using a higher supply voltage for EA through using an on-chip charge pump. Yet, a popular method is to use a PMOS pass transistor, (V_+ and V_- have to be swapped), and $V_{ddmin} = V_o + V_{ov}$, giving

$$\eta_{max} \approx \frac{V_o}{V_{ddmin}} = \frac{V_o}{V_o + V_{ov}}$$

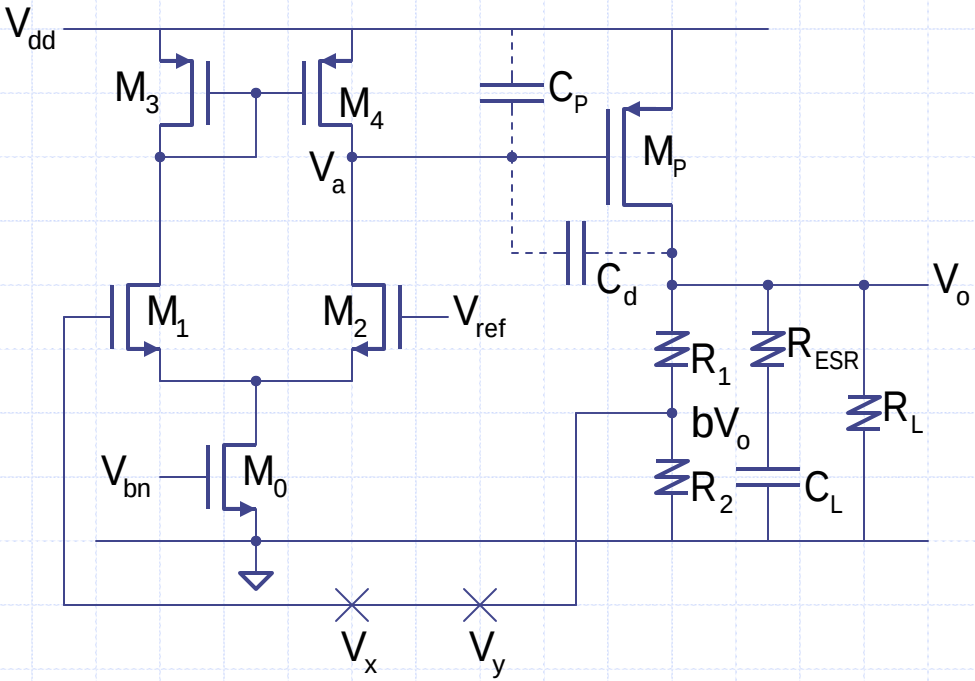
(η_{max} = 90% with the previous parameters)



Low Dropout Regulator

Simple Low Dropout Regulator

A simple LDR could be obtained by using a differential pair to drive the PMOS pass transistor. For V_{tn}=0.55V, $|V_{tp}|$=0.7V, and V_{ov}=0.2V, it is feasible to use V_{ref}=1.25V to bias M_0 to M_2. Also, let V_o=2.5V and V_{DO}=0.2V, then V_{ddmin}=2.7V. Clearly, the voltage swing of V_a (with V_{ref}=1.25V) is from 0.7V to 2.5V.



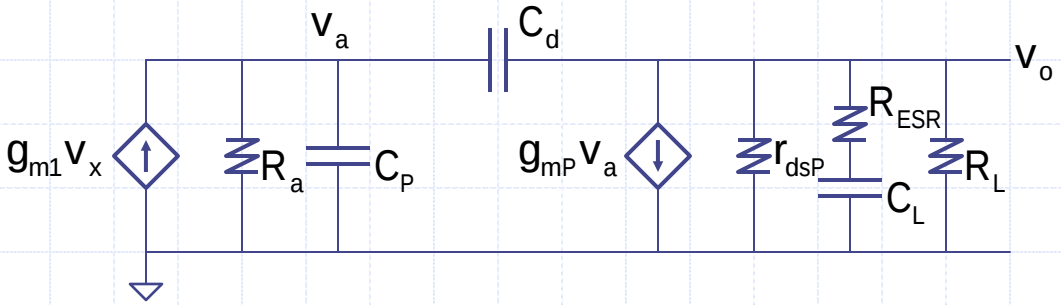
Complications in LDR Analysis

Although the simple LDR resembles a 2-stage amplifier of which the analysis is well-known, there are complications.

1. In many analyses, only the gate capacitance of the pass transistor C_{gP} ($=C_P$) is considered; but in fact the gate-drain overlap capacitance C_{gdoP} ($=C_d$) is quite large and should not be omitted.
2. The output current could change by 5 orders of magnitudes (say, from 10μA to 100mA), and the pass transistor will transit from the sub-threshold region to the active region.
3. For aggressive design in using a smaller pass transistor, it will operate in the triode region at high currents.
4. Both C_P and C_d depends on the load current.

Simple LDR: Small Signal Model

C_P and C_d are parasitic capacitors and are shown by dotted lines in pg. 8. By absorbing R_1+R_2 into R_L, the small signal model is



$$T(s) = \frac{-v_y}{v_x} = \frac{-bv_o}{v_x} = \frac{T_o(1+sC_LR_{ESR})(1-sC_d/g_{mP})}{(1+as+bs^2)}$$

with $T_o = bg_{ma}g_{mp}R_aR_o$ $\quad R_a = r_{ds2}||r_{ds4}$ $\quad R_o = R_L||r_{dsP}$

$$a = [C_P + (1+g_{mP}R_o)C_d]R_a + (C_d+C_L)R_o$$

$$b = (C_PC_d + C_PC_L + C_dC_L)R_aR_o$$

Simple LDR: Loop Gain Function

Note that $C_L >>> C_P$, C_d, we have

$$a \approx C_L R_o = C_L (R_L || r_{dsP})$$

$$b \approx (C_P + C_d) C_L R_a R_o$$

and $g_{mP}/C_d >> z_{ESR}$, then the loop gain function is given by

$$T(s) = \frac{T_o (1 + s/z_{ESR})}{(1 + s/p_o)(1 + s/p_a)}$$

with

$$T_o = b g_{ma} g_{mp} (r_{ds2} || r_{ds4})(R_L || r_{dsP})$$

$$z_{ESR} = \frac{1}{C_L R_{ESR}}$$

$$p_o = \frac{1}{C_L (R_L || r_{dsP})}$$

$$p_a = \frac{1}{(C_P + C_d)(r_{ds2} || r_{ds4})}$$

Simple LDR: Numerical Example

The simple LDR is designed using a 0.35μm CMOS process:

$\mu_n C_{ox}=110\mu A/V^2$, $\mu_p C_{ox}=35\mu A/V^2$, $V_{tn}=0.55V$, $|V_{tp}|=0.7V$, $\lambda_n=0.1/V@L=0.5\mu m$, $|\lambda_p|=0.1/V@L=1\mu m$

$V_{dd}=2.7V$, $V_o=2.5V$, $V_{ref}=1.25V$, $b=0.5$, $C_L=10\mu F$, $I_{1,2}=50\mu A$, $I_{omax}=100mA$

At $I_o=I_{omax}$, M_P is at the edge of active region, and

$$\left(\frac{W}{L}\right)_P = \frac{2\times 100m}{35\mu\times 0.2^2} = \frac{50,000\mu m}{0.35\mu m}$$

The gate capacitance C_P and gate-drain overlap capacitance C_{gdoP} ($=C_d$) depends on the load current I_o:

I_o	C_P	C_d
0.1mA	9.5pF	10pF
1mA	12.5pF	10pF
10mA	50pF	13pF
100mA	50pF	13pF

Simple LDR: Diff Pair Parameters

Consider the pass transistor to operate at I_{omax}=100mA first. To achieve $\lambda_n=|\lambda_p|$=0.1/V, L_n=0.5μm, and L_p=1μm, and

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2\times 50\mu}{110\mu\times 0.2^2} \approx \frac{12\mu m}{0.5\mu m}$$

$$\left(\frac{W}{L}\right)_{3,4} = 3\left(\frac{W}{L}\right)_{1,2} \approx \frac{67.5\mu m}{1\mu m}$$

$$g_{m1,2} = \frac{2\times 50\mu}{0.2} = 500\mu \text{ A/V}$$

$$r_{ds2,4} = \frac{1}{0.1\times 50\mu} = 200k\Omega$$

$$A_1 = 500\mu\times 100k = 50 \text{ V/V} \quad (34dB)$$

$$p_a = \frac{1}{63p\times 100k} = 160k \text{ rad/s}$$

Simple LDR: Output Stage Parameters

Consider I_{omax}=100mA and R_{ESR}=100mΩ:

$$g_{mP} = \frac{2\times 100m}{200m} = 1A/V$$

$$r_{dsP} = \frac{1}{0.25\times 100m} = 40\Omega$$

(L of M_P is 0.35μm, and $|\lambda_P|$=0.25/V)

$$R_L = \frac{2.5}{100m} = 25\Omega$$

$$A_2 = 1\times 15.4 = 15.4\ V/V \quad (23.7dB)$$

$$z_{ESR} = \frac{1}{10\mu\times 100m} = 1M\ rad/s$$

$$p_o = \frac{1}{10\mu\times 15.4} = 6.5k\ rad/s$$

and

$$T(s) = \frac{385(1+s/1M)}{(1+s/6.5k)(1+s/160k)}$$

Simple LDR: T(s) at Lower Currents

The output stage is affected by I_o. Let $I_o = f \times I_{omax}$, and

$$g_{mP}' = \sqrt{2 I_o \mu_p C_{ox} (W/L)_P} = \sqrt{f} \times g_{mP}$$

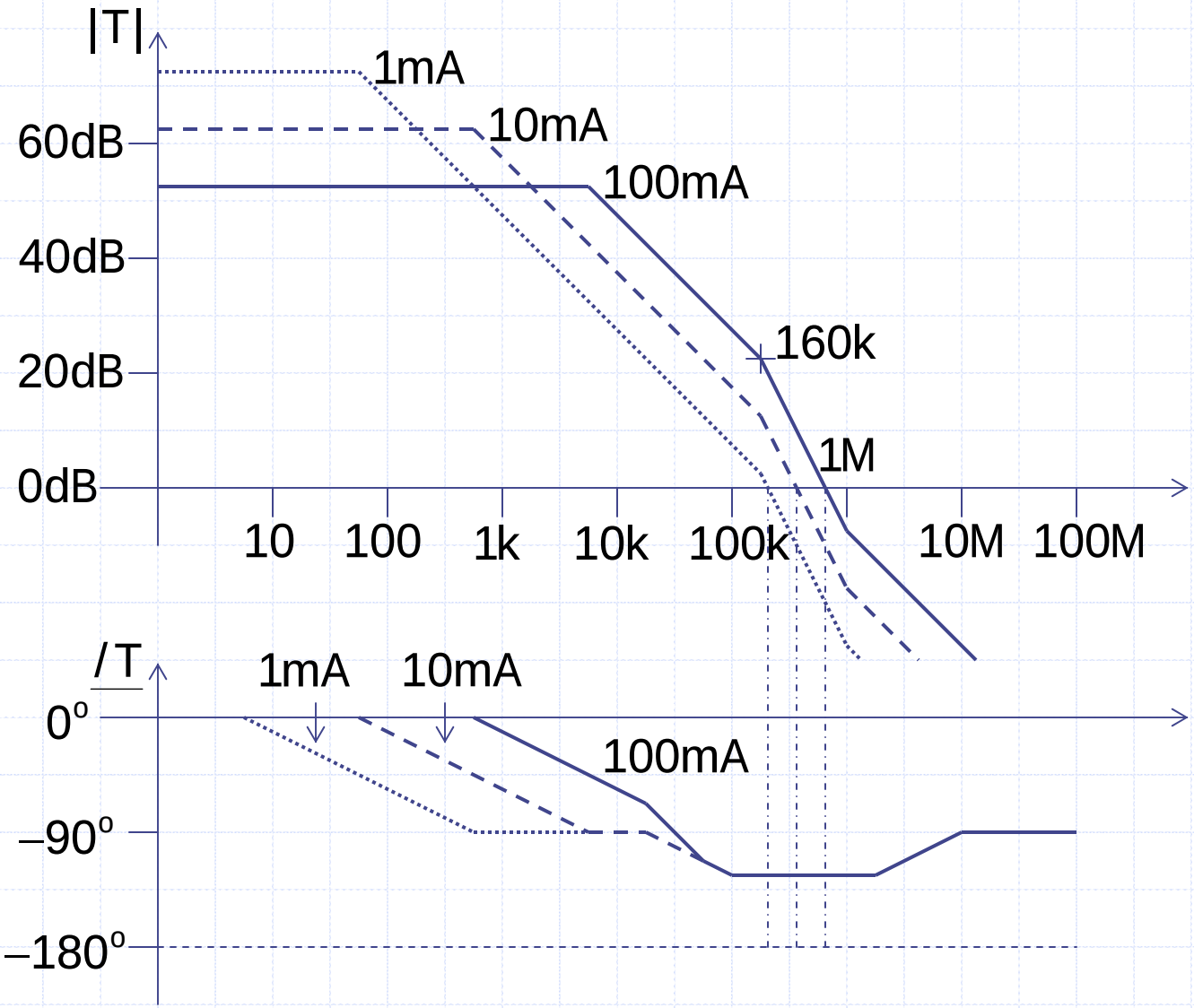
$$R_o' = (R_L' || r_{dsP}') = R_o / f$$

The loop gain function is then given by

$$T'(s) = \frac{(T_o / \sqrt{f})(1 + s/z_{ESR})}{[1 + s/(f \times p_o)](1 + s/p_a)}$$

I_o	T(s)
1mA	$\frac{3850(1 + s/1M)}{(1 + s/65)(1 + s/160k)}$
10mA	$\frac{1217(1 + s/1M)}{(1 + s/650)(1 + s/160k)}$
100mA	$\frac{385(1 + s/1M)}{(1 + s/6.5k)(1 + s/160k)}$

Simple LDR: Bode Plots of T(s)



Simple LDR: Computation vs Simulation

Computation:

I_o	T_o	UGF	ϕ_m
1mA*	71.5dB	32kHz	55°
10mA	61.5dB	57kHz	55°
100mA	51.5dB	100kHz	55°

Simulation:

I_o	T_o	UGF	ϕ_m
1mA*	57.1dB	13kHz	70°
10mA	56.2dB	46kHz	40°
100mA	45.8dB	94kHz	42°

* At 1mA M_P is in sub-threshold and resulted in large discrepancy.

Simple LDR: Remarks

(1) To maintain stability, a relatively large output capacitor C_L is used.

(2) A relatively large ESR (100mΩ) is needed to achieve a marginal phase margin (around 45^o).

(3) The gate-drain overlap capacitance C_d is miller multiplied by the gain of the output stage, but the gain is too low to affect the dominant pole p_o. However, the pole p_a should be modified to $1/(C_P+C_d)R_a$ for better accuracy.

(4) For low output current, the pass transistor enters sub-threshold region. A more accurate small signal model should take this into account.