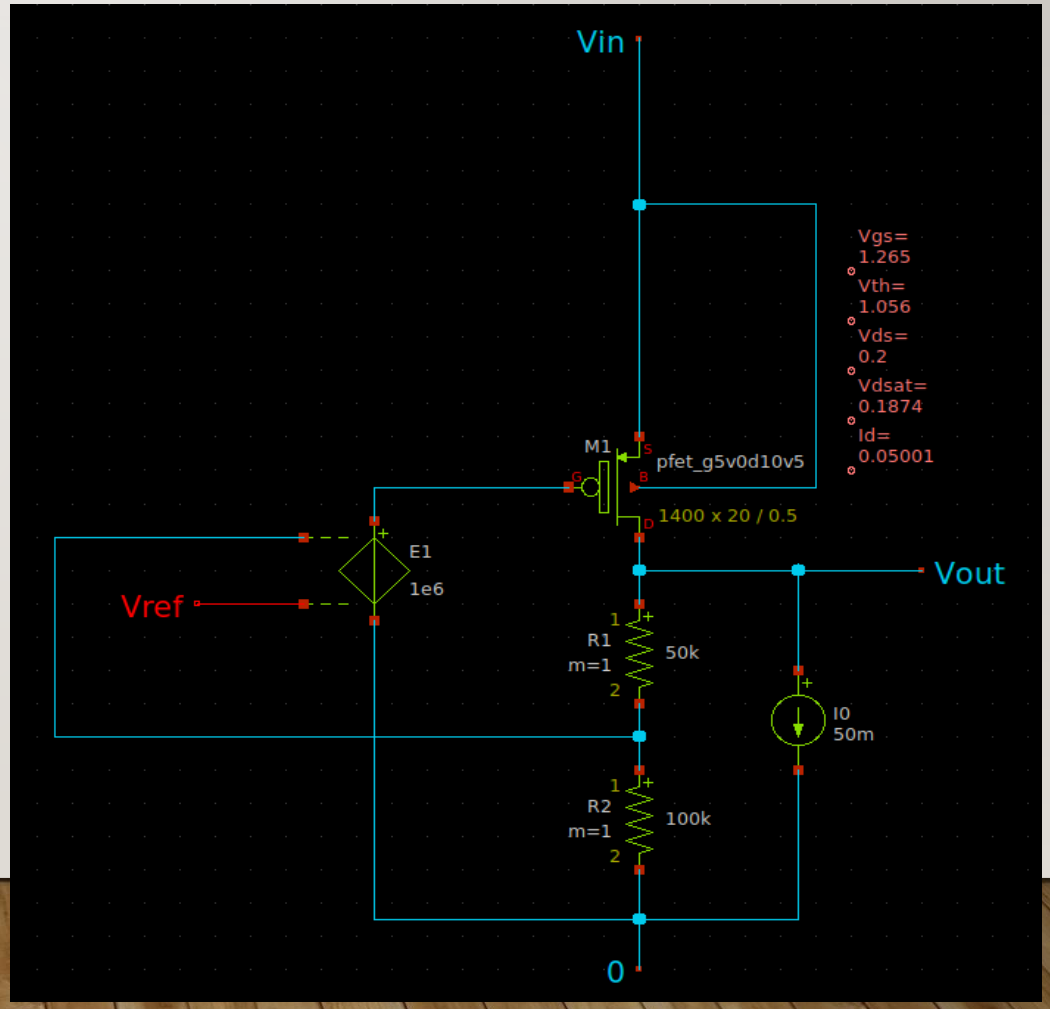
LDO DESIGN

PASS TRANSISTOR DESIGN

- I put the pass transistor in a feedback loop with the ideal amplifier and sweep W until it operates in saturation when Vin = 2v
  - Vref=1.2v
  - ILoad = 50mA
  - Vout = 1.8v
  - L=Lmin=0.5um

- I got W= 1400*20 um

vdsat	0.187436
vth	1.05642
id	0.050012
ibd	-2.8019e-10
ibs	-7.2801e-16
gbd	1.40002e-09
gbs	1.40548e-09
isub	8.63181e-16
igidl	0
igisl	0
igs	0
igd	0
igb	0
igcs	0
igcd	0
vbs	-5.17979e-07
vgs	1.26451
vds	0.199998



ERROR AMPLIFIER DESIGN

- I assume the requirement as follows:

Av > 50 dB

GBW > 30 MHz

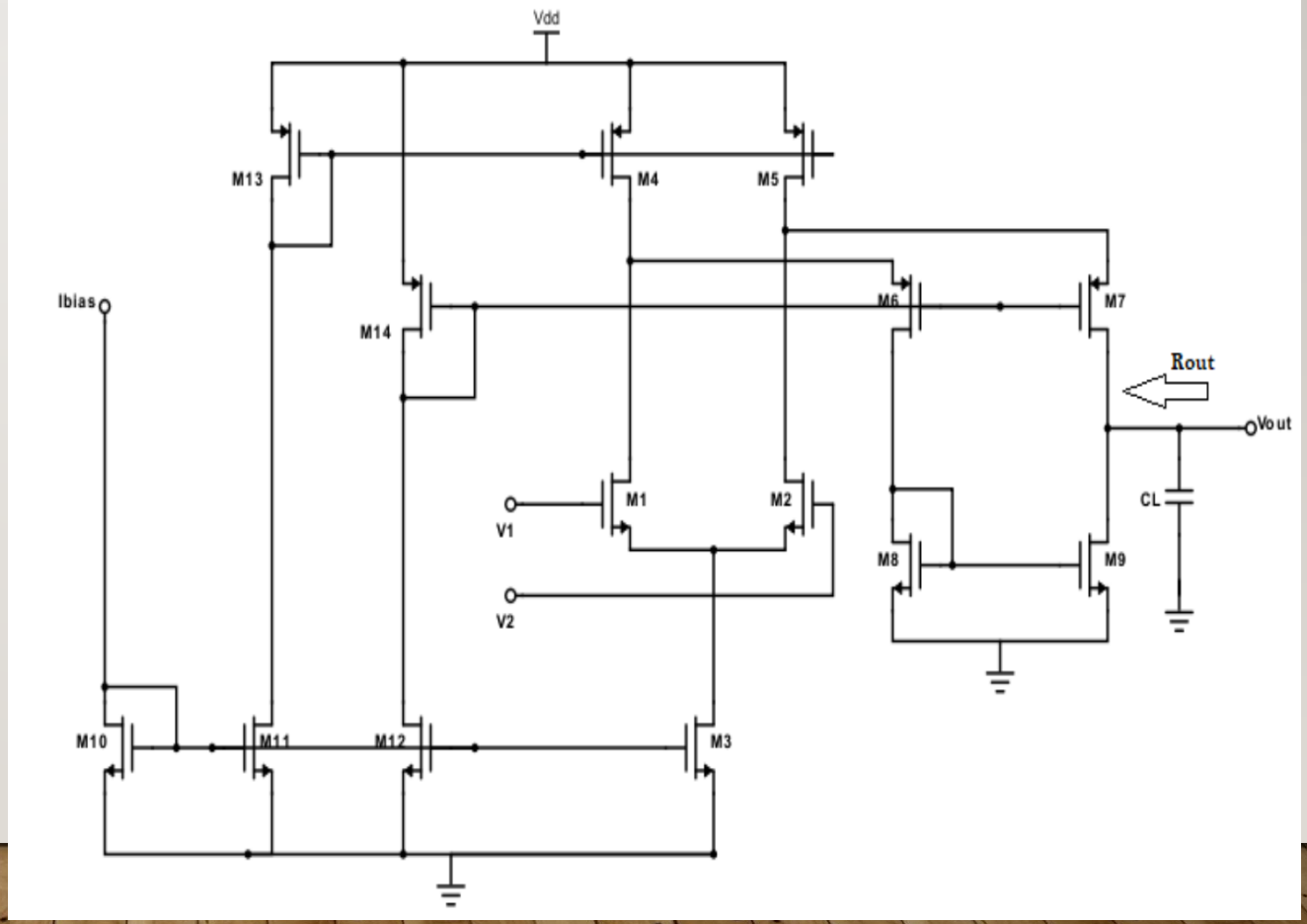
ICMR [0.8v - 1.6v]

SR = 20v/usec

Cl=1pf

Vdd = 2v

Power dissipation < 1mW



ERROR AMPLIFIER DESIGN

1- I1=I2=I3/2=Ibias/2 , I4=I5=1.5*I3 and I6-9=I4-I1

2- From SR I got Ibias

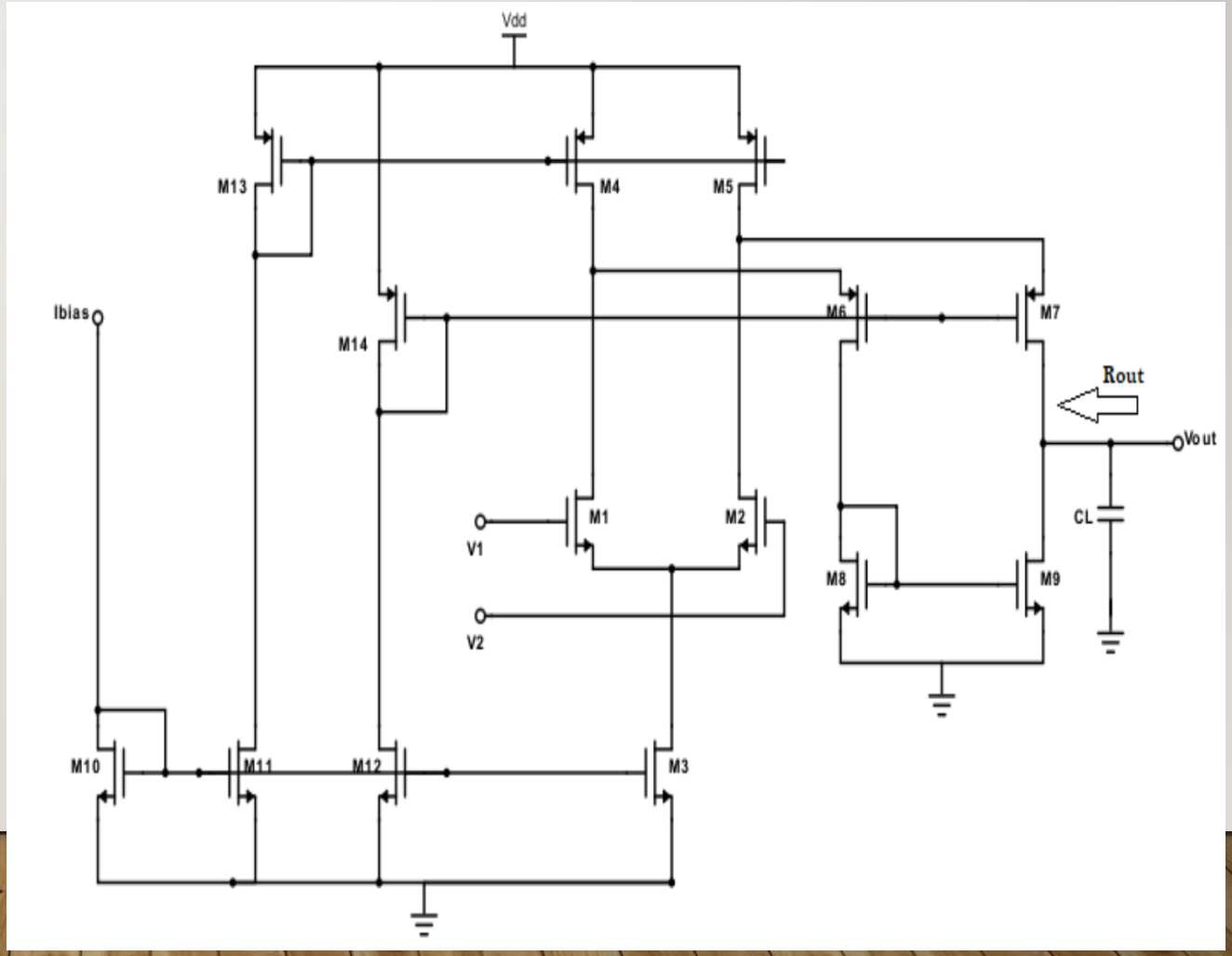
3- From GBW I got W/L)1,2

4- From ICMR- I got W/L)3

5- From ICMR+ I got W/L)4,5

6- I got W/L)6-9 that handle worst-case currents of I5

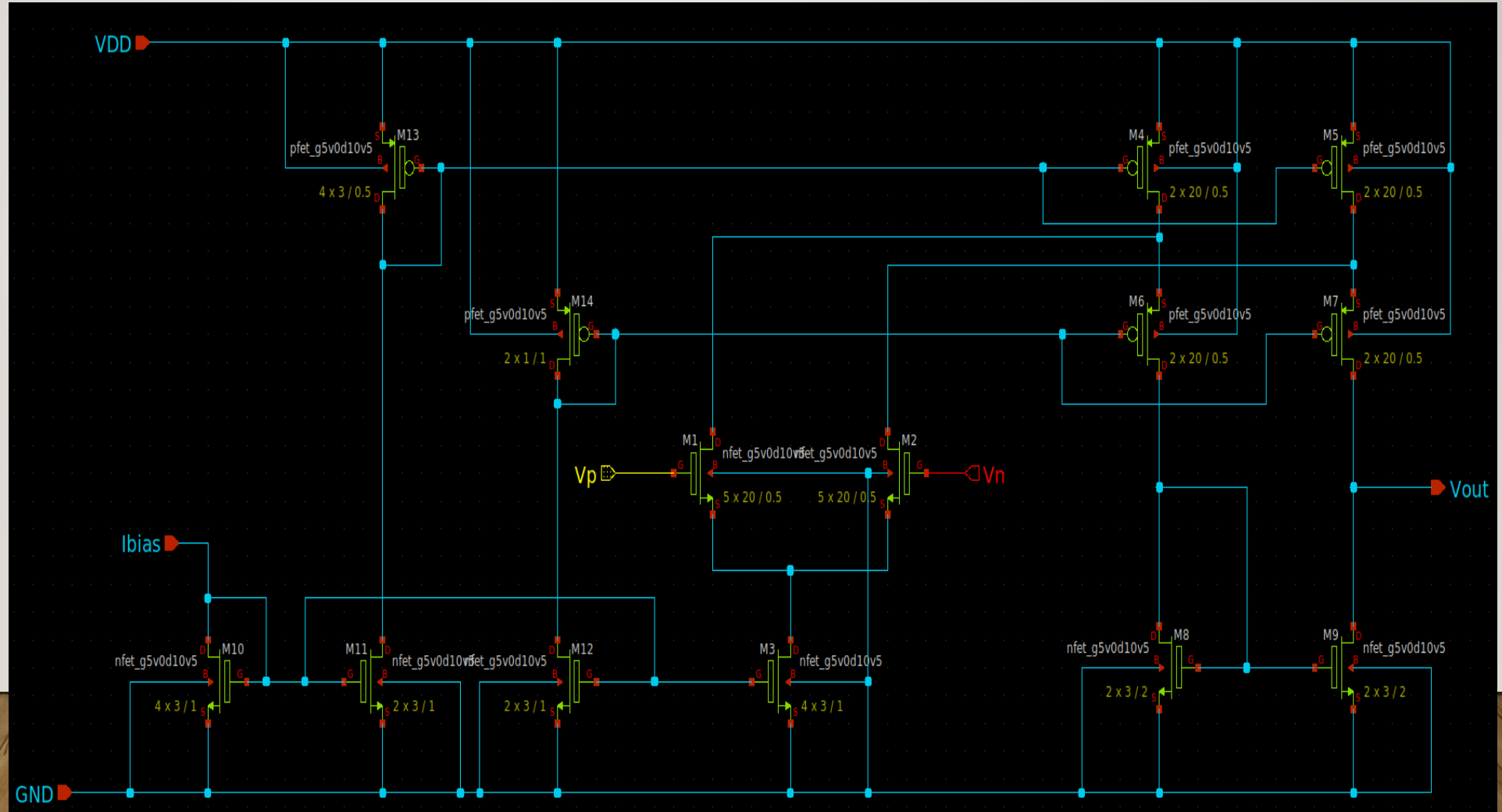
7- I got W/L)10-14 using current ratios



ERROR AMPLIFIER DESIGN

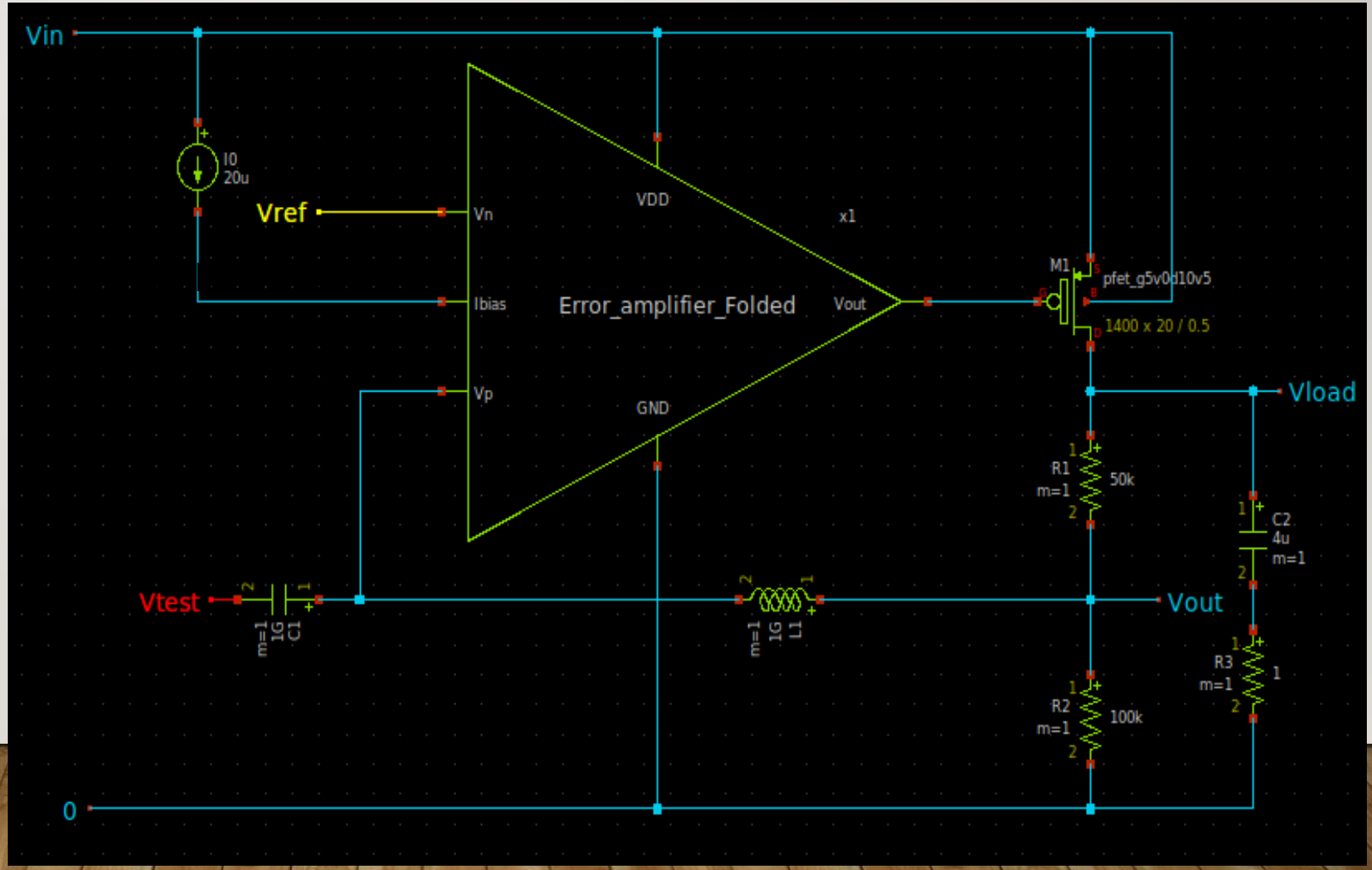
- Open loop results

@Vcm=1.2v
Adm = 55 dB
GBW= 47 MHz
Acm = -32 dB



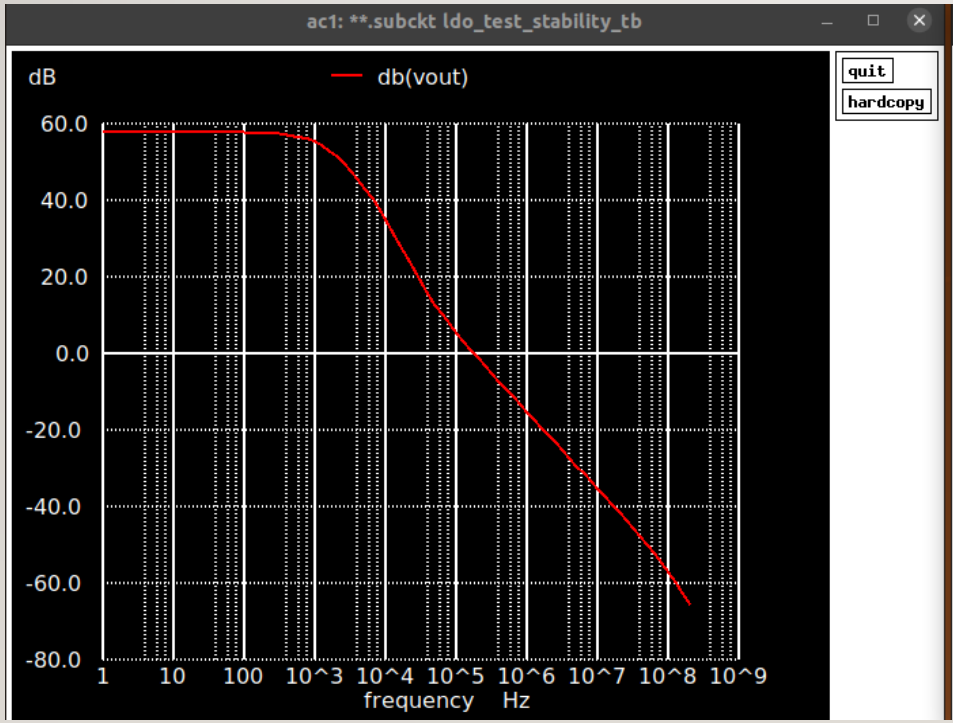
LDO STABILITY

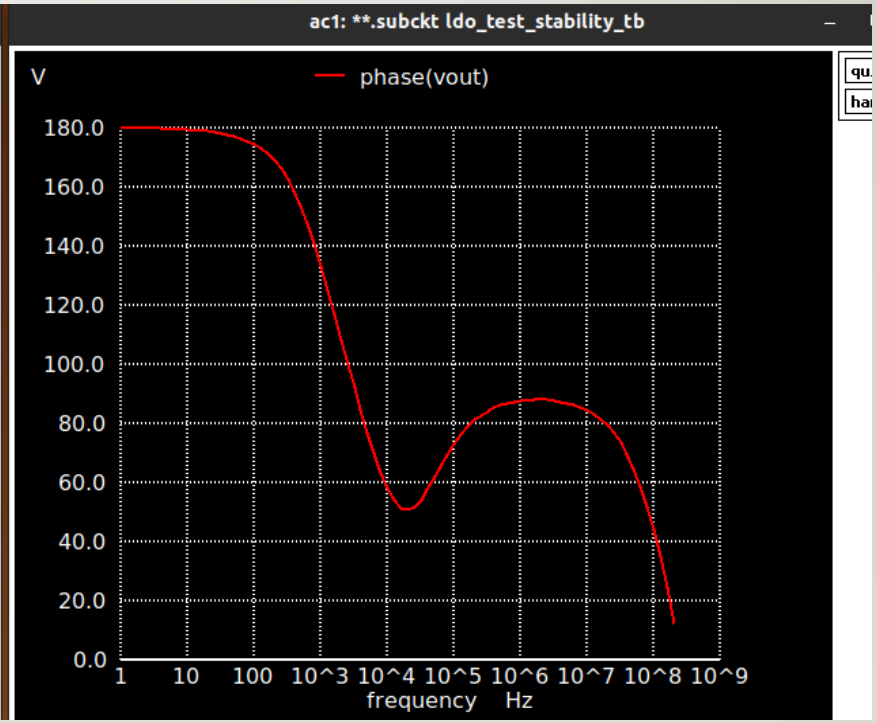
- I put the error amplifier in the loop to check stability
- I first checked at 50mA load and 2v supply (worst case)
- The optimum values of Co was 4uF and RESR=1ohm
- Av= 57.7dB, GBW = 177 KHz and PM = 80 deg



LDO STABILITY

@ 50mA load and 2v supply

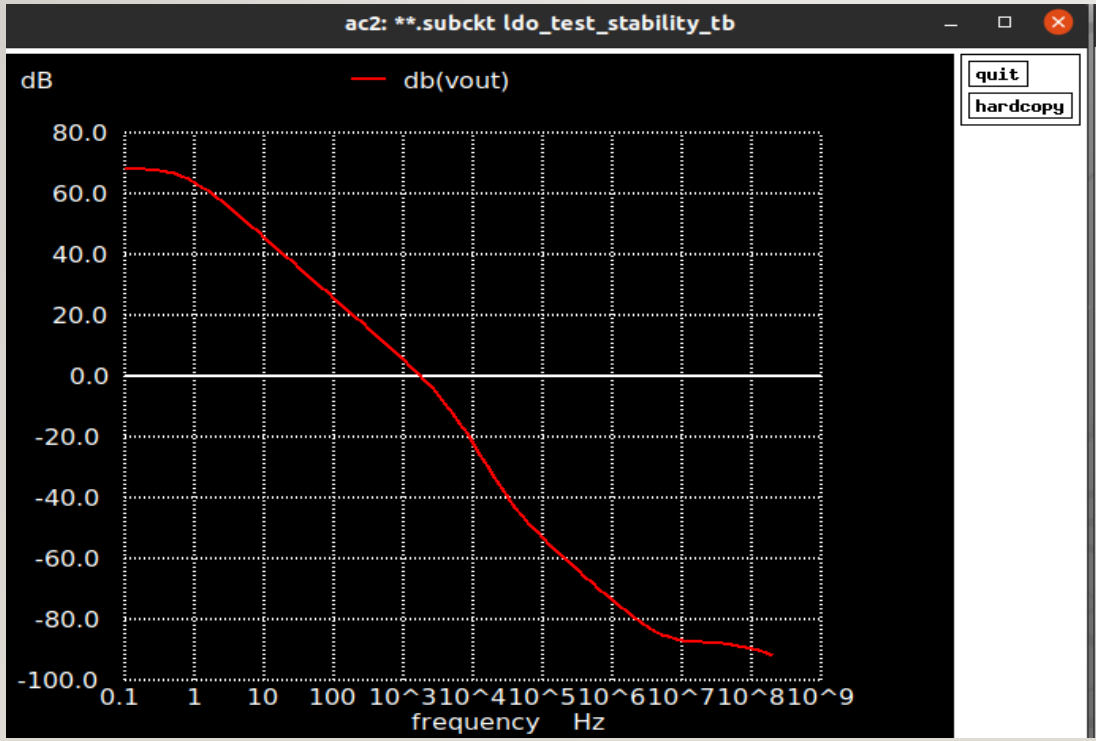


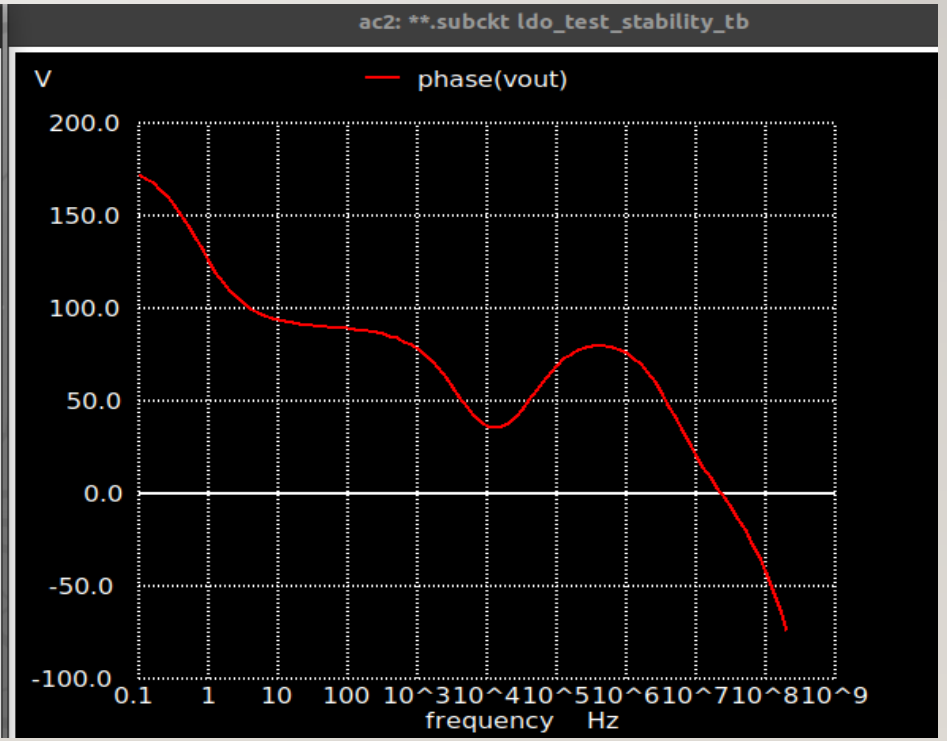



```
avd                =  5.775411e+01
gbw                =  1.767798e+05
pm                 =  7.995047e+01
```

LDO STABILITY

@ no load and 2v supply

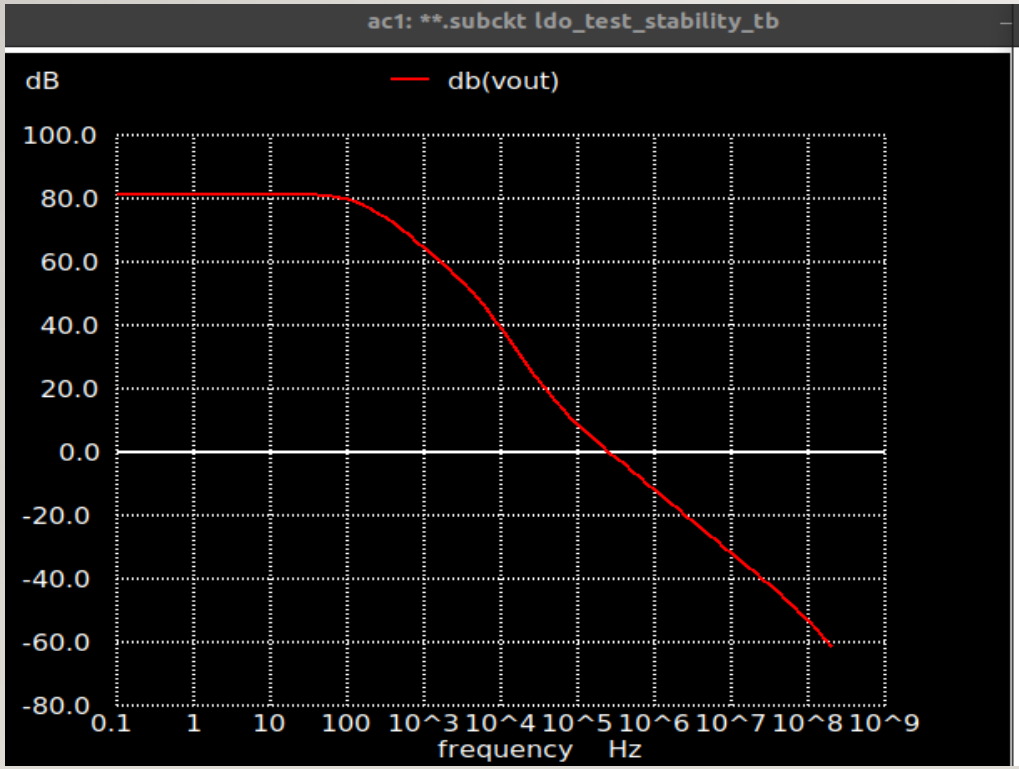


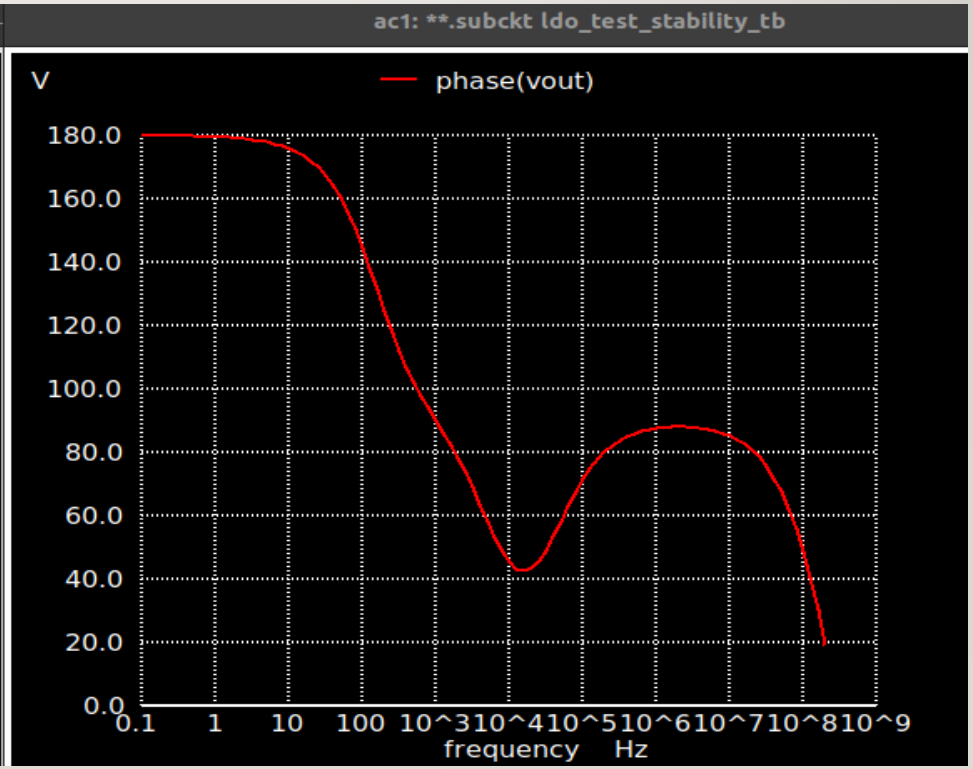



```
avd                =  6.376034e+01
gbw                =  1.762841e+03
pm                 =  6.990220e+01
```

LDO STABILITY

@ 50mA load and 3.6v supply

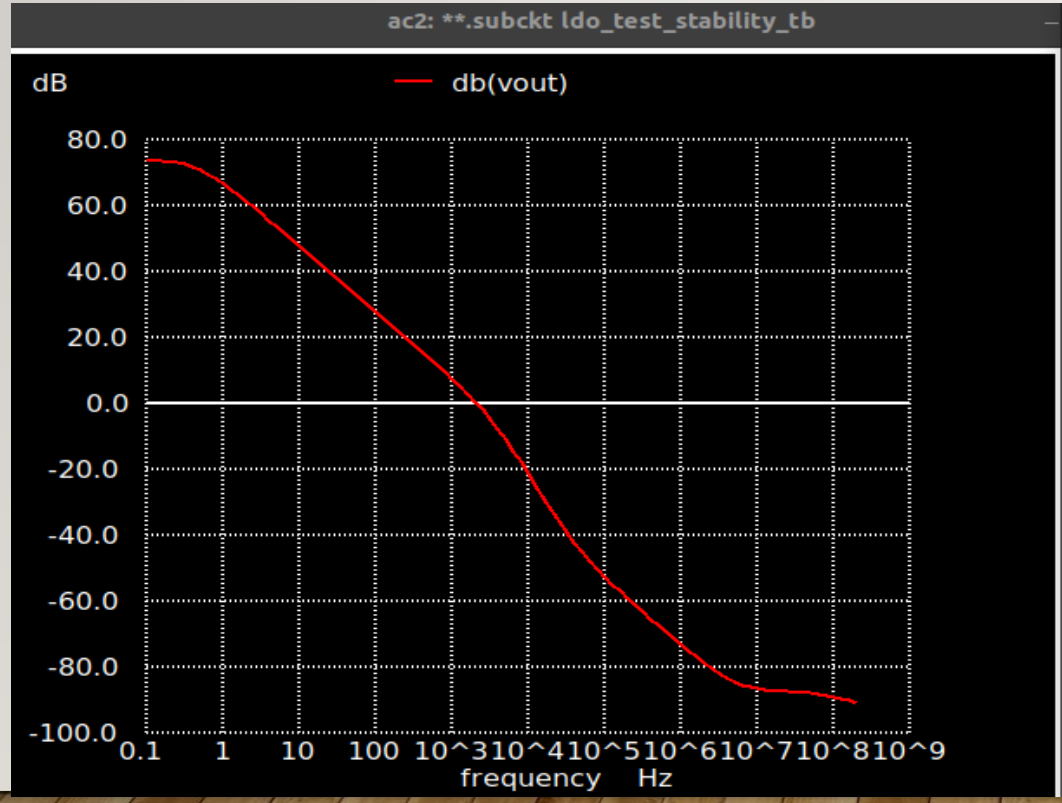


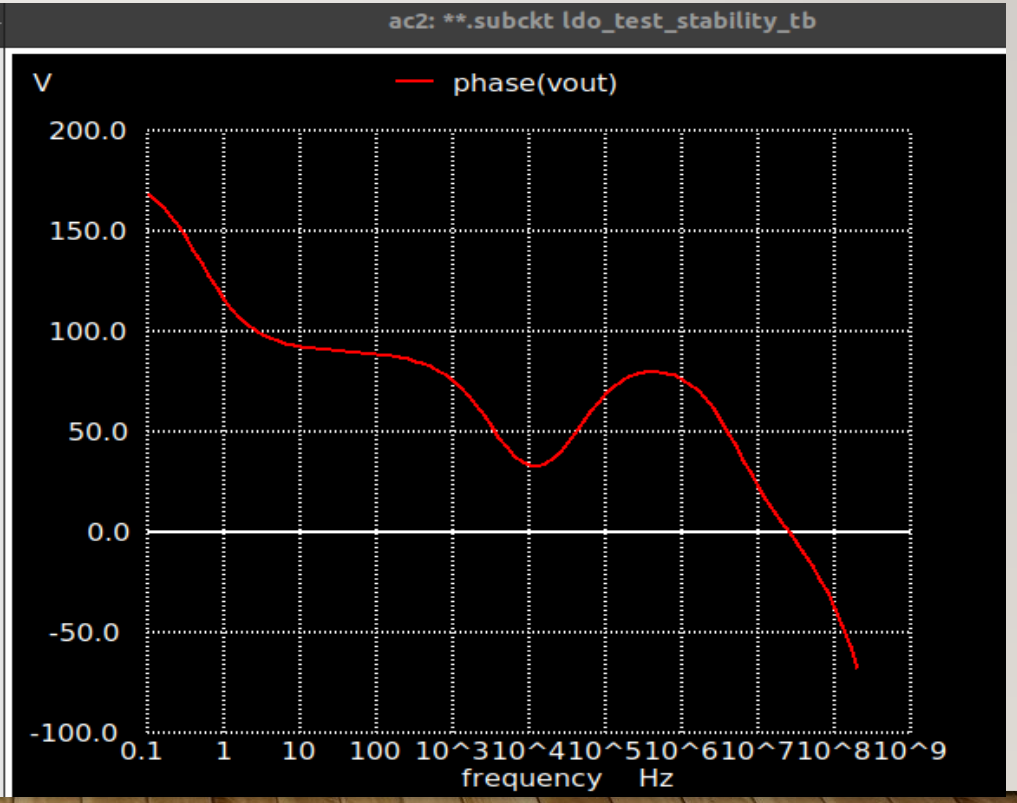



```
avd                    =  8.150401e+01
gbw                    =  2.584139e+05
pm                     =  8.242524e+01
```

LDO STABILITY

@ no load and 3.6v supply





avd	=	6.683176e+01
gbw	=	2.105604e+03
pm	=	6.223042e+01

DROPOUT VOLTAGE

@max load 50mA I started from Vsup = 2v and decreased it with little step until pass transistor was in triode region then got Vdo = 0.2V

@no load I made the same method but this time Vdo = 50mV

- Note: I made this simulation manually as there is no region parameter for the mosfet in ngspice.

LINE REGULATION

- I swept the input voltage from 2v to 3.6v and plotted the output for different load conditions 0,100uA,1mA,10mA and 50mA.
- I measured line regulation for the five previous cases: -
- Using the equation (Vmax-Vmin)/(1.8*1.6)

```
vmin              =  1.801394e+00
vmax              =  1.807411e+00
Line_Regulation @ 0 = 0.00208924
```

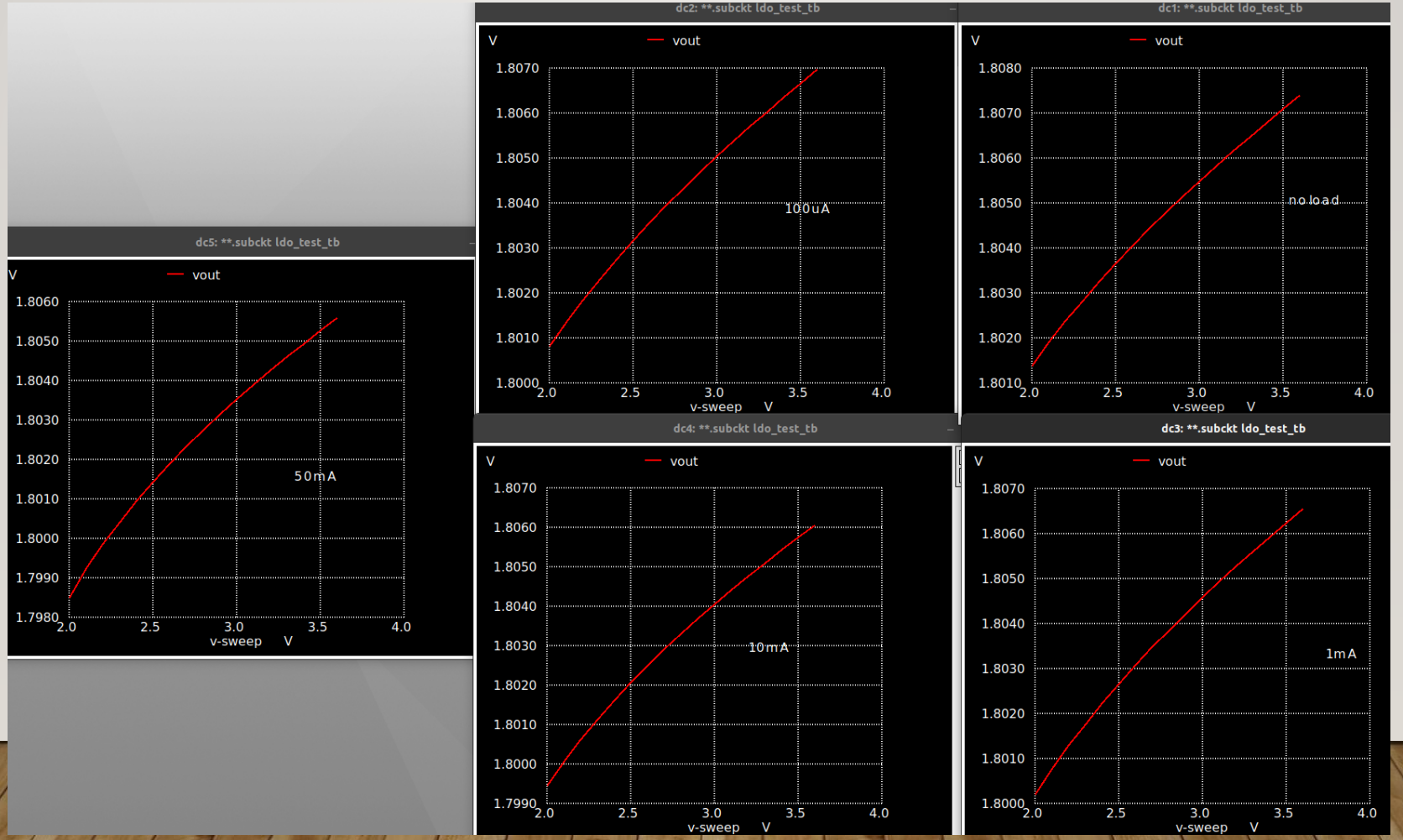
```
vmin              =  1.800822e+00
vmax              =  1.806982e+00
Line_Regulation @ 100u = 0.00213889
```

```
vmin              =  1.800216e+00
vmax              =  1.806555e+00
Line_Regulation @ 1m = 0.00220104
```

```
vmin              =  1.799453e+00
vmax              =  1.806069e+00
Line_Regulation @ 10m = 0.00229722
```

```
vmin              =  1.798509e+00
vmax              =  1.805600e+00
Line_Regulation @ 50m = 0.00246215
```

LINE REGULATION



LOAD REGULATION

- I swept the load from 0 to 50mA and plotted the output for different input conditions 2v, 2.5v, 3v and 3.6v.
- I measured load regulation for the four previous cases: -
- Using the equation (Vmax-Vmin)/(1.8*50m)

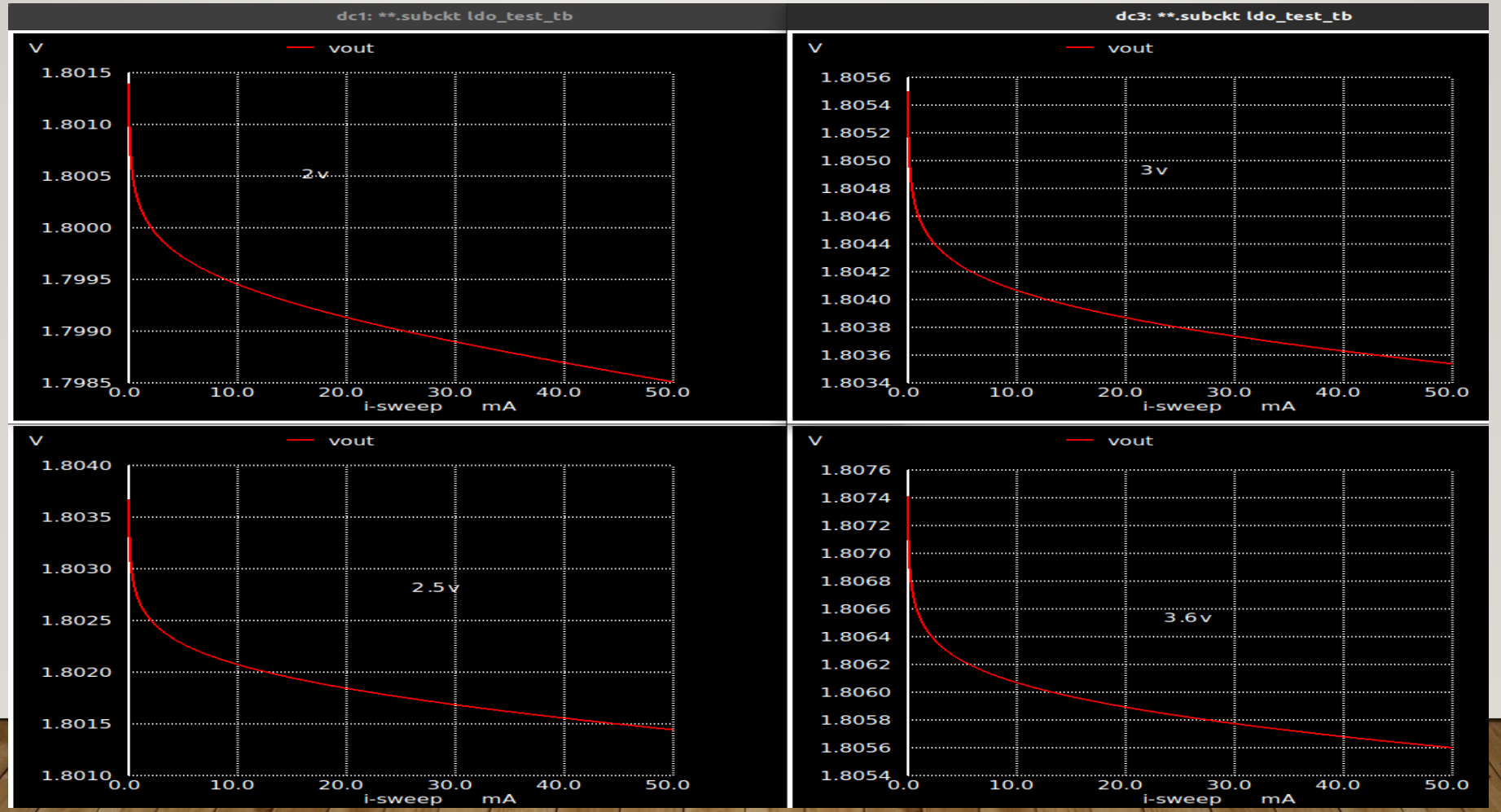
```
vmin                =  1.798509e+00
vmax                =  1.801394e+00
Load_Regulation @ 2 = 0.0320556
```

```
vmin                =  1.801443e+00
vmax                =  1.803669e+00
Load_Regulation @ 2.5 = 0.0247333
```

```
vmin                =  1.803537e+00
vmax                =  1.805498e+00
Load_Regulation @ 3 = 0.0217889
```

```
vmin                =  1.805600e+00
vmax                =  1.807411e+00
Load_Regulation @ 3.6 = 0.0201222
```

LOAD REGULATION



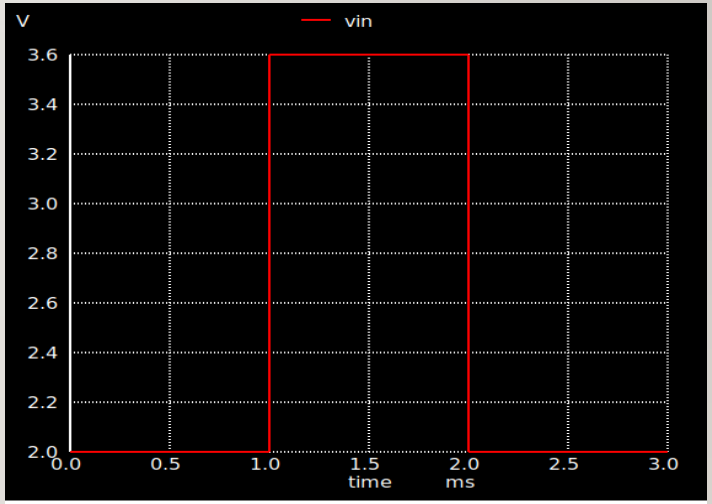
LINE TRANSIENT

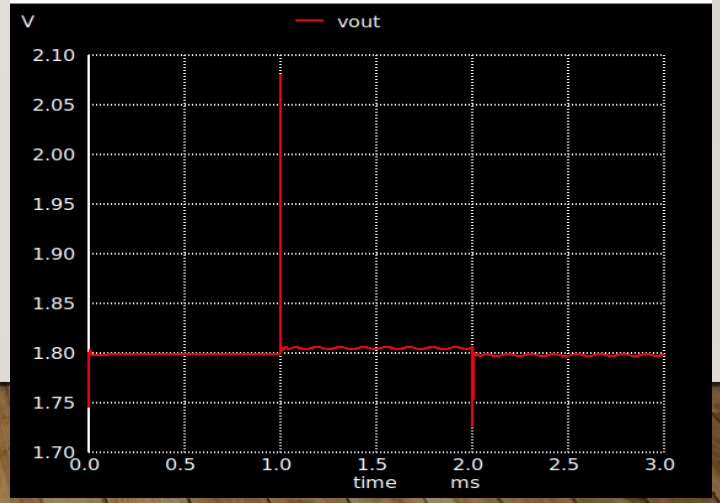
- I applied an input voltage pulse from 2v to 3.6v

with 1msec width and 1nsec rise and fall time

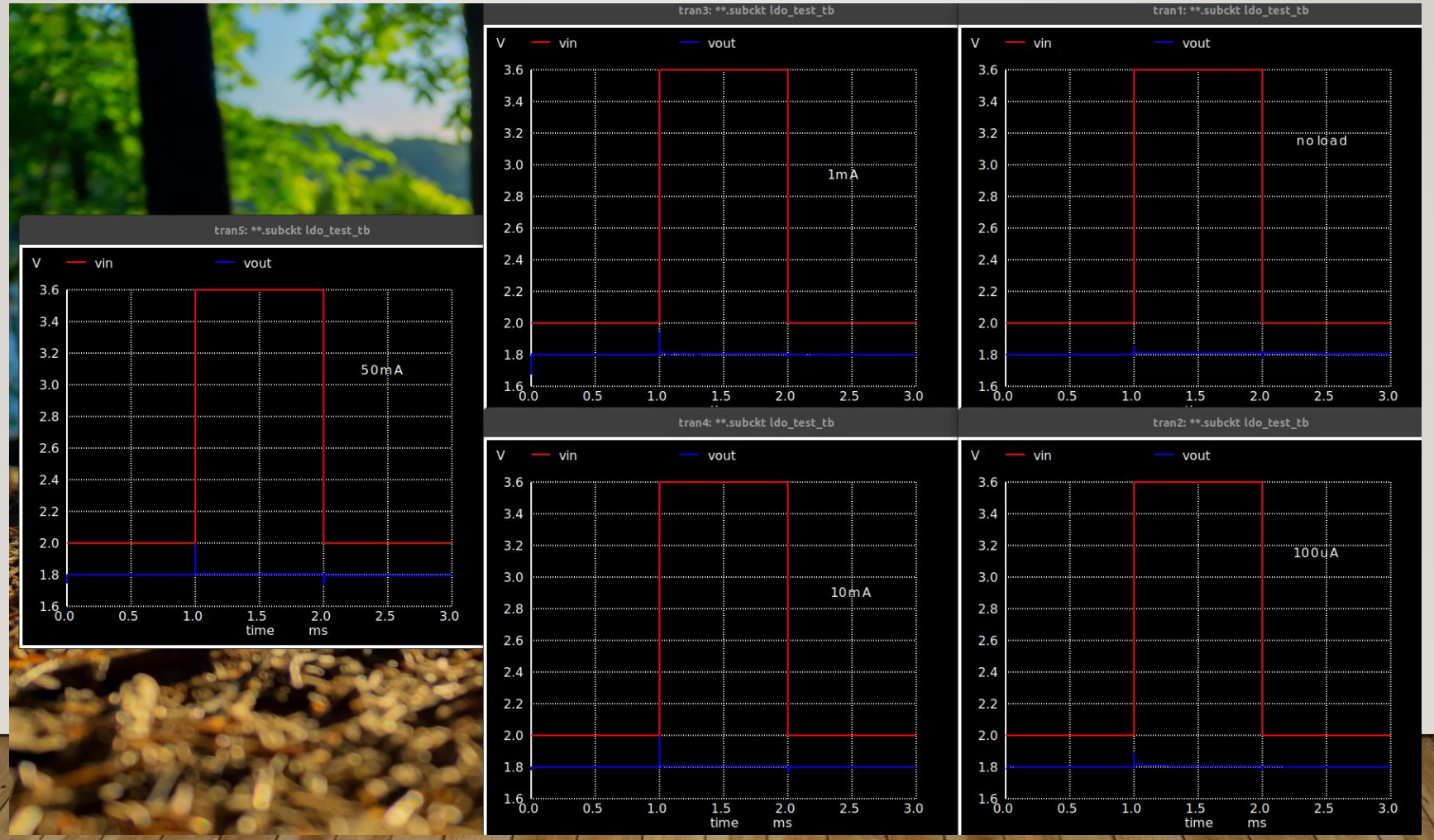
and simulated the circuit under the previous five load cases.

- The showed curve is under 50mA load.
- All the cases are plotted in next slide.





LINE TRANSIENT



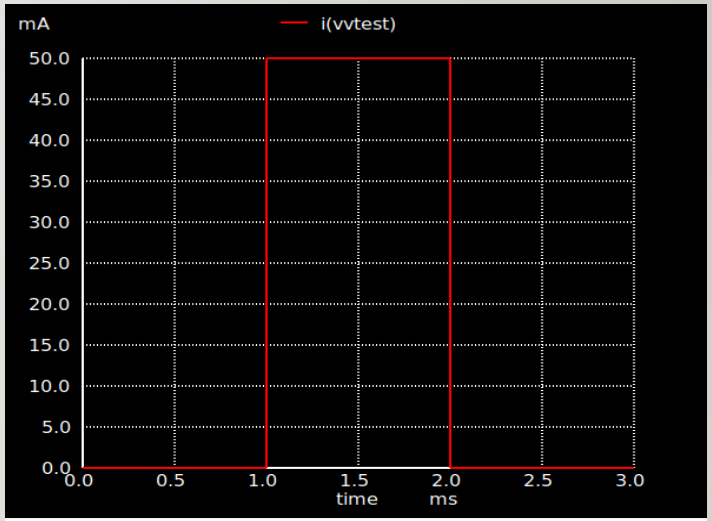
LOAD TRANSIENT

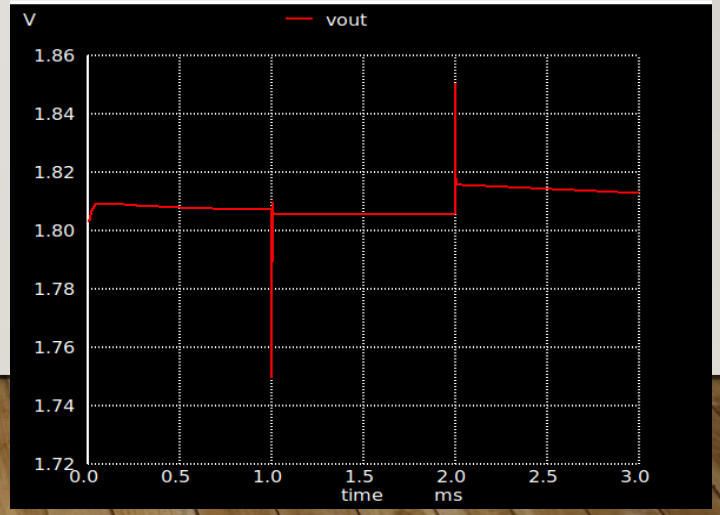
- I applied a load current pulse from 0 to 50mA

with 1msec width and 1nsec rise and fall time

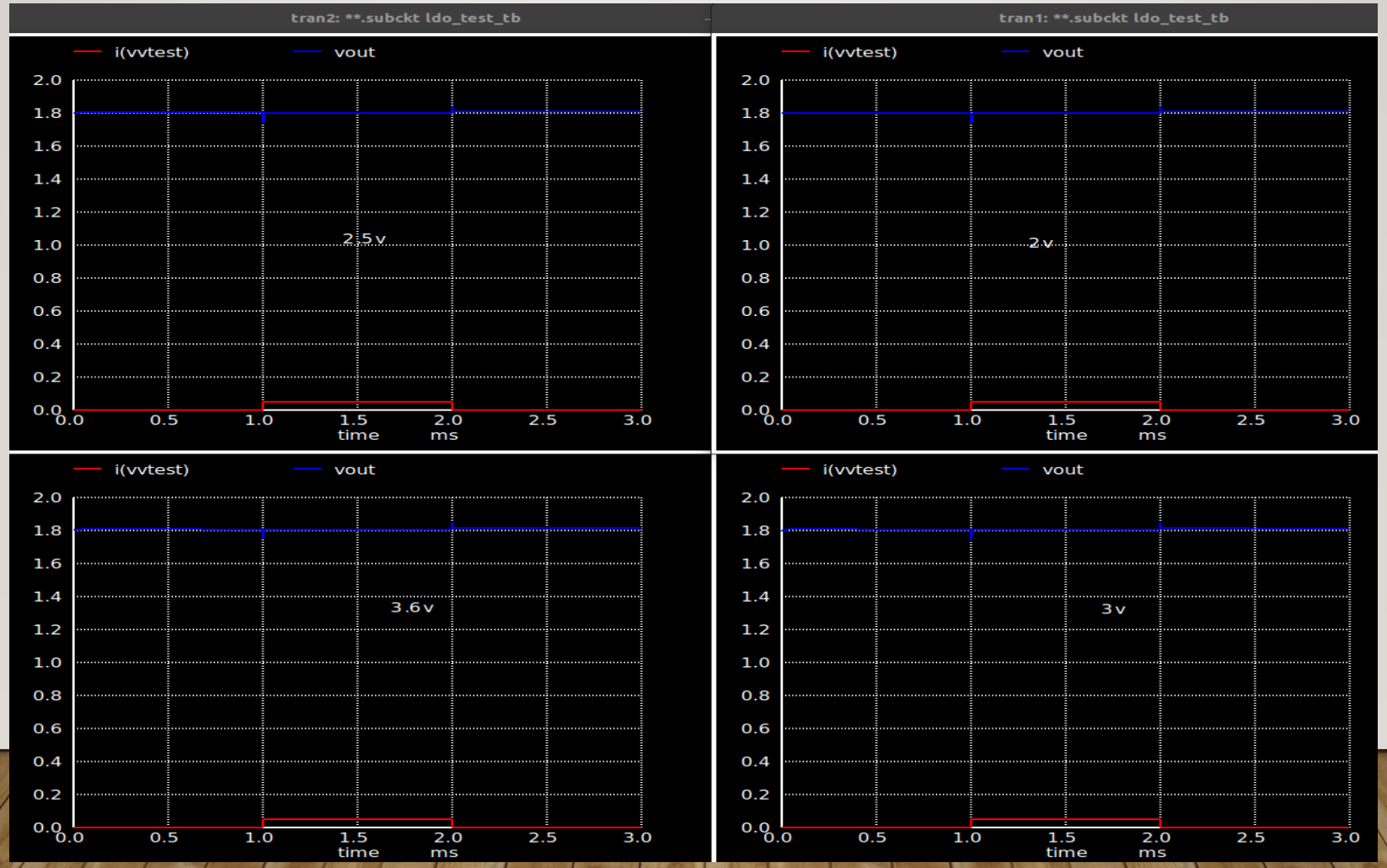
and simulated the circuit under the previous five load cases.

- The showed curve is with 3.6v input.
- All the cases are plotted in the next slide.

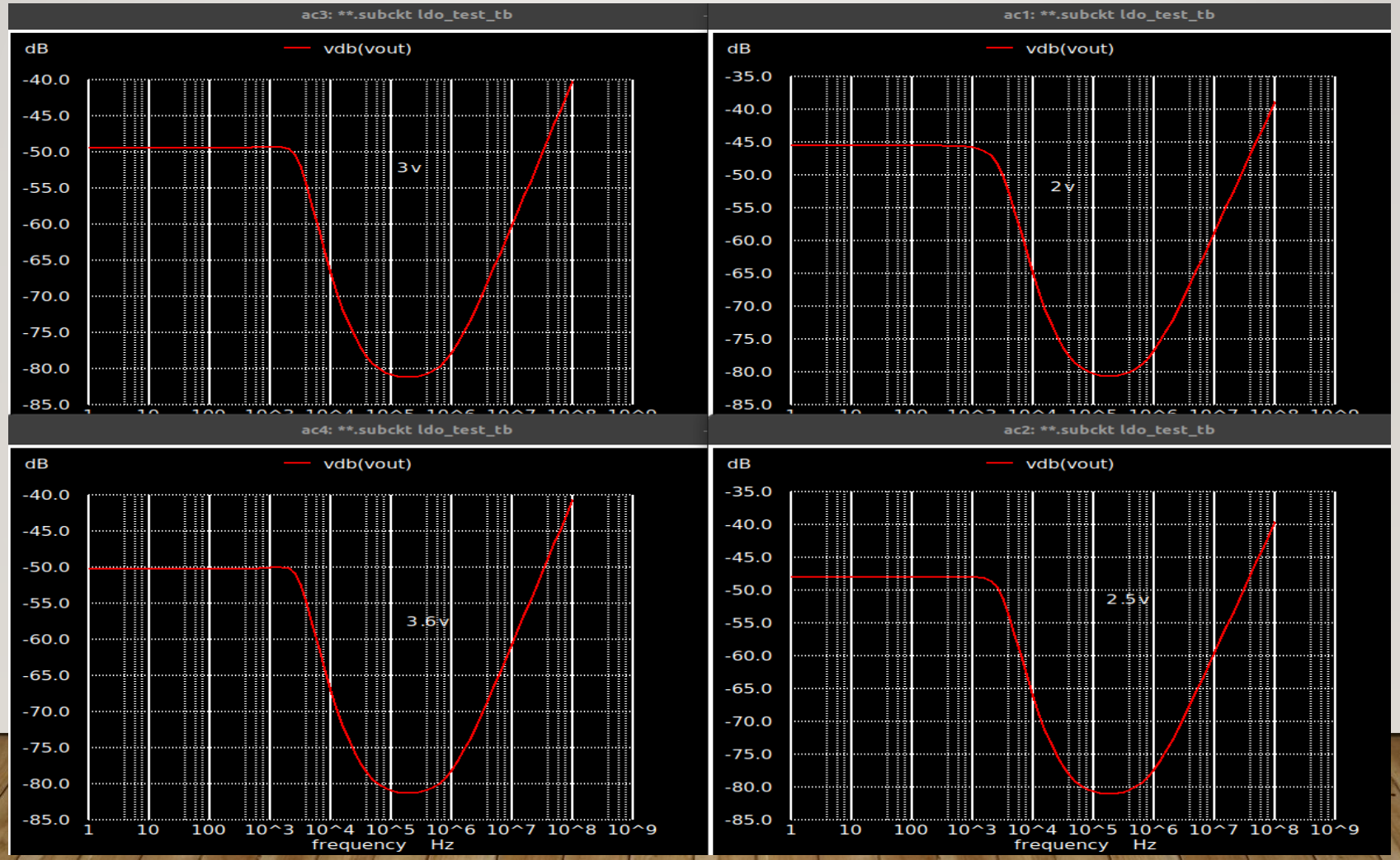




LOAD TRANSIENT



POWER SUPPLY REJECTION

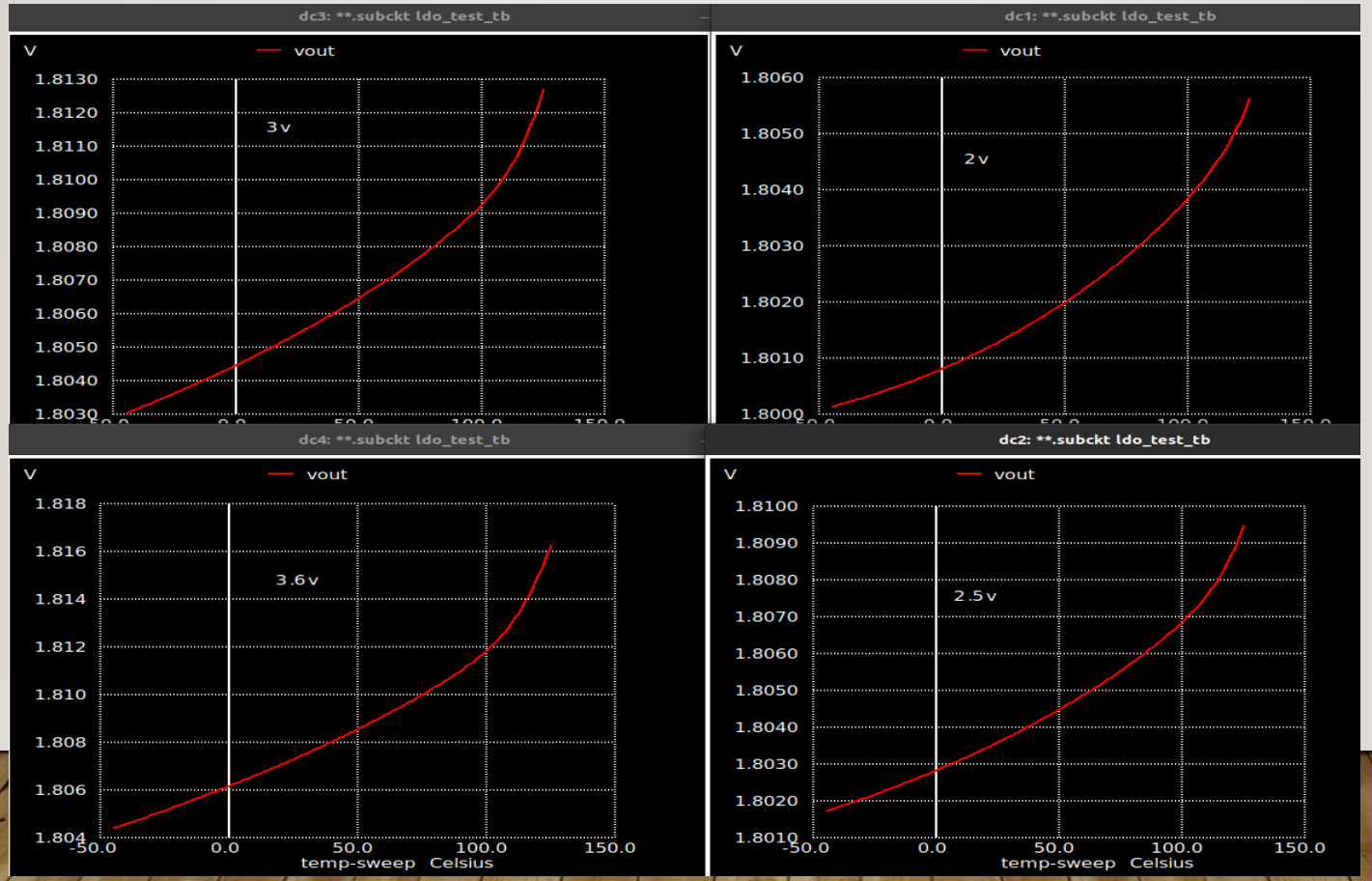


QUIESCENT CURRENT

- I swept the load from 0 to 50mA and measured the current at no load for different input voltages and It was approximately 100uA in all cases.

TEMPERATUREVARIATIONS

- I swept temperature from –45 deg to 125 deg at no load.



TEMPERATUREVARIATIONS

- I swept temperature from –45 deg to 125 deg at 50mA load.