Folded cascode OTA design

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Project Work

Analysis of folded-cascode OTA in a 22 nm CMOS Technology

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I. Introduction

Operational Transconductance Amplifier (OTA) is one of the most versatile and integral part in analog and mixed circuit applications mainly in Delta-Sigma modulators. The CMOS OTA is the main power consuming block and used to realize complex functions like integrators, comparators, high speed amplification or filtering etc [1]. One such important type of OTA is 'Folded-cascode OTA' (FC-OTA). This topology provides high gain, good input common mode level, better output swing, high bandwidth and offers self-compensation.

Several steps are necessary in designing an operation amplifier (op amp): starting from extracting the model parameters for given technology, analysing specifications, selection of topology, design of schematic as per calculations, design of test benches for the performance evaluation and finally some iterative CAD simulations to optimise the designed circuit. These are the ample steps taken to design analog integrated circuits (IC) at the initial phase [2]. However, the complete design of IC includes layout, it's verification and recheck from post-layout simulations.

II. Folded-cascode OTA

The optimization of telescopic cascode op amps on limited output swings and input/output common mode levels lead to the emergence of folded-cascode op amp. The FC-OTA provides a large dc gain from a single stage due to high output impedance and input transconductance of the differential pair. The former also makes the FC-OTA suitable for driving mainly capacitive loads, they can also drive resistive loads in feedback topology [4]. A common source input stage converts an input voltage to current, the current is then applied to common gate cascode stage. It is important to note the usage of opposite pairs i.e. nmos (input) and pmos (cascode) or vice versa to maintain the same voltage bias levels at input and output [5].

A. Principle of folded-cascode topology

The basic methodology of folded-cascode consists of an n-channel input device folded down and changing the type to p-channel cascode as shown in Fig.1.

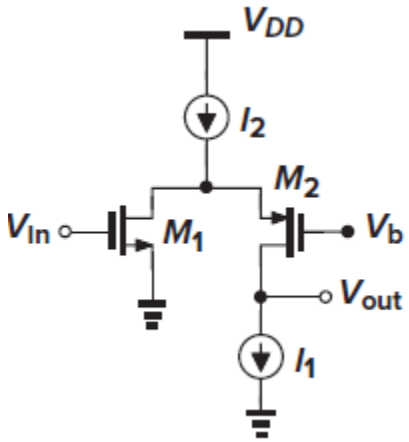

Fig.1: A simple folded-cascode structure [3]

In Fig. 1, I_2 is the total current flowing in the circuit, M1 & M2 are in common source and common gate configuration respectively. The input voltage is converted to current by M1, the signal path is then folded down and fed to M2. The current at drain of M2, I_{D2} is the difference between total current and current in M1, I_{D1}.

The operation is straight forward:

- when Vin < Vth1, M1 is off and M2 carries all of I_2 yielding Vout =(I_2+I_1)Rout.
- when Vin > Vth1, M1 turns on in saturation and caries a portion of I_2 yielding Vout = (I_{D2}+I_1)Rout, where I_{D2} = I_2-I_{D1}.
- when Vin further increases, all of I_2 flows through M1, I_{D1}=I_2.

From the square law equation for drain current [3], we can approximate the upper bound of the input voltage Vin as

$$\mathrm{Vin} = \sqrt{\frac{2I_2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + \mathrm{Vth} \qquad (1)$$

Where, μ_n is electron mobility for nmos, C_{ox} is oxide capacitance per unit area and (W/L) is known as aspect ratio of the transistor. If applied Vin is more the above limit, then M1 enters triode region [5].

B. Principle of Folded-cascode OTA

The folded-cascode topology discussed in previous section can be implemented to differential pairs, and hence also to op amps. As shown in Fig.2, the resulting circuitry consists of nmos differential pair M1-M2 at input stage with a pmos pair counterpart M6-M7 as cascode. This architecture uses a simple current mirror at load M8-M9 (usage of cascode current mirror types will be discussed later). The pmos current mirror M4-M5 acts as active load, their drains are connected to drains of M1-M2 to achieve higher common mode input range.

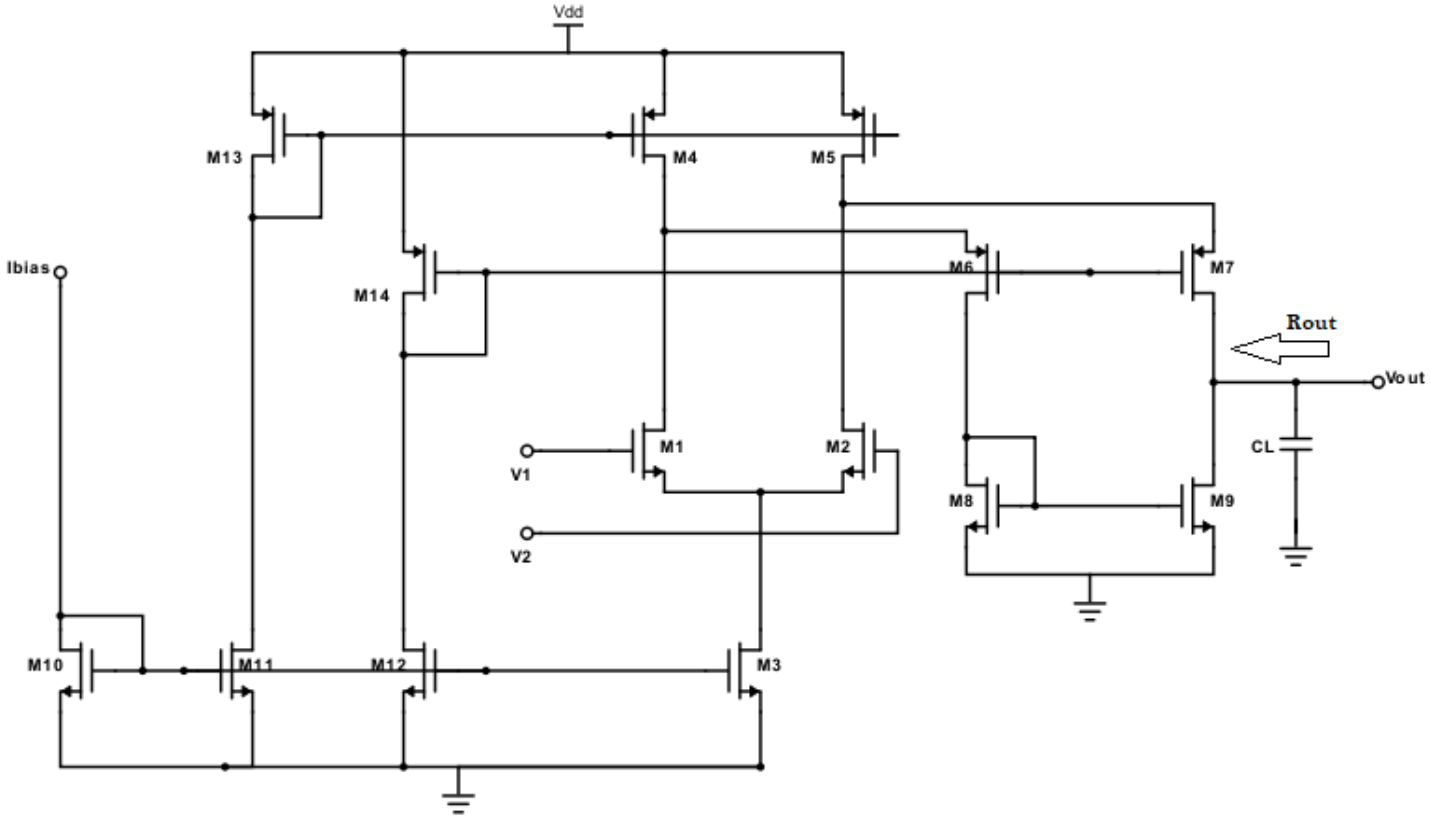

Fig.2: A folded-cascode OTA

A perfect balance of currents in the differential stage is not required as the excess current is steered into current mirror sink. Certainly, the bias currents I_4 and I_5 in the op amp must be designed higher than the tail current I_3 so that the dc current in the current mirror never goes to zero [2]. Usually, $I_4 = I_5 = (1.2 \text{ to } 2)\ I_3$. The bias currents in the cascode transistors M6-M7 are derived by current subtraction $I_6 = I_4 - I_1$. For proper establishment of these currents it is essential for both I_3 and I_4 to be derived from a single-bias network.

C. Small signal analysis

Using a small signal model, it is convenient to derive small-signal gain by intuitive analysis. A small voltage Vin, applied at the differential input will create small signal currents (i_d) in accordance with the transconductances of M1-M2. These drain currents reach the load capacitance C_L in two paths :

- Drain current of M1 passes directly from source to drain of M6 and reaches C_L.
- Drain current of M2 travels indirectly through M5, current mirror stage and then reaches C_L.

It is interesting to know that these two paths have minor variations in their transfer functions due to the poles exhibited by the current mirror [4]. A small-signal model is drawn based on the above assumptions.

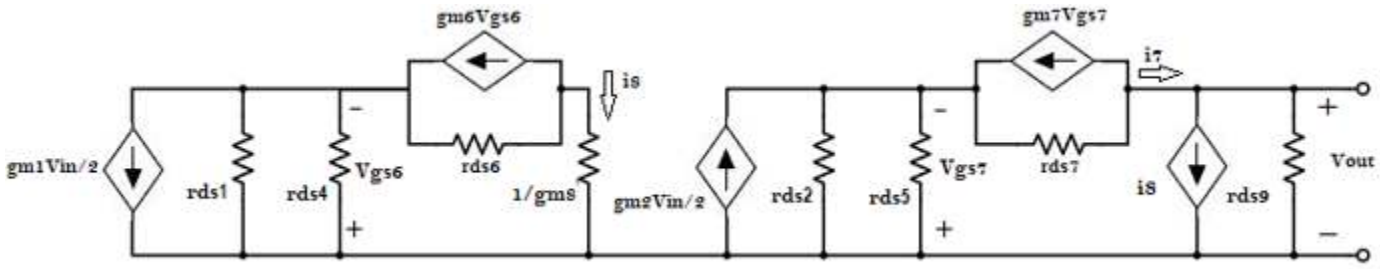

Fig.3: Small-signal model of Fig.2

The resistances looking into the sources of M6 and M7, are assigned as R_x and R_y to derive the transfer function of the two paths. On solving for the input resistance [2] looking into sources of cascode transistors M6 and M7, yields

$$R_x = \frac{r_{ds6} + {}^{1}/_{gm_8}}{1 + gm_6 rds_6} \approx \frac{1}{gm_6} \tag{2}$$

and

$$R_y = \frac{r_{ds7} + rds_9}{1 + gm_7 rds_7} \approx \frac{rds_9}{gm_7 rds_7} \tag{3}$$

Where *gm* is transconductance, *rds*=(1/gds) is output resistance of transistor. Using these equations, it is easier to write the small-signal voltage transfer function of Fig.3. The current i_8 is expressed as

$$i_8 = \frac{-gm_1\,(rds_1 || rds_4)\,Vin}{2[R_x + (rds_1 || rds_4)]} \approx \frac{-gm_1 Vin}{2} \tag{4}$$

and the current i_7 is written as,

$$i_7 = \frac{gm_2\,(rds_2 || rds_5)\,Vin}{2[R_y + (rds_2 || rds_5)]} \approx \frac{gm_2 Vin}{2(1+k)} \tag{5}$$

where, k is a low-frequency unbalanced factor [2] defined as

$$k = \frac{rds_9(gds_2+gds_5)}{gm_7 rds_7} \tag{6}$$

The output resistance, Rout as shown in Fig.2 is given by

$$R_{out} \approx (rds_9)||[gm_7 rds_7(rds_2||rds_5)] \tag{7}$$

The total current I_{out} flowing through Rout is the sum of i_7 and i_8. On solving for the total transfer function from Vout to Vin using Eq. (4-7), provides the gain of the op amp.

$$A_v = (\frac{2+k}{2+2k})gm_2 R_{out} \tag{8}$$

III. Design approach for FC-OTA

The design of op amp often need some specifications for initial calculations. These specifications intimate the designer in selection of topology for different stages used in the final circuit. A meticulous choice of the final circuit with proper biasing is essential for expected performance by designed op amp. The table 1 presents few specifications like dc gain (A_V), gain-bandwidth product (GBW), load capacitance C_L, supply voltage (V_{DD}), input common-mode range (ICMR) and slew rate (SR) to start with the design of FC-OTA.

Table 1: Specifications

Specifications	***Values***
A_v (dB)	40
GBW (MHz)	70
C_L (fF)	500
V_{DD} (V)	1.8
ICMR (V)	[0.6 : 1.6]
SR (V/µs)	50

A. Transistors and their model parameters

The given fully depleted silicon on insulator (FDSOI) technology by GLOBALFOUNDRIES 22nm FDX, provides a wide range of metal oxide field-effect transistors (MOSFETs) for varies low power and low-cost applications like wireless networking, Internet of Things (IoT), wearables and smart sensors. From their comprehensive base platform [6], two special thick-oxide transistors classified by their threshold voltage (Vt) are characterized for selection. The two transistors to be compared are 'EG low Vt' (eglvt) and 'EG super-low Vt' (egslvt), the minimum length for these transistors as per technology is L_{min} = 150nm.

The two n-channel transistors are biased properly with gate-source voltage (Vgs) and drain-source voltage (Vds) of V_{DD}/2. The aspect ratio (W/L = 5µm/500nm) of both transistors is kept equal for ease of comparison. Note that the bulk of egvts in this technology are connected to ground irrespective of nmos and pmos. The input and output characteristics are plotted for same sweeps of Vgs and Vds as shown in Fig.4.

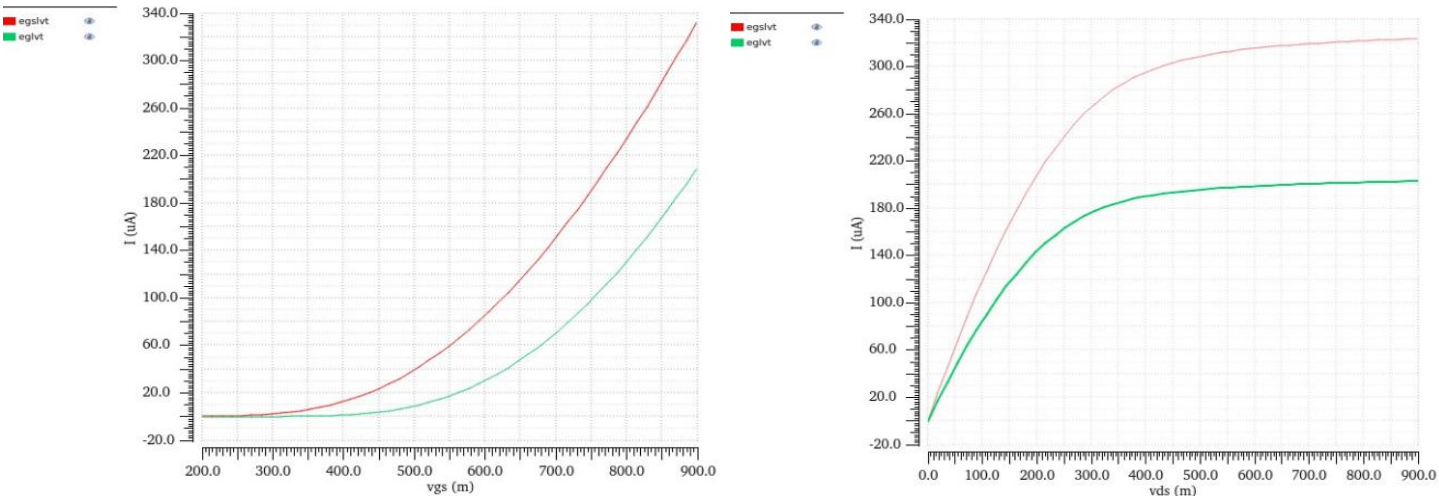

Fig.4: Input (left) and output (right) characteristics of two n-channel types

By above characterization, it can be concluded that egslvt has better current drawing capability for the given Vgs and has lower Vt compared to eglvt. In FC-OTA, we use cascode stage and current mirror stages which limits output swing. So, a low Vt transistor would be better choice. On further inspection on small signal parameters like *gm*, *rds* and intrinsic gain (*gm*rds*) following the steps in [5] egslvt is selected.

The model parameters for selected transistor are extracted (refer Appendix. A) and tabulated in table 2.

Table 2: Model parameters

Parameters	***nmos***	***pmos***
Vtn,p (mV)	200	-250
Kn,p (µA/V^2)	200	60
λ (V^{-1}) (L=450nm)	0.0175	0.018
λ (V^{-1}) (L=900nm)	0.0168	0.011

Where,

Kn = $\mu_n C_{ox}$ and Kp = $\mu_p C_{ox}$

Vtn and Vtp are threshold voltage of nmos and pmos respectively, μ_n is mobility of electrons in nmos and μ_p is mobility of holes in pmos. Two other important parameters are: η known as slope factor (refer Appendix. A) and λ known as channel length modulation (refer Appendix. B).

B. Selection of topology

The selection of differential pair type is based on the ICMR specification. As per table. 2, we select nmos differential pair as it can sense until V_{DD} in the upper limit. In case where lower limit is very close to V_{SS}, pmos pair is selected. To sense a complete range of ICMR from V_{SS} to V_{DD}, rail-to-rail op amp setup is used.

The next step is the selection of cascode stage, which is pmos common gate configuration as stated in section II. B. The current mirror stage is used to steer the current and to provide high output impedance. As shown in Fig.5, there are three structures that can be used for FC-OTA. Each structure has its own advantages and disadvantages based on application. A basic current mirror structure is used in our design for the ease of analysis. At the end, we compare the results using all these three structures as a part of design space exploration.

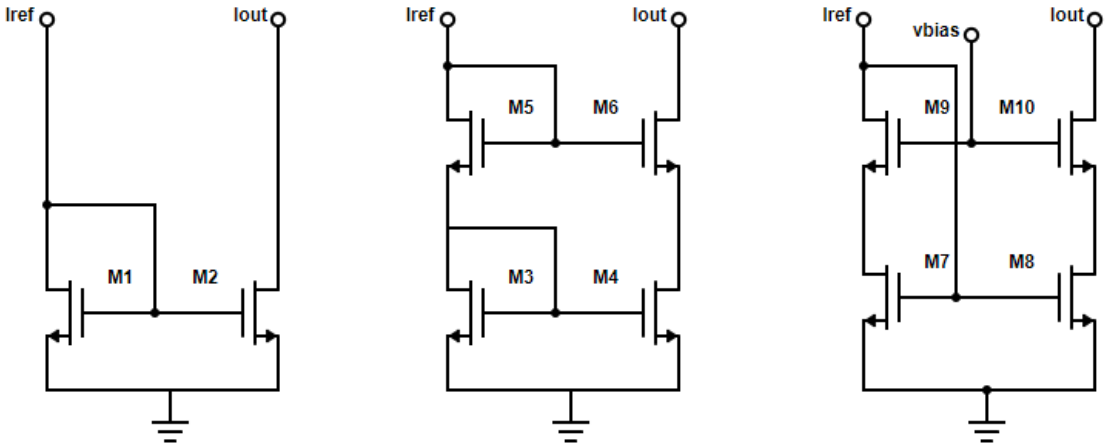

Fig.5: Current mirrors: basic (left), normal cascode (middle) and low-voltage cascode (right)

C. Design of FC-OTA

Sizing of the transistors in an op amp is done by approximate hand calculations at the initial step, later tuned by performing simulations in CAD tools. Using the specifications in table 1 and extracted model parameters in table 2 , an attempt is made to design the circuit in figure 2. From the differential topology, the dc current $I_1 = I_2 = I_3/2 = I_{bias}/2$.

- Calculate I_3 to satisfy the slew rate and C_L relation,

$$I_3 = SR.C_L \tag{9}$$

The bias currents I_4 and I_5 is set to 1.5 times I_3 , current flowing in the cascode stage $I_6 = I_4 - I_1$.

- Calculate the minimum transconductance required to attain GBW for specified C_L,

$$gm_{1,2} = 2\pi C_L.GBW \tag{10}$$

Now M1 & M2 can be sized using the equation designed from moderate inversion model, this equation is valid in all modes of operation, from strong to weak inversion [8].

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\eta gm^2}{2Kn}\frac{1}{I_{bias}-I_{bias,min}} \tag{11}$$

where,

$$I_{bias,min} = \frac{\eta k_B T g_m}{q} \tag{12}$$

room temperature T = 300 K, Boltzmann constant $k_B = 1.38 \times 10^{-23}$ $m^2kgs^{-2}K^{-1}$ and electron charge $q = 1.6 \times 10^{-19}$ C.

- Use the $ICMR_{min}$ voltage and the expression for Vgs from Eqn.1 to design M3

$$\left(\frac{W}{L}\right)_3 = \frac{2I_3}{Kn(ICMR_{min} - V_{SS} - \sqrt{\frac{2I_1}{Kn\left(\frac{W}{L}\right)_1}} - Vtp)^2} \tag{13}$$

Since M10 & M3 are current mirrors designed for same value of dc current, $(W/L)_3 = (W/L)_{10}$.

- M4 & M5 are to be designed for dc current $I_5 = 1.5I_3$ with an overdrive voltage of 150mV (Vsdsat) for each.

$$\left(\frac{W}{L}\right)_{4,5} = \frac{2I_5}{Kp(V_{sdsat5})^2} \tag{14}$$

The sizes of M4 & M5 should be large enough to satisfy $ICMR_{max}$. Check for

$$\left(\frac{W}{L}\right)_{45,} \geq \frac{2I_5}{Kp(V_{DD} - ICMR_{max} + V_{tn})^2} \tag{15}$$

- Design M6 & M7, M8 & M9 to handle worst-case currents of I_5,

$$\left(\frac{W}{L}\right)_{6,7} = \frac{2I_5}{Kp(V_{sdsat7})^2} \tag{16}$$

$$\left(\frac{W}{L}\right)_{8,9} = \frac{2I_5}{Kn(V_{dssat9})^2} \tag{17}$$

- The lengths of load current mirrors are kept high (refer Appendix. C), to avoid them from driving in weak inversion [8] and to provide high *rds*. The other transistors are sized according to biasing requirements.

Table 3: Transistor sizing

Transistors	***Width (µm)***	***Length (nm)***
M1,M2	24	450
M4,M5	36	
M6,M7	36	
M13	12	
M8,M9	8	900
M3,M10	12	
M11,M12	6	
M14	2	

D. Schematic of FC-OTA with biasing transistors

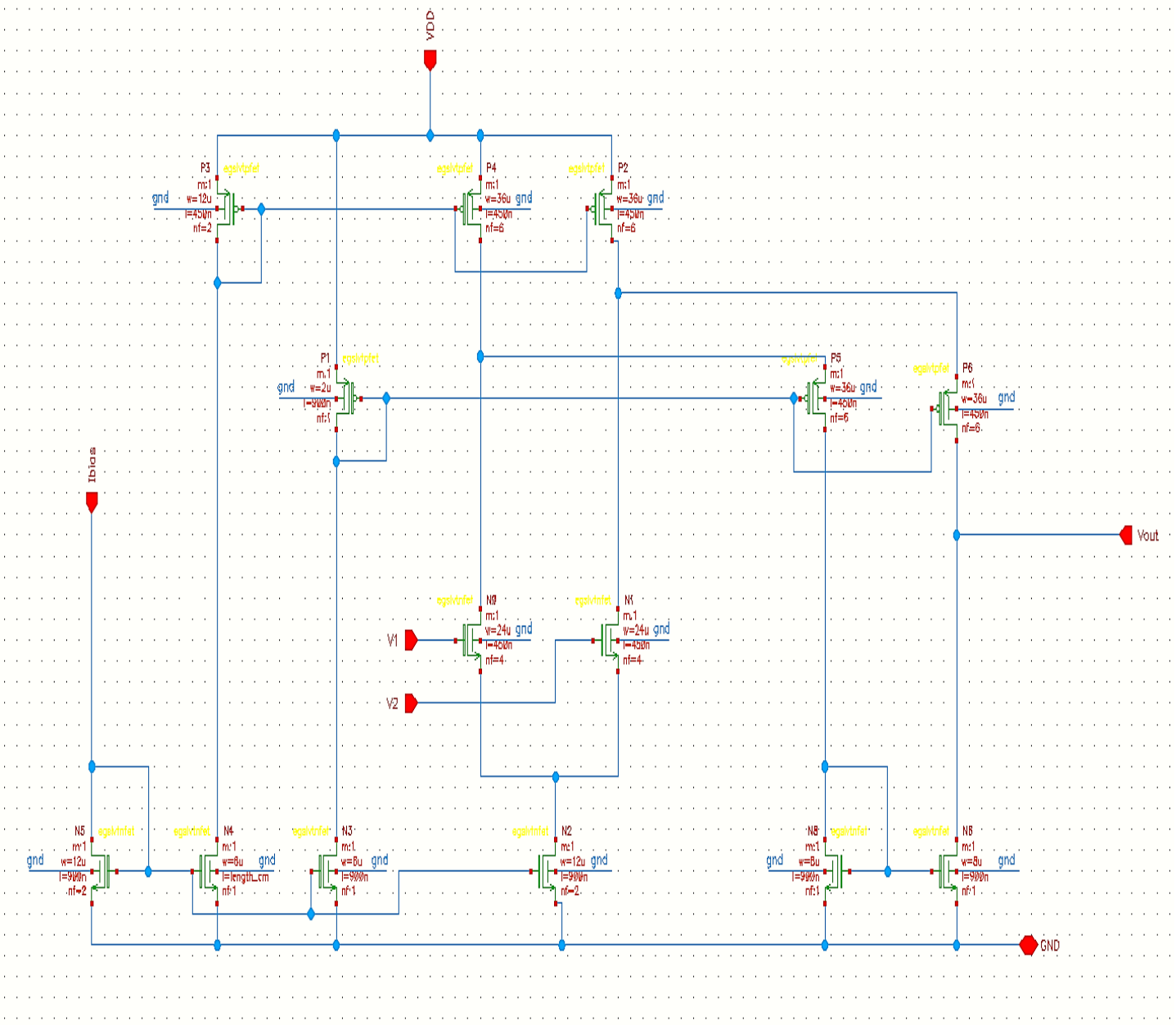

Fig.6: Schematic entry of FC-OTA

IV. Performance analysis of designed FC-OTA

The op amp is characterized by various performances like open-loop voltage gain, unity-gain bandwidth, common mode rejection ratio, power supply rejection ratio, noise, power and so on. These performance measures are fixed by the design parameters, e.g. transistor sizing, model parameters, bias currents etc.

A. Differential voltage gain, gain-bandwidth product and phase margin.

The differential voltage gain (A_{dm} or A_V) of an op amp is defined as the ratio of output voltage to differential input voltage and varies with respect to frequency. This is given by eqn. 6-8,

$$A_{dm} \approx \mathrm{gm}_1\{(\mathrm{rds}_9)|||[\mathrm{gm}_7\mathrm{rds}_7(\mathrm{rds}_2||\mathrm{rds}_5)]\} = 41.4\ \mathrm{dB} \tag{18}$$

$$GBW \approx \frac{gm_1}{2\pi C_L} = 74.86\ Mhz \tag{19}$$

Phase margin ≈ 180 – 103 = 77 degree

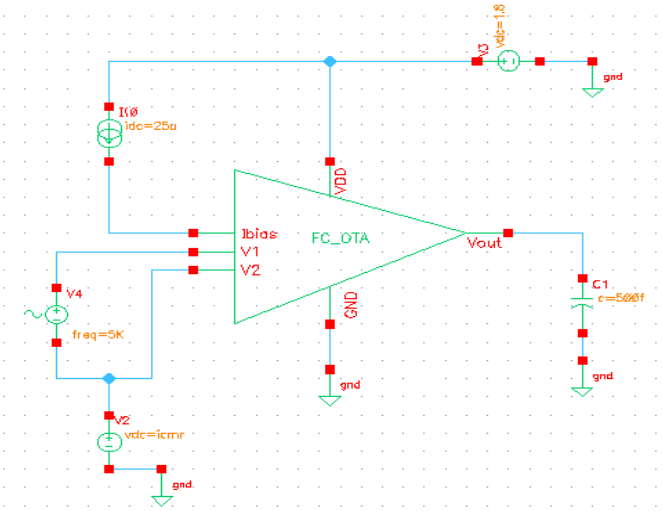

Fig.7: Testbench to measure Av and GBW

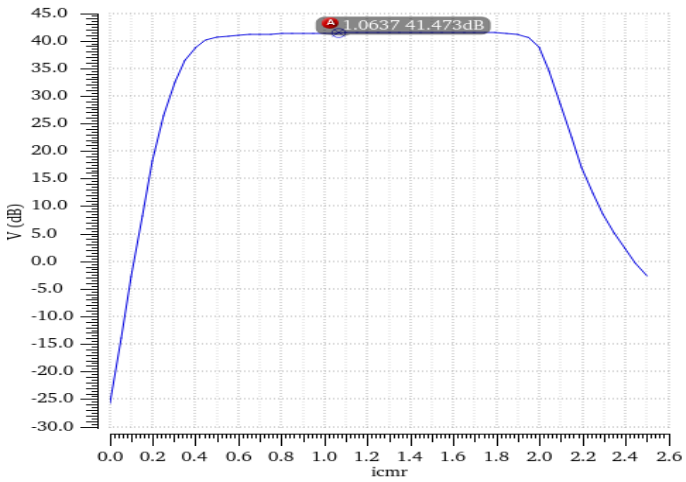

Fig.8: Av sweep over ICMR

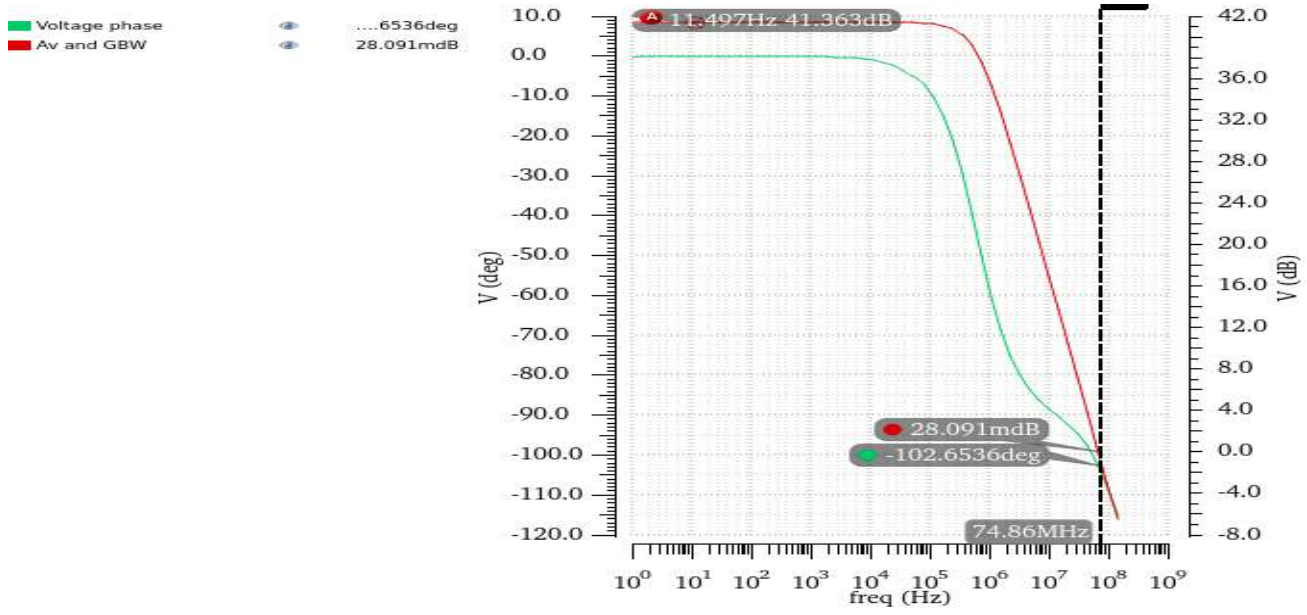

Fig.9: AC response

B. Common mode rejection ratio

Common mode rejection ratio (CMRR) is the ability of an op amp to reject the common mode signals at the input terminals. It is given by the ratio of differential mode gain to common mode gain. From [9] we can write,

$$CMRR = 20\log\left(\frac{2gm_2\, R_{out}\, rds_3}{rds_7+(rds_2||rds_5)}\right) \quad (20)$$

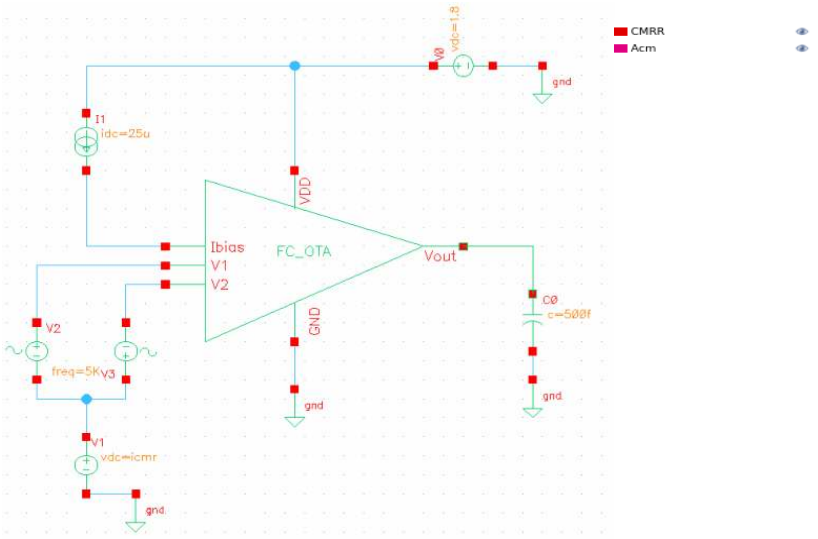

Fig.10: Testbench to measure CMRR and Acm

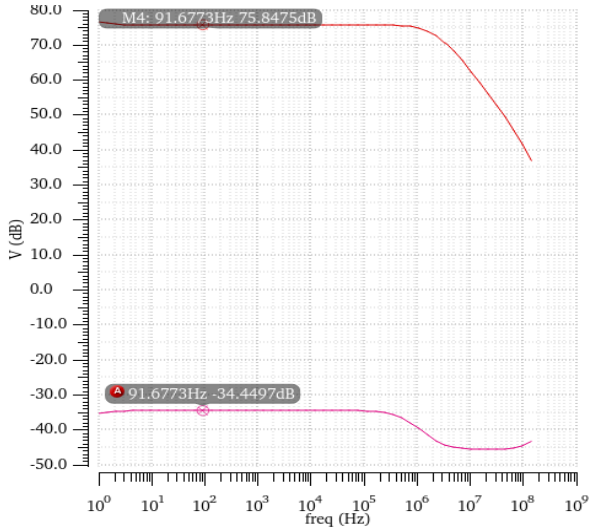

Fig.11: CMRR and Acm of FC-OTA

Therefore, CMRR = (A_{dm} – A_{cm}) in dB = [41.4 – (-34.4)] = 75.8 dB.

C. Input common mode range

The input common mode range (ICMR) specifies the range of the common mode input voltage values for which the differential stage continues to amplify the differential input. A dc sweep is performed for Vin from 0 to 2.5 V and output voltage is monitored.

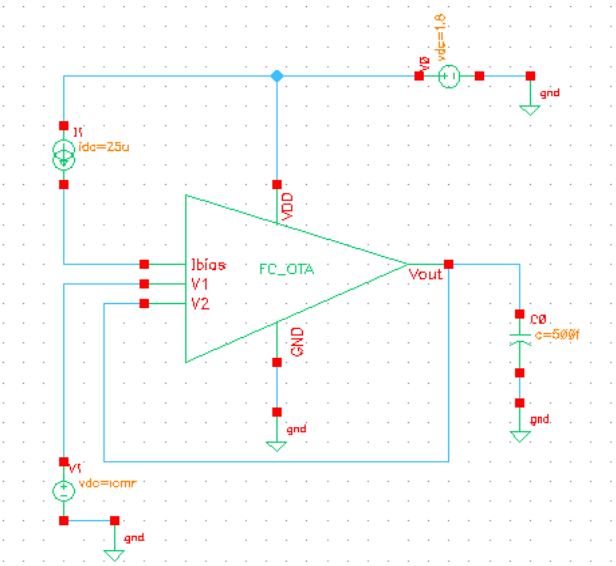

Fig.12: Testbench to measure ICMR

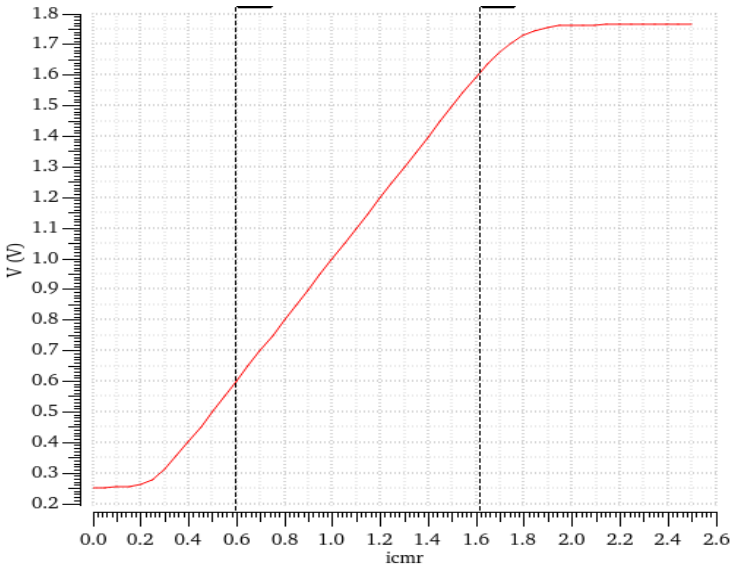

Fig.13: IMCR range 0.6 to 1.6

$$ICMR_{min} = V_{SS} + V_{dssat3} + V_{gs1} \quad (21)$$

$$ICMR_{max} = V_{DD} - V_{sdsat4} + V_{tn} \quad (22)$$

D. Output voltage swing range

The output voltage swing (OVSR) is the range in which the output voltage can vary without excessive distortion. They restrict maximum and minimum range of voltages, beyond this range transistors at output stage leaves saturation.

$$OVSR_{min} = (V_{dssat9} + V_{tn}) + V_{SS} \quad (23)$$

$$OVSR_{max} = V_{DD} - (V_{sdsat7} + V_{sdsat5}) \quad (24)$$

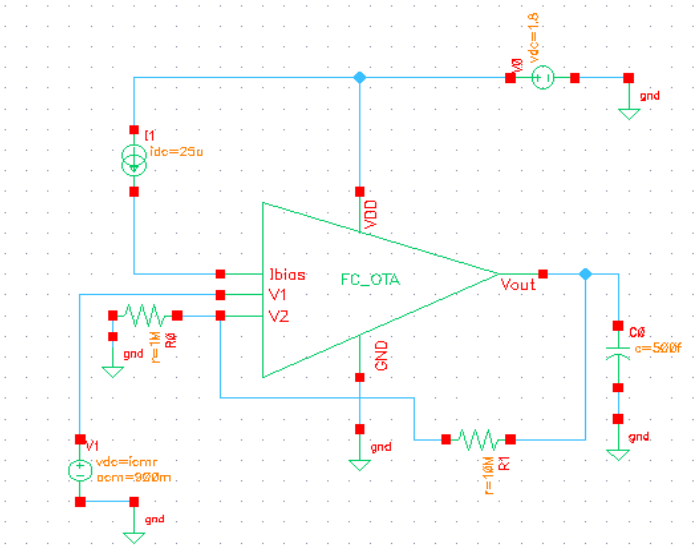

Fig.14: Testbench to measure OVSR

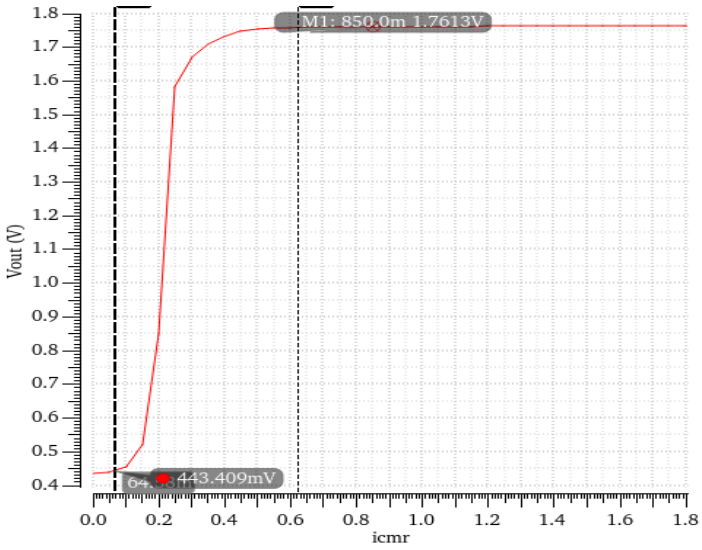

Fig.15: Output swing for ICMR

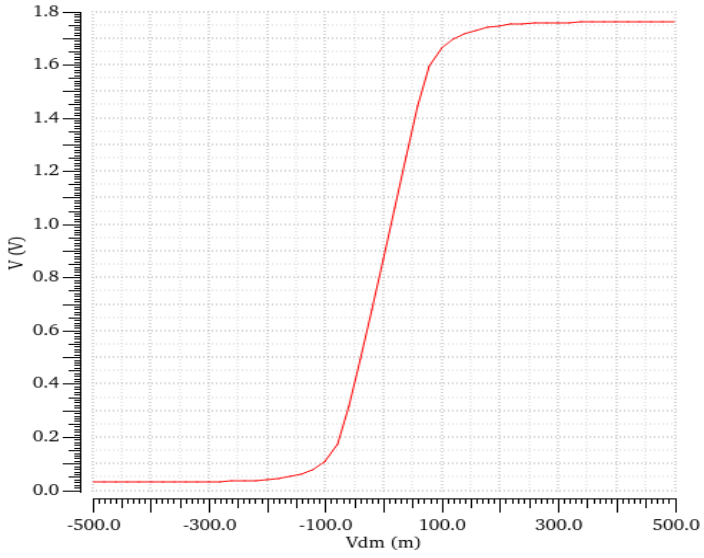

Fig.16: Output swing for differential input

E. Transient analysis

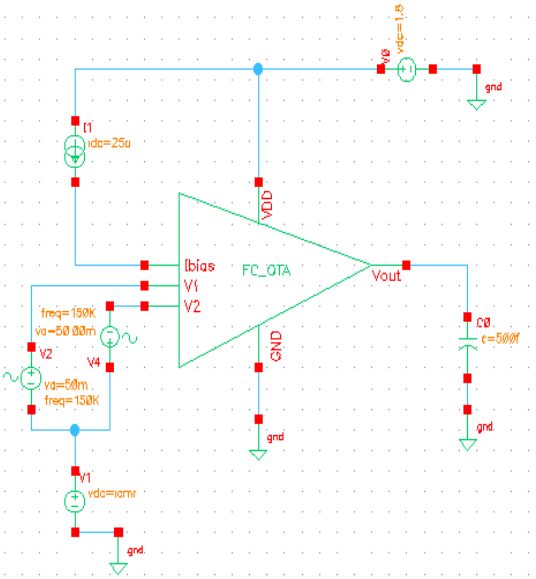

Fig.17: Testbench to perform transient analysis

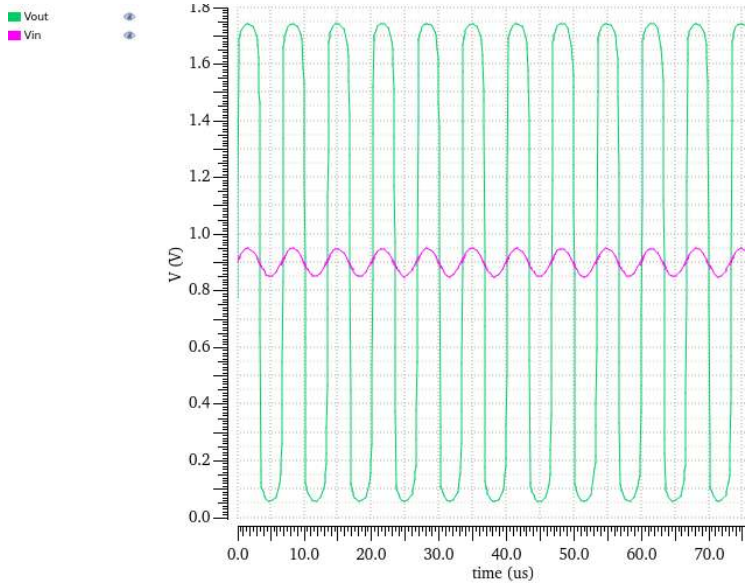

Fig.18: Transient analysis

F. Power supply rejection ratio

The power supply rejection ratio (PSRR) is a measure of the influence of power supply ripple on the op amp output voltage. It is defined as the ratio of the differential gain Av to the gain from the power-supply ripple to the output with the differential input set to zero ($A_{V,\,PS}$).

$$PSRR = \left(\frac{\Delta V_{DD}}{\Delta V_{out}}\right) A_V \tag{25}$$

$$PSRR \approx 20 \log\left(\frac{A_V}{A_{V,PS}}\right) \tag{26}$$

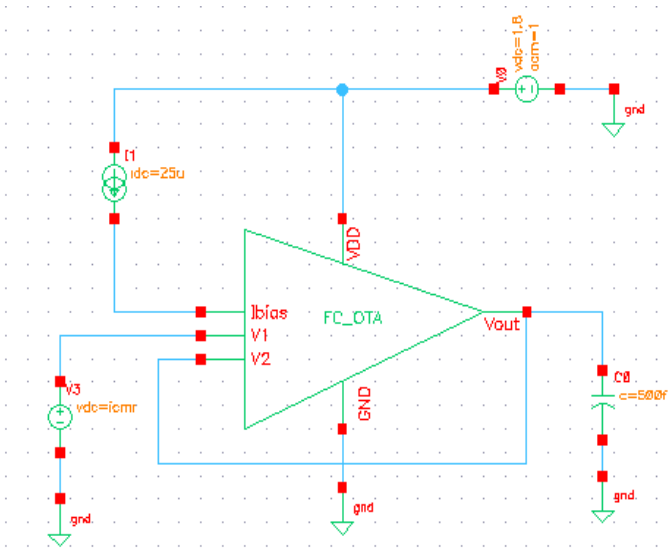

Fig.19: Testbench to measure PSRR

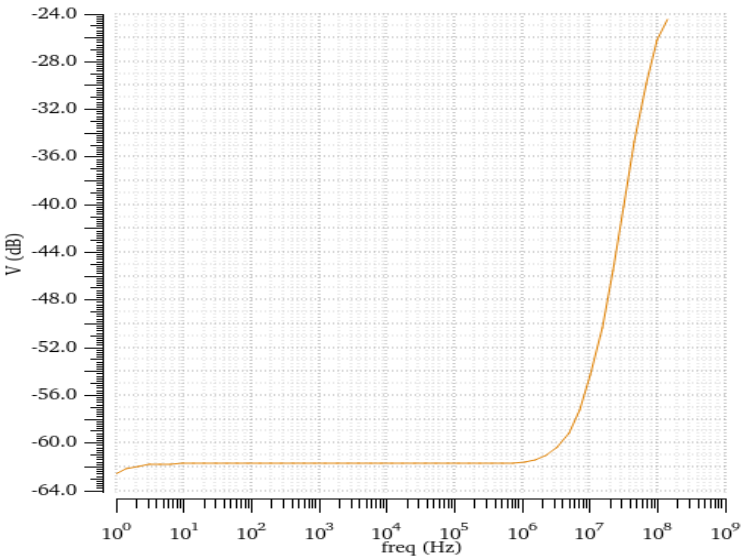

Fig.20: PSRR simulation result

Therefore, PSRR = A_V – $A_{V,\,PS}$ in dB = [41.4 – (61.7)] = 103.1 dB

G. Noise analysis

Noise analysis for output voltage is performed and equivalent input noise is plotted.

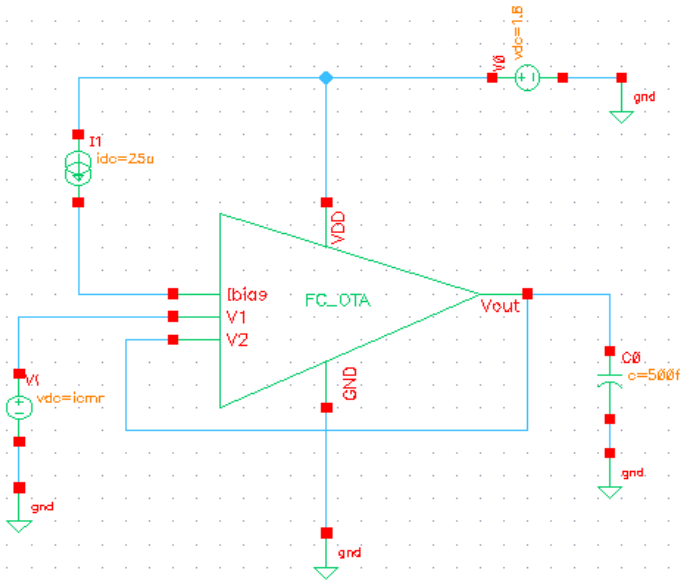

Fig.21: Testbench for noise analysis

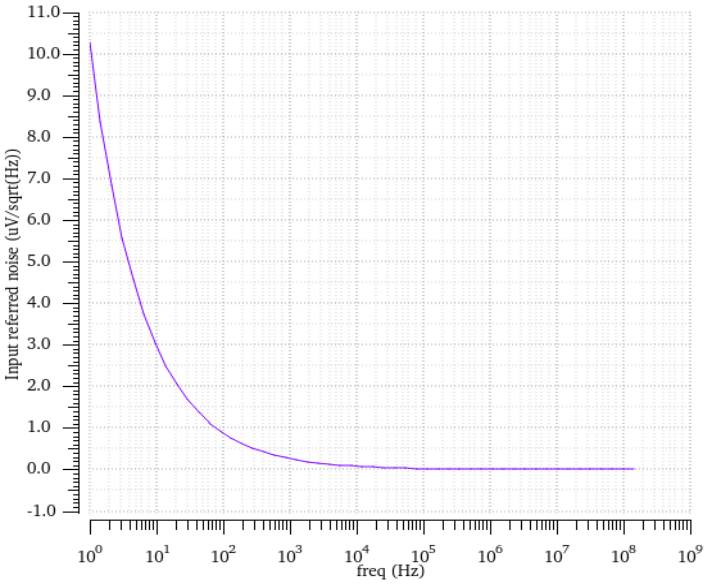

Fig.22: Input referred noise (1/f)

Device	Param	Noise Contribution	% Of Total
/I0/N6	flicker	4.4011e-15	26.61
/I0/N8	flicker	4.35099e-15	26.31
/I0/P4	flicker	2.25535e-15	13.64
/I0/N0	flicker	1.43886e-15	8.70
/I0/N1	flicker	1.42743e-15	8.63
/I0/P4	therm_sid	1.4984e-16	0.91
/I0/N8	therm_sid	4.80646e-17	0.29
/I0/N6	therm_sid	4.60913e-17	0.28
/I0/N1	therm_sid	3.49871e-17	0.21
/I0/N0	therm_sid	3.37682e-17	0.20

Spot Noise Summary (in V^2/Hz) at 5K Hz Sorted By Noise Contributors
Total Summarized Noise = 1.6537e-14
Total Input Referred Noise = 1.65238e-14
The above noise summary info is for noise data

Fig.23: Noise summary of designed FC-OTA

In fig. 23, total summary of noise contributors in FC-OTA are outlined. It is evident from the summary that current mirrors M8 & M9 are contributing up to 52 % of total noise. From fig. 22, we can observe that the input referred noise is $\leq$ 10.35 µV/√Hz.

H. Slew rate

The slew rate (SR) of an op amp is defined as the rate of change of output voltage or current caused by step change in the input voltage. It is given by eqn. 10,

$$SR = \frac{\Delta v_{out}}{\Delta t} \approx \frac{I_L}{C_L} \tag{27}$$

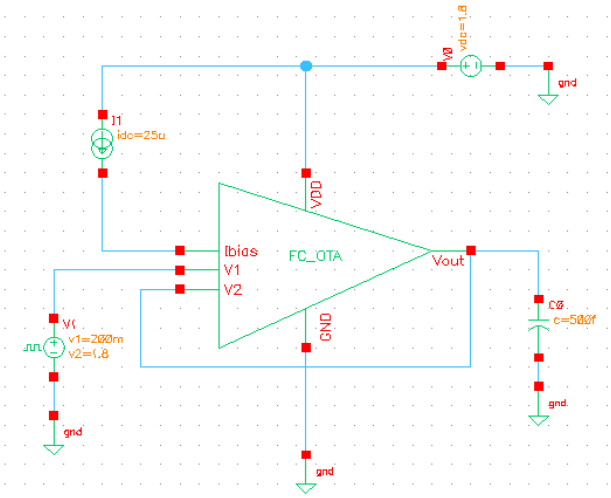

Fig.24: Test bench for slew rate

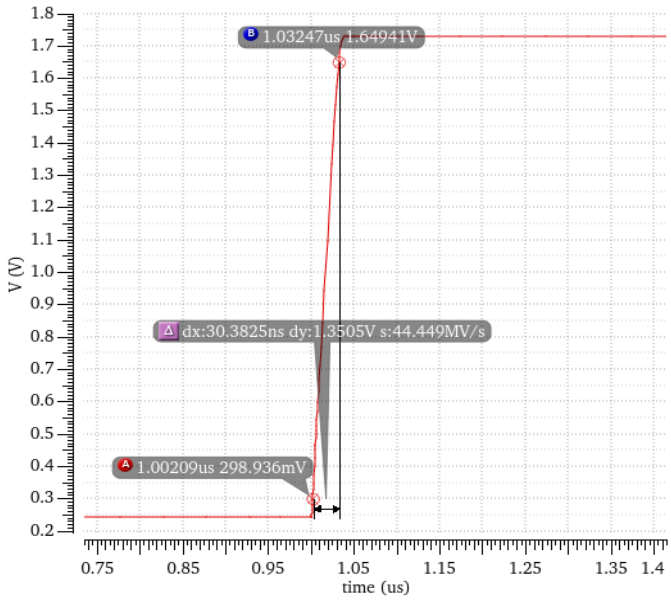

Fig.25: Slew rate for rising edge

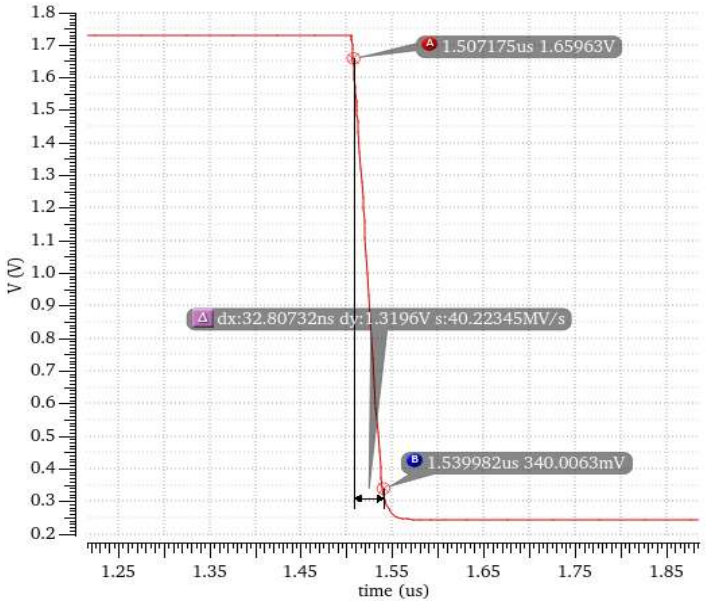

Fig.26: Slew rate for falling edge

Therefore, average slew rate is 42 V/µs.

V. Optimization of designed FC-OTA

The designed circuit is made completely parameterizable to optimize and determine the absolute performance limits with reasonable transistor sizes. For instance, we try to optimize the A_V and GBW and later perform some trade-offs. The eqn. 18 forms a strong base in understanding the parameters to be varied in order to increase gain.

$$A_{dm} \approx \mathrm{gm}_2\{(\mathrm{rds}_9)|||[\mathrm{gm}_7\mathrm{rds}_7(\mathrm{rds}_2||\mathrm{rds}_5)]\}$$

By intuitive analysis, we write two proportional expression for *rds* and *gm*

$$rds \propto {}^{L}/_{W} \tag{28}$$

$$gm \propto \sqrt{\frac{W}{L}} \tag{29}$$

- Rout should be increased to increase gain, which can be done by increasing *rds* of M8 & M9. A parametric sweep for width is made by keeping $L_{8,9}$ = 900nm.

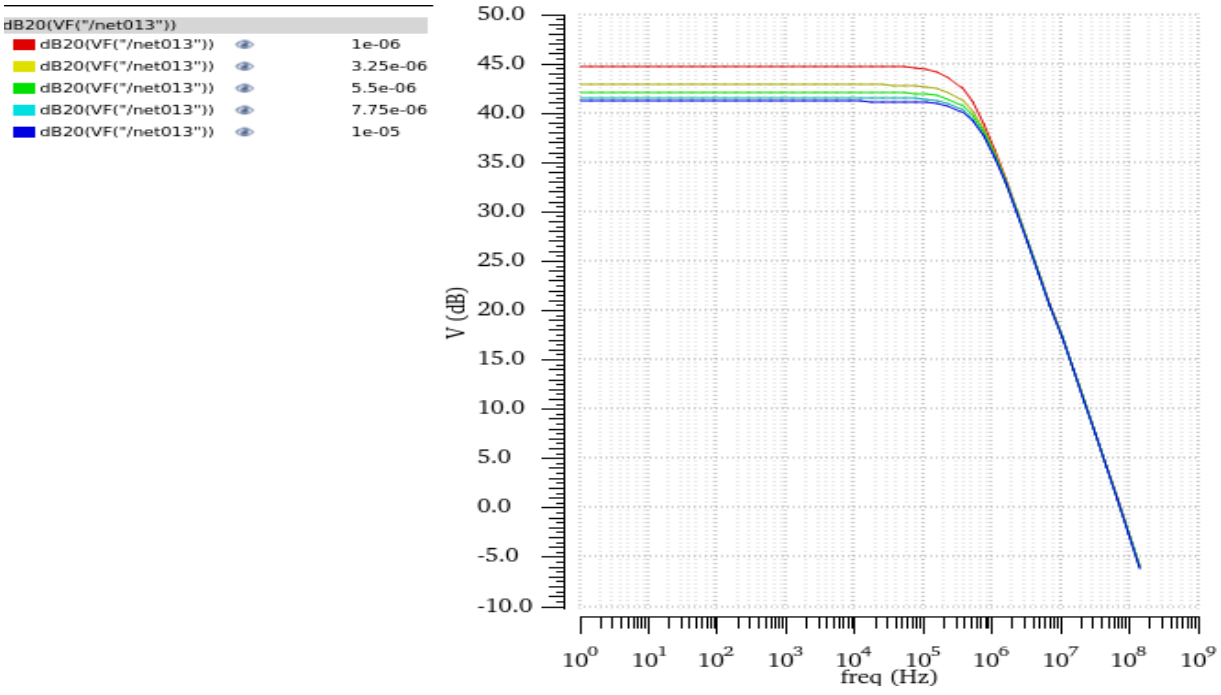

Fig.27: Parametric sweep for M8 & M9 width.

- From the figure 27, we select width as 6µm and perform parametric sweep for lengths.

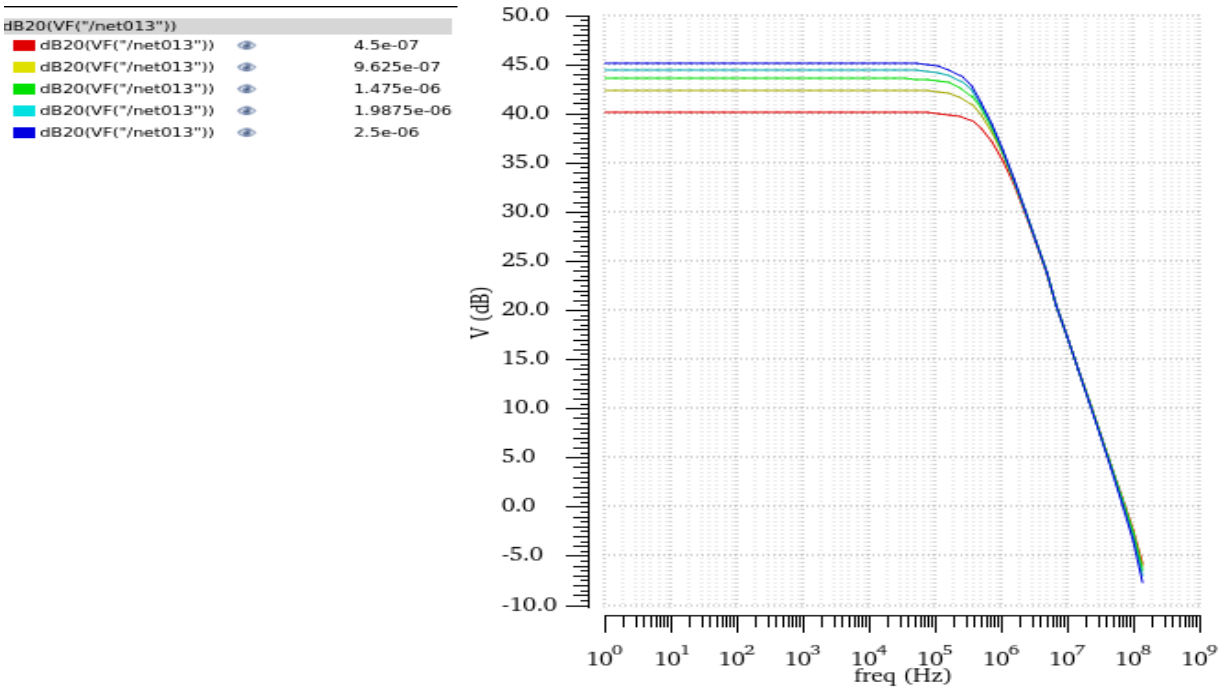

Fig.28: Parametric sweep for M8 & M9 length.

We select (W/L) of M8 & M9 as (6 µm/2 µm), which yields gain of 43 dB.

- From eqn. 29, increasing *gm* of M1 & M2 increases A_V and GBW. The width is increased to 30 µm and a parametric sweep for length is done.

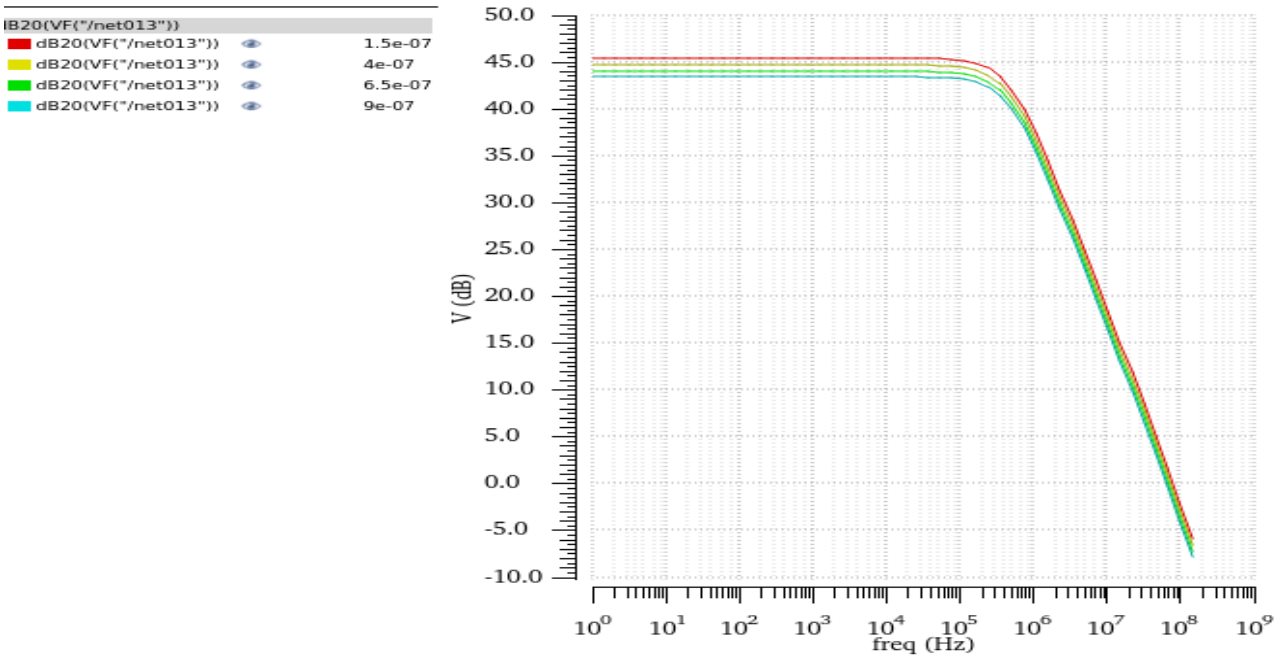

Fig.29: Parametric sweep for M1 & M2 length

- The gain and GBW reaches maximum for $L_{1,2}$ 150nm as shown in fig. 29. But, on performing noise analysis for this sizing it follows that M1 & M2 becomes the major contributors. Therefore, $L_{1,2}$ is selected to be little higher of 300nm and now M4 & M5 becomes the major noise contributors.
- Varying the sizes of cascode stage M6 & M7 and pmos current sources M4 & M5 would not be a good idea because they are in the second-degree parallel combination (eqn. 18) for gain contribution and it might drive them to triode region causing abrupt variation of dc current at load.

- Sweeping design parameters for the optimized gain 45dB.

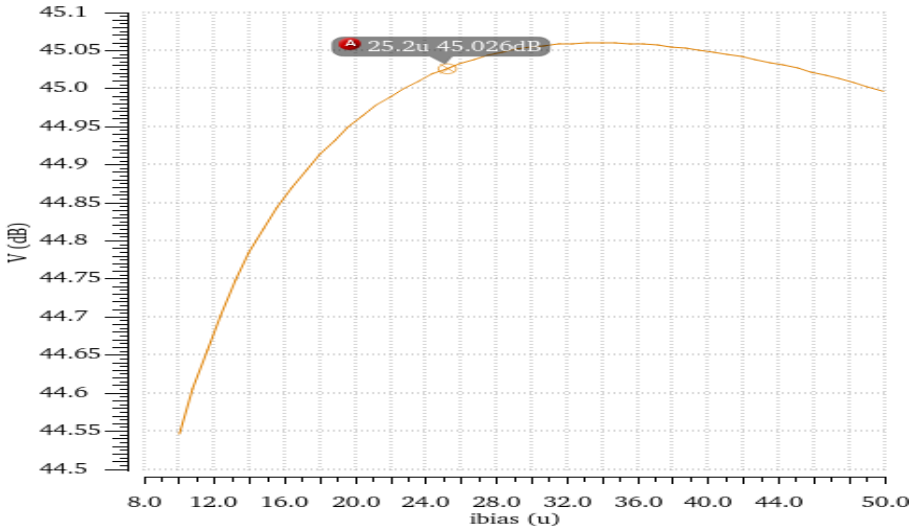

Fig.30: Gain vs ibias

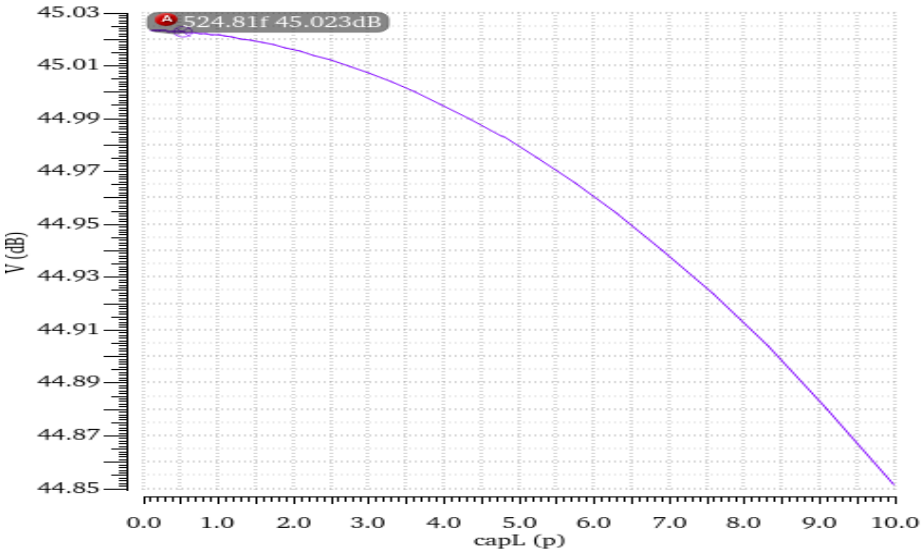

Fig.31: Gain vs load capacitor

VI. Results and conclusion

- Folded cascode operational transconductance amplifier is designed and implemented for the specifications in table 1.
- The op amp performances like A_V, GBW, CMRR, ICMR, OVSR etc were theoretically analyzed with the help of equations.
- Test benches are designed to evaluate the performances of the op amp and the evaluation was done for three circuit topologies discussed in section III. B.

Table 4: Performance comparison

Specifications	***Simple current mirror***	***Cascode current mirror***	***Low-voltage cascode***
A_V (dB)	41.4	78	69
GBW (MHz)	75	77	74
Phase margin (deg)	76.8	78	80
ICMR (V)	[0.6 : 1.8]	[0.6 : 1.8]	[0.6 : 1.8]
OVSR (V)	[0.4 : 1.4]	[0.6 : 1.2]	[0.3 : 1.45]
CMRR (dB)	75.8	112.4	103.4
PSRR (dB)	103	149	141
fc (KHz)	594	13	117
Power (mW)	0.24	0.242	0.26

- Use of cascode current mirror provides higher gain as the output impedance is very high, but output swing becomes substantially lower.
- Output swing gets better on using a low-voltage cascode current mirror as it consumes only two over drive voltages on both ends, but biasing them becomes more complicated which would reduce A_V.
- The designed FC-OTA was further optimized after some parametric sweeps, now it could reach a gain of 45 dB and GBW of 83MHz.

Table 5: New transistor sizing

Transistors	***Width (µm)***	***Length (µm)***
M1,M2	30	0.3
M4,M5	36	0.45
M6,M7	36	
M13	12	
M8,M9	6	2
M3,M10	12	0.9
M11,M12	6	
M14	2	

VII. Appendix

A. Extraction of model parameters

A simple EKV model setup for nmos and pmos is created with aspect ratio (W/L = 5µm/500nm), Vgs=V_{DD} /2 and Vds = V_{DD}. The Vt is extracted using linear extrapolation method (ELR) [7], visually at the zero crossing in Fig. 32. To determine the value of Kn or Kp, $\sqrt{I_D}$ versus Vgs is plotted. The slope '*m*' of the later plot (Fig.32) is used for calculation of Kn or Kp [2].

$$m = \left(\frac{Kn,p\ W}{2L}\right)^{\frac{1}{2}} \tag{30}$$

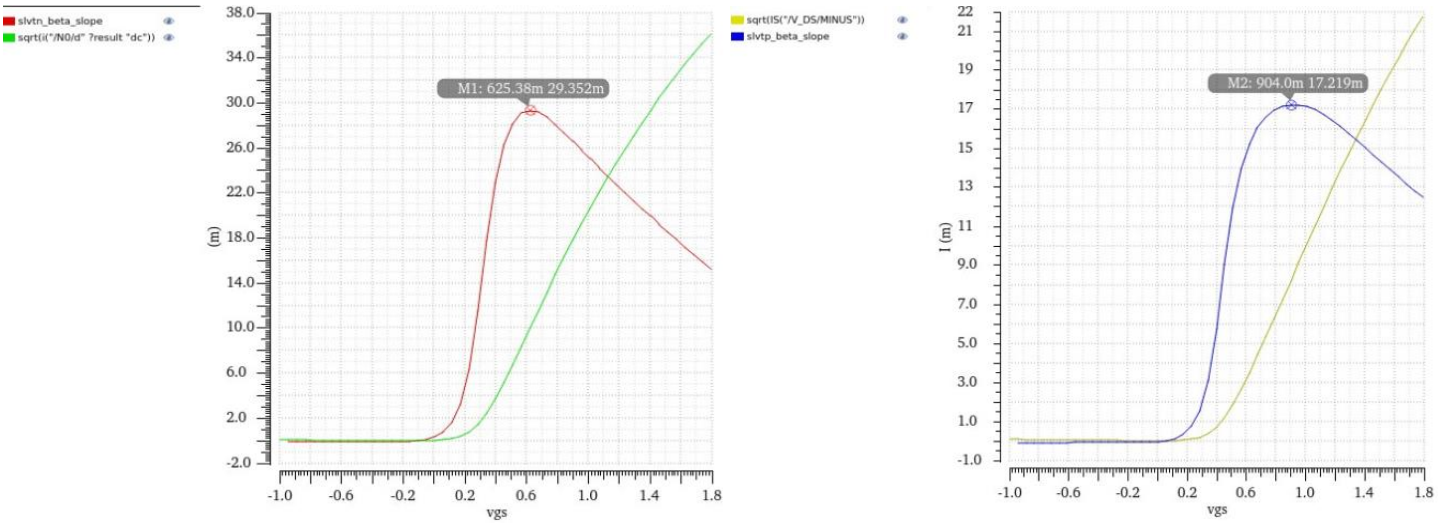

Fig.32: ELR method, nmos (left) and pmos (right)

The term slope factor (η) is given by the maximum of the subthreshold slope [8] in weak inversion and in strong inversion models the body effect.

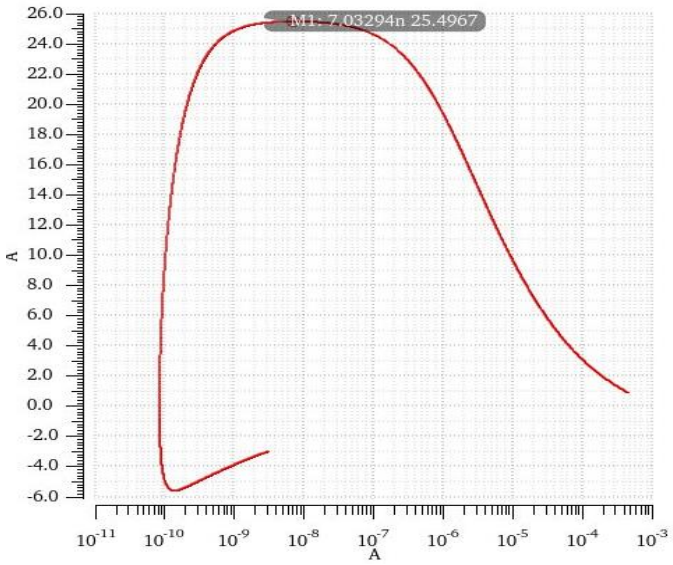

Fig.33: Plot of (ΔIds/ΔVgs)/Ids to find η

The flat part of the curve in figure 33 gives the value for $1/(\eta U_T)$,

$$U_T = \frac{k\,T}{q} \tag{31}$$

Where, T = 300 K, Boltzmann constant $k_B = 1.38 \times 10^{-23}$ $m^2kgs^{-2}K^{-1}$ and electron charge $q = 1.6 \times 10^{-19}$ C. The slope factor η is calculated from above equations is 1.5.

B. Plots for Channel length modulation

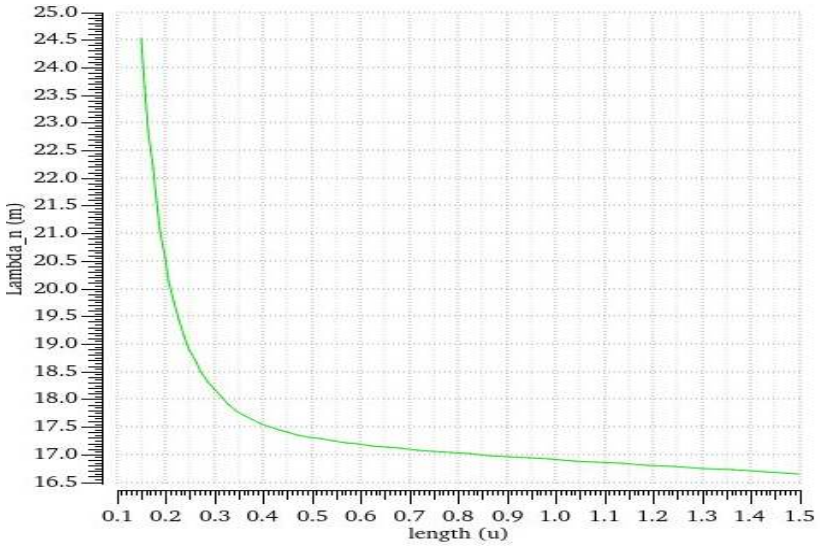

Fig.34: Channel length modulation of nmos

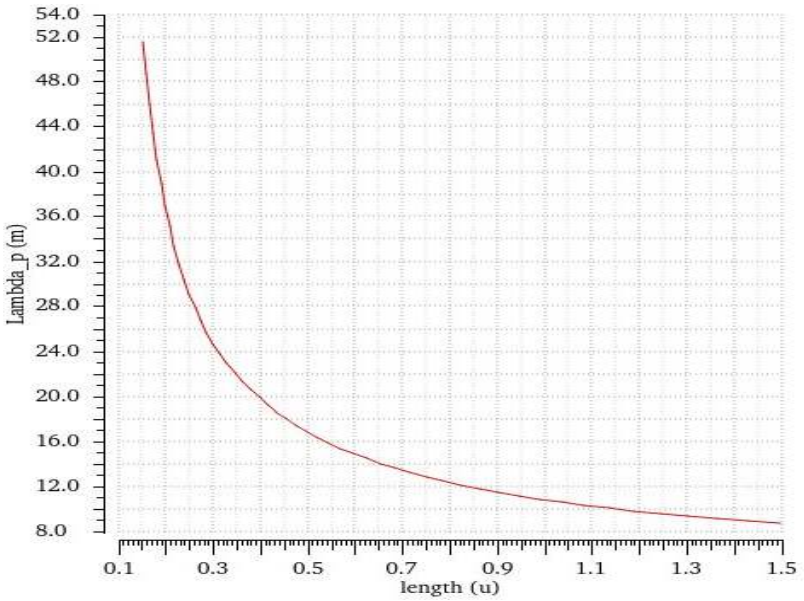

Fig.35: Channel length modulation of pmos

C. Sizing the current mirrors

The current mirror at the load in FC-OTA, gives a great contribution to the dc gain. Hence proper sizing is necessary. Setting dc current of 25µA to flow into the load, keeping width 8u, a parametric sweep for different length is performed.

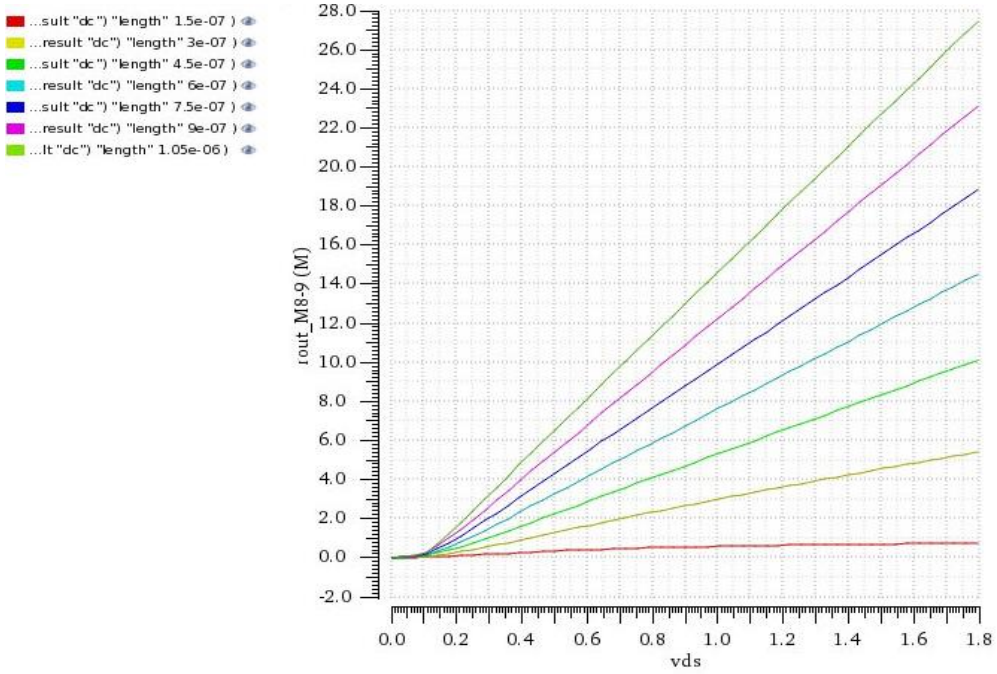

Fig.36: Rds of current mirror

From eqn. 7 and 9, its evident that *rds* of M8 & M9 should be high to keep Rout large.

$$R_{out} = (\mathrm{rds}_9)||[\mathrm{gm}_7\mathrm{rds}_7(\mathrm{rds}_2||\mathrm{rds}_5)] \approx \frac{A_V}{gm_2} \quad (32)$$

From figure 35, the length is selected to be 900nm to approach the required gain.

$(W/L)_{8,9}$ = (8µm/900nm)

VIII. References

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