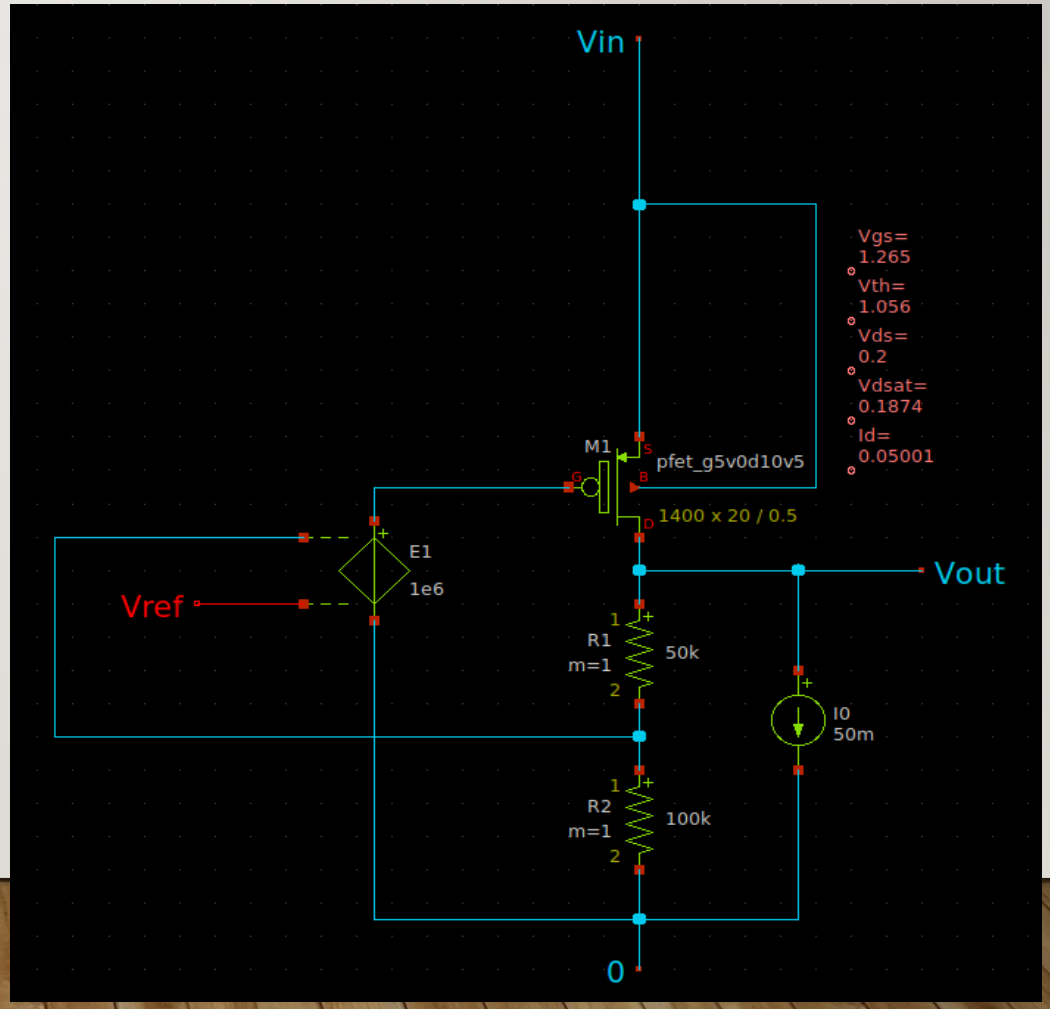
LDO DESIGN

PASS TRANSISTOR DESIGN

- I put the pass transistor in a feedback loop with the ideal amplifier and sweep W until it operates in saturation when Vin = 2v
  - Vref=1.2v
  - ILoad = 50mA
  - Vout = 1.8v
  - L=Lmin=0.5um

- I got W= 1400*20 um

vdsat	0.187436
vth	1.05642
id	0.050012
ibd	-2.8019e-10
ibs	-7.2801e-16
gbd	1.40002e-09
gbs	1.40548e-09
isub	8.63181e-16
igidl	0
igisl	0
igs	0
igd	0
igb	0
igcs	0
igcd	0
vbs	-5.17979e-07
vgs	1.26451
vds	0.199998



ERROR AMPLIFIER DESIGN

- I assume the requirement as follows:

Av > 50 dB

GBW > 30 MHz

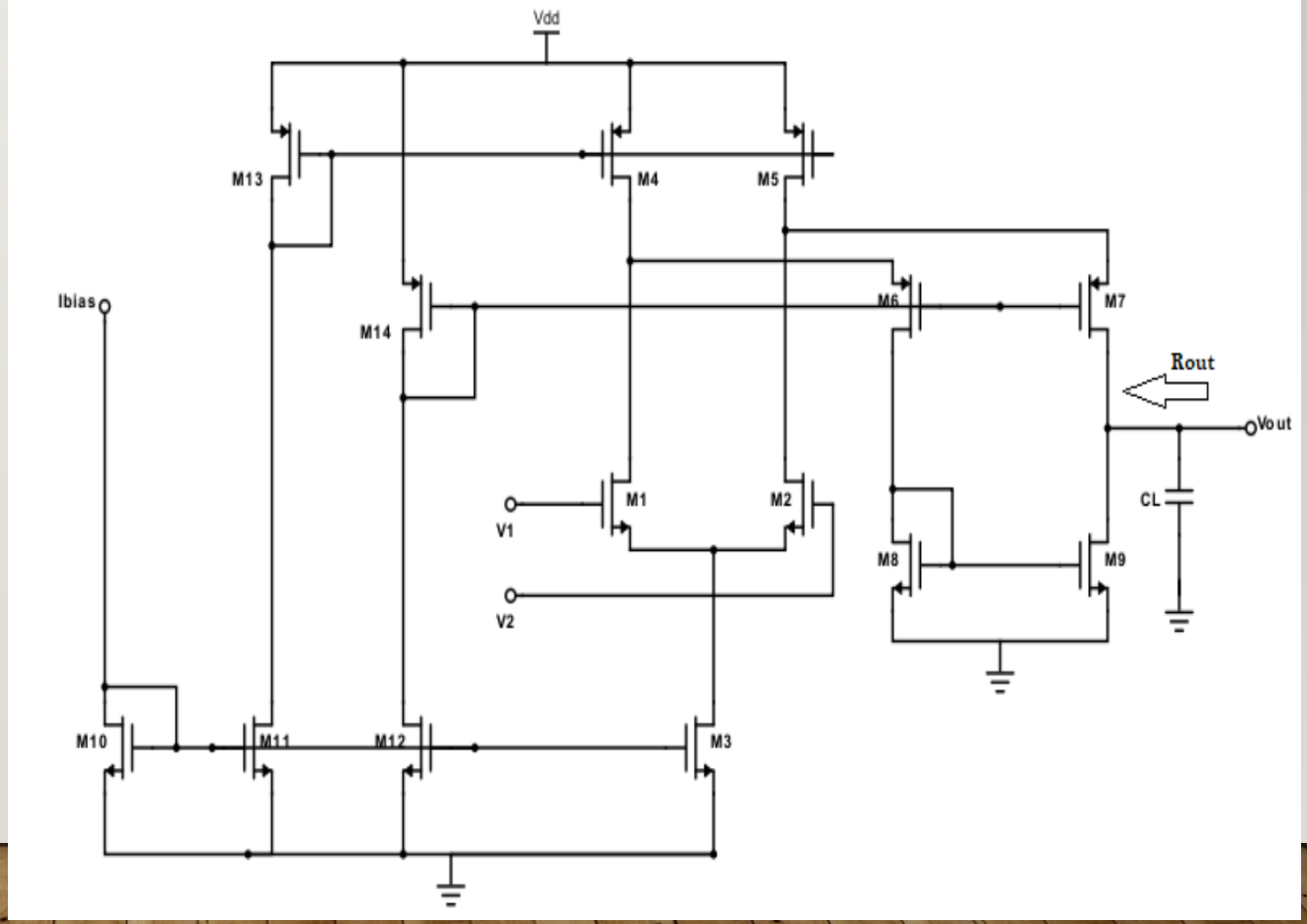
ICMR [0.8v - 1.6v]

SR = 20v/usec

Cl=1pf

Vdd = 2v

Power dissipation < 1mW



ERROR AMPLIFIER DESIGN

1- I1=I2=I3/2=Ibias/2 , I4=I5=1.5*I3 and I6-9=I4-I1

2- From SR I got Ibias

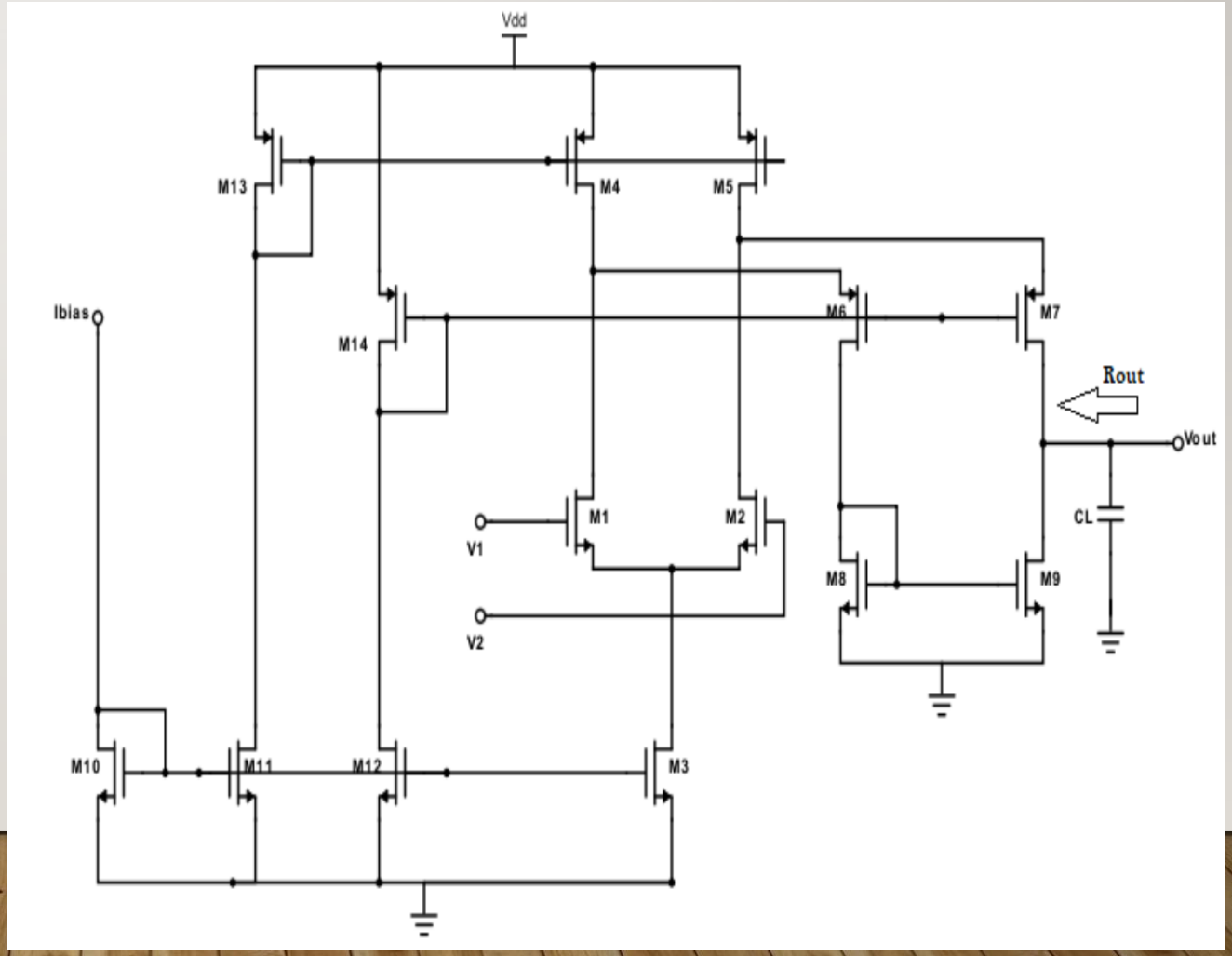
3- From GBW I got W/L)1,2

4- From ICMR- I got W/L)3

5- From ICMR+ I got W/L)4,5

6- I got W/L)6-9 that handle worst-case currents of I5

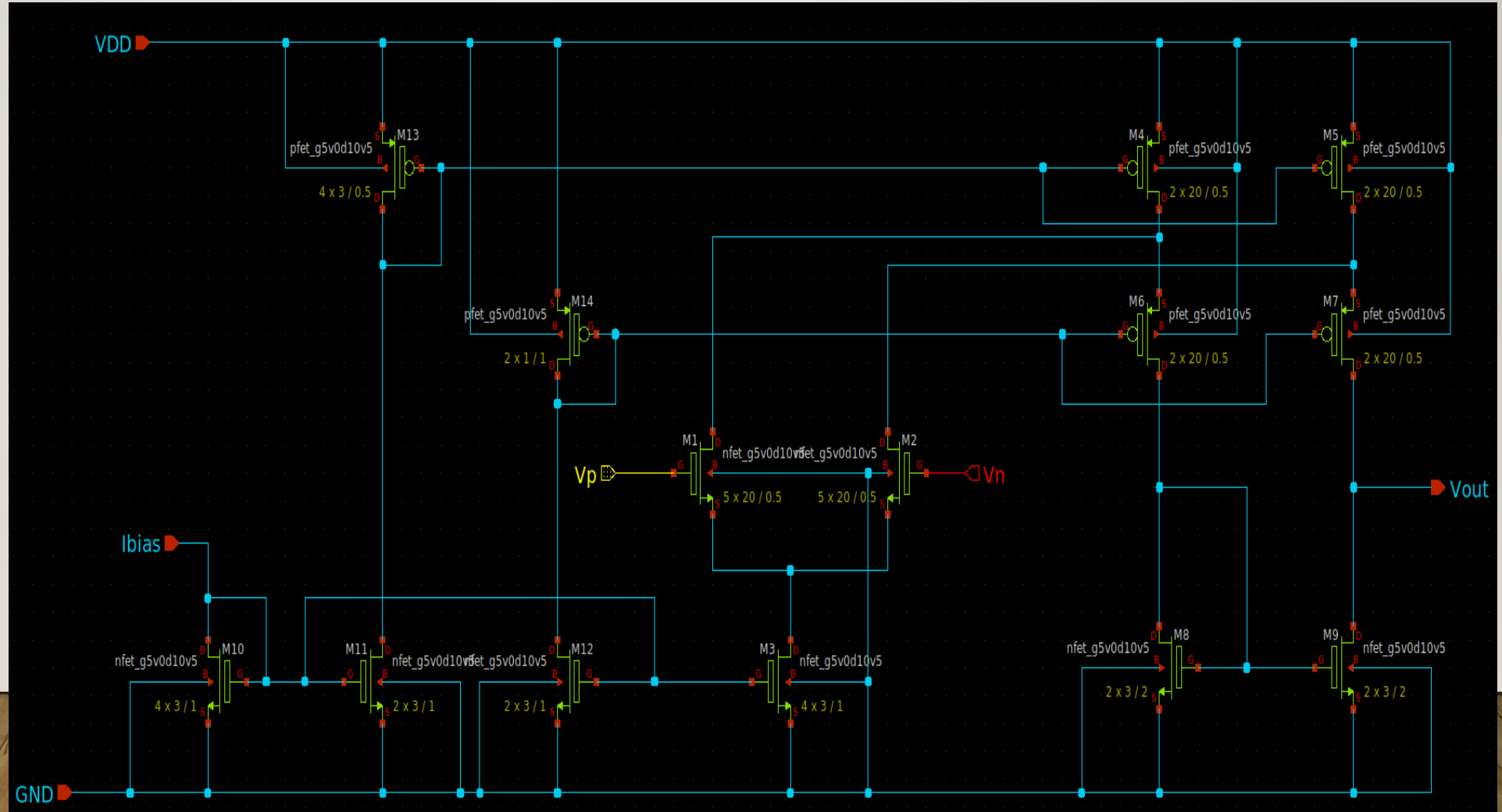
7- I got W/L)10-14 using current ratios



ERROR AMPLIFIER DESIGN

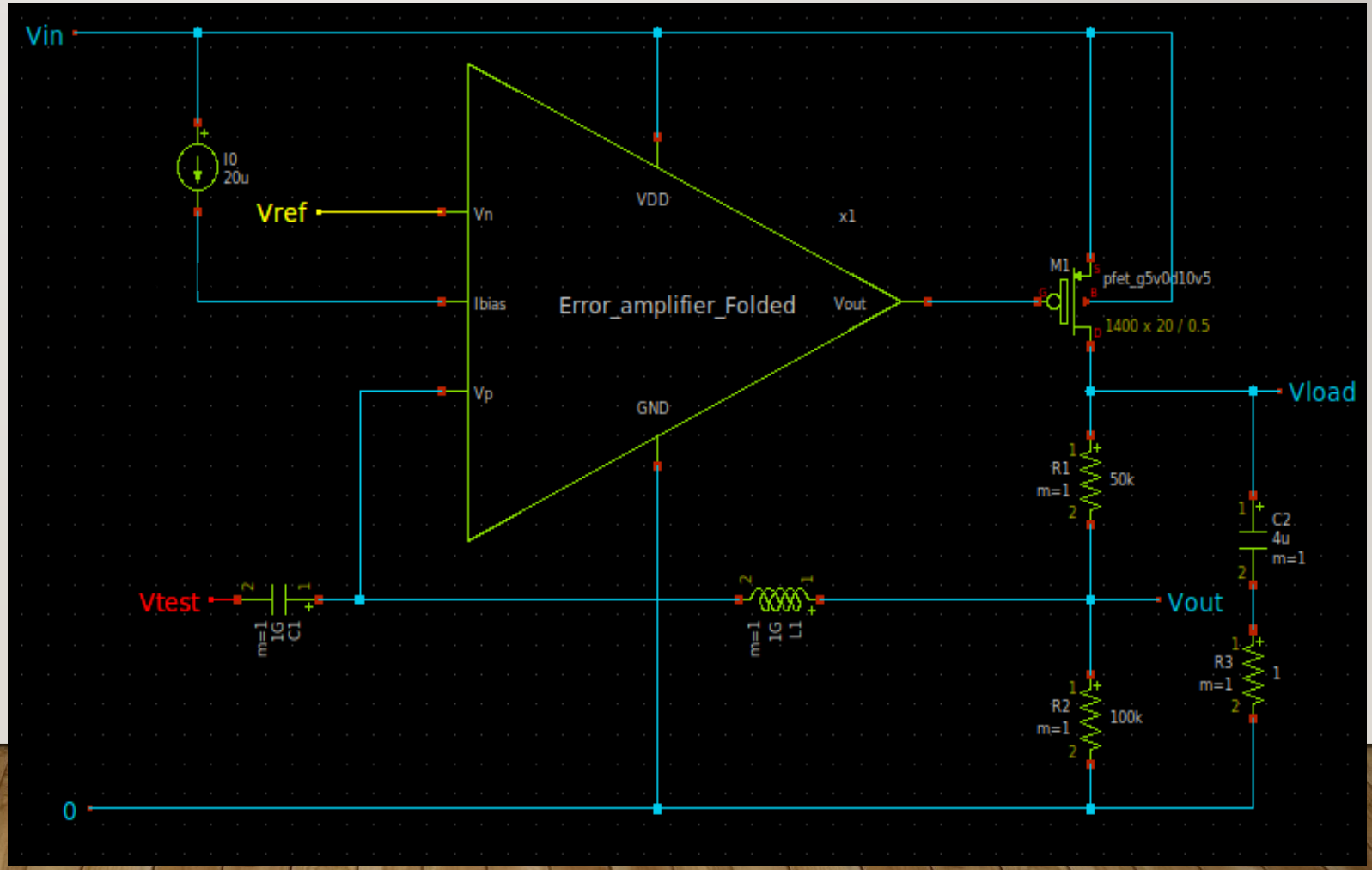
- Open loop results

@Vcm=1.2v
Adm = 55 dB
GBW= 47 MHz
Acm = -32 dB



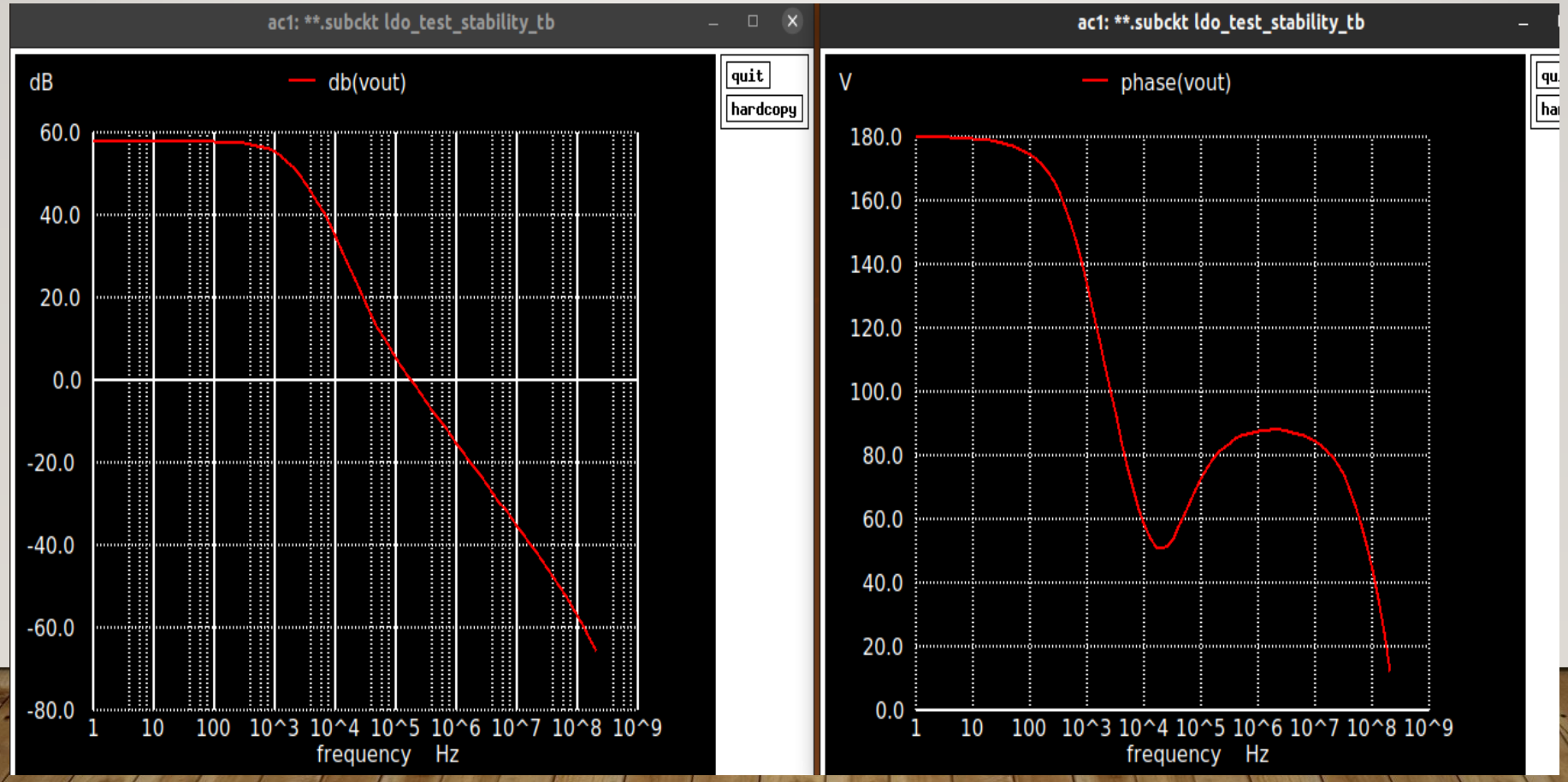
LDO STABILITY

- I put the error amplifier in the loop to check stability
- I first checked at 50mA load and 2v supply (worst case)
- The optimum values of Co was 4uF and RESR=1ohm
- Av= 57.7dB, GBW = 177 KHz and PM = 80 deg



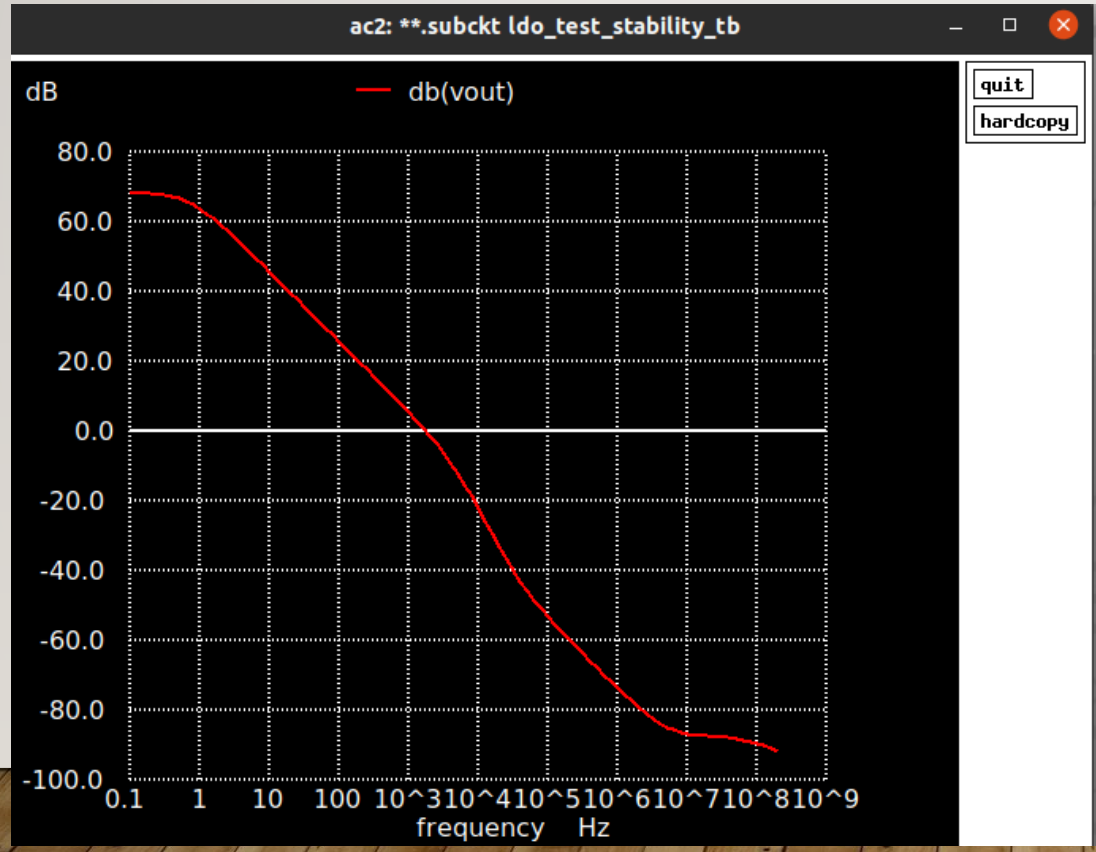
LDO STABILITY

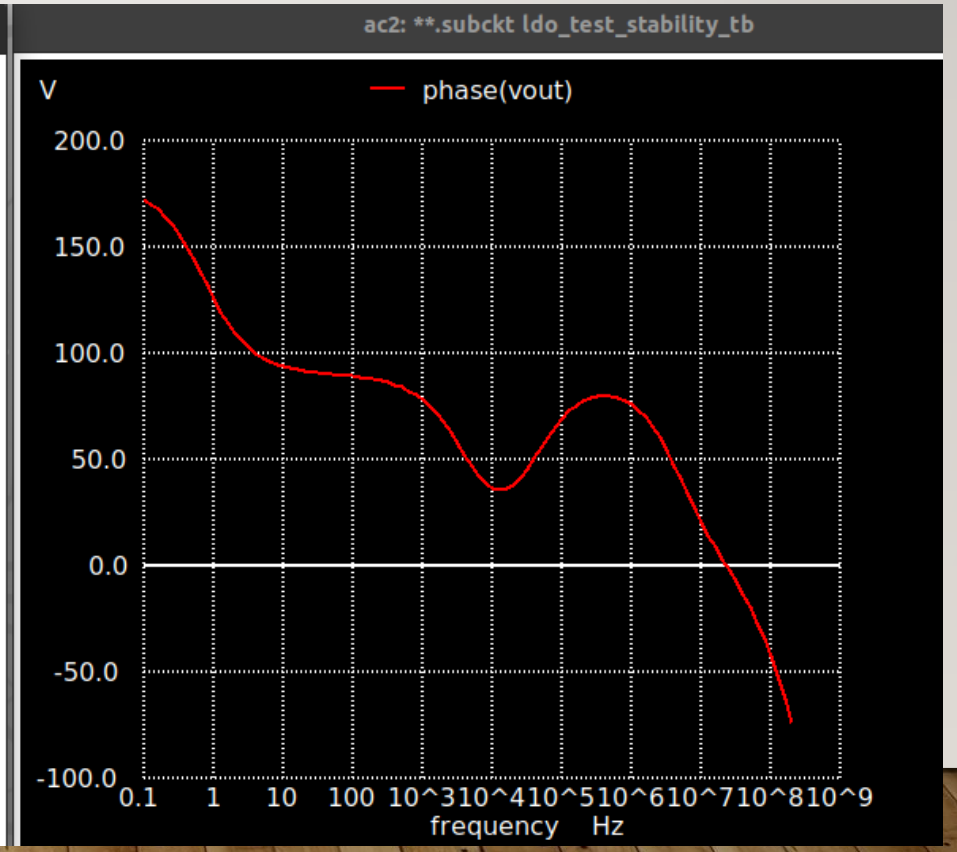
@ 50mA load and 2v supply



LDO STABILITY

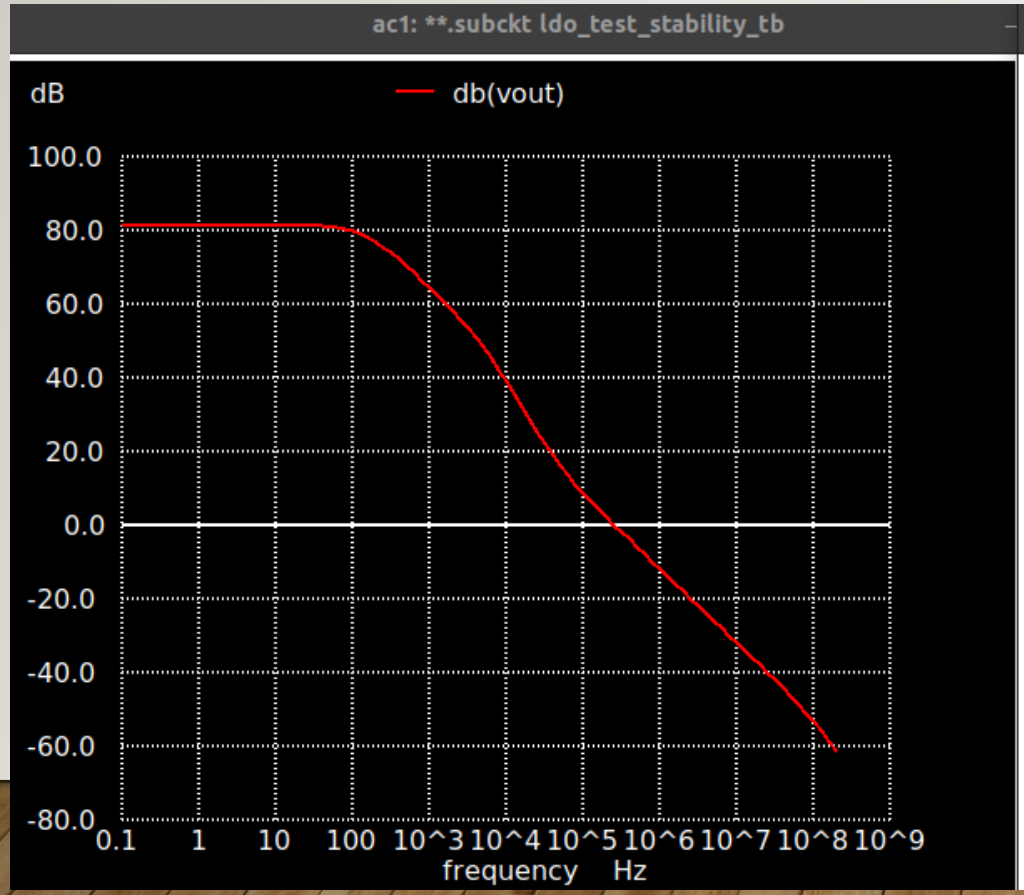
@ no load and 2v supply

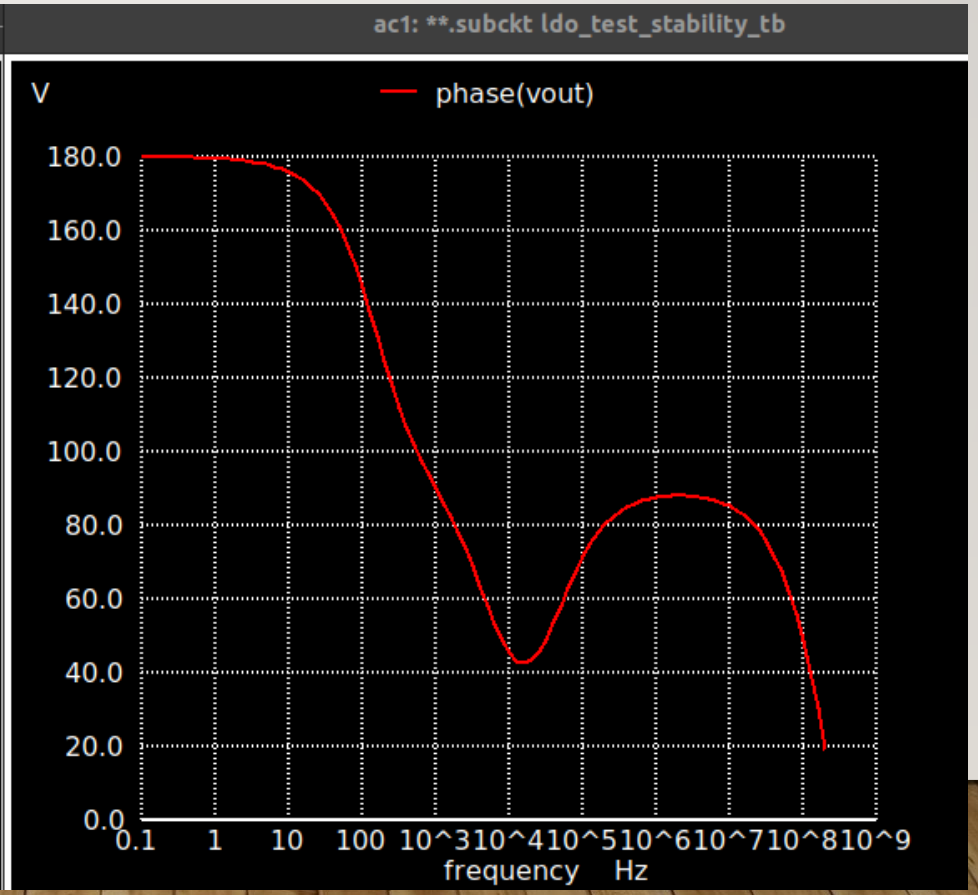




LDO STABILITY

@ 50mA load and 3.6v supply





LDO STABILITY

@ NO load and 3.6v supply