Design of a Low-power Bandgap Current Reference

RU Bei
Institute of Computer and Information Engineering
Xinxiang University
Xinxiang, China
E-mail: beita012345@163.com

***Abstract*—A low-power complementary metal oxide semiconductor (CMOS) bandgap current reference is proposed under the 1.8V supply voltage. The temperature compensation current generator was used in order to obtain an accurate 5μA current with lower temperature coefficient. Sub-threshold technology and advanced startup circuit were adopted to decrease the circuit power consumption. The current reference has been simulated based on SMIC 0.18μm CMOS technology. The simulation results show that it has significantly low power and low sensitivity to the temperature. The power consumption is only 35.22μW. The temperature coefficient is 42.62ppm/ºC under typical process with the temperature range from -40℃ to 125 ℃.**

Keywords-CMOS; current reference; low-power; sub-threshold technology; startup circuit

I. INTRODUCTION

The application of portable electronic systems such as wireless communication devices, consumer electronics and battery powered biomedical devices increase the requirements for lower-voltage and lower-power circuit techniques. [1] Bandgap reference is one of the essential units in analog circuits and mixed signal systems, which is used to offer benchmark voltage, current or frequency to the other circuit blocks. Its performance will seriously hamper the performance of the entire circuit systems.

The reference circuit mainly includes three kinds: Zener reference, XFET reference and bandgap reference in the design of analog integrated circuits. Recently, the bandgap reference has become a usual technique for the reference design. Because it is fully compatible with standard complementary metal oxide semiconductor (CMOS) technics and is very suitable for lower-voltage, lower-power and high performance applications.

In this paper, a CMOS bandgap current reference with very low power is proposed based on sub-threshold technology and advanced startup circuit, which is very beneficial to reduce the circuit power consumption at the same time to ensure reference precision.

II. DESIGN PRINCIPLES

Fig.1 shows the circuit of the bandgap current reference in the design.

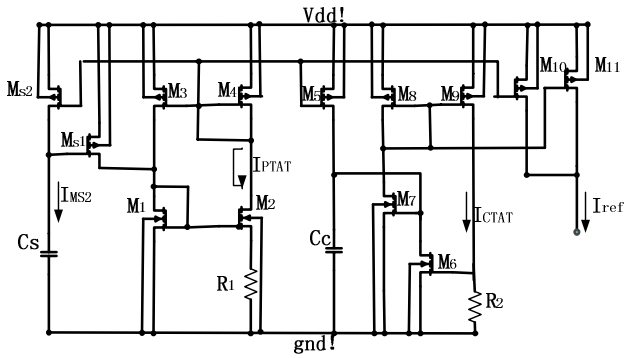

Figure 1. Circuit of the proposed current reference

A. Sub-threshold Technology

As shown in Fig.1, the current reference is composed of MOS transistors. The transistor has two primary operation regions in which current flows from the source to the drain: the weak inversion region (sub-threshold region) and the strong inversion region. When it works in the sub-threshold region, its gate-source voltage (V_{GS}) and the difference gate-source voltage between two MOS transistors (ΔV_{GS}) have two opposite temperature dependent parameters.[2] So the MOS transistors can be used to instead of bipolar junction transistors (BJTs) and form a CMOS bandgap reference. In the proposed circuit (as shown in Fig.1), MOS transistors M_1, M_2, M_6 operate in the sub-threshold region, and the other transistors work in saturated region.

When the MOS transistors operate in sub-threshold region, its V_{GS} must satisfy the followed equation:

$$V_{GS} < |V_{TH}| \tag{1}$$

where V_{TH} is the threshold voltage of MOS transistors.

And its drain current (I_{ds}) can be expressed as:

$$I_{ds} = n\mu C_{ox}\left(\frac{W}{L}\right)(V_T)^2 \exp\left[\frac{1}{nV_T}(V_{GS}-V_{TH})\right]\left[1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right] \tag{2}$$

where n is the sub-threshold factor ($1<n<3$). μ is the mobility. C_{ox} is the gate oxide capacitance per unit area. V_T=kT/q is the thermal voltage. V_{ds} is the drain-source voltage. W/L is the width length ratio.

978-1-4244-7161-4/10/$26.00 ©2010 IEEE

In practice, $V_{ds} >> V_T$, so the I_{ds} can be predigested as:

$$I_{ds} = n\mu C_{ox}\left(\frac{W}{L}\right)(V_T)^2 \exp\left[\frac{1}{nV_T}(V_{GS} - V_{TH})\right] \quad (3)$$

The I_{ds} exponentially changes along with the voltage (V_{GS}-V_{TH}). By the equation (1) and (3), we can see that the MOS transistors operating in sub-threshold region have a weak drain current comparing with the saturated region. In the same way, it has very low over driving voltage. So it is very favorable to low voltage design. In conclusion, the sub-threshold technology is a best choice for low-voltage and low-power application.

III. CIRCUIT DESIGN

In the circuit, an accurate 5μA reference current was generated using temperature compensation current generator.[3] The temperature independent reference current is generated by summing a proportional to absolute temperature(PTAT) current and a complementary to absolute temperature(CTAT) current. The temperature coefficient (TC) and magnitude of the reference current are influenced by the process variation. To calibrate the variation, two binary weighted current mirrors are used to control the temperature coefficient and magnitude. Besides, a startup circuit plays a very significant role in current reference circuits. It is because that there is an important problem in the circuit, which is the existence of "degeneration". So a startup circuit is necessary to bring out the reference circuit from a dead (zero current) operating point to its normal operating point and then is no longer used once the reference circuit starts operating properly. [4,5]

A. PTAT Circuit

The PTAT current generator is made up of M_1~M_4 and R_1 as shown in Fig.1. The current I_{PTAT} can be formed by the ΔV_{GS} between M_1 and M_2 as shown in equation (4):

$$I_{PTAT} = \frac{\Delta V_{GS}}{R_1} \quad (4)$$

When the MOS transistors work in sub-threshold region, their V_{GS} satisfy the followed relationship:

$$V_{GS} = V_{TH} + nV_T \ln\left[\left(\frac{L}{W}\right)(V_T)^2\left(\frac{I_{ds}}{n\mu C_{ox}}\right)\right] \quad (5)$$

So the ΔV_{GS} has a positive temperature coefficient. [2] Substituting the equation(5) into (4), we can get the current I_{PTAT}:

$$I_{PTAT} = \frac{(V_{TH1} - V_{TH2}) + nV_T \ln\left[\left(\frac{W}{L}\right)_2 \Big/ \left(\frac{W}{L}\right)_1\right]}{R_1} \quad (6)$$

We can see that the I_{PTAT} is in direct proportion to absolute temperature(T), which has a positive temperature coefficient. M_3 and M_4 copy I_{PTAT} as current mirror transistors, which made the current of M_3 is equal to I_{PTAT}. In order to ensure the current precision, the channel length of M_3 and M_4 should be sufficiently long that the channel length modulation effects can be negligible.

B. CTAT Circuit

The CTAT current generate circuit consists of transistors M_5~M_9, R_2 and compensated capacitance C_C. M_5 is used to copy the current from M_4 and offer a fixed low current to M_6 guaranteeing it works in sub-threshold region. So the gate-source voltage of M_6 (V_{GS6}) has a negative temperature coefficient. [6,7] As shown in equation (7), the value of I_{CTAT} is decided by R_2. It is because the voltage of R_2 is fixed in $V_{GS,M6}$ due to the negative feedback, [8] which is built up by M_7~M_9. The higher gain of the feedback loop is, the more precise the current is.

$$I_{CTAT} = \frac{V_{GS6}(T)}{R_2} \quad (7)$$

C. Weighted Current Mirrors

As shown in Fig.1, the weighted current mirror is made up of the transistors M_{10} and M_{11}. M_{10} is used to copy the current I_{PTAT}, and M_{11} is used to copy I_{CTAT} as shown in equation(8), (9). If the two currents (I_{M10} and I_{M11}) having opposite temperature coefficient are added in a proper ratio, the added current (I_{ref}) will have a low temperature drift.

$$\begin{aligned} I_{M10} &= m_1 I_{PTAT} = \frac{(W/L)_{10}}{(W/L)_4} I_{PTAT} \\ &= \frac{(W/L)_{10}}{(W/L)_4}\frac{nV_T}{R_1}\ln\left[\frac{(W/L)_2}{(W/L)_1}\right] \end{aligned} \quad (8)$$

$$\begin{aligned} I_{M11} &= m_2 I_{CTAT} = \frac{(W/L)_{11}}{(W/L)_9} I_{CTAT} \\ &= \frac{(W/L)_{11}}{(W/L)_9}\frac{V_{GS,M6}}{R_2} \end{aligned} \quad (9)$$

Where m_1 and m_2 are the weighted coefficients. So the output reference current (I_{ref}) can be described as:

$$I_{ref} = I_{M10} + I_{M11} = m_1 I_{PTAT} + m_2 I_{CTAT} \quad (10)$$

And the current temperature coefficients ($\partial I_{PTAT}/\partial T$ and $\partial I_{CTAT}/\partial T$) of the I_{PTAT} and I_{CTAT} are followed:

$$m_1 \frac{\partial I_{PTAT}}{\partial T} + m_2 \frac{\partial I_{CTAT}}{\partial T} = 0 \quad (11)$$

Combining equation (10) with (11), m_1 and m_2 can be obtained. Then the width length ratio of MOS transistors can be calculated by equation (8) and (9).

D. Startup Circuit

As shown in Fig.1, the startup circuit is consisted of M_{S1}, M_{S2} and C_S. Comparing with the conventional startup circuits, it does not continue to consume the current, thus decrease the total power consumption of the circuit. At the moment the supply is on, the voltage of the capacitance C_S is zero and the V_{GS} of M_{S1} is about the supply voltage (V_{dd}). Then M_{S1} is turned on, which generates the current and leads the PTAT circuit normally starts. At the same time, the current will charge to C_S till it achieves the V_{dd} and ensures the M_{S1} be switched off.

IV. Simulation Results and Analysis

The lower-power bandgap current reference has been successfully fabricated using SMIC 0.18μm 1.8V technology. The output reference current is 5μA. The power consumption is only 35.22μW.

Fig.2 shows the temperature characteristic of the bandgap current reference under typical process with temperature range from -40℃ to 125℃. The temperature coefficient $TC|_{TT}$ is 42.62ppm/℃ The design is also simulated under another four process corners. The temperature coefficients are: $TC|_{SS}$ is 52.43ppm/℃, $TC|_{FF}$ is 47.02ppm/℃, $TC|_{FNSP}$ is 56.93ppm/℃, $TC|_{SNFP}$ is 51.40ppm/℃.

Fig.3 shows the relationship between the output reference current and supply voltage. The circuit can operate at a low supply voltage 0.6V and output current change from 4.97μA to 5.05μA in the supply voltage range from 1.62 V to 2.00V. With a 1.8V supply voltage, the current reference generates a precise 5μA current.

Fig.4 shows the power supply rejection ratio (PSRR) of the current reference. The PSRR is above 40dB under the 10kHz frequency range.

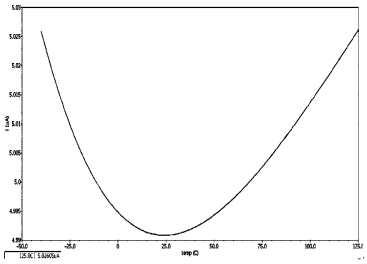

Figure 2. Temperature characteristic of current reference

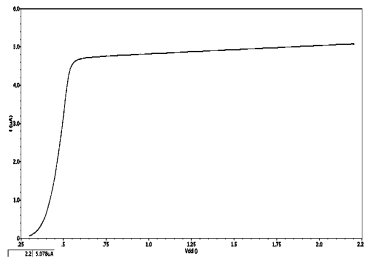

Figure 3. The relationship between the output reference current and supply voltage

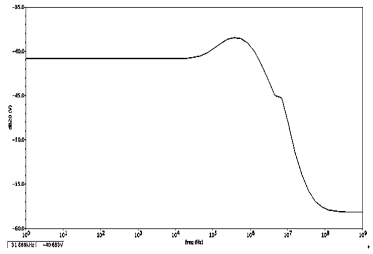

Figure 4. Power supply rejection ratio of the current reference.

V. Conclusion

A CMOS bandgap current reference based on SMIC 0.18μm 1.8V technology has been designed in this paper. The temperature compensation current generator was used in order to obtain low temperature coefficient. At the same time the sub-threshold technology and advanced startup circuit were adopted, which are very useful to reduce the circuit power consumption. The simulation results show that the power is only 35.22μW. The current reference is applicable to low-power and high-precision circuit systems.

References

[1] Guessab S, Benabes P and Kielbasa R: A passive delta-sigma modulator for lower-power application[J]. IEEE Circuits and Systems,2004,3:295-298.

[2] Yu GY. Design of low-voltage low-power CMOS reference[D]. Huazhong University,Wuhan, 2006. (in chinese)

[3] Byung D Y, Young K S, Jee S L,et al. An accurate current reference using temperature and process compensation current mirror[C]. IEEE Asian Solid-State Circuits conference, Taiwan, 2009:241-244.

[4] Qadeer A K, Sanjay K W, Kulbhushan M. Low power started circuits for voltage and current reference with zero steady state current[C]. ISLPED, Seoul,Korea, 2003:184-188.

[5] Harrison W T , Connelly J A , Stair R. An improved current-mode CMOS voltage reference. Proc Southwest Symposium, SSMSD, 2001, 1 :24.

[6] Vittoz E, Fellrath J. CMOS analog integrated circuits based on weak inversion operation[C]. IEEE J Solid-State Circuits.1977,12:224.

[7] Grotjohn T,Hoefflinger B. A parametric short-channel MOS transistor model for subthreshold and strong inversion current[J]. IEEE Trans Electron Devices. 1984,31(2):234.

[8] Xia X J. A CMOS voltage reference based on V_{GS} and ΔV_{GS} in the weak inversion region[J]. Journal of Semiconductors. 2008, 29(8):1523-1528.