TÉCNICO LISBOA

Design of Bandgap Voltage Reference with Curvature Compensation for the Space Industry

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Thesis to obtain the Master of Science Degree in

Electronics Engineering

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ABSTRACT

This Master thesis describes the design steps of a Bandgap Voltage Reference (BGV) with curvature compensation suitable to be used in the space industry. The BGV circuit is an essential block for high performance and reliable circuits, with a wide range of applications in many fields from analog to digital circuits. This work focuses on the design of the different sub-circuits which integrate the bandgap voltage reference and the implementation of the trimming sections, to improve the performance in all the special conditions that the circuit might be exposed to.

The circuit was designed in a 150 nm Silicon On Insulator (SOI) CMOS process technology, using components with radiation hardening characteristics. The simulations achieve a performance of 0.857 ppm/°C of temperature coefficient for a military temperature range, a 1.25 V output reference voltage, and with a power consumption of 2.325 mW.

KEYWORDS

Analog Integrated Circuits Design; Bandgap Voltage References; CMOS Technology; Curvature Compensation; Voltage References; Space Industry; Trimming Resistor.

RESUMO

Esta tese de mestrado descreve o projeto de uma fonte de tensão de referência. “Bandgap Voltage Reference” (BGV) com compensação da tensão de saída, com características adequadas a poder ser utilizada na industria espacial. O circuito BGV é um bloco primordial para circuitos de alto desempenho e confiabilidade, com aplicações em diferentes áreas desde circuitos análogos até digitais. Este trabalho foca-se no projeto dos diferentes blocos que integram o circuito “bandgap voltage reference” e a implementação de duas secções de ajuste, para melhorar o desempenho nas condições de funcionamento, a que o circuito poderá estar exposto.

O circuito foi projetado usando numa tecnologia CMOS de 150 nm “Silicon On Insulator” (SOI), com componentes que tem características para trabalhar em ambientes sujeitos a radiação. Aa simulações mostram resultados obtidos de 0.857 ppm/°C de coeficiente de temperatura para a gama de temperaturas militar, com tensão de referencia de 1.25 V e um consumo de 2.325 mW.

PALAVRAS-CHAVE

Desenho de Circuitos Integrados Analógicos; Bandgap Voltage Reference; Tecnologia CMOS; Compensação de Curvatura de saída; Voltagem de Referência; Industria Espacial; Ajuste de Resistência.

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ACRONYMS

AIDA	Analog Integrated Circuit Design Automation
E_g	Bandgap Energy
BGV	Bandgap Voltage Reference
BJT	Bipolar Junction Transistor
CMOS	Complementary metal–oxide–semiconductor
CTAT	Complementary to Absolute Temperature
DAC	Digital to Analog Converter
DC	Direct Current
ELDR	Enhanced Low Dose Rate
IT	Instituto de Telecomunicações
IC	Integrated Circuit
MIM	Metal Insulator Metal
MC	Monte Carlo
V_{os}	Offset Voltage
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
RHA	Radiation hardened Assurance
SEE	Single Event Effects
TC	Temperature Coefficient
TDRR	Temperature Dependent Resistor Ratio
Vt	Thermal Voltage
TID	Total Ionizing Dose
VREF	Voltage Reference

1 INTRODUCTION

In electronics, the analog and digital circuits consist of different blocks, having a specific function which allows them to work together in order to obtain a desired function. One of the most important blocks in a high performance circuit is the reference block, whose primordial function is to generate specific DC voltages and currents, independent from the variations in the circuit due to noise and changes in supply source and temperature.

This block is normally formed by various circuits as bias, start-up, and regulators. Those circuits are designed with passive and active components that by essence suffer variations in electrical parameters from external factors such as currents, noise, temperature and voltage.

During the 20th century, the field of electronics evolved tremendously adding devices, techniques, and topologies which allowing having an excellent performance and reliability on voltage reference blocks. Today, a broad range of control systems, instrumentation, and supply sources use this block as a fundamental part of them, meaning that the voltage reference is in almost every electronic equipment.

1.1 Motivation

Nowadays, the established priority for companies developing integrated circuits is to be more competitive through reliable products, urging improvements in voltage reference blocks. An area where it is extremely important to have accuracy and reliability in the measures and performance of equipment is the space industry. This is a particular industry because of the involved challenges owing to the cost in the creation, commissioning and maintenance works of such robust devices.

A collaboration with Instituto de Telecomunicações (IT) and Instituto Superior Técnico, a third party ask to redesign and implement a voltage reference block for integration with a Bandgap Voltage Reference circuit, Start-up circuit, Bias circuit and Power down circuit. This implementation has been based on a CMOS 150 nm technology with Radiation-Hardened components for space applications.

1.1.1 Analog Circuit Design

The analog circuit design is essentially analytic and more manual process, if is compared with digital design. The tendency for analog design are related to portability (CMOS technology scaling) and optimization.

1.1.2 Technology

The technology selected is a Silicon on Insulator (SOI) of Complementary metal–oxide–semiconductor (CMOS) in 150 nm. SOI technology specializes in microelectronics to reduce parasitic device capacitance to improve the performance. Besides the improvement, the technology possess radiation hardening capabilities.

1.1.3 Radiation Hardening

Radiation Hardening is the act of making an electronic component and systems resistant to damage or malfunctions caused by ionizing radiation. [1] The electronic components are susceptible to radiation damage.

The Radiation hardened Assurance (RHA), is in charge of ensuring that the Integrated Circuit (IC) can survive certain amounts of different types of radiation. There are some tests to assure it, for example Total Ionizing Dose (TID), Single Event Effects (SEE), and Enhanced Low Dose Rate (ELDR). These tests observe at how good electronics can survive to the levels of radiation.

1.1.4 Bandgap Voltage Reference

A bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. It produces a fixed (constant) voltage regardless of power supply variations, temperature changes and circuit loading from a device. It commonly has an output voltage around the theoretical 1.22 eV bandgap of silicon at 0 K.

1.2 Objectives

The objective of this work is to develop a radiation hardened curvature compensated bandgap voltage reference, with adjustable trimming through one-time programming. Using a CMOS 150 nm technology with tools as Cadence software, Eldo Simulator and AIDA software.

The following goals are set for this project:

- Analyze the state of the art and bibliography related to each circuit that forms the voltage reference circuit, choosing an architecture for each part.
- Create a schematic using the technology related to the design kit provided.
- Corroborate the results obtained in the previous collaboration.
- Define the related key performance to the architecture and create the simulation benches.
- Validate the schematic with the simulation benches.
- Optimize the design with AIDA software for typical and with specific corners.

- Deliver the design database to the final user.

Provide the client with the database generated during the process of this project with the best results archived.

1.2.1 Analog Integrated Circuit Design Automation

An essential objective in this project is the optimization of the circuit using the Analog Integrated Circuit Design Automation (AIDA) software. In particular, from this powerful tool the use of the AIDA-C is required for the circuit sizing.

"AIDA-C is the circuit-level synthesizer supported by state-of-the-art multi-objective optimization kernels, where the robustness of the solutions is attained by considering user-defined worst case corners, that account for process variations and(or) PVT corners." [2].

AIDA software had proved the efficiency and high performance in several publications [3] [4] [5] not only for sizing the devices at schematic level but also in layout level. In section 4, a brief explanation of the set-up for circuits in this software is mentioned.

1.3 Outline

The structure of this document is composed by 5 chapters from the introduction to the reference related and focused on Bandgap Voltage Reference. The first chapter gives a quick introduction to the project based on the motivation and goals. The second chapter presents a basic concepts of voltage reference followed by the state of the art in bandgap voltage reference circuits and a conclusion with a comparison between some architectures. The third chapter explain the blocks used and designed in order to obtain the desired circuit. Simulations and results are presented on chapter 4 how these results were obtained and small improvements on the design. Finally, chapter 5 shows the final conclusion of this work and future work.

2 BACKGROUND & STATE OF THE ART

The Bandgap Voltage Reference is a specific type of voltage references whose main function is to give a constant value of voltage regardless of any variation of the parameters.

2.1 Voltage Reference

The voltage reference circuit is a system that generates a constant output voltage. Ideally, the system isn't affected by the operating voltage, load current, temperature, time or any other disturbance.

This circuit is normally confused as a voltage regulator, but even when both circuits are quite similar, the accuracy between these systems distinguishes one from another. The voltage reference is a circuit which is extremely precise at its output signal, with a reduced noise and a long-term stability. [6]

2.2 Performance Measures

The characterization of a circuit is probably the most emblematic way to quantify its performance, and to be related to a similar system. A voltage reference is measured to identify its reliability and accuracy, such as mentioned before. Providing a highly accurate output voltage regardless of the disturbance around, far-reaching performance in steady and transient state.

The performance of the system in the steady state suffer an influence from the regulations in the line and load, mismatches in the components (as non-ideals), and the well-known channel length modulation effect (λ). On the other hand, the transient state is being influenced by others factors as:

- Temperature Coefficient (TC).
- Linear Regulation.
- Power Supply Rejection Ration (PSRR).
- Output Noise.

2.2.1 Temperature Coefficient

The different operating temperatures in which the system works impact on the performance of every component in the circuit making the output voltage or reference voltage (V_{REF}) a temperature dependent signal. This characteristic is also known as temperature coefficient (TC) and in general form is given by

$$TC = \frac{1}{Reference} * \frac{\partial Reference}{\partial Temperature} \qquad \textit{Equation 1}$$

A particular case to express the Equation 1, where the variation of temperature (ΔT) in the circuit and its alteration suffered at the output voltage ($\Delta V_{REF(nom)}$) are represented. Evaluated in parts-per-million per degree Celsius ($ppm/℃$) is defined in Equation 2.

$$TC = \frac{\left(V_{REF(max),V_{IN(nom)}} - V_{REF(min),V_{IN(nom)}}\right)}{(T_{max} - T_{min}) * V_{REF(nom)}} = \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{\Delta T * V_{REF(nom)}} * 10^6 \qquad \textit{Equation 2}$$

2.2.2 Line Regulation

Line regulation (S) is a variation in the output signal of the system respect to the input voltage variation at a given temperature ($\Delta V_{REF,T(nom)}$), which is normally considered the nominal temperature.

$$S = \frac{\Delta V_{REF,T(nom)}(\Delta V_{IN})}{\Delta V_{IN}} \qquad \textit{Equation 3}$$

In Equation 3, is the representation of this measurement where ΔV_{IN} is the variation of the input voltage at nominal temperature.

2.2.3 Power Supply Rejection Ratio

The PSRR is defined as the ratio of change in the output voltage to reject the noise at specific frequencies on the power supply, expressed in decibels (dB). The expression is given by

$$PSRR(f) = 20 \log \frac{V_{REF,AC}(f)}{V_{IN,AC}(f)} \qquad \textit{Equation 4}$$

Where $V_{IN,AC}(f)$ is the power supply affected by noise at a certain frequency, which can be related directly to $V_{IN} = V_{IN,AC} + V_{IN(nom)}$, therefore the output voltage $V_{REF}(f)$ is an AC coupled reference voltage measured at the output of the voltage reference circuit, such that $V_{REF}(f) = V_{REF(nom)} + V_{REF,AC}(f)$. [6]

2.2.4 Output Noise

Noise is a factor that limits the performance of the circuit. This factor in created by different physical phenomena and is random motion of electrons and holes. There several types of noise, in where this project focus on thermal, shot and flicker noise.

The thermal noise is the random motion of electrons due to the thermal energy, the shot noise is the one created by the junction of two materials where an electric field exists, and the flicker noise is originated for the imperfections of the materials by itself.

The output noise parameter is commonly specified in spectral densities, noise voltage per root hertz$\left(\mathrm{V}/\sqrt{\mathrm{Hz}}\right)$, having a peak-to-peak voltage in a certain bandwidth.

2.3 Bandgap Voltage Reference

In the present, the most popular voltage reference circuit for bipolar and CMOS technology is the Bandgap Voltage Reference (BGV).

2.3.1 Background

In 1964, David Hilbiber published for first time this circuit's concept [7], but only became popular until 1971, when Robert Wildar published one of the most popular topologies in bandgap voltage reference circuits, [8] and it was first implemented in a commercial integrated circuit (LM113). In 1974 another popular topology was published by Paul Brokaw, better known as Brokaw bandgap. [9]. These topologies are represented in Figure 1.

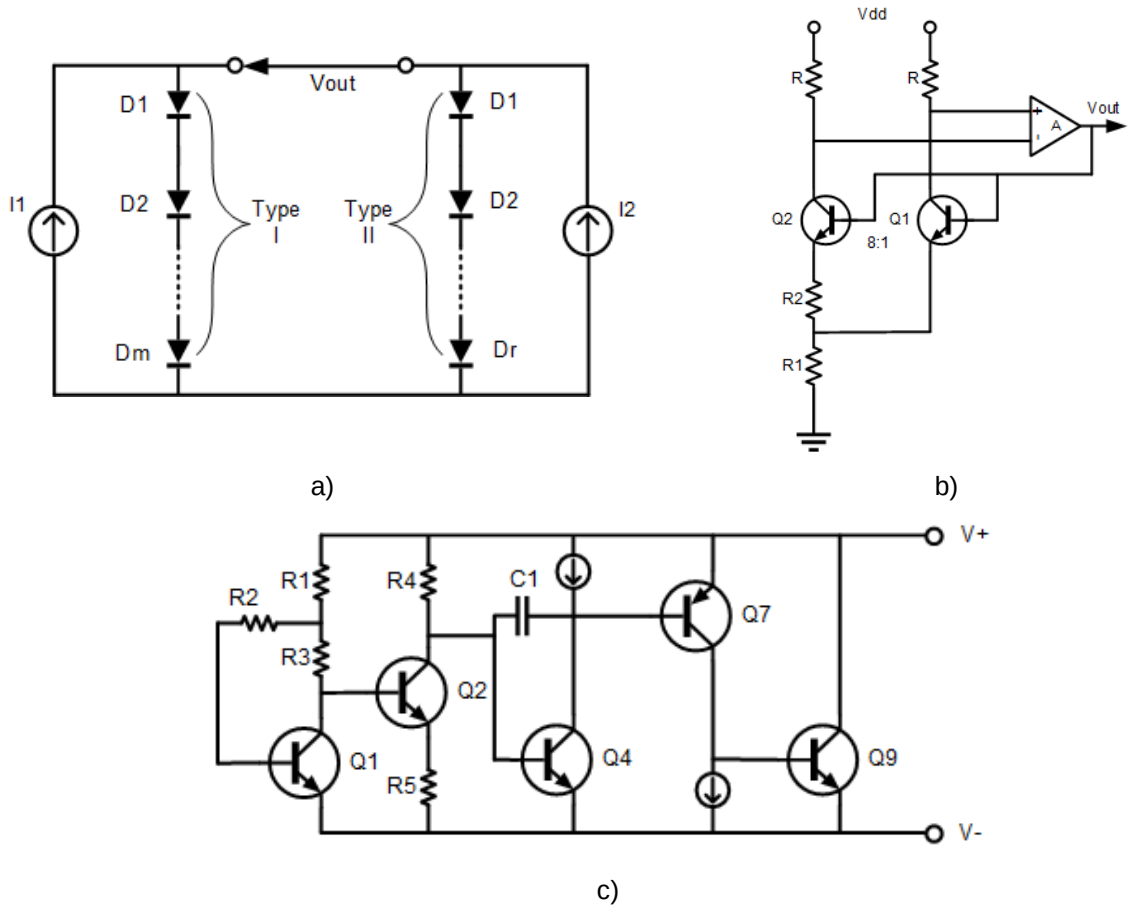


Figure 1 - Background Topologies, a) The basic circuit of the reference voltage source [7], b) The theoretical circuit of a Brokaw bandgap [9], c) Schematic diagram of LM113 (simplified). [8]

2.3.2 Operating Function

The bandgap energy (E_G) is the energy gap between conduction and valence band in semiconductors. For the particular case of Silicon, the bandgap energy is equal to 1.12 electron volt (eV) at 300 K. In the design of a BGV circuit, this value is determined by extrapolating back the PN junction voltage at 0 K of temperature. Finding the back-extrapolated energy at $1.206\ eV$.

This characteristic names the BGV circuit, based on subtracting the voltage of a forward-biased diode (or BJT) having a negative temperature coefficient (TC) from a voltage proportional to absolute temperature (PTAT).

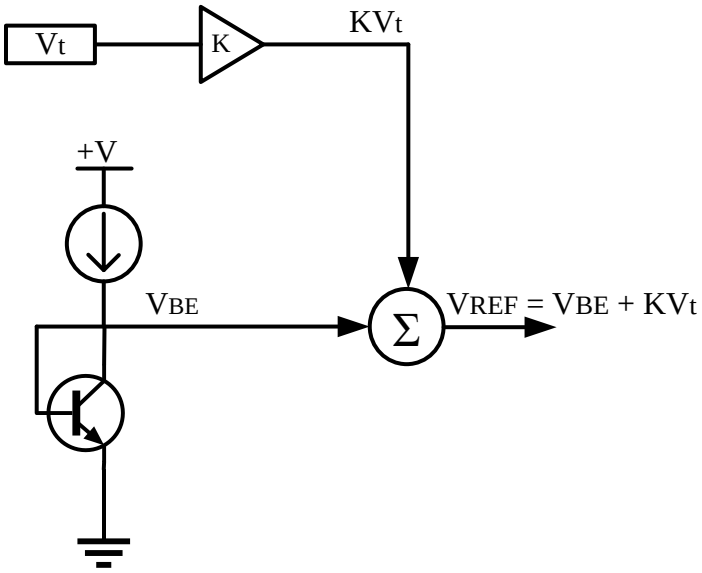


Figure 2 - BGV Operating Function.

Figure 2, illustrates the operating function of a bandgap reference circuit, where the PTAT voltage is obtained by amplifying a difference in the voltage of the two forward-biased base-emitter junctions. The PN junction generates a complementary to absolute temperature voltage (CTAT) also known as emitter-base voltage (V_{EB}) for the case of PNP transistors, this voltage also generates a thermal voltage (V_T) which is a PTAT.

The thermal voltage is amplified by a constant K and added to the emitter-base voltage (V_{EB}) or CTAT, resulting in the expression given by Equation 5. Where the output voltage is the sum of two components (CTAT & PTAT).

$$V_{REF} = V_{EB} + K * V_T \qquad \textit{Equation 5}$$

The thermal voltage is expressed in Equation 6 as the multiplication of Boltzmann's constant ($k = 1.38 * 10^{-23} J/K$) multiplied by an absolute temperature (T) and divided by the electron charge ($q = 1.6 * 10^{-19} C$).

$$V_t = \frac{kT}{q} \qquad \textit{Equation 6}$$

In other words, the operating function of the system is the correspondent compensation of PTAT voltage (V_{PTAT}) and a CTAT voltage (V_{CTAT}) to seek a V_{REF} with $TC = 0$. This compensation can be expressed as the sum of both voltages, such as

$$V_{REF}(T) = m_1 * V_{PTAT}(T) + m_2 * V_{CTAT}(T) \qquad \textit{Equation 7}$$

The m_1 & m_2 components are weighted parameters for the equation. Differentiating Equation 7 with respect to temperature is obtained the Equation 8.

$$\frac{\partial V_{REF}(T)}{\partial T} = m_1 * \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 * \frac{\partial V_{CTAT}(T)}{\partial T} \qquad \textit{Equation 8}$$

Figure 3 illustrates an approximation of the temperature variation of the reference voltage. There is a condition to achieve near zero TC voltage when the output voltage is derivate with respect to the nominal temperature, represented in Equation 9.

$$\left.\frac{\partial V_{REF}(T)}{\partial T}\right|_{T=T(nom)} = 0 \qquad \textit{Equation 9}$$

This partial derivation can also be applied to the general equation of the operating function, which is the Equation 5 and resulting in Equation 10, given by

$$\frac{\partial V_{REF}(T)}{\partial T} = \frac{V_{BE}(T)}{\partial T} + K\frac{V_t(T)}{\partial T} = 0 \qquad \textit{Equation 10}$$

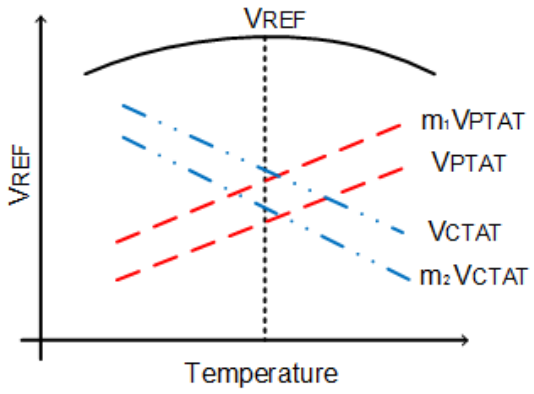


Figure 3 - Graph of the compensation between VPTAT and CTAT.

2.3.3 Analysis for Base-Emitter Voltage

A very popular technology to implement the BGV circuit is the CMOS technology in which the principle of working is similar to the ones of the bipolar technology. In bipolar technology, the theory is quite similar to the NPN and PNP junctions presenting a few obvious modifications.

For NPN transistors, If the early effect is neglected, the bias current to work on the active region is given by Equation 11 where is shows the dependency of temperature.

$$I_C(T) = I_s(T) * e^{\left(\frac{V_{BE}}{V_T}\right)} \qquad \textit{Equation 11}$$

The temperature dependent collector current $I_c(T)$ is equivalent to the bias current, $I_s(T)$ is the temperature dependent saturation current, that is given by

$$I_s(T) = J_s(T) * A_E \qquad \textit{Equation 12}$$

$$I_C(T) = J_C(T) * A_E \qquad \textit{Equation 13}$$

where A_E is the base-emitter junction area, $J_s(T)$ is the saturation current density and $J_C(T)$ is the collector current density.

Thus, inserting Equation 12 and Equation 13 into Equation 14, gives

$$J_C(T) * A_E = J_s(T) * A_E * e^{\left(\frac{V_{BE}}{V_t}\right)} \qquad \textit{Equation 14}$$

Without doing depth on the semiconductor physics of BJT [6], the base-emitter voltage V_{BE} is given by

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE}(T_0)\frac{T}{T_0} - \rho\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) + \frac{kT}{q}\ln\left(\frac{J_C(T)}{J_C(T_0)}\right) \qquad \textit{Equation 15}$$

Where V_{G0} is the bandgap voltage of Silicon at 0 K previously mentioned as the extrapolated bandgap energy (E_g) equals to $1.206\ V$, ρ is a process dependent temperature constant. The subscript 0 designates an appropriate quantity at a reference temperature T_0.

Assuming that collector current is a temperature depend, which can be represented as

$$I_C(T) = a * T^{\theta} \qquad \textit{Equation 16}$$

Where a is a constant and θ is the order of temperature dependency, if $\theta = 0$ implies that the collector current is independent of temperature, and if $\theta = 1$ implies that the collector current varies linearly with temperature.

The collector current density at temperature T with respect to the collector current density at the reference temperature T_0 is given by

$$\frac{J_C(T)}{J_C(T_0)} = \left(\frac{T}{T_0}\right)^{\theta} \qquad \textit{Equation 17}$$

Due to this, Equation 15 is simplified as

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE}(T_0)\frac{T}{T_0} - (\rho - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \qquad \textit{Equation 18}$$

The base-emitter voltage is nonlinearly related to temperature, and due to $V_{BE}(T_0)$ the $V_{BE}(T)$ should vary with the biasing condition (which depends on the collector current) as well as the transistor size. [6]

2.4 High Order Compensation

Nowadays, the industry uses a high order compensation circuit due to the benefices in reliability and accuracy. A first order compensation is the one represented in Equation 5. To improve the performance of the circuit, in particular, to reduce the temperature coefficient over an extensive range of temperatures is imperative the compensation of the CTAT & PTAT voltages with a nonlinear term or higher order compensation.

The compensated error between CTAT and PTAT voltages as nonlinear terms is known as curvature error. Besides this error, all the variations of components in the circuit forms a crucial factor which affects the accuracy of the system. These variations can be reduced with implementations techniques in each process technology to improve the reliability of the whole circuit.

The high order compensation is also known as *curvature compensation* or *curvature correction*. Theoretically, the adjustment to obtain a near-zero temperature coefficient voltage is based on the proper scale of CTAT and PTAT voltages which in reality are rarely precisely and linearly proportional to temperature.

A better understanding of the dependency in temperature is clearly seen with the expansion of Taylor series for CTAT & PTAT voltages at $\mathrm{T} = \mathrm{T}_0$, represented in Equation 19 and Equation 20.

$$V_{CTAT}(T) = a_0 + a_1\left(T + T_{(nom)}\right) + a_2\left(T + T_{(nom)}\right)^2 + a_3\left(T + T_{(nom)}\right)^3 + \cdots, \qquad \textit{Equation 19}$$

$$V_{PTAT}(T) = b_0 + b_1\left(T + T_{(nom)}\right) + b_2\left(T + T_{(nom)}\right)^2 + b_3\left(T + T_{(nom)}\right)^3 + \cdots, \qquad \textit{Equation 20}$$

The a_k and b_k are constant coefficients of the $k-th$ order temperature dependent terms with respect to $T_{(nom)}$. Although the coefficient associated with the nonlinear terms can be small, they could become

dominant sources of curvature error at temperature notably superior or minor than $T_{(nom)}$. Assuming the voltage reference obtained by temperature depends on a weighted sum of CTAT and PTAT voltages.

Rewriting Equation 7 for a higher compensation is expressed in Equation 21.

$$V_{BE}(T) = m(T) * V_{CTAT}(T) + n(T) * V_{PTAT}(T) \qquad \textit{Equation 21}$$

The combined functions $m(T) * V_{CTAT}(T) + n(T) * V_{PTAT}(T)$ are voltage functions with nonlinear terms (high order functions).

2.4.1 Second Order Compensation

A topological diagram of second order compensation for the temperature in a voltage reference circuit is represented in Figure 4. The addition of a voltage with second order TC at the appropriate temperature region will be able to increase the reference voltage at the selected temperature region, and thus archive a low TC reference voltage over a wide temperature range.

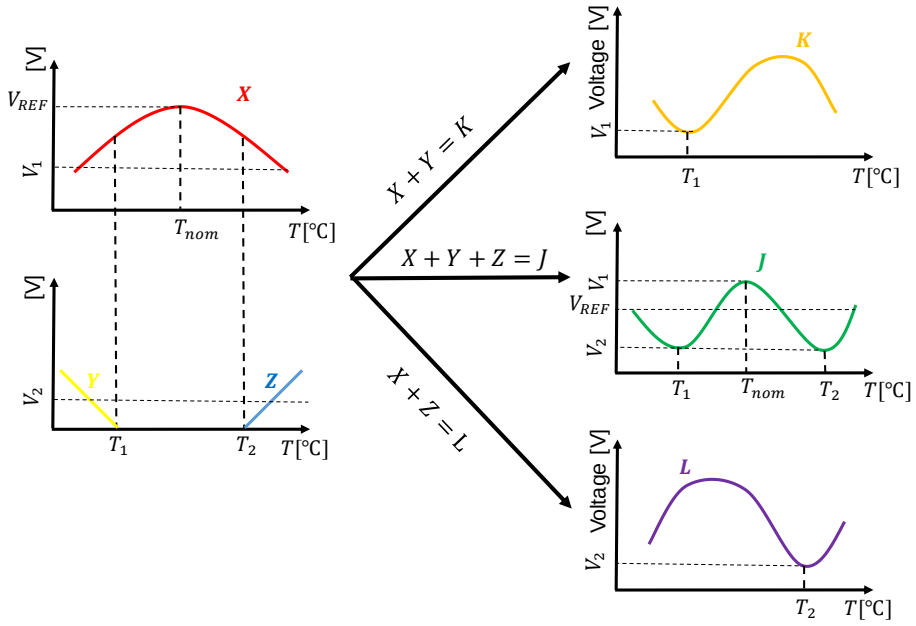


Figure 4 - Representation of second order compensation of the BGV.

This second order temperature dependent voltage is expressed in correspondence to the Equation 21, such that

$$V_{BE}(T) = m * V_{CTAT}(T) + n * V_{PTAT}(T) + s(T - T_{(nom)})^2 \qquad \textit{Equation 22}$$

Where m & n, are temperature independent constant values adopted from $m(T)$ & $n(T)$. An additional the second order temperate depended voltage $s(T - T_{(nom)})^2$, in which s must be assumed to be a constant form the Taylor series.

2.5 Curvature Compensation Techniques

There are various techniques used to cancel the higher order components. Every technique is based on different principles, even when these techniques have some limitations with respect the others is always important to consider the architecture and the application of the circuit to pick the one which suits better. Some of the most important techniques are explained below.

2.5.1 PTAT2

PTAT^2 technique is to offset the negative temperature dependence of the logarithmic term in V_{BE} with a positive parabolic term as is illustrated in Figure 5.

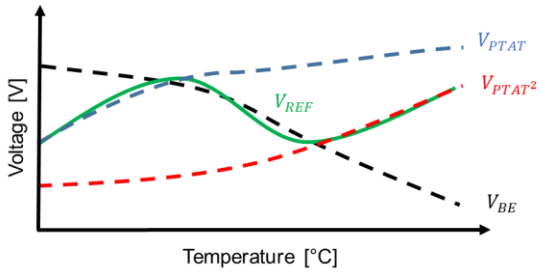


Figure 5 - Representation of PTAT2 technique.

The lower temperature range is mainly controlled by the V_{BE} and by the linear PTAT component $(V_{BE} + V_{PTAT})$. As a result, the first half of the temperature range exhibits the curvature of a first order reference. This behavior is used to cancel the increasingly negative temperature dependence of the base-emitter voltage at higher temperatures.

2.5.2 Temperature Dependent Resistor Ratio

The Temperature Dependent Resistor Ratio (TDRR) is based on generating a high order term by exploiting the temperature dependence of difference resistors in a specific technology. Figure 6, illustrates an example of a technique where the TC of different resistors is used to compensate the higher order components. The objective is generated a PTAT^2 voltage without an important increase of the power consumption.

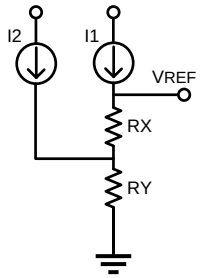


Figure 6 - Example circuit of TDRR technique.

Where I_1 equals to $\frac{BV_{CTAT}}{R_2}$, I_2 equals to $\frac{AV_{PTAT}}{R_1}$ and V_{REF} is given by

$$V_{REF} = \frac{AV_{PTAT}}{R_1}R_Y + \frac{BV_{CTAT}}{R_2}R_Y + \frac{BV_{CTAT}}{R_2}R_X \qquad \textit{Equation 23}$$

Where A and B are temperature independent constants, and R_1 & R_2 are form the core of BGV. The advantage of this technique is a simple implementation having an increase of the power consumption, but depending on the technology for use resistors with different TC.

2.5.3 β compensation

In Bipolar technology, the β gain of the forward-current is an exponential temperature dependence that can be overworked to correct the high order behavior of the diode voltage, $\beta \propto e^{-1/T}$. And for this technology the current gain β increases exponentially with rising temperatures.

Figure 7 shows the exponential characteristic mentioned above with a simple circuit.

The V_{REF} for this circuit is given by

$$V_{REF} = -\left(XT + \frac{YT}{\beta}\right)R - V_{BE} \qquad \textit{Equation 24}$$

Where X and Y are temperature independent constants and T is temperature.

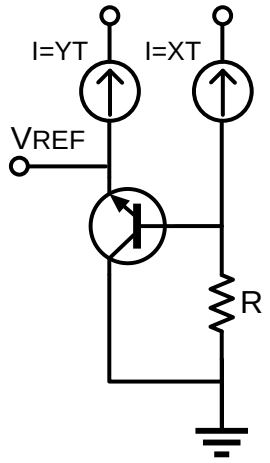


Figure 7 - Example circuit of β compensation.

2.5.4 Piecewise Linear Compensation

The piecewise linear compensation or multi-point curvature compensation, works dividing the range of temperature into multiples and consecutives non-overlapping sections, and implementing various circuit of temperature compensation with altered temperature sections.

Some of the advantages to perform temperature compensation in separate temperature sections are:

- Size
- Direction

The size because of the reduced covered section in each segment, where the curvature of $V_{CTAT}(T)$ and $V_{PTAT}(T)$ can be approximated to be linear.

The direction, which mean the signs of the slope of each adjacent section, as seen in Figure 8. The variation of the reference voltage in adjacent sections won't be accumulated, allowing the extraction of a low TC reference voltage over a wide temperature range.

The voltage variation can be reduced with a narrower temperature range and the whole temperature range can be sub-divide into different section to obtain a small TC over the range. All the circuits used to create the curvature compensation are sensitive to temperature.

It is important to mention that there are some other techniques which are not only intended for compensation, but to cancel the nonlinearity terms.

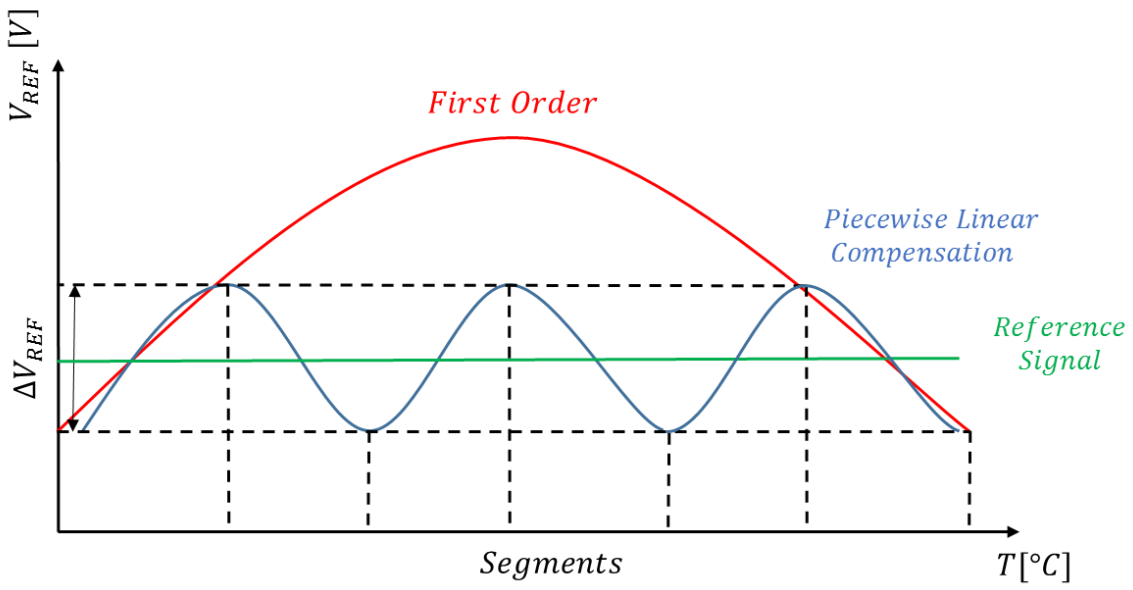


Figure 8 - Illustration of Piecewise Linear Compensation technique.

2.6 Topology

A wide assortment of topologies for second order compensation was published in the last 15 years, is quite complex to decide on which is better than others, these topologies were implemented with different stages and techniques but all following the principle of the compensation.

A topology used as influence to implement this project is a popular architecture proposed in 2001 by Malcovati P., Maloberti F., & Pruzzi M. [10]. The characteristics and results presented, fix into the type of topology look to fulfill the specifications for this project.

Figure 9 shows the schematic of the bandgap circuit presented on the publication, this circuit also require an Operational Amplifier, Start-up circuit and the second order compensation.

Table 1 shows the results presented in this publication in a BiCMOS technology.

Table 1 - Results presented by Malcovati P., Maloberti F., & Pruzzi M. [10]

Technology [µM]	VREF [V]	TC [ppm/ °C]	TR [°C]		Supply Voltage [V]	Power [µW] @ 25 °C
			From	To		
0.8	0.54	7.5	0	80	1	92

As expressed by the authors the architecture used allow a direct implementation of the curvature compensation method.

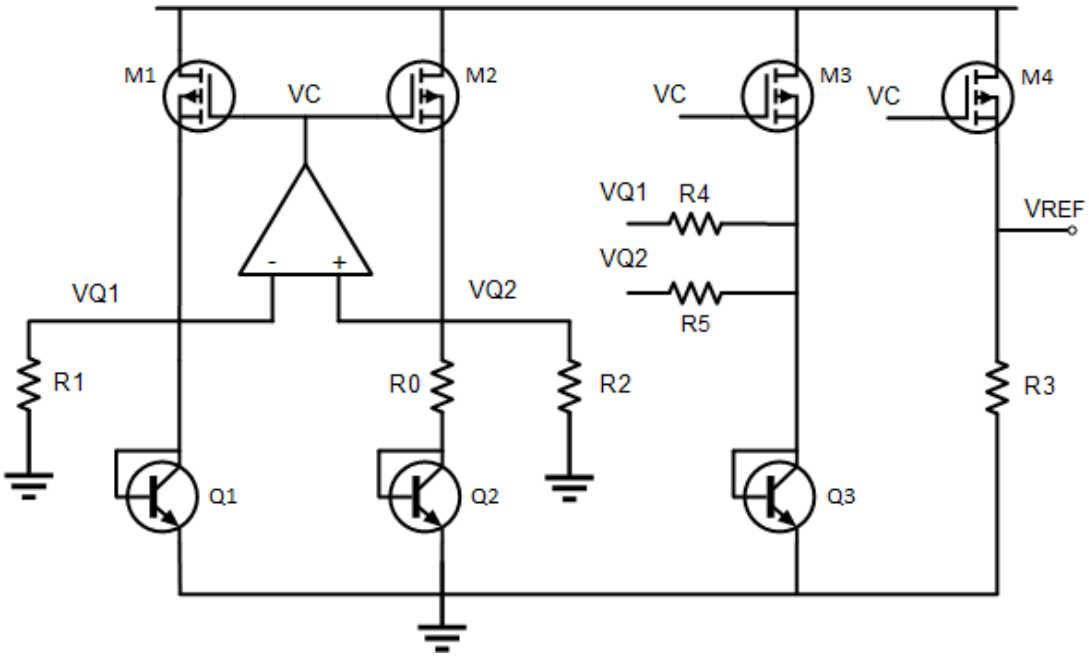


Figure 9 - Topology proposed in 2001 by Malcovati P., Maloberti F., & Pruzzi M.

2.7 Circuit Comparison

Knowing that there are more than a few parameters to be considered in a comparison of Bandgap Voltage Reference circuit and even more different techniques. In a simplification Table 2 shows a correlation of the recent publications.

Table 2 - Correlation between some architectures.

Ref.	Tech. [µM]	VREF [V]	TC [ppm/°C]	TR [°C]		Supply Voltage [V]	PSRR [dB]	Year	Topology
				From	To				
[11]	0.18	1.2437	8.62	-25	115	2.5	100	2010	1st Order Compensation
[12]	0.35	1.09	3.1	-20	100	3	80	2010	2nd Order Compensation
[13]	0.11	0.603	13.5	-40	140	1	60	2011	1st Order Compensation
[14]	0.16	1.0875	5	-40	125	1.8	74	2011	Curvature Compensation with Chopper Amp.
[15]	0.18	1.66	48.7	-10	100	3.5	76	2011	1st Order Compensation
[16]	0.35	3	2.1	-40	125	-	-	2011	Curvature Compensation with a second Amp.
[17]	0.35	0.6177	3.9	-15	150	2.5	-	2012	Curvature Compensation with a second Amp.
[18]	0.35	1.175	1.5	-40	120	5	-	2012	2nd Order Compensation
[19]	0.18	0.82	15.67	-55	125	1.7	96.56	2013	2nd Order Compensation
[20]	0.18	1.195	7.72	-40	125	2.6	62	2013	1st Order Compensation
[21]	0.18	0.767	4.5	-40	120	1.2	-	2014	Curvature Compensation with a second Amp.
[22]	0.5	1.2937	4.1	-40	125	2.7	82	2015	Curvature Compensation with a second Amp.
[23]	0.35	1.25	2	-55	125	3.3	81.93	2016	2nd Order Compensation
Spec	0.15	1.25	<10	-55	125	3.3	>60	-	2nd Order Compensation

2.8 Specifications

The specifications proposed in this project are reflected on Table 3, where the BGV must be stable and with 7 bits to facilitate the trimming section.

A crucial request for this implementation are the feature that helps to avoid the radiation effects, which are using a specific technology and 10 µA of current in each branch of the circuit. Also considerations in the output filter to eliminate the internal noise.

The specifications not mentioned in Table 3 will be indicated as needed.

Table 3 - Specifications for the project.

Voltage Reference [V]	Supply Voltage [V]	Current Cons. [mA]	TC [ppm/°C]	Minimum Current for branch [µA]	No. Bits for trimming	PSRR [dB]
1.25	3.3	<1	<10	10	7	>60

2.9 Conclusion

The efforts were based on improving the circuit on reference [10] and [23], due to the properties and characteristic of the architecture as was mentioned before. This project is made in 150 nm CMOS technology with Atmel foundry.

Choosing a suitable architecture to implement took several considerations, from the performance presented in their respective publication to the specifications needed for the new circuit. Discarding the topologies with just a first order compensation due to the low temperature coefficient intended to accomplish.

The selection of architecture was reduced as well from the possible consideration of implement a second operational amplifier for the curvature correction. Being easy to implement just one operational amplifier and compensate the output though another bipolar transistor with a couple of resistors.

In general, the selection of this topology facilitates the application of techniques to improve the quality of the circuit. The chosen topology is surly older if comparted with recent topologies, but the architecture not only allows modifications in the different blocks of the circuit, also proves to have a good performance in a recent implementation as demonstrated in [23]. These results literally influenced the decision of maintain the chosen topology.

3 CIRCUIT DESIGN

The bandgap voltage reference circuit framework and design is presented. Each stage of the circuit, the characterization and also the considerations made for the circuit are explained in more detail.

3.1 Bandgap Voltage Reference

The topology used to implement the BGV circuit for this project is the one based on the principle of the one proposed in [10] which is an adaptation of [24]. As previously mentioned, this architecture was first implemented in CMOS technology 350 nm in the foundry of XFAB, obtaining good results [23]. In consequence, it was decided to implement it in a new technology, which in this case is CMOS 150 nm of Atmel foundry.

Some modifications to the circuit done in XFAB are implemented to improve the performance and to migrate to a smaller technology and with similar specifications. The BGV architecture is illustrated as a block diagram in Figure 10. Furthermore, Atmel 150nm technology is also looking for a second order compensation of output voltage.

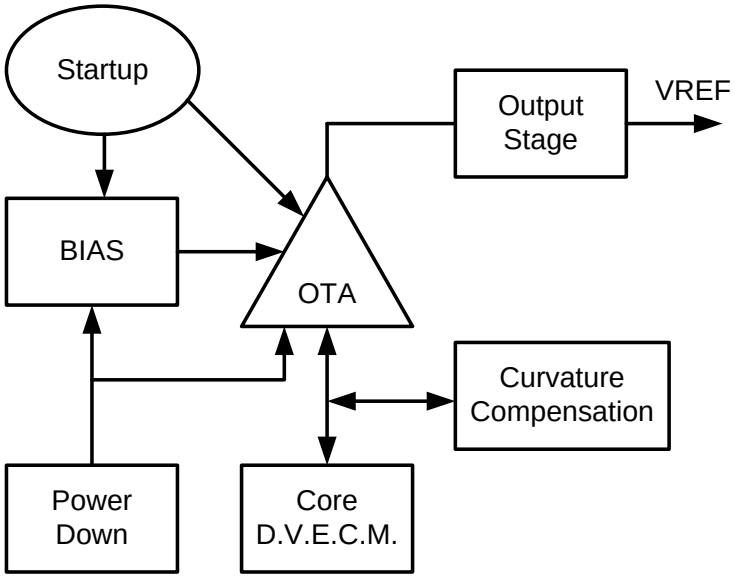


Figure 10 - BGV Block Diagram.

Hence, the whole circuit is divided into 7 sub-circuits (Bias, Curvature Compensation, OTA, Output Stage, Power-Down, Start-up & Core). These sub-circuits perform a particular function which allow the BGV to function as specified.

In general, the Bandgap Voltage Reference circuit works with the principle of compensation method as demonstrated in Chapter 2. Considering that this circuit is a metastable system, which means it can be stable in equilibrium and quasi-equilibrium state. As will be explained later, a startup circuit is implemented to force to reach the equilibrium by providing an excitation in the circuit. Just having in mind that should be analyzed in transient and stable state.

3.2 Component Characterization

An important part to analyze in the circuit is the characterization of every component used in the circuit. Essential information of the devices is obtained; from the datasheet of the foundry. A brief analysis of the components is presented in the following sections.

3.2.1 MOSFETs

The metal-oxide semiconductor field-effect transistor (MOSFET), is a popular component in the design of the analog circuits due to its properties and simple structure. There are two types of structures for these components, which are N-type & P-type better known as NMOS and PMOS transistors. Figure 11 illustrates the symbols of the NMOS and PMOS.

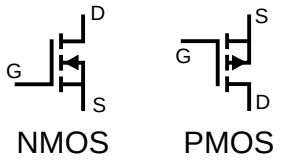


Figure 11 - MOSFET Symbols.

The parameters to be modified in these components are Width “W”, Length “L” and the Multiplication Factor “M”. For reference purposes, these components are 3.3V MOS having a maximum voltage rating from Drain to Source of 3.6 V. The threshold voltage (V_{th}) for a rate of $W/L = 1$ is 0.63V for typical conditions.

3.2.2 BJT – Vertical PNP

The Bipolar Junction Transistor (BJT) is essential in the BGV, used for the generation of temperature dependent voltage. For the case of this voltage reference the vertical PNP transistors will be implemented in the CMOS process, illustrated in Figure 12. Nevertheless, the PNP has some characteristics that can be considered as limitations. The gain of the transistor (β), is very low when compared to an NPN transistor,

defined as $\beta = \mathrm{I_C}/\mathrm{I_B}$. In this case the BJT will be configured as a diode; connecting the base terminal with the collector terminal converts the base emitter voltage V_{EB} into the fixed junction voltage.

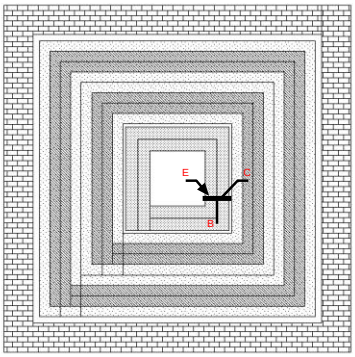


Figure 12 - Vertical PNP Transistor (Extracted Layout).

The V_{EB} (T) will force the collector current (I_C), and the transistor size will depend on the emitter area (A_E). Knowing the A_E is fixed in this case, some simulations were made with different biasing condition to evaluate the base emitter voltage with respect to temperate. A representation with the obtained results is shown in Figure 13.

From the bottom to the top of the signals in the graph are the biasing conditions from 10 µA up to 20 µA, changing the temperature from -55 °C to 125 °C. Having $V_{EB}(T) = 783.881\ mV$ at $T = 25$ ℃ for $I_C = 10\ \mu A$.

The temperature dependency (TD) of V_{EB} for the PNP transistor is a nonlinear parameter and is given by

$$\frac{\partial V_{EB}(T)}{\partial T} \qquad \textit{Equation 25}$$

The values of temperature dependency for different key temperatures are shown in Table 4, specifically for $I_C = 10\ \mu A$.

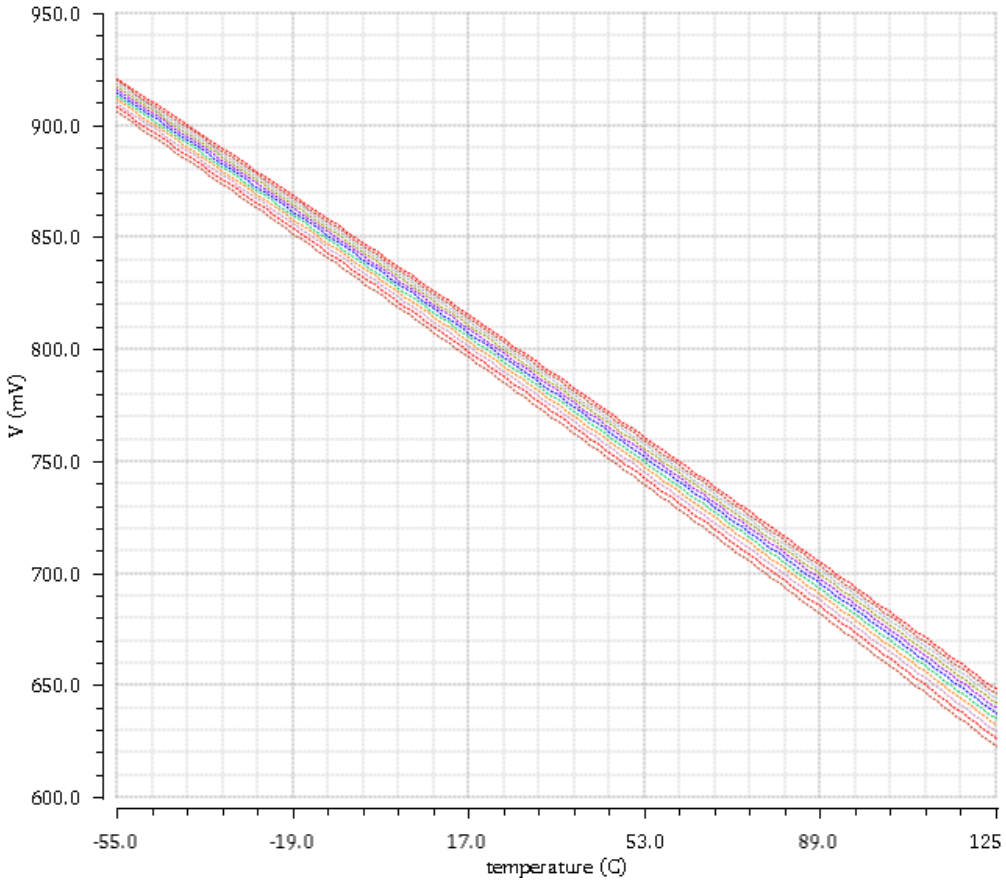


Figure 13 – Temperature variation of PNP transistor with different biasing.

The nonlinearity as is exposed above represents a possible error in the curvature, and just for practical analysis this dependency will be considered as

$$\frac{\partial V_{EB}(T)}{\partial T} \approx -1.56 \qquad \textit{Equation 26}$$

There are two considerations for the BJT which are the limited β and the base resistance R_b. This resistance is generated by a series of resistances for the N transistors connected in series. These considerations will be overlooked to calculate the circuit in a theoretical form.

Table 4 – V_{EB} of Vertical PNP dependency for key temperatures.

T [°C]	V_{EB} [mV]	TD [mV/K]
-55	905.853	1.4788
0	822.748	1.5421
25	783.884	1.5672
125	622.817	1.6505

3.2.3 Resistor

One of the most important components in the BGV is the resistor. The potential impact in the behavior of the whole circuit is high due to the temperature coefficient (TC) and the variability of its value in relation with temperature.

In this technology, more specifically in the foundry used in the chosen model, the poly resistance is the one that suffers less due to variations in temperature. Characterizing a couple of devices is possible to make a quick comparison between these models.

3.2.3.1 Characterization

As mentioned above, the resistor is an intrinsic device that not only transform voltage to current or the other way around. Properly adjusting its value will influence the current and voltage. The most important parameter in the resistors is the sheet resistance (Ω/sq), which describes the resistance of a resistor in a square unit, temperature and voltage sensitivities, such that

$$R(T) = R_{sheet}(1 + T_{CR1}(T - T_r) + T_{CR2}(T - T_r)^2 \dots + T_{CRn}(T - T_r)^n \quad \textit{Equation 27}$$

$$R(V) = R_{sheet}(1 + V_{CR1}(T - T_r) + V_{CR2}(T - T_r)^2 \dots + V_{CRn}(T - T_r)^n \quad \textit{Equation 28}$$

Where T_{CRn} and V_{CRn} are the n order coefficient of temperature and voltage respectively. [6]. Therefore, a comparison of the models considered for this characterization are shown in Table 5.

Table 5 - Resistor characterization.

	rplow	rphigh	Unit
Sheet Resistance	235	900	Ω/sq
1st order VC	0	0	ppm/V
1st order TC	-3500	-2410	ppm/°C

Considering the references above, a small simulation was performed with both models for the range of temperature using the values that are listed in the Table 6 and applying a voltage source of 900 mV. The obtained results are presented in Figure 13 where the most horizontal line is rplow and the diagonal line is rphigh. The resistance variation is interpreted by current against temperature, values for the key temperatures are shown in Table 7.

Table 6 - Test parameters in resistors.

	R [Ω]	W [µm]	L [µm]
rplow	31999.4	1.8	231.06
rphigh	32001.3	1.8	61.78

Table 7 - Temperature characterization of resistors.

Temp [°C]	rplow [KΩ]	rphigh [KΩ]
-55	31.53	37.32
0	30.7	32.81
25	30.4	31.04
125	29.56	25.74

The values of current in the graph for the range of temperature are interpreted as variations in the resistance value, and is clearly observed that these values aren't linear which means the variation is not linear in neither of the two cases. The most horizontal line represents the rplow model and is the one chosen to be part of the design because it has the smallest variation of both models.

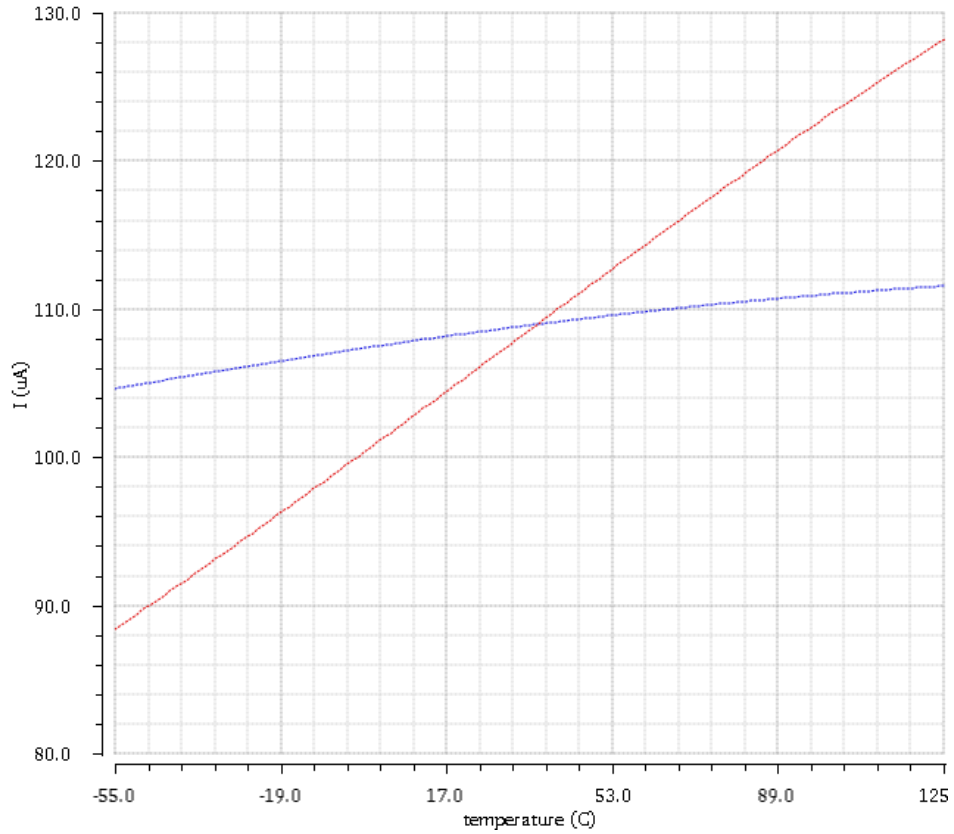


Figure 14 - Variation of current v. temperature of rplow (the linear) and the rphigh (the transveral) resistors.

As represented in Table 6, the length “L” of rplow is way bigger than for rphigh, which is considered for the size of the circuit.

This will be an important parameter when the unitary value of resistance is chosen to implement the trimming on the circuit.

3.2.4 Capacitor

The capacitor used in this implementation is a Metal Insulator Metal (MIM) Capacitor which has a Capacitance per Unit Area (C_{NYNX}) equal to $1.6\ \mathrm{fF}/\mu\mathrm{m}^2$ at $25\ ℃$.

Allowing an incremental scaling of $0.001\mu m$ for width and length. The layout is illustrated in Figure 15.

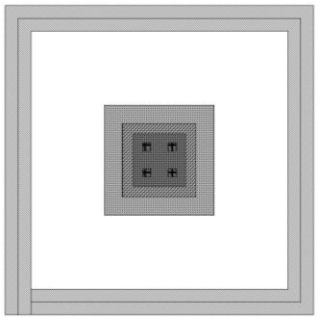


Figure 15 - Metal Insulator Metal Capacitor (Extracted Layout).

3.3 Sub-Circuits

Once the characterization of the components is done, the next step is the analysis and design of each stage of the circuit.

3.3.1 Drain Voltage Equalization Current Mirror (Core)

The drain voltage equalization current mirror is better known as the core or the PTAT (ΔV_{EB}). Being the difference of V_{EB} between two Bipolar Junction Transistors biased with different current densities (ΔJ), and as demonstrated before the current density is associated to the emitter areas (A_E). Figure 16 illustrates how the ΔV_{EB} is obtained from the BJTs $(Q_0\ \&\ Q_1)$.

An important consideration must to be assumed is that the emitter areas have a ratio between them of 1:N, and the bias current or emitter current (I_E) are equals.

From the Figure 16 and with the mentioned considerations, the Equation 29 is obtained.

$$\Delta V_{EB} = V_{EB0} - V_{EB1} \qquad \textit{Equation 29}$$

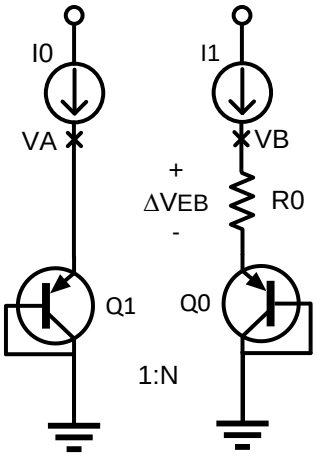


Figure 16 - ΔV_{EB} Extraction.

Using the Equation 14 into Equation 29 yields ΔV_{EB} as

$$\Delta V_{EB} = V_T \ln\left(\frac{I_{E0}}{J_s A_{E0}}\right) - V_T \ln\left(\frac{I_{E1}}{J_s A_{E1}}\right) \quad \textit{Equation 30}$$

$$\Delta V_{EB} = V_T \ln\left(\frac{A_{E1}}{A_{E0}}\right) \quad \textit{Equation 31}$$

$$\Delta V_{EB} = V_T \ln(N) \quad \textit{Equation 32}$$

Directly from Figure 16, if $V_A = V_B$, the ΔV_{EB} will be the same as the voltage in R_0, due so the current flowing through the resistor is defined as

$$I_0 = \frac{\Delta V_{EB}}{R_0} = \frac{V_T \ln(N)}{R_0} \quad \textit{Equation 33}$$

Due to this relationship, it is possible to increase the current flowing through R_0 by decreasing the resistance, which will be considered for one of the specifications $(10\ \mu A)$.

In order to ensure the conditions of equality in the circuit such as the currents $(I_0 = I_1)$ and the voltages $(V_A = V_B)$. A current mirror is implemented to give a better similitude between the currents, and for the voltage a drain voltage equalization technique is used implementing an operational amplifier (in this case

OTA) in the positive feedback loop with its input connected to the drains of the transistors in the current mirror as is show in Figure 17.

From this new configuration, $V_A = V - \ \& V_B = V +$, it forces the transistors to have the same potential and thus equal drain voltage.

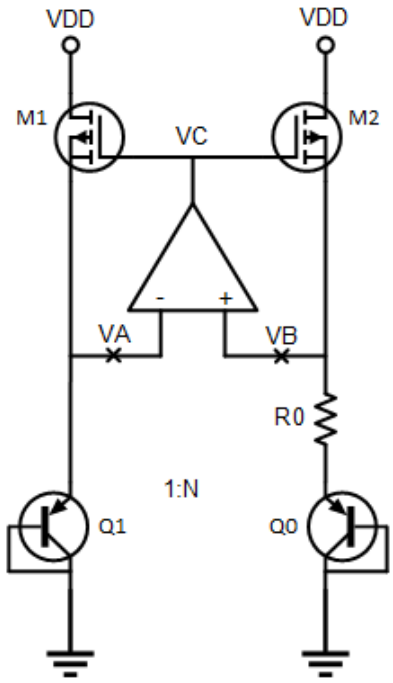


Figure 17 - Connection of Core with Amp-Op.

3.3.2 Operational Transconductance Amplifier

The Operational Transconductance Amplifier (OTA) is an operational amplifier with high impedance in the input and output stages. Its principal function is to produce an output current based on differential input voltage, also known as Voltage Controlled Current Source (VCCS).

One of the characteristics of the OTA circuit is that it only drives capacitive loads, because a resistive load diminishes the gain of the circuit, unless the resistive load is very large. An apparent limitation is the difficulty of archive high value of bandwidth, but on the assumption that is used on BGV circuit this restriction is no longer a problem.

Considering the characteristics of this type of OPAMP in combination of ease analysis and implementation, a 2nd stage Miller OTA circuit was selected to carry out the duty for this BGV.

Figure 18, illustrates the schematic used for the implementation of OTA, where the first stage is a differential pair (transistors M3 and M4) with active load (M0 and M1). The second stage is a common source amplifier

(M2), biasing by a current mirror formed by M5, M6 and M7. A capacitor (XC0) between first and second stages is used as the Miller compensation.

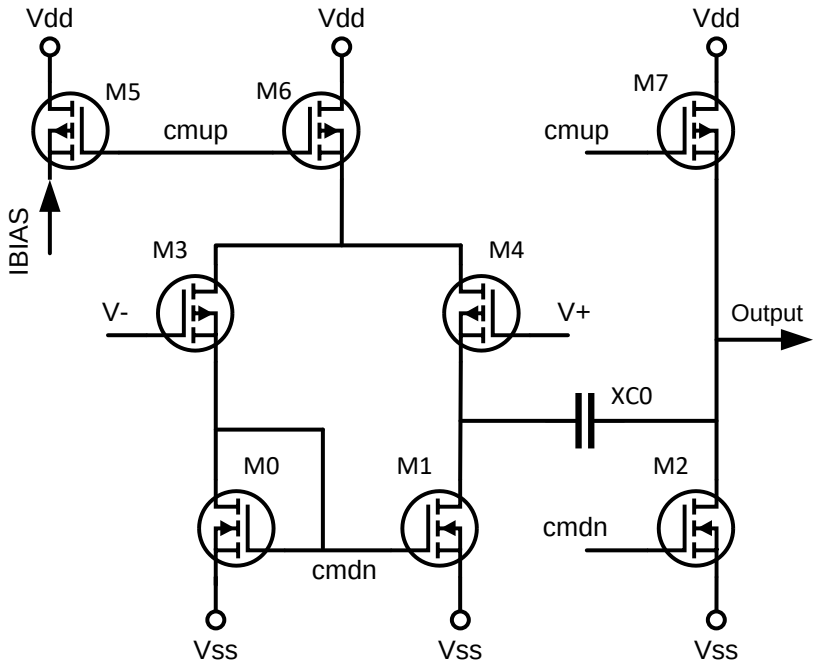


Figure 18 - Operational Transconductance Amplifier schematic.

3.3.2.1 Analysis

An extremely important consideration is the matching of the differential pair of transistors, due to the voltage offset generated. The first stage converts the differential input voltage into a current by means of transconductance g_{m3}. The second stage is a transimpedance amplifier, which converts the current into a voltage. This architecture generates two poles at the outputs of both stages and those are split by the capacitor (C).

The gain of this circuit A_V is given by multiplying the gains of both stages, such as

$$A_V = A_{v1} * A_{v2} \qquad \textit{Equation 34}$$

Where A_{v1} and A_{v2} represents the gains of each stage. For the first stage, the gain is obtained by multiplying the transconductance g_{m3} against the resistance of the stage R_{s1}, presented in Equation 35.

$$A_{v1} = g_{m3} * R_{s1} \qquad \textit{Equation 35}$$

The output resistance R_{s1} of this block is given by

$$R_{s1} = \frac{1}{g_{o41}}$$ *Equation 36*

The g_{o41} is representation of $g_{o4} + g_{o1}$, the transconductance of 1st stage output transistors. For the 2nd stage the gain is defined in a similar way, such as

$$A_{v2} = g_{m2} * R_{s2}$$ *Equation 37*

The R_{s2} is given by

$$R_{s2} = \frac{1}{g_{oL}} = \frac{1}{(g_{o7} \parallel g_{o2} \parallel g_L)}$$ *Equation 38*

Being $g_{o7}\ and\ g_{o2}$ the respective transconductance of transistors MO7 and MO2, and g_L the transconductance of the load.

Regarding the bandwidth, it is due to the Miller effect of capacitance. The bandwidth product (GBW) is related as is shows in Equation 39. [25]

$$GBW = \frac{g_{m3}}{2\pi * C}$$ *Equation 39*

The position of the dominant pole (f_d) and the non-dominant pole (f_{nd}) are shown in Equation 40 and Equation 41 respectively. [25]

$$f_d = \frac{g_{o41}}{2\pi * A_{v2} * C}$$ *Equation 40*

$$f_{nd} = \frac{g_{m3}}{2\pi * C_L} + \frac{1}{1 + \frac{C_{n2}}{C} + \frac{C_{n2}}{C_L}}$$ *Equation 41*

A parasitic capacitance of the output transistor (C_{n2}) is indispensable to calculate the non-dominant pole. The C_L is the load capacitance. In order to calculate the phase margin, the formula presented in Equation 42 is used.

$$PM = 90 - \tan^{-1}\frac{GBW}{f_{nd}}$$ *Equation 42*

Taking into account the specifications established for the design of this project, such as the minimum current per branch, along with the equations of the PMOS transistors presented in Equation 43 and Equation 44, and using the method in [25].

A theoretical component was calculated as an initial point of the circuit. To evaluate these equations almost all the models were considered ideals.

$$g_{m_n} = \frac{2 * I_{SD_n}}{\left(V_{SG_n} - |V_T|\right)}$$ *Equation 43*

$$\left(\frac{W}{L}\right)_n = \frac{g_{m_n}}{K_p * \left(V_{SG_n} - |V_T|\right)}$$ *Equation 44*

Where n is the number of transistors analyzed, I_{SD_n} is the source-drain current in the transistor, V_{SG_n} is the voltage between source and gate terminals, K_p is defined as the transconductance coefficient. The W & L are the Width and Length of the transistor.

The analysis started from the output stage (2nd stage). As previously mentioned this analysis was an outline design to serve as a starting point for the optimization with the assigned tool, indicated in future chapters.

3.3.2.2 Offset Voltage

The offset voltage (V_{os}) in an amplifier has two components, the systematic and the mismatch offset. In the case of this OTA circuit, due to the relatively low gain per stage, the differential pair and the second stage play a primordial role.

Analyzing the systematic input offset voltage in the first stage of the amplifier, if the inputs of this stage are grounded, theoretically, the quiescent output voltage at the drain of active load transistors $(M0\ \&M1)$ must have the same voltage. However, these voltages aren't equal as they present an offset of a few hundreds of Nano-volts (nV). The cause for these small variations is the mismatch in the devices of the differential pair, and it is here where the second stage helps to reduce this offset.

The ratios of width and length (W/L) of the transistors in the active load and the one of second stage $(M2)$ should be selected to maintain the current density equal in these devices. In this circuit is given by, [26]

$$\frac{(W/L)_0}{(W/L)_2} = \frac{(W/L)_1}{(W/L)_2} = \left(\frac{1}{2}\right) * \frac{(W/L)_6}{(W/L)_7} \qquad \textit{Equation 45}$$

As for the mismatch input offset voltage, it is complicated to determine those variations with simple equations, and due to this a Monte Carlo analysis is used to measure the offset, where 3σ is used as the measure.

In 1998, the Pelgrom model was proposed in [27], which establish an estimative for transistor mismatch states. This set up that the mismatch between a pair of MOS transistors is occasioned by the difference in their threshold voltages (ΔVT), and can be described by its standard deviation, expressed in Equation 46.

$$\sigma \Delta VT = \frac{A_{VT}}{\sqrt{WL}} \qquad \textit{Equation 46}$$

The A_{VT} is a parameter given by the foundry (Atmel), which in this case is $7.5\ \mu m.mV$ for PMOS.

Assuming, the V_{os} in terminals of the differential pair is independent one to another for random variations, the offset voltage can be predicted by

$$\sigma V_{os} = \sqrt{{V_{os,p}}^2} \qquad \textit{Equation 47}$$

Using Equation 46 & Equation 47, it can be determined an approximation of the mismatch offset.

3.3.3 Current Mirror

There are several currents mirrors in the whole BGV, but the main current mirror is the one integrated by M1, M2 and M3, which are PMOS transistors in Figure 19. These transistors act as current sources to the BJTs and copying the current to the output resistance (R_3), which convert the current to voltage reference.

If the output current (I_3) is not identical to I_1 & I_2, it will result as an error in the compensation of temperature, due to a non-ideal current mirror.

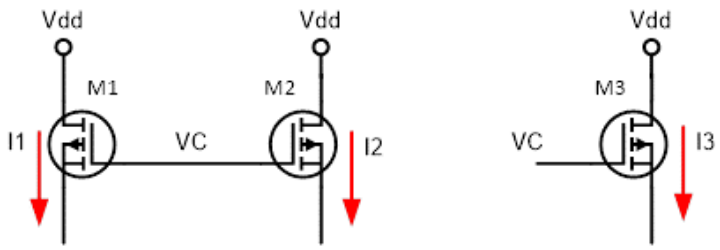


Figure 19 - Upper Current Mirror.

In this case simple current mirror is implemented. If all the transistors work in saturation mode, their V_{SG} are equal and the channel length modulation effect is neglected, this assure an accurate copy of the current. [6]

3.3.3.1 Current Mirror Mismatch

The current mismatch is a problem that affects the whole bandgap circuit; the unmatched current of the principal branches (I_1 & I_2) generates an unbalance voltage on the inputs of the OTA circuit. This mismatch in the current mirror could be caused by a channel length modulation problem, and as for the variations in the technology used, it is also important to emphasize that the gate to source voltage (V_{SG}) must be as equal as possible, and that the transistor works on the saturation region.

The mismatch in the current mirror can be improved by using a cascode current source which increase the output impedance. Figure 20, shows the implementation of this cascade current source. The insertion of another level in the circuit increases the power consumption in the whole circuit.

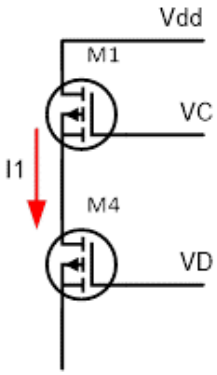


Figure 20 - Cascode representation.

In Figure 20, a simple cascode is implemented, where the transistor M_4 regulates the drain voltages of M_1, the gain of M_4 determines the quality in the regulation of M_1. Considering the constants, the voltages in the terminals of M_1 and M_4, the output impedance of the cascode current mirror is given by

$$R_{Cascode} = \left(1 + gm_4 R_{SD_1}\right) R_{SD_4} + R_{SD_1} \quad \textit{Equation 48}$$

Supposing $R_{SD_1}\ and\ R_{SD_4} \gg 1$, the Equation 49 approximates the impedance.

$$R_{Cascode} = gm_4 R_{SD_1} R_{SD_4} \quad \textit{Equation 49}$$

This improves the output resistance by factor of the transistor M_4, as clearly seen.

3.3.4 Bias Circuit

A self-bias circuit is implemented for biasing current into the OTA block, and also for generating a polarization voltage for the cascode stage in the current mirror of the BGV. In Figure 21 the architecture used to implement this circuit is illustrated, where the transistor M_2 is four times bigger than M_1.

For the core of the self-bias circuit, the relationship of the current of the branch are given by

$$I_{M1} = \beta (V_{GS} - V_t)^2 \quad \textit{Equation 50}$$

$$I_{M2} = 4 * \beta (V_{GS} - V_t)^2 \quad \textit{Equation 51}$$

The current mirror created by transistors $M_3, M_4\ and\ M_5$ conducts a current through a cascode stage formed by $M_6, M_7, M_8\ and\ M_9$, which gives the output current.

Due to the top mirror the relation current through the transistors is equal, which also pass through a resistor.

$$I_{M1} = I_{M2} = I \quad \textit{Equation 52}$$

$$V_{GS1} = V_{GS2} = R * I \quad \textit{Equation 53}$$

The resistance value is obtained by substituting terms between those equations and using the general formula for the transconductance, given by

$$g_{m1} = \left(\frac{2 * I}{V_{GS1} - V_t}\right) \quad \textit{Equation 54}$$

The ratio between the M_4 and M_5 is 2:1 to reduce the current and also to reduce the consumption, this is according to the specifications.

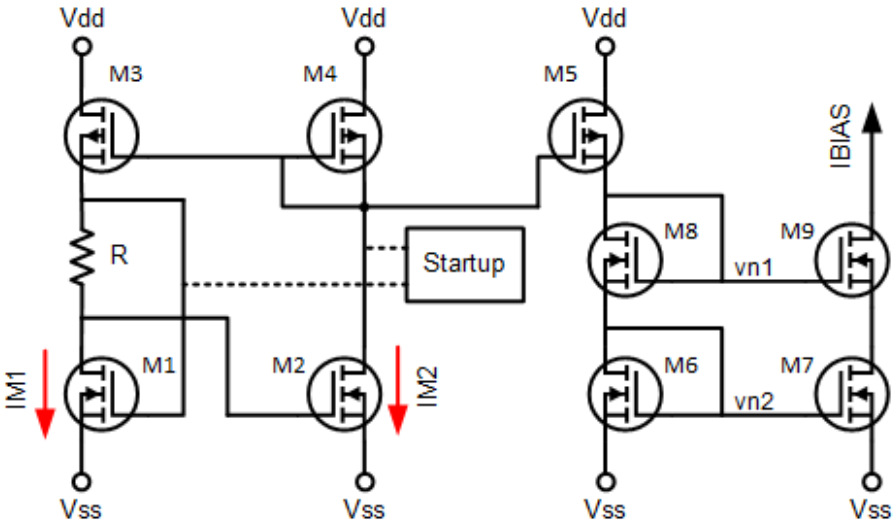


Figure 21 - Self-Bias Circuit schematic.

There is another stage of the bias that is formed by two mirror transistors of the cascode previously mentioned and there is also a configuration which supplies the voltage gate for the second stage in the cascode of the bandgap reference. Figure 22 illustrates the configuration to generate the polarization voltage for the second stage of cascode.

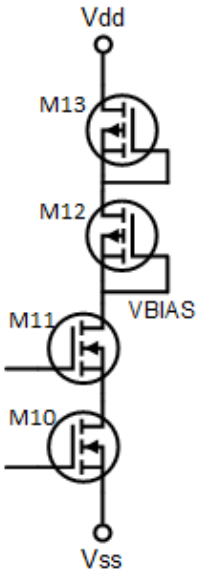


Figure 22 - Configuration of VBIAS (polarization for cascode).

3.3.5 Start-up Circuit

A startup circuit is a section of BGV that "Starts-Up" the circuit keeping out the undesired operation points, and once it reaches the desire operation point it doesn't interference with the operation of the circuit.

The difference voltage at the terminals of R_0 (ΔV_{EB}), due to the variation upon the currents flows through the devices in the BGV. Won't be characterized by the linearity of I-V relationship between the BJT and the resistor causing two operating points.

The current mirror will drive the current reaching the stable operation when the inputs of the OTA circuit are equal $(V_A = V_B)$, in other words, when the voltage at the R_0 terminals is equal to ΔV_{EB}.

Thus, the expression to represent the linear behavior of the current through R_0 with respect of ΔVR_0 is given by Equation 55. Taking into account the current mismatch between the two branches of the current mirror as a constant (δ), the initial conditions equal to zero, and the emitter area of the BJTs, yields the Equation 56. As explained in [6].

$$I_{R_0} = \frac{\Delta VR_0}{R_0} \qquad \textit{Equation 55}$$

$$I_{\Delta V_{EB}} = -\delta \left[\frac{A_{E_0} + A_{E_1} e^{(\Delta V_{EB}/V_T)}}{A_{E_0} - A_{E_1} e^{(\Delta V_{EB}/V_T)}}\right] \qquad \textit{Equation 56}$$

One of the reasons considered in the selection of this architecture is the addition of two parallel resistors $(R_1 \; and \; R_2)$ to make the relationship I-V more linear, but this causes that turning on the BJTs $(Q_0 \; and \; Q_1)$ requires a great amount of current flowing through these resistors [10].

Hence, in order to achieve a desired operating point a startup circuit which will fulfill the requirements must be implemented. There are a couple of methods to implement this section, which are injecting or extracting current, upsetting the equilibrium of the circuit forcing the OTA circuit to restore the equilibrium and generating a reference. This reference will turn the startup circuit off and isolate the startup circuit from the bandgap core.

It is important to consider that even when the startup circuit can be detached from the bandgap core during the equilibrium (as desired), and not be affected in the dynamic or static performance of the BGV after power up, the performance of this stage directly affects the setting time of the BGV.

In this project the startup circuit is based on the method of injecting current to initiate the circuit. The architecture is illustrated in Figure 23 where an active biased current mirror formed by $MS_4 \; and \; MS_5$, the

gate of these transistors is connected to the main current mirror as it seem on Figure 31. Along with two logical inverters formed by a couple of NMOS $(MS_0 - MS_2)$ and PMOS $(MS_1 - MS_3)$ transistors, and a pull-down resistor (RS_0).

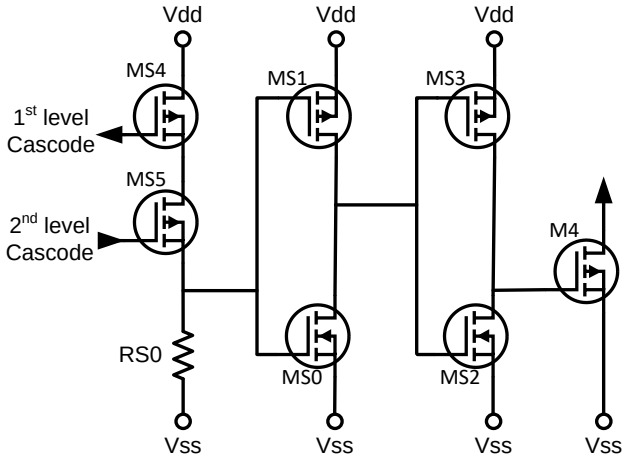


Figure 23 - Startup Circuit schematic.

When the circuit starts, the pull-down resistor (RS_0) is at low level, the logical output of the second inverter is zero (grounded), due to this the MS_5 injects a current into the mirror exciting the output in the OTA circuit. This forces the circuit to move from the relaxation condition (one of the operating points mentioned above), and makes the resistor RS_0 work converting the current into voltage, when there is enough voltage at the input of the first inverter the startup circuit will be shut down.

3.3.6 Second Order Compensation

The second order compensation principle explained in the previous chapter is implemented in the schematic, based on the knowledge that there are two crucial currents paths in the circuit which are the one passing through $Q_0 \; and \; Q_1$. These currents can be injected or extracted from those transistors at the respective nodes $(V + and \; V-)$, affecting the output voltage of the circuit.

The implementation of a second order compensation in the schematic is following the line proposed in [10]. This compensation is a BJT Subtracting Current Technique which adds a BJT current source with second order temperature dependency achieving the second order curvature correction. The BJT subtracting current technique was first discussed in [28].

Figure 24 illustrates the solution to correct the nonlinear term which is a combination between VPTAT (V_{EB}) and another V_{EB} with temperature-independent current, mirroring the current from the main current mirror $(M_1 \; and \; M_2)$ and injecting the current into a BJT (Q_2) with the same configuration as the other BJTs, and producing the V_{EB} needed to correct the nonlinearity. From Equation 15 it can be determined the Equation 57 and Equation 58 for each term, given by

$$V_{EB2} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) - \gamma\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \quad \textit{Equation 57}$$

$$V_{BE1,2} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) - (\gamma - 1)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \quad \textit{Equation 58}$$

Where the same conditions as in Equation 14 apply. The difference from these terms refers to the nonlinear term, as indicated in Equation 59.

$$V_{NL} \cong V_{EB2} - V_{BE1,2} = \frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \quad \textit{Equation 59}$$

A couple of resistors $(R_4\ and\ R_5)$ with the same value are implemented to subtract the proportional current of the nonlinear term. Those resistors will drain the current from the main mirror the proportional current (I_{NL}), thus leading to [10]

$$V_{REF} = V_T\left(\frac{R_3\ln(N)}{R_0}\right) + V_{EB}\left(\frac{R_3}{R_1}\right) + V_{NL}\left(\frac{R_3}{R_{4,5}}\right) = \frac{R_3}{R_1}\left(\frac{R_1\ln(N)}{R_0}V_T + V_{EB} + \frac{R_1}{R_{4,5}}V_{NL}\right) \quad \textit{Equation 60}$$

The values of the compensation resistor are obtained by comparing Equation 58 and Equation 60, resulting in Equation 61.

$$R_{4,5} = \frac{R_1}{\gamma - 1} \quad \textit{Equation 61}$$

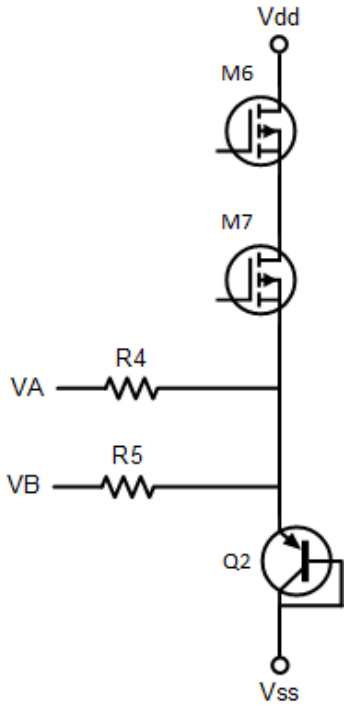


Figure 24 - Second Order Compensation schematic.

3.3.7 Output Stage

The output stage is a simple single-ended stage formed by a current mirror and a resistor (R_3), connected to an output filter. Illustrated in Figure 25.

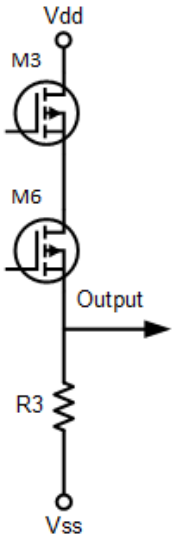
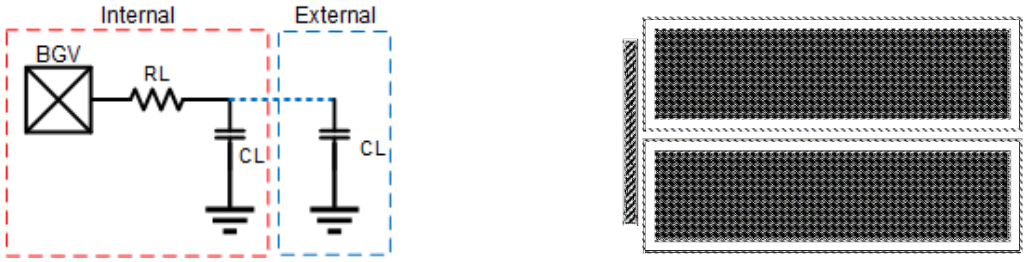


Figure 25 - Output Stage schematic.

3.3.8 Output Filter

The output filter was implemented with integrated components (resistor of 5 KΩ & capacitor of 50 pF), and a unique external component (ideal) which is a decoupling capacitor of 10 µF, being taken into account for simulations as illustrated in Figure 26.



a) b)

Figure 26 - Output Filter, a) schematic representation, b) layout representation.

3.3.9 Power Down Circuit

A Power down block, which is one of the specifications for this implementation, is a power down section that allows a very low power consumption when activated. This is a common practice in many analog circuits.

To reduce the power consumption when the circuit is disabled, the power down circuit is activated making the bandgap circuit to “turn-off”. This block is composed by several transistors that work as switches which closes isolating the circuit from the power supply.

The core circuit is basically two inverters connected in series and with a respective capacitor at its output; working at a high logical level the inverters pass the signal, resulting in two different logical levels $(0 \ \& \ 1)$. These logical levels will supply gate voltages for different transistors strategically located in every stage of the BGV forcing its function as switches and isolating the consumption, grounding or biasing with V_{DD}, the circuits in every block.

Those transistors have a small sizing value because they are just as indispensable to work as switches. Illustrated in Figure 27 is the core of the power down circuit, presenting two inverters that provide both voltage levels to shut down the circuit.

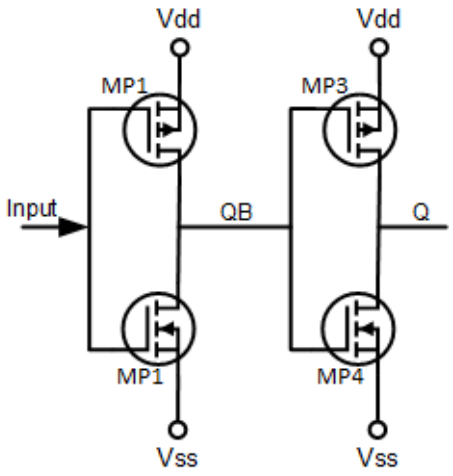


Figure 27 - Core Power Down Circuit schematic.

3.4 BGV Circuit

The Bandgap Voltage Reference circuit, as previously demonstrated, is integrated by several sub-circuits, allowing it to work properly. Having in mind that the equilibrium state is achieved with the help of the startup circuit as mentioned before, and to demonstrate the operation, the circuit is analyzed.

When the circuit is in the stable state, the currents passing through the main current mirror formed by $M_0, M_1 \ and \ M_2$ are identical to each other allowing to have one of the most important conditions to extract the temperature dependency of the circuit $(I_0 = I_1 = I_3 = I)$.

The voltages at the input of the OTA will be equal to the voltage produced by the voltage sources. The PNP transistors are connected as diodes with a ratio of 1: N to provide the required temperature dependent voltages. Following the principle of 3.3.1 and the Figure 31 these voltages are given by

$$V- = V_{EB0} \quad \textit{Equation 62}$$

$$V+ = I * R_0 + V_{EB1} \quad \textit{Equation 63}$$

Due to the high impedance at the input of the OTA circuit clamps the voltage at the same level, resulting in

$$V- = V+ = V_{EB0} = I * R_0 + V_{EB1} \quad \textit{Equation 64}$$

$$V_{EB0} - V_{EB1} = I * R_0 \quad \textit{Equation 65}$$

$$\Delta V_{EB} = V_T \ln(N) = I * R_0 \quad \textit{Equation 66}$$

Equation 66, was previously demonstrated in Equation 33. Therefore, the current in $R_1 \, and \, R_2$ is proportional to V_{EB}, and the current I flowing through R_0 is a PTAT and is given by

$$I = \frac{V_T \ln(N)}{R_0} + \frac{V_{EB}}{R_1} \quad \textit{Equation 67}$$

Once more following the Figure 31, the output voltage is given by

$$V_{REF} = V_{OUT} = I * R_3 = V_T \left[\frac{R_3 \ln(N)}{R_0}\right] + V_{EB}\left(\frac{R_3}{R_1}\right) = \frac{R_3}{R_1}\left[\frac{R_1 \ln(N)}{R_0} V_T + V_{EB}\right] \quad \textit{Equation 68}$$

The equation above is true if the components were ideal and the voltage offset is neglected.

By making a comparison between Equation 68 and Equation 5, we realize that the circuit is a first order compensated BGV where the compensation is ensured by the values of N and R_0/R_1 ratio.

$$K = \frac{R_1 \ln(N)}{R_0} \quad \textit{Equation 69}$$

Inserting Equation 69 into Equation 5,

$$V_{REF} = V_{EB} + V_T * \frac{R_1 \ln(N)}{R_0} \quad \textit{Equation 70}$$

To achieve $TC = 0$, the resistor ratio is given by

$$\left.\frac{\partial V_{REF}}{\partial T}\right|_{T=25℃} = \frac{R_1 \ln(N)}{R_0} * \frac{\partial V_T}{\partial T} + \frac{\partial V_{EB}}{\partial T} = 0 \quad \textit{Equation 71}$$

Using Equation 71, and with $N = 8$ which is selected due to the area relation in the layout, a numerical example is presented to explain how the circuit was dimensioned before the optimization.

$$\frac{R_1 \ln(8)}{R_0} * 86.25 - 1.56 * 10^3 = 0 \qquad \textit{Equation 72}$$

$$\frac{R_1 \ln(8)}{R_0} = \frac{1.56 * 10^3}{86.25} \approx 18.086 \qquad \textit{Equation 73}$$

$$\frac{R_1}{R_0} \approx 8.7 \qquad \textit{Equation 74}$$

$$R_1 = 8.7 * R_0 \qquad \textit{Equation 75}$$

From Equation 67, and with the conventional considerations

$$I = \frac{0.0257025\ V \ln(8)}{R_0} + \frac{0.783888\ V}{8.7 * R_0} \qquad \textit{Equation 76}$$

Solution for R_0,

$$R_0 \approx \frac{0.143315889}{I} \qquad \textit{Equation 77}$$

Assuming the minimum allowed current ($I = 10\ \mu A$)

$$R_0 \approx 14.3315\ K\Omega \qquad \textit{Equation 78}$$

Continuing with the analysis and knowing that the current through $R_1\ and\ R_2$ is the CTAT portion of the circuit, it can be expressed as

$$I_{CTAT} = I_{R1} = I_{R2} = \frac{V_{EB}}{L * R_0} \qquad \textit{Equation 79}$$

Where L is a compensation added to compensate the I-V relationship, that is given by

$$L = \frac{\frac{\partial V_{EB}}{\partial T}}{\frac{\partial V_T}{\partial T} * \ln(N)} \qquad \textit{Equation 80}$$

From the numerical example above, the relation between R_1 and R_0 is given by

$$R_1 = R_2 = L * R_0 \qquad \textit{Equation 81}$$

Finally, to obtain a particular reference voltage, Equation 82 is expressed in function of R_0, where R_3 is given by

$$R_3 = D * R_0 \qquad \textit{Equation 82}$$

Yields,

$$V_{REF} = V_{EB} * \frac{D}{L} + V_T * D * \ln(N) \qquad \textit{Equation 83}$$

Where D is the compensation needed to achieve the reference voltage required, given by

$$D = \frac{V_{REF}}{V_T * \ln(N) + \frac{V_{EB}}{L}} \qquad \textit{Equation 84}$$

3.5 Trimming – Resistor Network

Due to the process variations and mismatches in the manufacturing process, all components vary from their designed values. Particularly in this case those variations are translated as voltage variations in the reference output. To achieve the accuracy at the output a post-fabrication technique to adjust the circuit is implemented, called “trimming”. This is done with one time programming method through communication protocol.

This technique has a potential harmful point if it is improperly and integrated on the circuit; the effectiveness of the trimming network depends on its prefabrication design. An important aspect to consider in the implementation of this technique is the Temperature Coefficient (TC) of the error voltage causing the offset; the TC of the trim voltage must be equal to it.

The nonlinear compensation of components (second order) in collaboration with random offsets are usually discriminated compared with the linear errors [29], as expressed in Equation 59. Figure 28 illustrates the variations of temperature dependent components in the circuit. The variations in the PTAT voltage are the resistor mismatch and process variations on it.

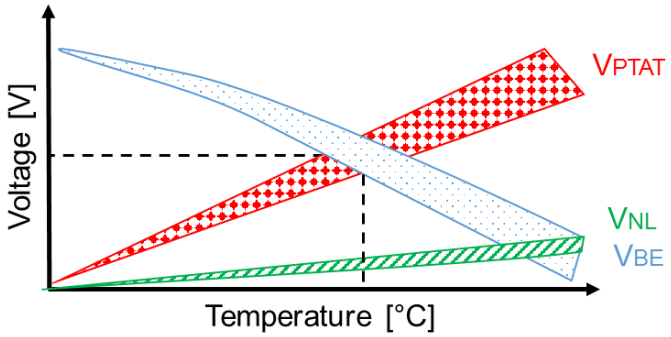


Figure 28 - Variations of temperature dependent components in the circuit.

Being more specific, a trimming is implemented in the current circuit in some of the resistors on the circuit to improve the accuracy of the output voltage. This resistor network is controlled by bits which are limited by specification, controlling the value of the resistor for particular cases as corners or special conditions. For a given number of bits (b), exists different input values as expressed in Equation 85.

$$2^b = M \qquad \textit{Equation 85}$$

In this case, there are two targets to treat, one is related to the variation in the temperature range and the other to the output voltage amplitude. From Figure 31, $R_0, R_4\ and\ R_5$ are implemented as a resistor network solving the target of temperature coefficient. Figure 29 represents the configuration used for these resistors.

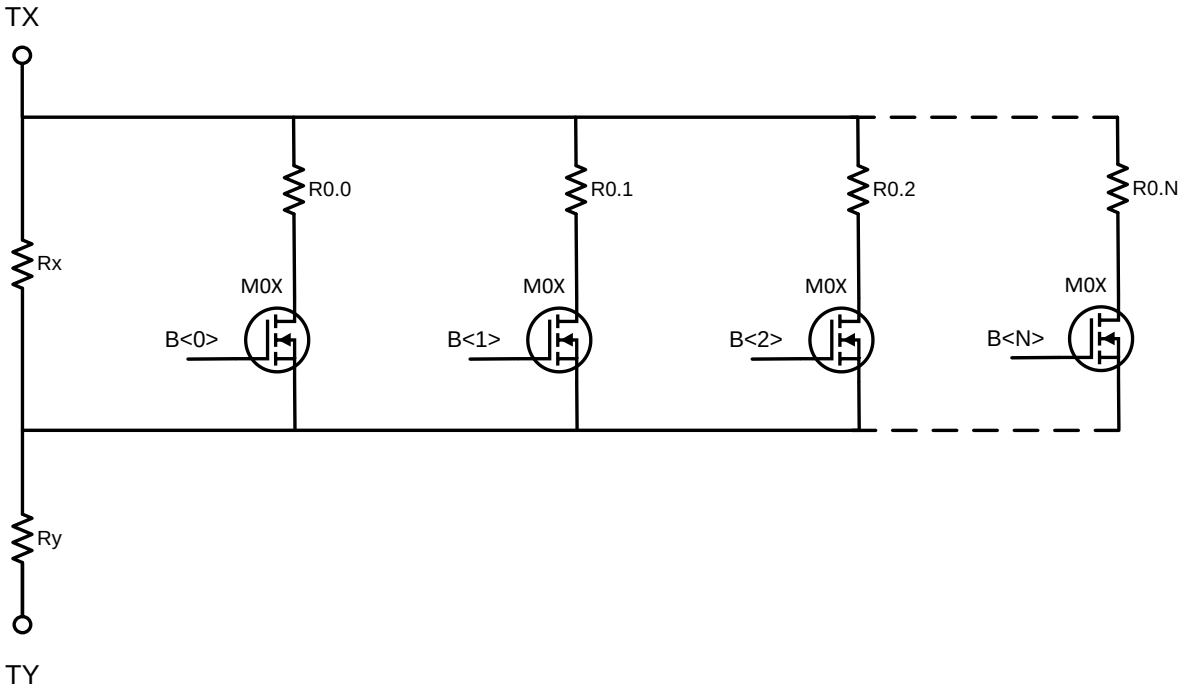


Figure 29 - Representation of trimming configuration in R0.

3.5.1 Resistor Values

To calculate the values of every resistor, a full simulation with all corners and variables is needed to obtain the values of the resistors in extreme cases, later on, these values will be achieved with trimming. For the whole range of temperature and corners the maximum and minimum values are taken into account.

From Figure 29, R_Y is the fixed value resistance which with series & parallel resistances rules will reach the maximum and minimum values and all the intermediate values. These equations are given by

$$R_{Max} = R_X + R_Y \qquad \textit{Equation 86}$$

$$R_{Min} = (R_X \parallel R_{0.0} \parallel R_{0.1} \parallel \cdots \parallel R_{0.N}) + R_Y \qquad \textit{Equation 87}$$

Another important aspect to be considered when these values are calculated are the transistors $(M_{00}, M_{01}, \ldots)$, which work as switches, due to the internal resistances that these components have and their property of increasing this resistance as temperature increases for the NMOS transistors.

Adding this consideration into Equation 87, will end as given in Equation 88.

$$R_{Min} = (R_X \parallel (R_{0.0} + R_{M00}) \parallel (R_{0.1} + R_{M01}) \parallel \cdots \parallel (R_{0.N} + R_{M0N})) + R_Y \qquad \textit{Equation 88}$$

Moreover, a third resistor network is proposed whose target is the amplitude in the output voltage is proposed as a possible solution to improve the offset voltage at the output of the circuit. Figure 30 illustrates the configuration used in this resistor.

V_{OUT} is given in Equation 89.

$$V_{OUT} = V_{REF}\left(1 + \frac{\Delta R}{\Sigma R}\right) \qquad \textit{Equation 89}$$

The V_{REF} is the reference voltage, ΔR is the value of each resistor, and ΣR is the sum of all resistors in the string. This trimming circuit will improve the accuracy of the output voltage in the BGV.

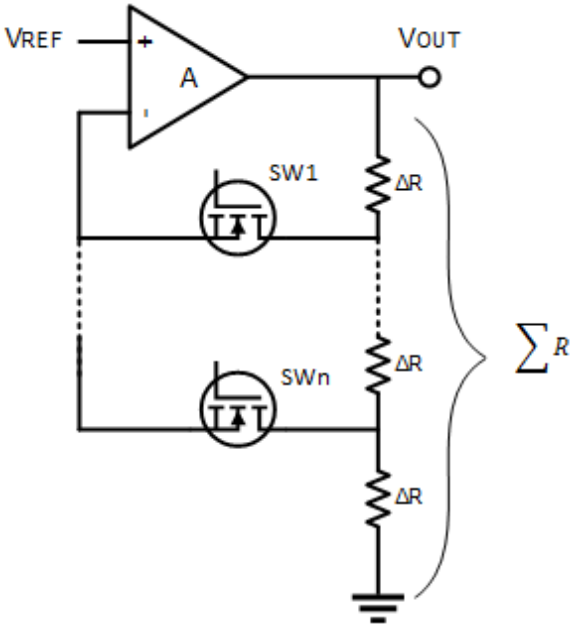


Figure 30 - Trimming network at the output of the BGV.

Having in mind the possible issue in the area and layout design occasioned by the size, and the number of resistors, as well as the transistors that work as switches for these resistor networks.

3.5.1 Number of Bits

The design of the resistor network range is determined by the desired accuracy with a tolerance consideration $(\pm\%\, accuracy)$ for the circuit. In other words, the number of bits used in the trimming is defined by the least significant bit (LSB) value required and also by the expected tolerance (FS). Following the algorithm proposed in [29], the number of bits is given by

$$\#Bits \geq \frac{\ln\left(\frac{FS}{LSB}+1\right)}{\ln(2)} \qquad \textit{Equation 90}$$

Where the LSB can be determined by

$$LSB \leq \frac{(\pm\%\, accurancy) * ref}{K_C} \qquad \textit{Equation 91}$$

The reference value is indicated by ref for the trimming network, for instance, if these values were in function of voltage, the value of reference will be the output voltage at the circuit. In Equation 91, K_C is a "comfort factor" which is defined by an engineering index that balances cost and performance. [29]

The expected tolerance is defined as

$$FS = LSB(2^{\#\, Bits} - 1) \qquad \textit{Equation 92}$$

One of the specifications given for this project is the number of bits. After analyzing the correction margin needed to compensate the TC for every corner, one more bit was added. In fact, the number of bits for this circuit is indeed careless due to the interface that is going to be used for the programming, which might be I^2C for one time programming.

For this project the number of bits is not a problem. Even when the specification points out a number, that number can be increased due to the type of interface which will be implemented for the bits. If consulted with the final user, this won't represent an issue.

3.6 Summary

The bandgap voltage reference circuit as indicated in this chapter is a complex circuit. Taking into account the number of analysis and calculation needed for the design in every block. Some considerations mentioned in this chapter were based on the first results of simulations in the block as feedback system to improve some aspects of the performance.

Based on the topology proposed in [10], and the topology proposed in [23], the circuit proposed in this work improves general aspects of the framework and performance. Using a new technology which is characterized in the design of circuits for radiation environment.

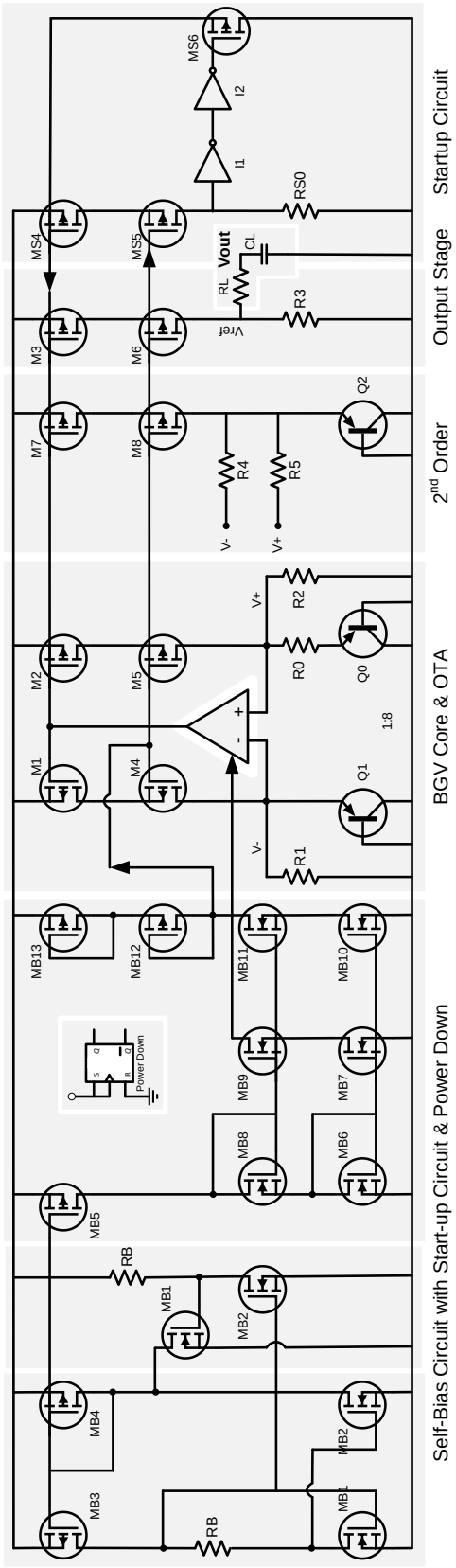


Figure 31 - Bandgap Voltage Reference schematic.

4 SIMULATIONS & RESULTS

The proposed project is composed by two stages, which are represented in workflows. The first stage is based on the design and validation of subcircuits, from the interface of Cadence to the test-benches. On the other hand, the second workflow is integrated by simulations and optimization using AIDA-C, including the post-optimization validation of the circuit.

4.1 First stage

The design of schematic circuits was performed with the graphical interface of Cadence, using an Atmel foundry which was chosen for this project. These designs were exported as a netlist to be validated before its simulation adding the expected measurements and calculations.

Figure 32 shows an example of a design in cadence, and if observed in the graphical environment of the tool is really helpful, as it facilitates the generation of test-bench with the interface.

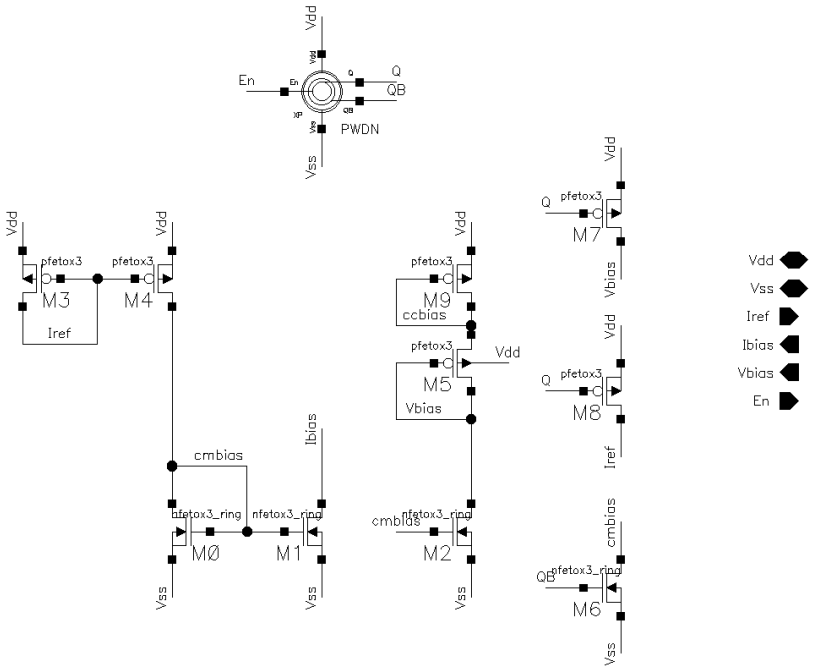


Figure 32 – Example of design in cadence.

The established workflow facilitates the execution of every step, taking into account possible issues and required time to design and optimize every block. The operational transconductance amplifier (OTA), was

the first block to be designed following the design criteria presented in previous chapter. Figure 33 shows the workflow of the 1st stage.

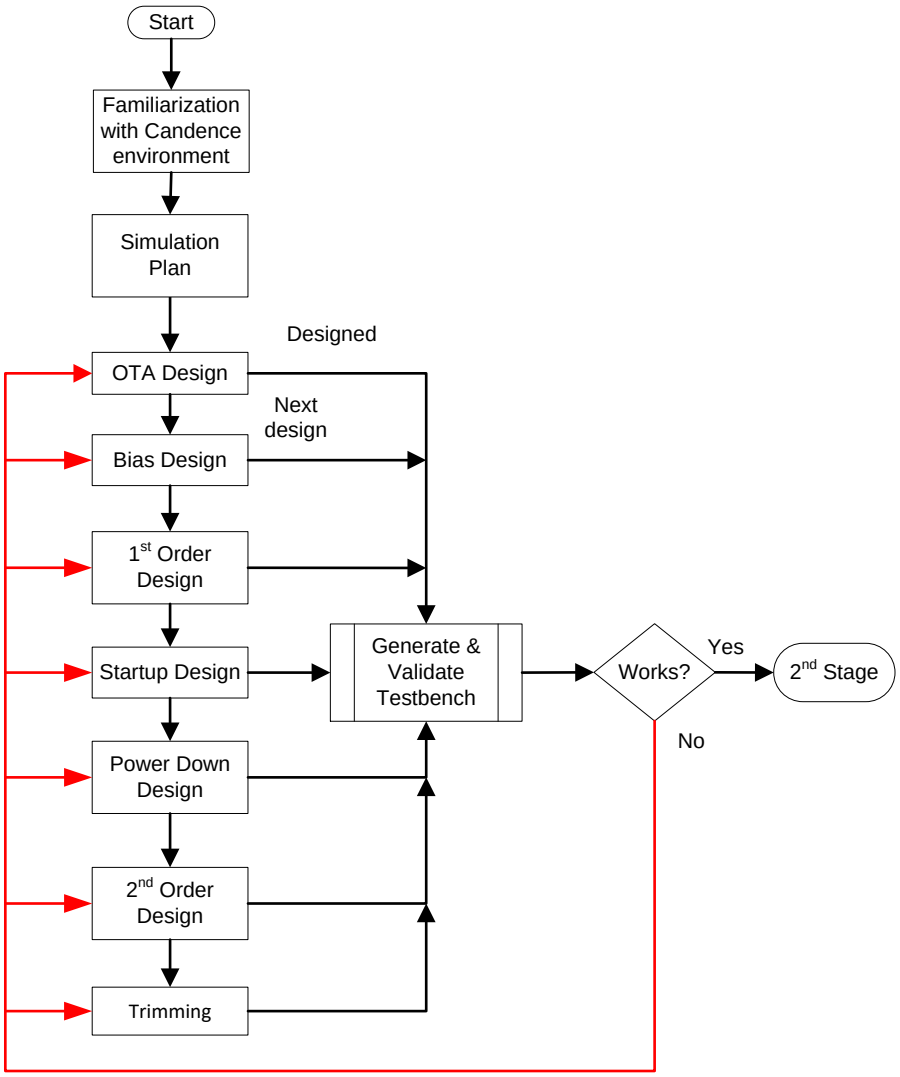


Figure 33 - 1st Stage workflow.

An operational transconductance amplifier is designed with a simple and popular topology, the Miller amplifier with two stages. This topology needs a current reference to be completed which in this case is a bias circuit; following this logic the next designed circuit was the bias circuit.

Different topologies for a bias circuit were considered from the simple ones with an external current source to the more complex topologies, e.g. self-bias circuits with different cascode and mirrors, which reduce the mismatch in the current sources.

The subsequent designed circuits were the core circuit and first order compensation of bandgap, which, as explained in the previous chapter, requires a start-up circuit to initiate. These circuits include the

corresponding transistors that integrate the power down block, facilitating its consecutive implementation in the circuit.

The bandgap circuit, as mentioned above, was initially designed for first order compensation, being successively modified to achieve the second order compensation with the use of cascode configuration for the current mirrors.

Finally, a trimming section was implemented to compensate the variations in the circuit. The design of this block considered the values needed to compensate those variations, reaching the maximum and minimum values on the resistor (core and second order resistors) in the respective section.

The upper circuit design performed to simulate the whole circuit as a single test-bench with the external sources for the power down and the supply voltage, as is shown in Figure 34.

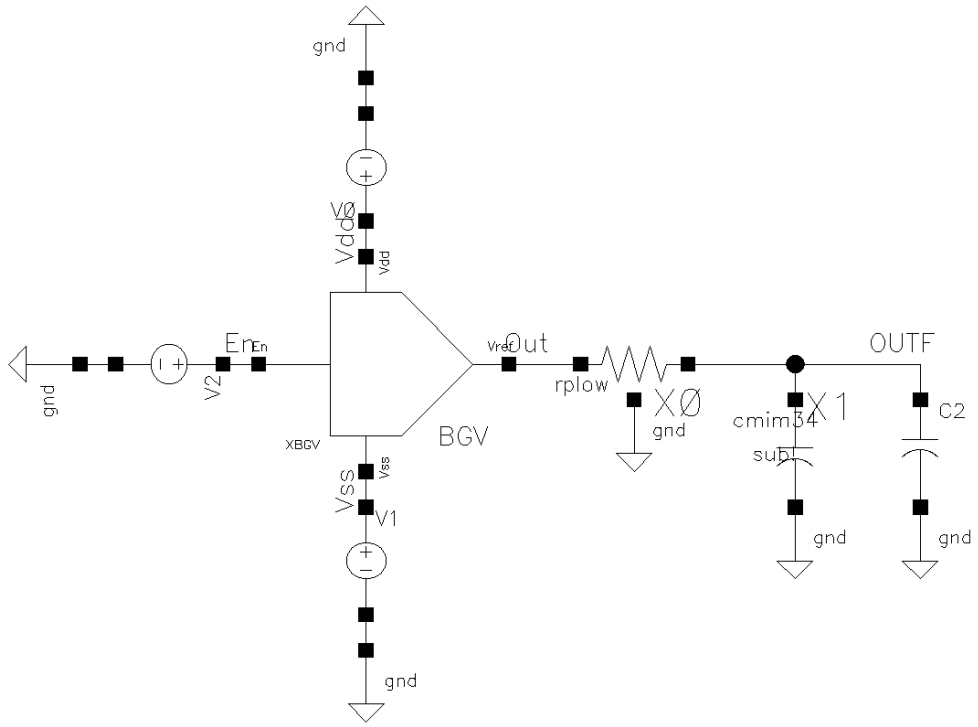


Figure 34 - Upper level design of BGV circuit.

4.2 Second Stage

The second stage initiates after the validation of test-bench for every block, being simulated with Mentor Eldo. With regard to the analysis (AC, DC, etc.), an individual file was generated to simplify the simulations.

According to the first stage order, starting with the operational transconductance amplifier, and finishing with the second order compensation with trimming sections. All the simulations were performed circuit by circuit several times to corroborate the results, and making small modifications looking for a better performance. Figure 35 represent a workflow for the second stage.

A key part in this project is the sizing of the transistors, resistors, and capacitors of the different blocks of the circuit. An “Analog Integrated Circuit Design Automation” (AIDA) software was used to optimize the sizing on the devices.

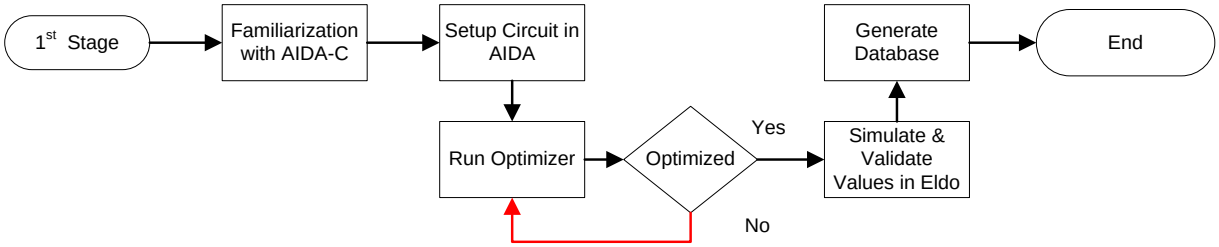


Figure 35 - 2nd Stage Workflow.

4.2.1 Optimization

AIDA-C, which is the part of the software for sizing the circuits as indicated in the section 1.2.1, obtains exceptional results in almost every block of the BGV, proving to be a good choice to optimize the sizing in analog circuits in the shortest period, if compared with other options on the market. This tool was provided by the ICG team with the purpose of achieving the objectives and corroborating it, effectiveness.

The interface of AIDA is quite intuitive as the framework implements an analog IC flowing at circuit level, focusing on design optimization and having highly efficient searching methods combined with an accurate circuit level simulation. [2] The overview of AIDA is illustrated in Figure 36.

The setup of the test-bench is through an interface of the AIDA software where it is necessary to create a *“.XML”* file, in which the parameters are introduced as well as the constraints desired to accomplish in the simulations of the circuit.

This tool also allows to modify the constraints, relaxing or adjusting the requirements to obtain a better circuit performance; improving the response time to find a positive solution.

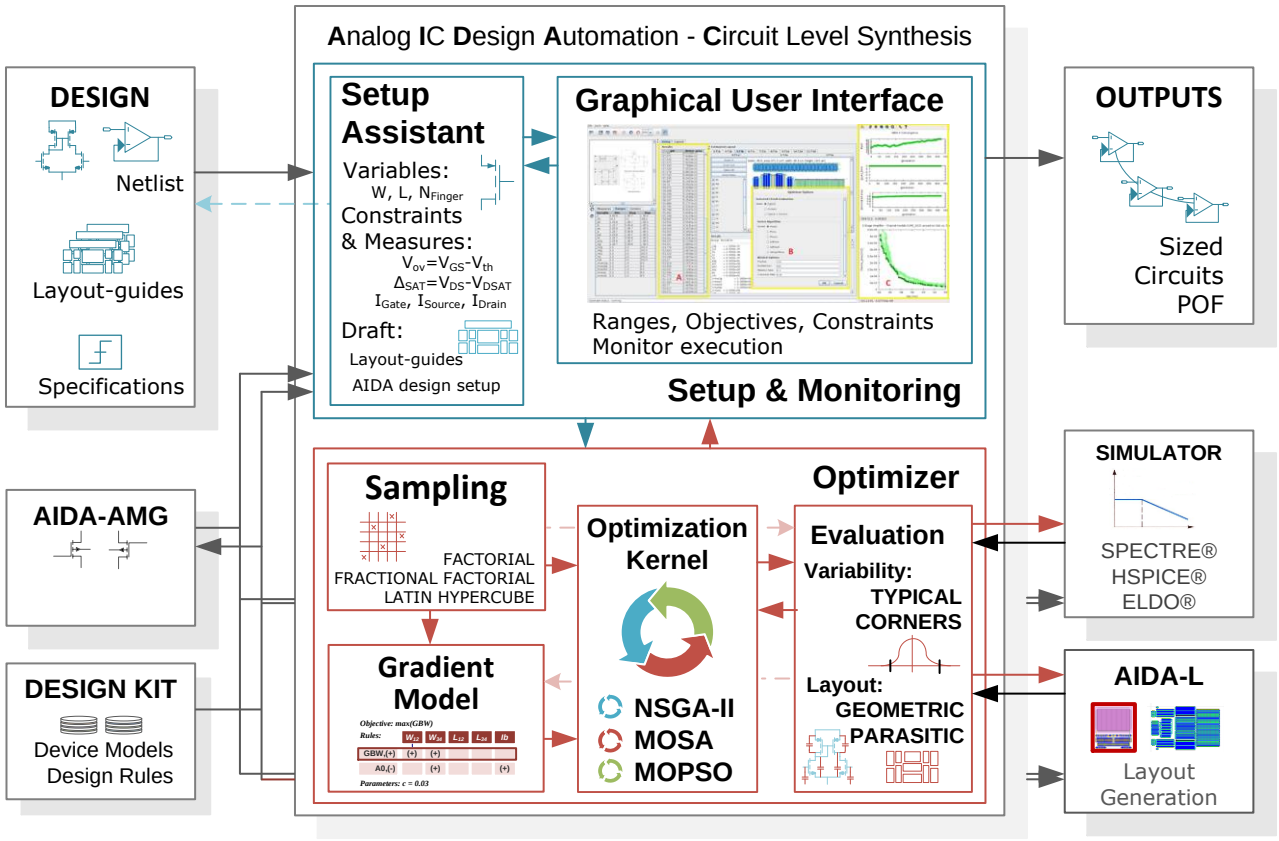


Figure 36 - AIDA Overview. [2]

4.3 Analyses

The analyses made to evaluate the circuits, can be classified into three different types, which are AC, DC and Transient analyses. For every block of the circuit specific measurements were extracted from the simulations.

4.3.1 AC Analysis

The AC analysis used to evaluate the power supply rejection ratio (PSRR), defined in chapter 2, was performed considering an AC voltage source in the main supply voltage and measuring the output of the circuit at the frequencies of 1 Hz and 1 MHz.

4.3.2 DC Analysis

In the case of the DC analysis, the DC operating point with a sweep of military temperature from −55 ℃ to 125 ℃ was evaluated for every block of the simulated circuit. The measures requested in the simulations are:

- Current Consumption.
- Output Voltage.
- Offset Voltage at $25\ ℃$.
- Thermal Coefficient.
- Minimum Current per branch.

Additionally, a particular simulation to verify the unique operating point of the circuit was effectuated. In order to corroborate the loop between the output voltage of the amplifier and the input of the startup circuit, the loop is opened inserting a voltage source which executed a sweep from 0 to 3.3 V. This not only shows the unique operating point of the circuit, but it also helps to identify whether the startup circuit has an influence on the circuit after start-up.

4.3.3 Transient Analysis

The transient analysis is basically used to simulate the power down mode, and the stability of the whole circuit, along with a particular case to determine the start-up of the circuit.

4.3.4 Monte Carlo Analysis

The Monte Carlo simulations were used to obtain the values from every measurement evaluated on the previous analysis. Using 1000 iterations for every case, with mismatch and process conditions, due to the available time for the simulations.

4.4 Simulation Conditions

The simulation conditions are highly influenced by the specifications were the range of temperature, the supply voltage, the current consumption per branch, and the models of devices are important considering the impact on the results.

When those parameters vary from the typical conditions for the specified limits, where all the possible combinations are presented, these situations are called process corners. For the technology and also for the foundry (Atmel 150 nm) used in this project, there are 32 corners and 1 typical condition, where all the combinations of parameters previously mention will take part in the simulations.

4.4.1 Process Variation and Typical Design

The typical condition in the process design is a null consideration of the variation in parameters which belongs to the process. A graphic representation of the process variation is illustrated in Figure 37, where the performance parameter (θ) of the typical condition shifts due to the variation of process parameter (Γ).

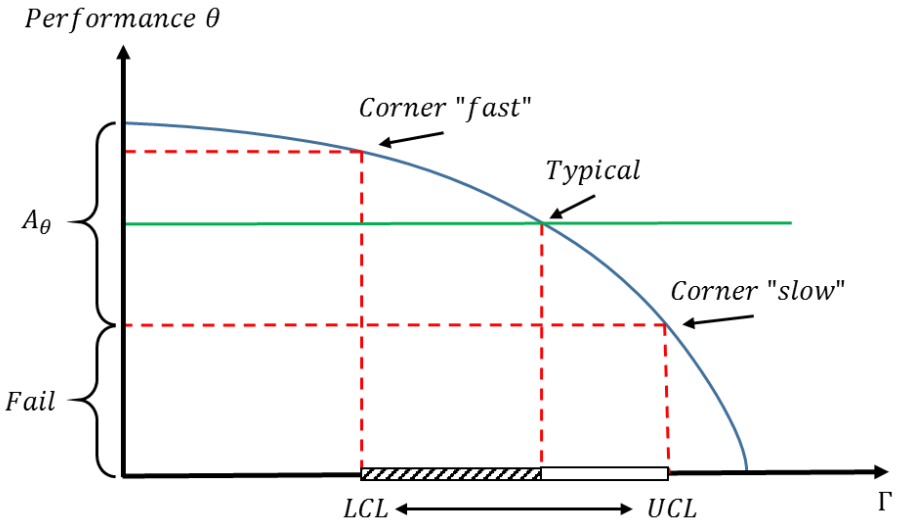


Figure 37 - Graph of parameter performance against process corner variation. [6]

In the Figure 37, A_θ is the acceptable circuit performance range for θ, in a specific requirement. This requirement is defined between the Lower Control Limit (LCL) and the Upper Control Limit (ULC), also known as 3σ. [6]

Table 8 - Corners applied in the project with MOS technology.

Best Case				Slow to Fast			
#	RC	Temp	VDD	#	RC	Temp	VDD
1	RC Low	-55	Low	17	RC Low	-55	Low
2	RC Low	-55	High	18	RC Low	-55	High
3	RC Low	125	Low	19	RC Low	125	Low
4	RC Low	125	High	20	RC Low	125	High
5	RC High	-55	Low	21	RC High	-55	Low
6	RC High	-55	High	22	RC High	-55	High
7	RC High	125	Low	23	RC High	125	Low
8	RC High	125	High	24	RC High	125	High

Worst Case				Fast to Slow			
#	RC	Temp	VDD	#	RC	Temp	VDD
9	RC Low	-55	Low	25	RC Low	-55	Low
10	RC Low	-55	High	26	RC Low	-55	High
11	RC Low	125	Low	27	RC Low	125	Low
12	RC Low	125	High	28	RC Low	125	High
13	RC High	-55	Low	29	RC High	-55	Low
14	RC High	-55	High	30	RC High	-55	High
15	RC High	125	Low	31	RC High	125	Low
16	RC High	125	High	32	RC High	125	High

Taking into consideration that not only the parameter process variation affects the BGV, but also the local variations mostly integrated by mismatch.

As mentioned above, the combinations for the process variations are called “corners”, because they represent the limits of the process just like the word itself suggests. In this project, the corners used to simulate all the stages of the circuit during its design are shown in Table 8, where they are integrated in groups of 8, representing “Best Case”, “Worst Case”, “Slow to Fast” and “Fast to Slow” process.

4.5 Operational Transconductance Amplifier Simulations

The operational amplifier is a keystone on the development of this project, due to its importance and the time it takes to optimize this block. Simulations were carried out for the AC, DC and transient analysis to determine the best performance with different measures.

The principal measures taken into account for these analysis are:

- Current Consumption
- Power Supply Rejection Ratio
- Gain DC
- Gain Bandwidth
- Phase Margin
- Voltage Offset
- Noise Output
- Slew Rate

Using the basic rules for the design of this circuit the active load section, the differential pair, and the transistors biasing were optimized with the same length (L), width (W) and the multiplicity (M) to avoid as much as possible the mismatch between them.

The project was setup in AIDA-C with the objectives of having the maximum power supply rejection ratio and minimizing the voltage offset which are the main parameters that affect the performance of the OTA for this particular application.

The sizing obtained during the optimization for those parameters is shown in Table 9. All of these values are the ones calculated by AIDA-C, and chosen for this project due to their good performance in the measurements.

The performance obtained with this sizing is shown in Table 10 and Table 11, a decisive conclusion for the selection of values was not made by only taking into account the simulations and optimization of the close-loop circuit with and ideal current source as bias, but also by considering the performances obtained from

the combination of the Self-Bias Circuit and the Operational Transconductance Amplifiers, as mentioned in section 4.7.

Table 9 - Sizing of OTA.

Transistors	Width [µm]	Length [µm]	Multiplicity
Active Load	3.53	2.71	5
Bias Source	12.07	3.17	2/4/7
Differential Pair	5.74	2.66	7
2nd Stage	3.58	2.03	14
Capacitor	50	39	1

Taking the extreme condition for the bias generator as is explained in section 4.6, simulations were made with those values (with an ideal source), and also with the extreme conditions of the verticals PNP with the relation presented in Figure 13. The results of these simulations are presented in Table 10 & Table 11. The constraints considered was a general performance for an OTA circuit.

Even when the parameter of area of devices is not a constraint for this particular circuit, the estimated is around $6394.3\ \mu m^2$ without connections.

Table 10 - Simulation results of OTA close loop circuit, header in green typical performance.

		IDD [µA]		PSRR [dB]		PSRR [dB] @1 MHz		GDC [dB]		GBW [MHz]	
Ibias [µA]	**VCM**	Best	Worst	Best	Worst	Best	Worst	Best	Worst	Best	Worst
17.983	0.6	117.73	117.97	133.31	123.31	75.493	65.428	97.75	95.414	10.11	5.03
	0.783	117.62	117.88	131.29	121.53	75.294	65.298	98.697	96.785	10.15	5.04
	1	117.48	117.77	128.6	118.58	75.021	65.103	99.275	97.524	10.19	5.05
20.84	0.6	136.38	136.38	132.69	121.99	76.863	66.737	97.312	94.615	10.89	5.41
	0.783	136.26	136.56	129.32	119.6	76.663	66.604	98.348	96.123	10.93	5.42
	1	136.1	136.43	126.61	116.56	76.394	66.37	98.977	96.93	10.98	5.44
26.18	0.6	171.22	171.58	132	119.04	78.886	68.662	96.53	93.102	12.19	6.04
	0.783	171.07	171.45	126.33	116.46	78.685	68.506	97.726	94.981	12.24	6.05
	1	170.88	171.29	123.57	113.19	78.427	68.224	98.446	95.912	12.29	6.07
Constraints		≤ 300		≥ 60		≥ 60		≥ 70		≥ 0.1	

Ibias	VCM	IDD [µA]	PSRR [dB]	PSRR [dB] @1 MHz	GDC [dB]	GBW [MHz]
20.84	0.783	136.38	123.24	71.238	97.62	7.5067

Table 11 - Simulation results of OTA close loop circuit, header in green typical performance.

		PM [°]		Voff [µV]		NO [µV]		SR [MV/s]	
Ibias [µA]	**VCM**	Best	Worst	Best	Worst	Best	Worst	Best	Worst
17.983	0.6	69.995	60.114	1.7309	9.922	92.116	139.59	12.692	9.816
	0.783	69.965	60.044	3.74004	7.8142	92.108	139.66	12.664	9.7794
	1	69.938	60	4.43358	6.6527	92.115	139.76	12.653	9.7559
20.84	0.6	70.277	60.322	3.33282	9.4723	92.305	139.2	14.649	11.371
	0.783	70.246	60.249	5.45489	7.1331	92.298	139.27	14.762	11.331
	1	70.22	60.182	3.73181	9.3489	92.306	139.36	14.663	11.303
26.18	0.6	70.663	60.595	6.41816	8.6078	92.534	138.86	18.723	13.913
	0.783	70.631	60.514	4.95172	10.63	92.523	138.93	18.751	14.208
	1	70.604	60.446	2.4763	12.905	92.529	139.02	18.422	14.196
Constraints		[60 - 90]		≤ 100		≤ 150		≥ 0.5	

Ibias	**VCM**	**PM [°]**	**Voff [µV]**	**NO [µV]**	**SR [MV/s]**
20.84	0.783	66.114	0.37082	113.01	12.795

4.6 Self-Bias Circuit Simulations

The self-bias circuit, as mentioned before, provides the reference current for the OTA and also a voltage gate to polarize the second cascode transistor in the BGV. The sizing of this block was optimized to reduce the variation of the output current (reference current) in all of the corners trying to be as close as $20\ \mu A$ in every condition. The reference current for different corners is illustrated in Figure 38.

For the case of the polarization voltage for the cascode, it was optimized afterwards, when the BGV circuit was set up. Another objective of this optimization was to reduce the current consumption of the block, unfortunately the post optimization showed that the consumption is still high compared with other sections.

Also the size values for the transistors were chosen not only based on the stand-alone performance but with the OTA as an active load. This is represented in Table 12 which also shows the simulation results with an ideal load (stand-alone performance).

Table 12 - Simulation results of bias circuit with ideal load and with OTA circuit.

	Typical	**Max w/corners**	**Min w/corners**	**Peak to Peak**
IDD [µA]	244.47	287.92	215.37	72.55
IREF [µA]	20.899	26.18	18.03	8.15
IREF w/OTA [µA]	20.84	26.1004	17.983	8.1174

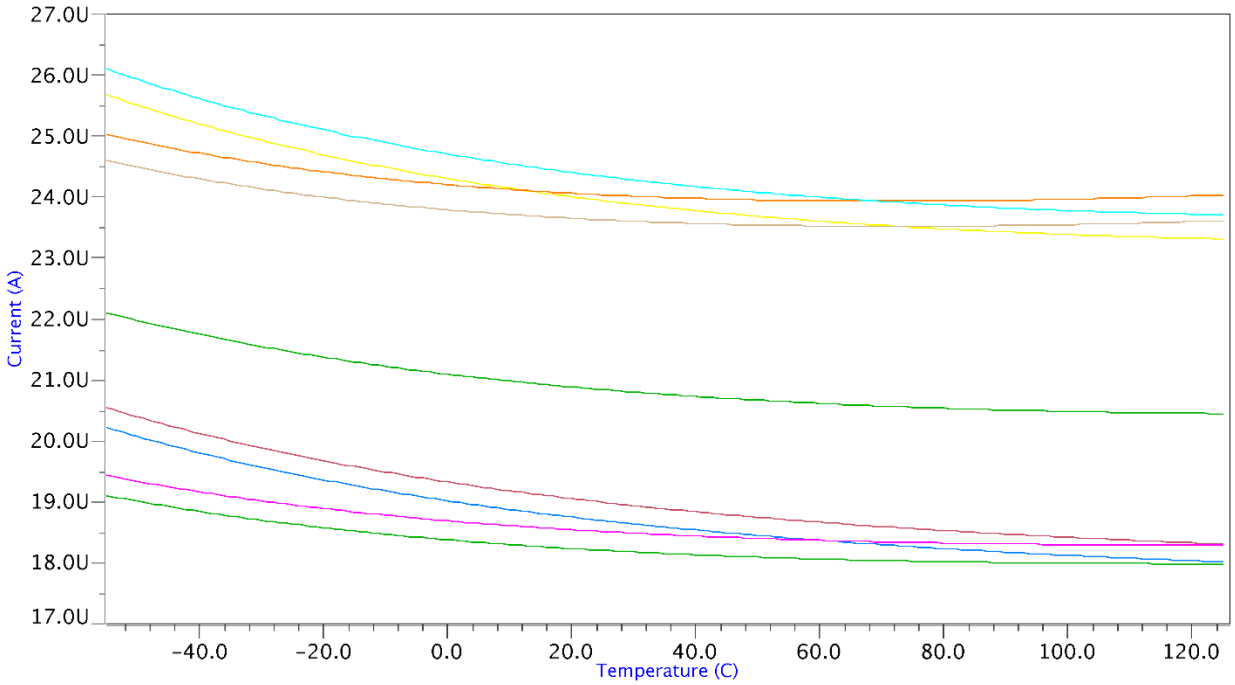


Figure 38 - Reference Current obtained for self-bias circuit for the 32 different corners.

4.7 SBC & OTA (BOTA) Simulations

The BOTA block is composed by the Bias and OTA circuits represented in Figure 39, those were simulated working together allowing to see the best performance of both circuits. The measurements considered for these simulations were the same for both circuits.

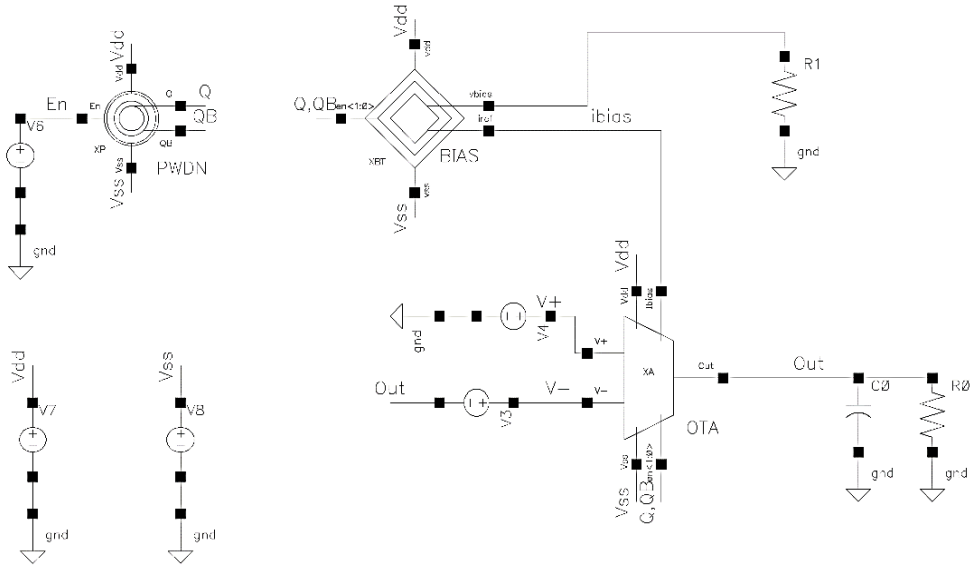


Figure 39 - Upper level schematic of S-B & OTA (BOTA) circuits from cadence.

The results are represented in Table 13. The decision about the sizing values was taken based on the performance of this combination.

Table 13 - Simulation results of S-B & OTA circuits.

	Typical	Best	Worst
IREF [µA]	20.84	17.9828	26.1004
IDD [µA]	372.9	331.08	448.4
IDD - Amp [µA]	136.38	117.77	170.7
IDD - BIAS [µA]	236.52	207.42	280.06
PSRR [dB]	109.61	117.05	102.8
GDC [dB]	97.62	99.157	93.741
GBW [MHz]	7.5068	12.152	5.0795
PM [°]	66.117	70.253	60.337
Voff [µV]	0.9624	0.96247	13.069
NO [µV]	120.74	97.089	150.17
SR [MV/s]	13.204	19.369	6.7918

4.8 1st Order Bandgap Voltage Reference Simulations

The implementation of the first order compensation bandgap voltage reference was made at the beginning with a simple current mirror; the core and the output stage were integrated for the different components previously characterized.

The simulation made for this architecture showed that the power supply rejection ratio (PSRR) was low. As a solution a cascode mirror for the current sources in the circuit was implemented, improving the PSRR.

Figure 40 represents the output voltage of the circuit obtained after improving the PSRR with the cascode in the power supply.

Table 14 shows the results from the simulation with the cascode mirror and with typical conditions.

Table 14 - Simulation results of 1st order BGV.

	Requirement	Typical
TC [ppm/° C]	≤ 20	11.717
VBG [V]	1.25 ± 0.4%	1.2497
Voff @25 °C [µV]	≤ 500	255.22
IDD [mA]	≤ 1	758.04
IR0 [µA]	≥ 10	10.062
PSRR @ 1 Hz [dB]	≥ 60	83.782
PSRR @ 1 MHz [dB]	≥ 60	126.9

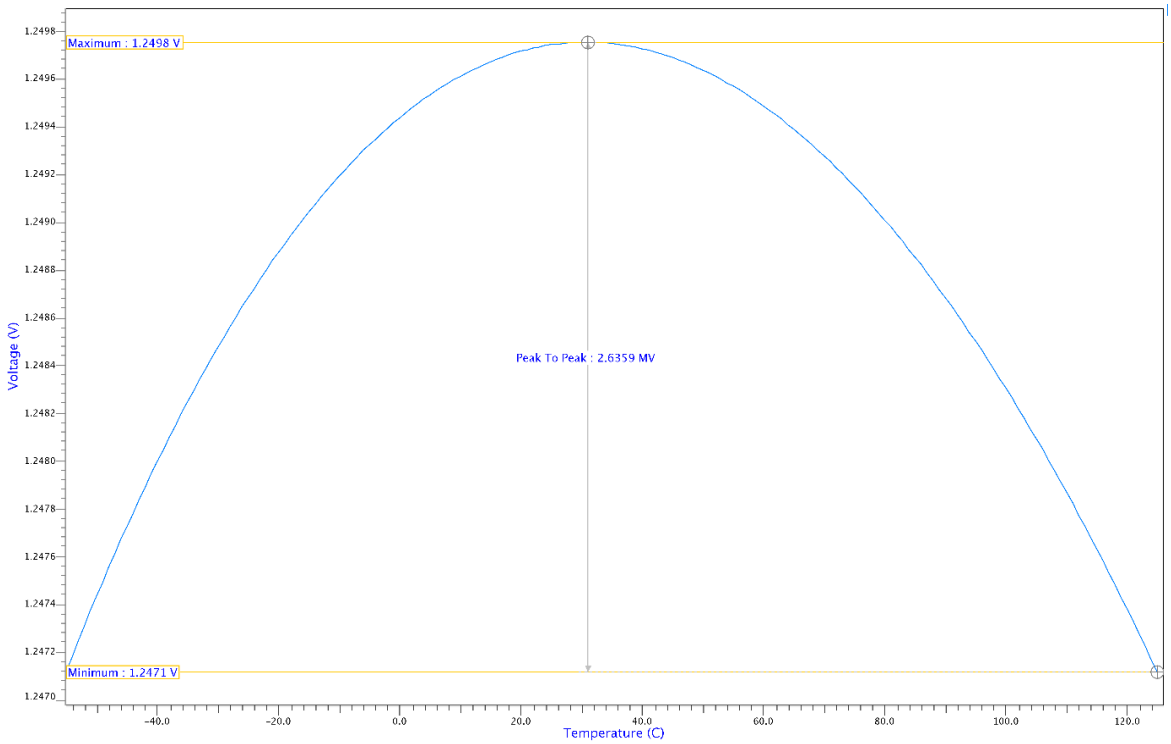


Figure 40 - Reference Voltage of 1st order BGV.

4.9 2nd Order Bandgap Voltage Reference Simulations

The implementation of the second order, follows the method mentioned in previous chapters. Also, the optimization for this circuit configuration was performed in AIDA-C, results presented in Table 15. A key point of this presented solution is the small TC obtained for the sizing presented on Table 16.

As a consideration for the TC measurement expressed in section 2.2.1, the temperature coefficient was not only evaluated for the whole waveform but was split into different sections to cover the temperature range. Figure 41 illustrates an example of this division.

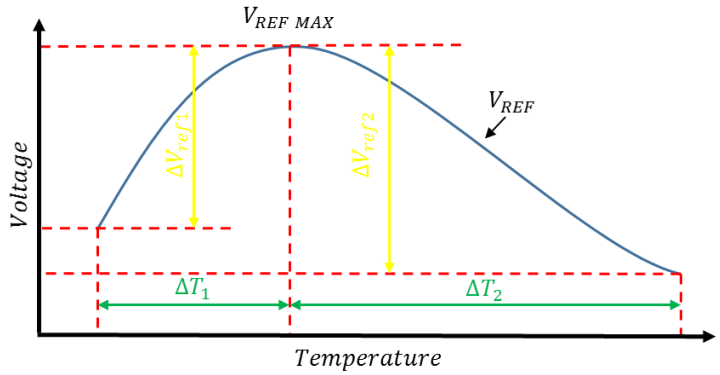


Figure 41 - Representation of split measurements for TC.

Applying, Equation 93 for each part to be measured for temperature range, given by

$$\Delta ppm_n = \frac{\Delta V_{refn}}{\Delta T_n * 10^6} \qquad \textit{Equation 93}$$

Where n is determined by the section to be measured. The purpose of this measurement is to help with analysis of the cubic function given by the curvature compensation. Figure 42 shows the reference voltage obtained with the second order compensation for typical conditions based on the sizing of Table 16.

Table 15 - Simulation results of 2nd order BGV.

	Requirement	Worst	Typical	Best
TC [ppm/° C]	≤ 20	34.164	0.13184	0.13184
VBG [V]	1.25 ± 0.4%	1.2392	1.25003	1.2633
Voff @25 °C [µV]	≤ 500	13300	25.496	25.496
IDD [µA]	≤ 1000	750.72	634.45965	548.96
IR0 [µA]	≥ 10	11.2339	13.27544	16.0785
PSRR @ 1 Hz [dB]	≥ 60	73.05	77.628	79.628
PSRR @ 1 MHz [dB]	≥ 60	121.34	121.8117	124.05

From the results presented in Table 14 is possible to realize that a few measurements for corners are off-specification. Different trimming networks were implemented in order to improve this. This improvement is presented in section 4.12.

Table 16 - Sizing of 2nd order BGV.

		Width [µm]	Length [µm]	Multiplicity
Transistor	Top level current mirror	2.59	4.95	8
	Bottom level current mirror	18.17	4.99	16
Resistor	R0	2	25.36	1
	R1 & R2	2	187.25	1
	R3	2	206.7	1
	R4 & R5	2	57.35	1

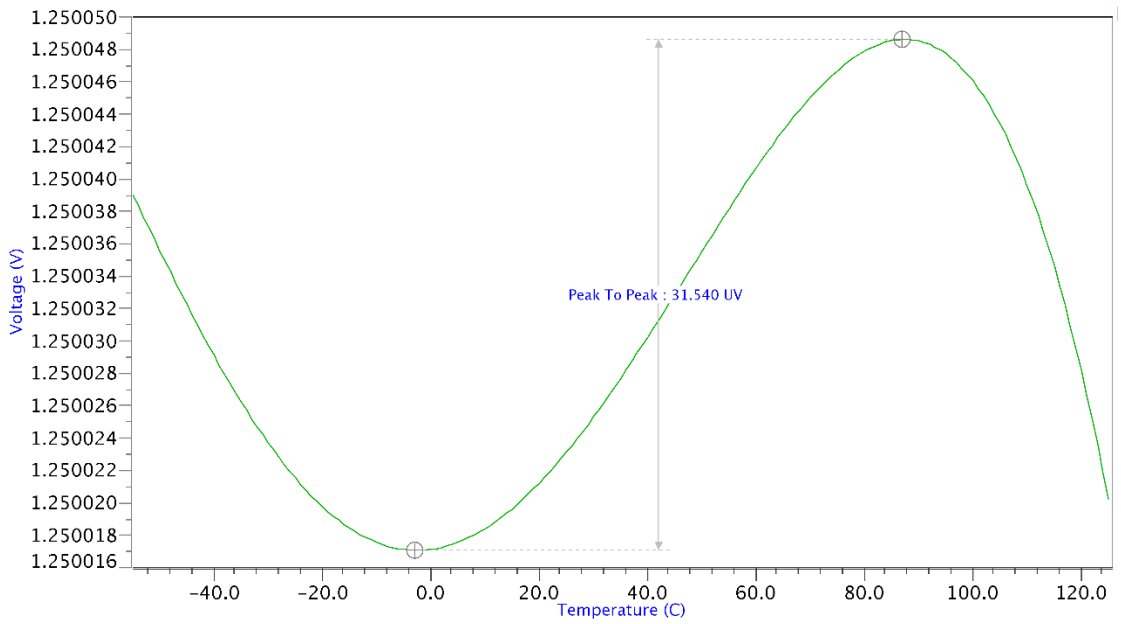


Figure 42 - Reference voltage of 2nd order BGV.

4.9.1 Simulation with Corners

The results presented in Table 15 where obtained from simulations with and without corners, where the reference voltage suffers from what is mentioned in section 4.4.1. Figure 43 shows the reference voltage for corners whose values are in Table 15.

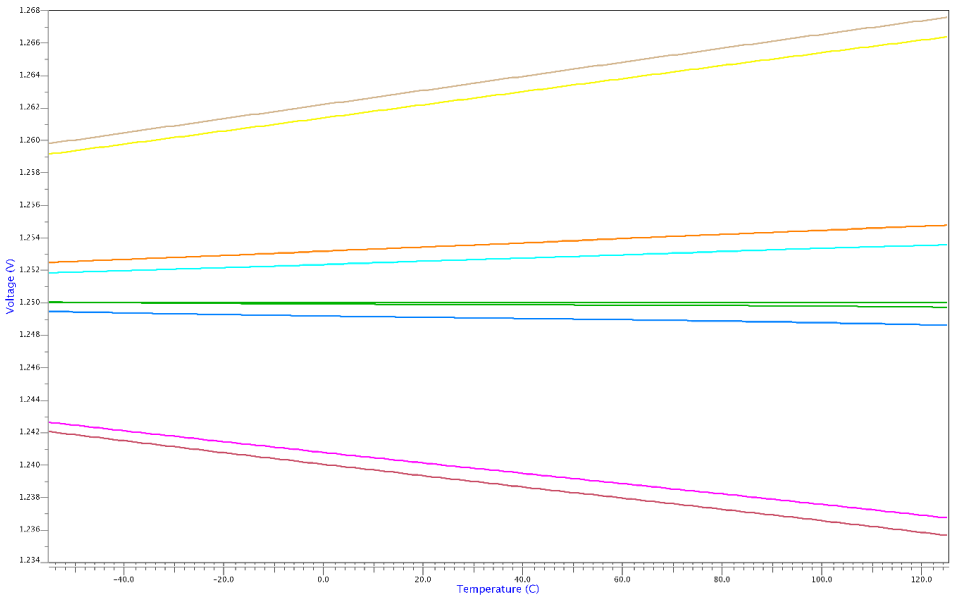


Figure 43 - Reference voltage of 2nd order BGV with corners.

4.9.2 Monte Carlo Analysis

Monte Carlo simulations are applied to analyze random variations related with process and mismatches (variables in the components) in the circuit, evaluated as mentioned in section 4.3.4 with 1000 iterations. Table 17 shows the results obtained for temperature coefficient, reference voltage, and power supply rejection ratio, presented in Figure 44, Figure 45 & Figure 46 respectively.

Table 17 - Results from Monte Carlo simulations.

	Mean Value	Standard Deviation	3σ - MAX	3σ - MIN
TC [ppm/° C]	20.56758	15.77585	101.15664	0.13184
VBG [V]	1.25048	0.03236	1.35784	1.14613
PSRR @ 1 MHz [dB]	69.85273	9.5213	117.35865	54.08016

In the next figures, the historic representation (bar function) is in green, the probability density function (function slightly to the left) in yellow and the Gaussian distribution (centered function) in blue.

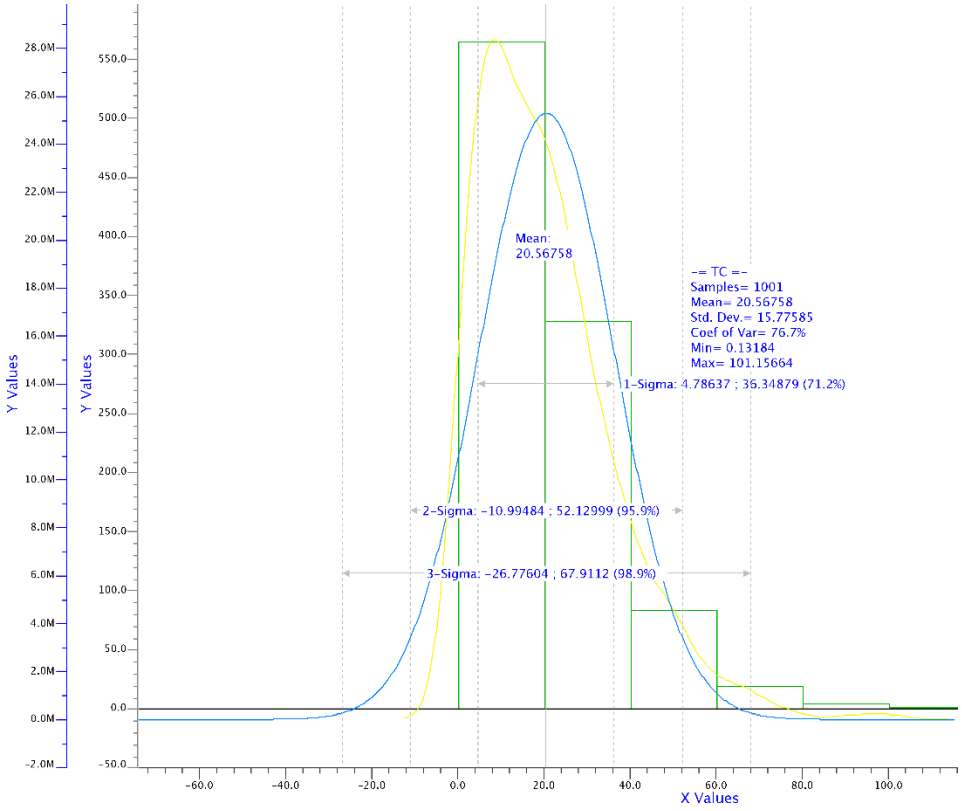


Figure 44 - Monte Carlo simulation of TC.

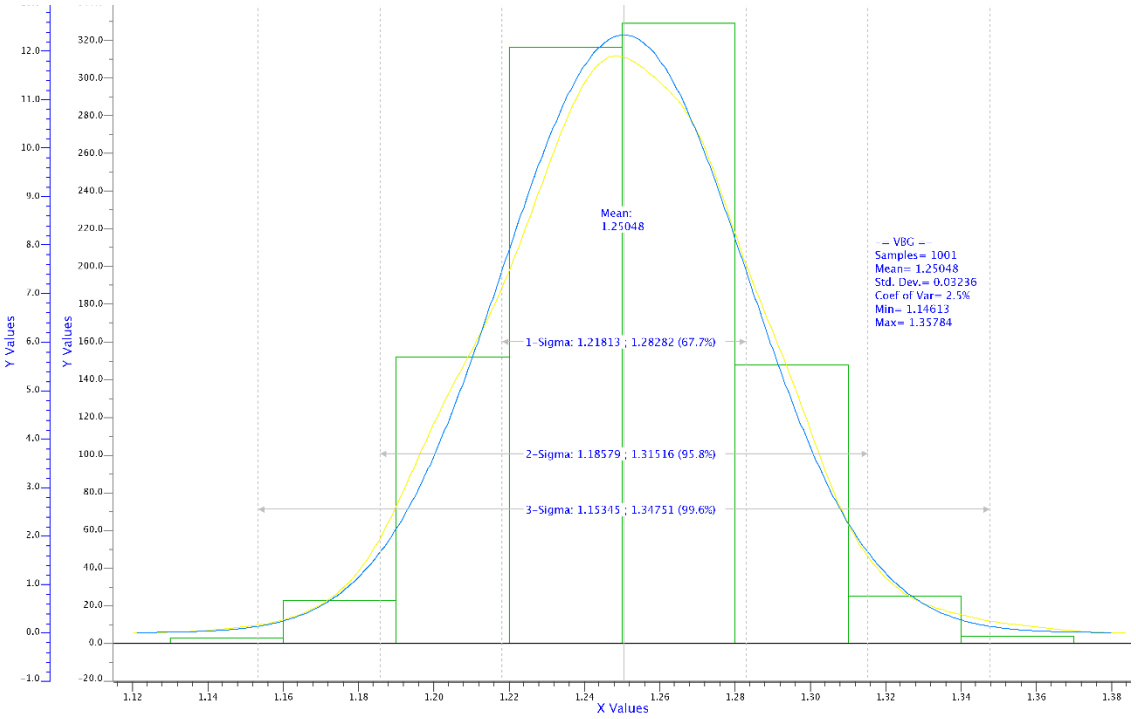


Figure 45 - Monte Carlo simulation for reference voltage.

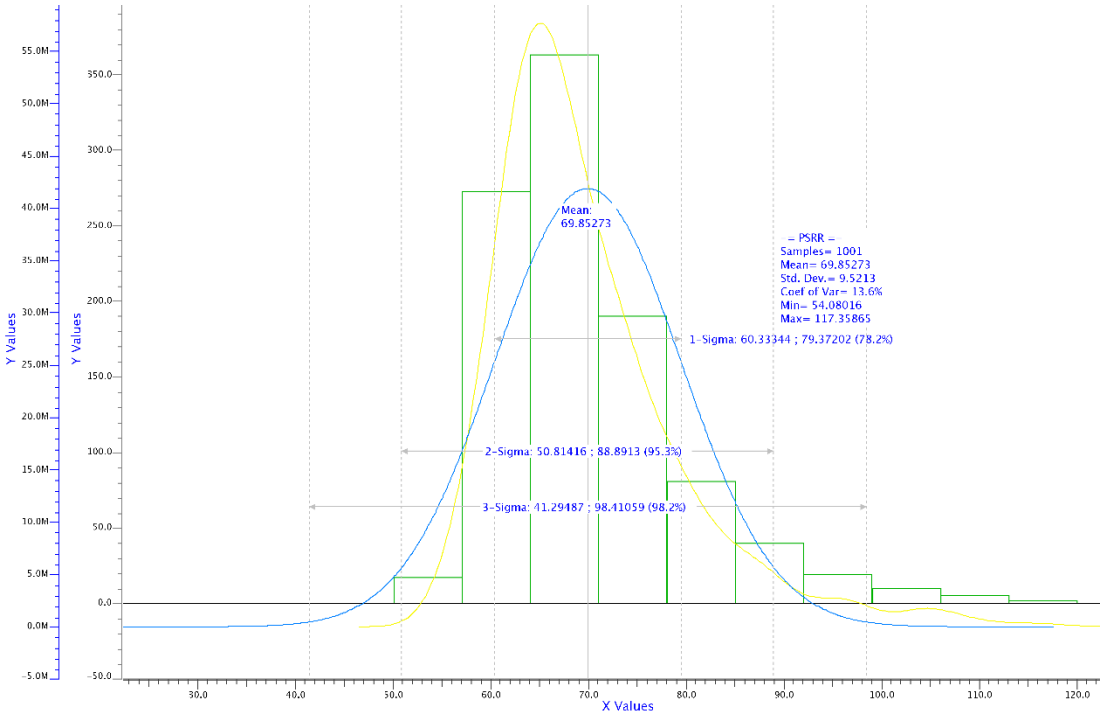


Figure 46 - Monte Carlo simulation for PSRR.

4.10 Stability

From the section 3.3.5, the bandgap voltage reference can have more than just one DC operating point, due to this, and to corroborate the good function of the startup circuit, a unique DC operating point simulation was executed.

This method basically consists in open the loop between the output and the startup input circuit, inserting a DC source sweeping voltage from 0 to 3.3 V; proving the effectiveness of the startup circuit and the DC operating point of the circuit. A representation of this method is shown in Figure 47.

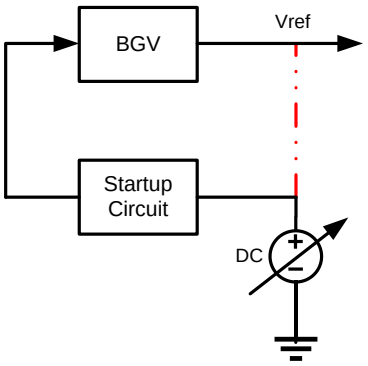


Figure 47 - Representation of Unique DC Operating Point Method in the Circuit.

Figure 48 shows the output voltage of the BGV for all corners applying this method.

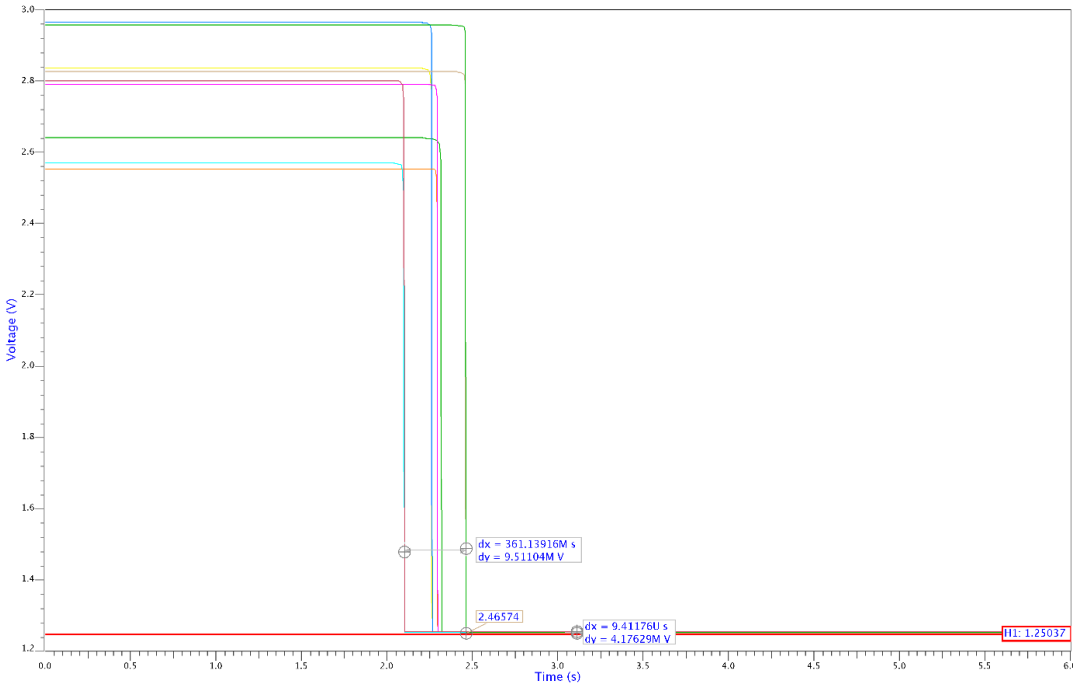


Figure 48 - Output voltage with unique DC operating point method.

4.10.1 Start-up of the circuit

The start-up of the circuit was simulated through a transient analysis and considering $\pm 0.4\% V_{Ref}$. Obtaining results in the range of $1.36815\, ms\ to\ 4.20772\, ms$ depending on the corner for this parameter. These simulations were evaluated with a supply voltage with a rising time of $1\, ms$; since it is not a requirement from the specifications, it doesn't represent a problem. These values are illustrated in Figure 49.

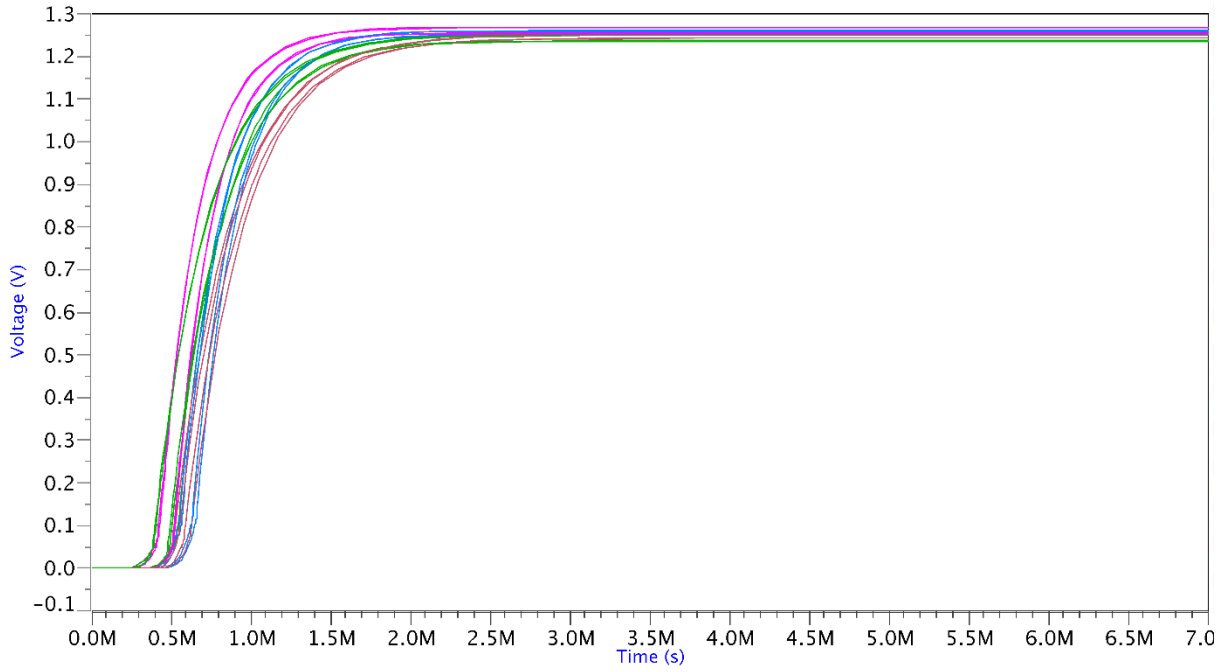


Figure 49 - Graph of time range to set-up for corners.

4.11 Power Down Mode

The power down mode is the main function of the power down circuit (PDC), which is reduce the consumption of the circuit when this circuit is enabled as expressed in section 3.3.9. A transient analysis is required to analyze this function in the circuit.

Enabling the PDC forces the circuit to be in a "turn-off state", and when disabled, the BGV is turned on. The power down block decreases the supply to zero when enable and increases when disable. This configuration was established due to the ease that represents the implementation and also for the specifications.

Figure 50 illustrates the output voltage of the circuit working in these modes of the power down, where the power down mode is enabled from $0\ s$ to $6\ \mathrm{ms}$, the period is given by $1\ \mathrm{ms}$ for rising and falling time and $4\ ms$ of pulse width, subsequently it is disabled with a similar period duration.

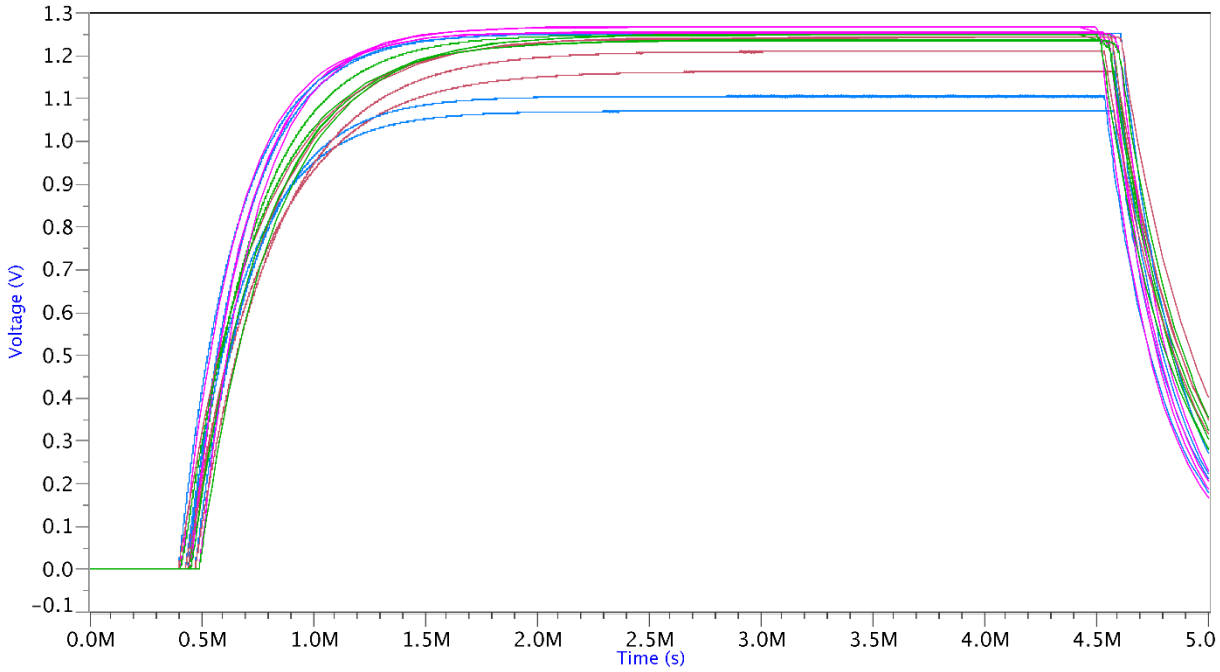


Figure 50 - Output voltage with the power down mode for corners.

4.11.1 Power Consumption

Based on the function of power down, it is possible to determine the two average values of consumption when it is enabled and disabled. The current consumption is also known as quiescent current, which is the current needed to run the BGV in steady state.

The power consumption is given by

$$P_{Consumption} = V_{Supply} * I_{Consumption} \qquad \textit{Equation 94}$$

Figure 51 illustrates a graph of the current consumption of the circuit.

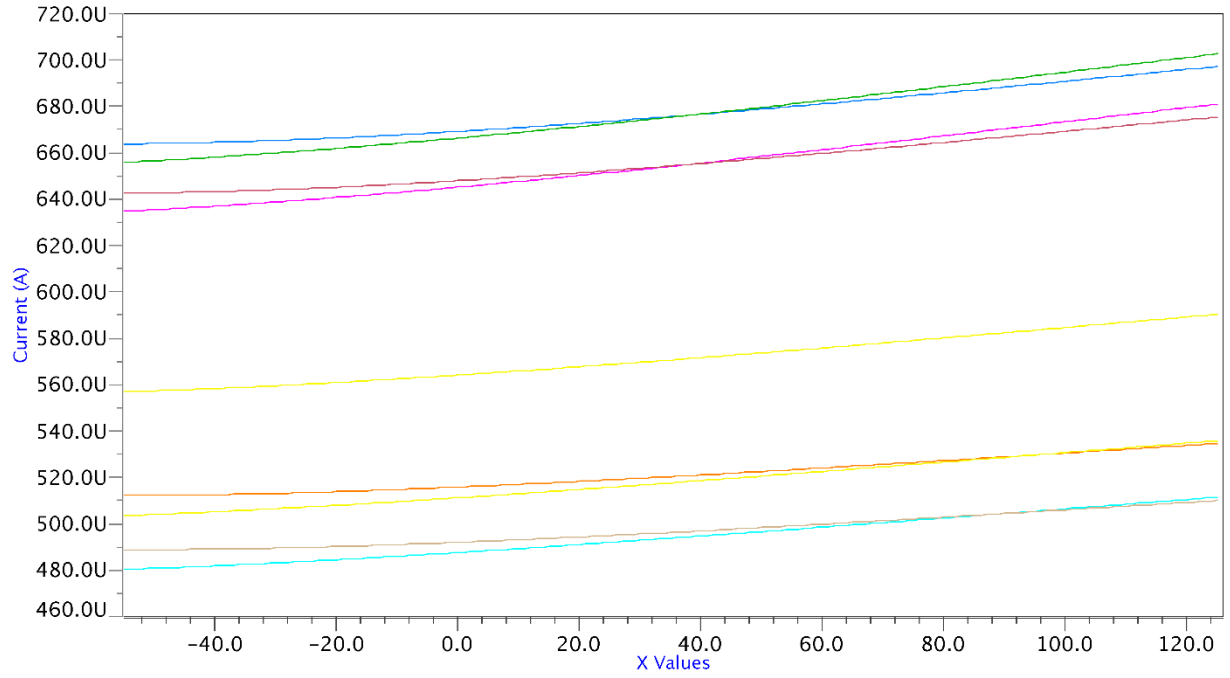


Figure 51 - Current Consumption of BGV for corners against temperature.

Table 18 indicates the consumption values in both states of the circuit when it is working with the power down function.

Table 18 - Current Consumption of BGV with Power Down Mode.

	Enable			Disable		
	Worst	**Typical**	**Best**	**Worst**	**Typical**	**Best**
OTA [µA]	1.33E-04	1.30E-04	1.26E-04	169.97	144	124.55
S-BIAS [µA]	1.73E-04	1.69E-04	1.65E-04	263.74	221.4	189.85
Startup [µA]	201.87	184.04	167.44	96.299	71.941	54.535
BGV [µA]	209.19	186.61	167.93	750.72	634.46	548.96

With these values, a simple calculation is used to determined the typical power consumption, which in this case is $2.093\ mW$.

4.12 Trimming

The trimming section was implemented in the core resistance (R_0), and in the resistances for the second order compensation $(R_4\ and\ R_5)$. With 7 bits in every arrangement of resistors following the structure as presented in Figure 29.

Table 19 and Table 21, show the resistances variations occurred for the different combinations in all the corner cases and temperature range.

Table 19 - Variation of R0 for all cases.

			Temperature				
Corner	**LR0**	**R [Ω]**	**-55**	**0**	**25**	**86**	**125**
Typical	25.36	3189.53	3128.72	3048.75	3018.28	2960.57	2936.03
[1-4]	26	3268.69	3208.2	3125.18	3093.95	3034.78	3009.62
[5-8]	25.3	3182.11	3122.37	3041.58	3011.19	2953.61	2929.13
[9-12]	25.6	3219.22	3159.15	3077.41	3046.65	2988.39	2963.63
[13-16]	24.9	3132.64	3073.32	2993.81	2963.89	2907.23	2883.14
[17-20]	25.5	3206.85	3146.89	3065.47	3034.83	2976.8	2952.13
[21-24]	24.8	3120.27	3061.06	2981.87	2952.07	2895.63	2871.64
[25-28]	26	3268.69	3208.2	3125.18	3093.95	3034.78	3009.62
[29-32]	25.3	3182.11	3122.37	3041.58	3011.19	2953.61	2929.13

The theoretical values were calculated for 7-bit network on the R_0 are presented in Table 20.

An important issue to be considered is the switches resistance. In order to reduce the impact of this resistance, the width (W) of these switches was increased to $15\ \mu m$.

Table 20 - Theoretical values for the R0 network.

	Value [Ω]
RY	2300
RX	1020.96
R0.0	2041.92
R0.1	4083.84
R0.2	8167.68
R0.3	16335.36
R0.4	32670.72
R0.5	65341.44
R0.6	130682.88

The same considerations where made for the resistors which compensate the second order.

Table 21 - Variation of R45 for all cases.

			Temperature				
Corner	**LRY**	**R [Ω]**	**-55**	**0**	**25**	**86**	**125**
Typical	57.35	7146.19	7052.44	6869.32	6800.41	6669.9	6614.41
[1-4]	57.35	7146.19	7052.44	6869.32	6800.41	6669.9	6614.41
[5-8]	56.9	7090.53	6997.26	6815.57	6747.21	6617.72	6562.67
[9-12]	55.9	6966.85	6874.64	6696.14	6628.98	6501.77	6447.68
[13-16]	55.5	6917.37	6825.59	6648.37	6581.69	6455.39	6401.69
[17-20]	57.9	7214.22	7119.88	6935	6865.44	6733.67	6677.65
[21-24]	57.9	7214.22	7119.88	6935	6865.44	6733.67	6677.65
[25-28]	59.3	7387.37	7291.56	7102.2	7030.96	6896.01	6838.63
[29-32]	58.6	7300.79	7205.72	7018.6	6948.2	6814.84	6758.14

And Table 22 for the R_{45} network.

Table 22 - Theoretical values for the R45 network.

	Value [Ω]
RY	5540
RX	1870.44
R45.0	1870.44
R45.1	3740.88
R45.2	7481.76
R45.3	14963.52
R45.4	29927.04
R45.5	59854.08
R45.6	119708.16

In the APPENDIX B **– RESISTOR NETWORKS**, all the combinations and values are presented for both resistor networks.

4.12.1 Measurements with Trimming

Once the full circuit is implemented with both trimming networks, all the simulations were performed once more in order to validate the new data results and possible issues by sweeping the programming codes of the bits to detect the best programming code (combination) for every corner case.

First, the core resistor network obtains good results but still is a possibility to improve the results adjusting the second network. Once the first sweep of the code is done, the second follows the same procedure, and, as expected, the results improved thus better values in voltage reference and temperature coefficient are achieved. The values obtained from both sweeps are shown in Table 23 and Table 24.

Table 23 - Results from the first sweep (core trimming).

Corner	Code	TC	SW0	SW1	SW2	SW3	SW4	SW5	SW6	R Value [Ω]
Typical	57	0.615	0	1	1	1	0	0	0	1325.805
[1-4]	39	1.06	0	1	0	0	1	1	1	1500.86625
[5-8]	58	0.658	0	1	1	1	0	0	1	1316.079375
[9-12]	53	1.155	0	1	1	0	1	0	0	1364.7075
[13-16]	77	1.674	1	0	0	1	1	0	0	1131.2925
[17-20]	53	0.712	0	1	1	0	1	0	0	1364.7075
[21-24]	76	1.261	1	0	0	1	0	1	1	1141.018125
[25-28]	39	0.762	0	1	0	0	1	1	0	1500.86625
[29-32]	58	0.685	0	1	1	1	0	0	1	1316.079375

The second sweep performed maintaining the new values from the first sweep.

Table 24 - Results from the second sweep (compensation trimming).

Corner	Code	SWY0	SWY1	SWY2	SWY3	SWY4	SWY5	SWY6	R Value [Ω]	TC	VBG @ 25 °C
Typical	32	0	0	1	1	1	1	1	6800.08	0.5729	1.2517
[1-4]	24	0	0	1	0	1	1	1	6915.95	0.6103	1.2521
[5-8]	33	0	1	0	0	0	0	0	6786.96	0.4524	1.2516
[9-12]	25	0	0	1	1	0	0	0	6900.32	0.8066	1.2529
[13-16]	33	0	1	0	0	0	0	0	6786.96	1.4279	1.2550
[17-20]	28	0	0	1	1	0	1	1	6855.47	0.6013	1.2519
[21-24]	33	0	1	0	0	0	0	0	6786.96	1.1635	1.2542
[25-28]	32	0	0	1	1	1	1	1	6800.08	0.6515	1.2507
[29-32]	30	0	0	1	1	1	0	1	6827.18	0.6195	1.2526

4.12.2 Monte Carlo Analysis with Trimming

The Monte Carlo (MC) analysis is extremely important for the design of the circuit, because it allows to have a better overview of possible noise, a random variation as well mismatches that the circuit could present after fabrication.

Unfortunately, the results obtained from the MC simulation didn't fulfill the expectations and showed a big problem with the maximum value of 3σ for random variations in the circuit as represented in Table 25.

Table 25 - Results of Monte Carlo.

	3σ - Min	3σ - Max	Mean
TC [ppm/°C]	0.20037	129.3245	21.3842
VBG [V]	1.13499	1.35159	1.25055
Voff @25 [V]	3.19E-05	0.11501	0.02619

This issue represents a possible failure at the creation of this design, so a correction was a must on these values. Digging into the problem, an individual MC analysis for each block on the circuit was carried out finding the contribution and impact of each one, the analysis was performed maintaining the circuit without variation during the simulation and making the block receive the variations. Table 26 shows the results of these simulations.

Table 26 - Results of the impact of every sub-block.

	TC [ppm/°C]			VGB [V]			Voff @ 25 [V]		
	3σ-Min	**3σ-Max**	**Mean**	**3σ-Min**	**3σ-Max**	**Mean**	**3σ-Min**	**3σ-Max**	**Mean**
OTA	0.456	128.799	20.005	1.135	1.356	1.251	4.12E-05	0.1145	0.02654
Bias	0.545	0.613	0.573	1.251	1.251	1.251	1.73E-03	0.00178	0.00176
Startup	0.573	0.573	0.573	1.251	1.251	1.251	1.76E-03	0.00176	0.00176
Current Source	0.516	21.384	5.82	1.242	1.265	1.251	1.90E-06	0.01569	0.00347
Trimming R0	0.556	18.247	4.49	1.244	1.259	1.251	5.96E-08	0.00957	0.00243
Trimming R45	0.539	1.447	0.746	1.25	1.253	1.251	1.20E-04	0.00315	0.00178

As observed in the Table 26, the biggest contributor to the random variations is the operational transconductance amplifier which reaches a high value and mean. The impact of sub-blocks due to the random variations and noise doesn't have a proportional contribution of the blocks.

4.12.2.1 Issue Correction

From the results of every block impact, seems that the OTA circuit is the one which contributes the most to this variation. By analyzing it, was found that the size of transistors in the differential pair and active load was small which allowed a more probabilistic mismatch and noise in it.

The simplest solution was to increase this size, maintaining the ratio W/L and, of course, the multiplicity; with this change the transistors area improves and the circuit have a better performance. This method was made with two & four times the ratio, giving better results when the ratio is four times bigger than its original size, as shows in Table 27.

Table 27 - Results of MC analysis with 4 times the ratio of the diff. pair and active load in OTA.

	TC [ppm/°C]			VGB [V]			Voff @ 25 [V]		
	36-Min	**36-Max**	**Mean**	**36-Min**	**36-Max**	**Mean**	**36-Min**	**36-Max**	**Mean**
Full	0.224	41.875	10.111	1.2226	1.2796	1.2522	8.27E-06	0.02966	0.00821
OTA	0.354	25.281	5.511	1.2232	1.2794	1.2521	2.49E-06	0.02947	0.00698
Bias	0.971	1.107	1.046	1.2519	1.2520	1.252	1.95E-03	0.00205	0.002
Startup	1.045	1.047	1.046	1.252	1.252	1.252	2.00E-03	0.002	0.002
Current Source	0.349	20.853	5.838	1.2422	1.2659	1.2520	1.83E-05	0.01593	0.00356
Trimming R0	0.474	19.140	4.543	1.2444	1.2598	1.2520	2.39E-05	0.00982	0.00257
Trimming R45	0.580	2.284	1.066	1.2503	1.2534	1.2520	3.70E-04	0.0034	0.00202

Another method used to solve this issue was to re-size the operational transconductance amplifier using AIDA-C one more time, but with the whole circuit and just focusing on the amplifier, optimizing the block working in the whole system, and not an individual block as previously done. AIDA-C with the Monte Carlo constraint was used this time. [30] This provides a new optimized size which was used for the simulations obtaining the next results.

Table 28 - Results of MC analysis with new OTA sizing.

	TC [ppm/°C]			VGB [V]			Voff @ 25 [V]		
	36-Min	**36-Max**	**Mean**	**36-Min**	**36-Max**	**Mean**	**36-Min**	**36-Max**	**Mean**
Full	0.257	38.057	8.909	1.224	1.277	1.2508	1.53E-06	0.02778	0.00695
OTA	0.576	11.779	3.25	1.229	1.271	1.2511	2.80E-06	0.02121	0.00517
Bias	0.629	0.733	0.65	1.251	1.251	1.2511	1.11E-03	0.00112	0.00111
Startup	0.641	0.642	0.641	1.251	1.251	1.2511	1.11E-03	0.00111	0.00111
Current Source	0.623	26.037	6.023	1.237	1.265	1.2510	9.64E-06	0.0154	0.00332
Trimming R0	0.634	18.336	4.805	1.243	1.258	1.2511	5.08E-07	0.0083	0.00221
Trimming R45	0.626	1.685	0.833	1.249	1.252	1.2510	9.88E-07	0.00254	0.00107

Due to the new values the sweeps of codes at the trimming were eventually made it again to achieve a better performance. Table 29 and Table 30 show the results for the new OTA sizing in the whole circuit for the core trimming and for the compensation trimming respectively.

Table 29 - TC results from the core trimming sweep with new OTA sizing.

Corner	Code	TC	SW0	SW1	SW2	SW3	SW4	SW5	SW6
Typical	57	0.7121	0	1	1	1	0	0	0
[1-4]	39	0.6843	0	1	0	0	1	1	0
[5-8]	58	0.5243	0	1	1	1	0	0	1
[9-12]	52	1.2735	0	1	1	0	0	1	1
[13-16]	77	1.7006	1	0	0	1	1	0	0
[17-20]	52	1.0445	0	1	1	0	0	1	1
[21-24]	76	1.2136	1	0	0	1	0	1	1
[25-28]	39	0.7913	0	1	0	0	1	1	0
[29-32]	58	0.8344	0	1	1	1	0	0	1

With the results presented in Table 30, it can be seen that with this new sizing the values for the corner case remain within specs.

Table 30 - Results of compensation trimming sweep with new OTA sizing.

Corner	Code	SWY0	SWY1	SWY2	SWY3	SWY4	SWY5	SWY6	TC	VBG @ 25 °C [V]	Voff@25 °C [V]
Typical	31	0	0	1	1	1	1	0	0.6414	1.2511	1.11E-03
[1-4]	33	0	1	0	0	0	0	0	0.6473	1.2493	7.00E-04
[5-8]	32	0	0	1	1	1	1	1	0.5242	1.2510	1.04E-03
[9-12]	36	0	1	0	0	0	1	1	0.7522	1.2498	1.90E-04
[13-16]	33	0	1	0	0	0	0	0	1.4818	1.2542	4.20E-03
[17-20]	36	0	1	0	0	0	1	1	0.5904	1.2493	6.90E-04
[21-24]	31	0	0	1	1	1	1	0	1.2111	1.2537	3.73E-03
[25-28]	32	0	0	1	1	1	1	1	0.7912	1.2499	8.00E-05
[29-32]	30	0	0	1	1	1	0	1	0.6843	1.2518	1.85E-03

Both of these solutions presents good conditions with a slightly better performance with the new OTA sizing. In Table 31 shows the new sizing values for the operational transconductance amplifier. It is important to consider that this sizing was made with the whole circuit.

Table 31 - New OTA sizing.

Transistors	Width (µm)	Length (µm)	Multiplicity
Active Load	11.8	11.51	13
Bias Source	6.71	2.19	3/13/13
Differential Pair	16.78	3.44	12
2nd Stage	8.48	1.1	4
Capacitor	13	32	1

4.12.2.2 Final MC results

Due to the performances shown in the second method (new sizing), this method was chosen to conclude the final result with all the parameters. As can be seen in Figure 52, the stability during the MC analysis maintains reliable and the current consumptions is still under 1 mA.

Table 32 presents the final results for the Monte Carlo analysis which it is compared with Table 25, the improvement is quite visible.

Table 32 - Final Results of MC simulation.

	36-Min	36-Max	Mean	St.Dev.
TC [ppm/°C]	0.25736	38.05758	8.90965	6.38549
VBG [V]	1.22477	1.27778	1.25084	0.00871
Voff @25 [V]	1.53E-06	0.02778	0.00695	0.00531
PSRR @ 1 Hz	69.26003	140.87518	81.6459	8.81652
PSRR @ 1 MHz	134.42145	136.47917	135.48292	0.2604

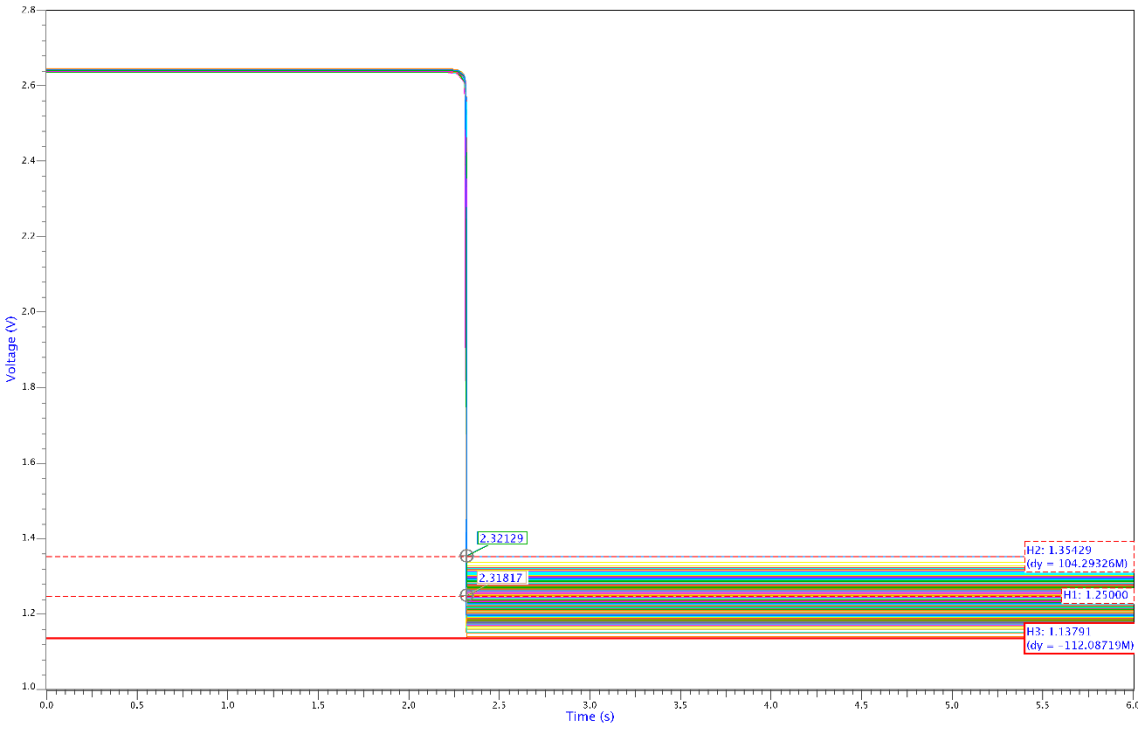


Figure 52 - Unique Operating Point with MC simulation.

4.13 Final Analysis & Comparison

Finally, all the results reach and accomplish the specifications of the project obtaining good outcomes. To compared this project with the state of the art, which is indicated in Table 2, it should be made some considerations, e.g. technology, topology, power consumption, etc.

The overall performance of the BGV circuit proves to satisfy the expectations in almost every measure. When a deeper analysis was made in the case of Monte Carlo, it is clearly seen that with a really small adjustment in the trimming values, and perhaps with a better performance in the amplifier, the results will improve even more.

A comparison between similar projects is represented in Table 33, there the most related works to this one are indicated from one made it in CMOS 350 nm technology and one implemented in silicon. This comparison is a wide overview of this project even when the technologies and topologies aren't the same.

Table 33 - Final Comparison.

	This Project		CMOS 350 nm		Silicon Project	
	Typical	**Worst**	**Typical**	**Worst**	**Typical**	**Worst**
IDD [µA]	704.82	835.76	737	962	2.34e3	3.35e3
TC [ppm/°C]	0.85702	1.6093	2	10.991	7.75	10.46
VGB [V]	1.2511	1.249/1.254	1.249	1.274/1.251	1.235	1.21/1.26
PSRR [dB]	81.833	81.057	84.406	81.926	56.54	64.695

It must be considered that the sizing of every block of the circuit was made by the optimization in AIDA-C and without any constraints in size, since it was not specified.

5 CONCLUSION

This master thesis has explored the steps involved in the design of bandgap voltage reference, with special characteristics specified for the space industry. The last chapter of the thesis includes the final conclusion regarding the general work, the accomplishments, and a projection of the future work related with the circuit.

5.1 Accomplishments

All the objectives established at the beginning of this project were accomplished and the results attained are considered satisfactory. From the creation of the project library in cadence to the delivery of the database to the final user who requested the circuit.

An overview of the stages accomplish during the work are listed below.

- Creation of project library in Cadence.
- Bibliography of relevant architectures.
- Creation of schematics using the proportioned technology (CMOS 150 nm).
- Definition of key performances in every schematic.
- Generation of simulation plan & test benches.
- Validation of test benches.
- Creation and setup of AIDA-C project.
- Validate the AIDA-C optimization on realistic set of performances.
- Deliver to the final user the design database.

Every sub-circuit created in this project was sized to correctly operate in specification and in collaboration with the other sub-circuits to obtain the final result.

As was mentioned in the previous chapter, there are many possible approaches for improving the results. The decisions taken to not implement those techniques was based on the performance, complexity, available time and a possible inexperience in the field.

AIDA-C proves to be an excellent optimizer software which facilitates and reduce the time to calculate a good dimension in every component. In the lack of experience that a designer could have implementing new architectures or even in the migration from one technology to another, the software is really helpful.

5.1.1 Future Work

Following the common workflow in the creation of IC designs, the next stage involves the creation of the layout and validation of the performance before fabrication. The final user has shown great interest in follow the next stages of this workflow in order to obtain the IC.

The next suggestions intent to give a further insight into what the next stages of this projects involves.

- In order to reach a lower level of variation during the Monte Carlo simulations, it is important to consider a recalculation of the trimming networks and increasing the operating range on their values. With a correct range of resistor value, it will be possible to improve the results obtained in table.
- If during the creation of layout, it is possible to notice a possible fabrication problem caused by the size of certain devices, e.g. the differential pair in the operational transconductance amplifier and current sources, it should be considered to adjust the size of these components maintaining their ratio to guaranty the reliability of the circuit.
- An optional alternative to improve the performance of the circuit is to modify the architecture of the amplifier to a one with focus on reduced the offset. Another possibility is the implementation of a technique to reduce these variations, e.g. The Chopper method.
- The offset voltage could be corrected through a trimming section with a classical topology of DAC systems, correcting the output voltage, if is considered as issue.

Finally, it is expected that the performance of this work will be reliable and in accordance with the results presented in this document.

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APPENDIX A – CIRCUIT NETLIST

Netlist of Operational Transconductance Amplifier.

```
*** Cell name: OTA2
*** View name: schematic

.PARAM WA=11.8
.PARAM WB=6.71
.PARAM WC=13
.PARAM WD=16.78
.PARAM W2G=8.48
.PARAM LA=11.51
.PARAM LB=2.19
.PARAM LC=32
.PARAM LD=3.44
.PARAM L2G=1.1
.PARAM MA=13
.PARAM MB=3
.PARAM MB1=13
.PARAM MB2=13
.PARAM MC=1
.PARAM MD=12
.PARAM M2G=4

.SUBCKT OTA2 OUT IBIAS VDD VSS EN<1> EN<0> V+ V-

    X0 OUT 2NGOTA VSS cmim34 wm={(WC) * 1u} lm={(LC) * 1u} mltm=(MC)
    XMA9 2NGOTA EN<0> VSS VSS nmosox3_ring w={(0.88) * 1u} l={(0.36) * 1u} mltm=(1)
    XMA2 OUT 2NGOTA VSS VSS nmosox3_ring w={(W2G) * 1u} l={(L2G) * 1u} mltm=(M2G)
    XMA1 2NGOTA CMDOTA VSS VSS nmosox3_ring w={(WA) * 1u} l={(LA) * 1u} mltm=(MA)
    XMA0 CMDOTA CMDOTA VSS VSS nmosox3_ring w={(WA) * 1u} l={(LA) * 1u} mltm=(MA)
    MA8 IBIAS EN<1> VDD VDD pmosox3 L={(0.36) * 1u} W={(0.6) * 1u} M=1
    MA7 OUT IBIAS VDD VDD pmosox3 L={(LB) * 1u} W={(WB) * 1u} M=MB2
    MA6 IDPOTA IBIAS VDD VDD pmosox3 L={(LB) * 1u} W={(WB) * 1u} M=MB1
    MA5 IBIAS IBIAS VDD VDD pmosox3 L={(LB) * 1u} W={(WB) * 1u} M=MB
    MA4 2NGOTA V+ IDPOTA VDD pmosox3 L={(LD) * 1u} W={(WD) * 1u} M=MD
    MA3 CMDOTA V- IDPOTA VDD pmosox3 L={(LD) * 1u} W={(WD) * 1u} M=MD

.ENDS
```

Netlist of Self-Bias Circuit.

```
*** Cell name: BTAS2
*** View name: schematic

.PARAM W1=2.59
.PARAM W2=18.17
.PARAM L1=4.95
.PARAM L2=4.99
.PARAM M1=8
.PARAM M2=16

.SUBCKT BTAS2 EN<1> EN<0> IREF VBIAS VDD VSS

    XM25 VBIAS VN1 IRCC2 VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM26 IRCC2 VN2 VSS VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM13 IRCC VN2 VSS VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM12 VN2 VN2 VSS VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM11 IREF VN1 IRCC VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM10 VN1 VN1 VN2 VSS nmosox3_ring w={(6) * 1u} l={(1) * 1u} mltm=(8)
    XM6 VR EN<0> VSS VSS nmosox3_ring w={(0.88) * 1u} l={(0.36) * 1u} mltm=(1)
    XM5 VL CNSU VSS VSS nmosox3_ring w={(9) * 1u} l={(0.36) * 1u} mltm=(1)
    XM4 CNSU VR VSS VSS nmosox3_ring w={(9) * 1u} l={(0.36) * 1u} mltm=(1)
    XM1 VL VX VSS VSS nmosox3_ring w={(16.1) * 1u} l={(2) * 1u} mltm=(4)
    XM0 VX VR VSS VSS nmosox3_ring w={(16.1) * 1u} l={(2) * 1u} mltm=(1)
    M17 NET10 NET10 VDD VDD pmosox3 L={(L1) * 1u} W={(W1) * 1u} M=M1
    M9 VN1 VC VDD VDD pmosox3 L={(2) * 1u} W={(20.15) * 1u} M=8
    M8 VL EN<0> VC VDD pmosox3 L={(0.36) * 1u} W={(0.6) * 1u} M=1
    M7 VC EN<1> VDD VDD pmosox3 L={(0.36) * 1u} W={(0.6) * 1u} M=1
    M16 VBIAS VBIAS NET10 VDD pmosox3 L={(L2) * 1u} W={(W2) * 1u} M=M2
    M3 VL VC VDD VDD pmosox3 L={(2) * 1u} W={(20.15) * 1u} M=16
    M2 VR VC VDD VDD pmosox3 L={(2) * 1u} W={(20.15) * 1u} M=16
    X0 VR VX VSS rplow lrp={(2) * 1u} wrp={(2) * 1u} mltm=(1) s=28 paras=1
    X1 VDD CNSU VSS rplow lrp={(4.42) * 1u} wrp={(2) * 1u} mltm=(1) s=50 paras=1
    X4 VN1 VSS VSS cmim34 wm={(55.56) * 1u} lm={(45) * 1u} mltm=(2)
    X6 EN<0> VSS VSS cmim34 wm={(80) * 1u} lm={(20) * 1u} mltm=(1)
    X5 IRCC2 VSS VSS cmim34 wm={(26.67) * 1u} lm={(15) * 1u} mltm=(4)
    X2 VC VSS VSS cmim34 wm={(40) * 1u} lm={(40) * 1u} mltm=(40)
    X3 VC VSS VSS cmim34 wm={(80) * 1u} lm={(20) * 1u} mltm=(1)

.ENDS
```

Netlist of Power Down Circuit.

```
*** Cell name: PD
*** View name: schematic

.SUBCKT PD Q QB VDD VSS EN

    DP0 VSS EN nd AREA=4.72e-13
    XMP1 Q QB VSS VSS nmosox3_ring w={(2) * 1u} l={(1.5) * 1u} mltm=(1)
    XMP0 QB EN VSS VSS nmosox3_ring w={(2) * 1u} l={(1.5) * 1u} mltm=(1)
    XP0 QB VSS VSS cmim34 wm={(45.71) * 1u} lm={(35) * 1u} mltm=(1)
    XP1 Q VSS VSS cmim34 wm={(45.71) * 1u} lm={(35) * 1u}  mltm=(1)
    MP3 Q QB VDD VDD pmosox3 L={(1.5) * 1u} W={(6) * 1u} M=1
    MP2 QB EN VDD VDD pmosox3 L={(1.5) * 1u} W={(6) * 1u} M=1

.ENDS
```

Netlist of Startup Circuit.

```
*** Cell name: SUAF2
*** View name: schematic

.SUBCKT SUAF2 IN OUT VDD VSS EN<1> EN<0>

    XM8 IOUT EN<0> VSS VSS nmosox3_ring w={(2) * 1u} l={(64) * 1u} mltm=(1)
    XM2 IOUT IMID VSS VSS nmosox3_ring w={(12.15) * 1u} l={(2) * 1u} mltm=(1)
    XM0 IMID IIN VSS VSS nmosox3_ring w={(12.15) * 1u} l={(2) * 1u} mltm=(1)
    X0 VSS IIN VSS rplow lrp={(40) * 1u} wrp={(2) * 1u} mltm=(1) s=10 paras=1
    M13 IIN IN CCSU VDD pmosox3 L={(4.99) * 1u} W={(18.17) * 1u} M=16
    M12 VSS IOUT OUT VDD pmosox3 L={(2) * 1u} W={(150) * 1u} M=3
    M7 IIN EN<1> VDD VDD pmosox3 L={(1.5) * 1u} W={(2) * 1u} M=1
    M11 CCSU OUT VDD VDD pmosox3 L={(4.95) * 1u} W={(2.59) * 1u} M=8
    M3 IOUT IMID VDD VDD pmosox3 L={(2) * 1u} W={(32.15) * 1u} M=1
    M1 IMID IIN VDD VDD pmosox3 L={(2) * 1u} W={(32.15) * 1u} M=1

.ENDS
```

Netlist of Trimming Networks.

```
*** Cell name: TR5
*** View name: schematic

.SUBCKT TR5 B<0> B<1> B<2> B<3> B<4> B<5> B<6> TX TY SUB

    XF NET3 TX SUB rplow lrp={(8.47) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XX TY NET3 SUB rplow lrp={(19.28) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X0 SW0 TX SUB rplow lrp={(15.28) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X1 SW1 TX SUB rplow lrp={(32.58) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X2 SW2 TX SUB rplow lrp={(67.2) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X3 SW3 TX SUB rplow lrp={(136.55) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X4 SW4 TX SUB rplow lrp={(275.61) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X5 SW5 TX SUB rplow lrp={(555.25) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X6 SW6 TX SUB rplow lrp={(1120.62) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1

    XM6 SW6 B<6> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM5 SW5 B<5> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM4 SW4 B<4> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM3 SW3 B<3> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM2 SW2 B<2> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM1 SW1 B<1> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM0 SW0 B<0> NET3 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)

.ENDS

*** Cell name: TR7
*** View name: schematic

.SUBCKT TR7 B<0> B<1> B<2> B<3> B<4> B<5> B<6> TX TY SUB

    X1 SW1 TX SUB rplow lrp={(30.14) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XF NET03 TX SUB rplow lrp={(15.65) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X0 SW0 TX SUB rplow lrp={(14.32) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XX TY NET03 SUB rplow lrp={(46.69) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X2 SW2 TX SUB rplow lrp={(61.78) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X3 SW3 TX SUB rplow lrp={(125.08) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X4 SW4 TX SUB rplow lrp={(251.74) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X5 SW5 TX SUB rplow lrp={(505.26) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    X6 SW6 TX SUB rplow lrp={(1013.16) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1

    XM1 SW1 B<1> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM4 SW4 B<4> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM6 SW6 B<6> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM0 SW0 B<0> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u mltm=(1)
    XM3 SW3 B<3> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u mltm=(1)
    XM2 SW2 B<2> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)
    XM5 SW5 B<5> NET03 SUB nmosox3_ring w={(15) * 1u} l={(0.36) * 1u} mltm=(1)

.ENDS
```

Netlist of Bandgap Voltage Reference.

```
*** Cell name: BGVT
*** View name: schematic

.PARAM W1=2.59
.PARAM W2=18.17
.PARAM L1=4.95
.PARAM L2=4.99
.PARAM M1=8
.PARAM M2=16

.SUBCKT BGVT VREF B<0> B<1> B<2> B<3> B<4> B<5> B<6> BY<0> BY<1> BY<2> BY<3> BY<4> BY<5>
BY<6> VDD VSS EN

    XI0 1OUT IBIAS VDD VSS Q QB V+ V- OTA2
    XI1 Q QB IBIAS 2OUT VDD VSS BTAS2
    XI3 Q QB VDD VSS EN PD
    XI2 2OUT 1OUT VDD VSS Q QB SUAF2
    XI4 B<0> B<1> B<2> B<3> B<4> B<5> B<6> V+ RG0 VSS TR5
    XM9 V+ QB VSS VSS nmosox3_ring w={(0.88) * 1u} l={(0.36) * 1u} mltm=(1)
    XM8 V- QB VSS VSS nmosox3_ring w={(0.88) * 1u} l={(0.36) * 1u} mltm=(1)
    M4 V+ 2OUT CC+ VDD pmosox3 L={(L2) * 1u} W={(W2) * 1u} M=M2
    M1 CC+ 1OUT VDD VDD pmosox3 L={(L1) * 1u} W={(W1) * 1u} M=M1
    M3 V- 2OUT CC- VDD pmosox3 L={(L2) * 1u} W={(W2) * 1u} M=M2
    M0 CC- 1OUT VDD VDD pmosox3 L={(L1) * 1u} W={(W1) * 1u} M=M1
    M7 COMP2 2OUT CC2 VDD pmosox3 L={(L2) * 1u} W={(W2) * 1u} M=M2
    M6 CC2 1OUT VDD VDD pmosox3 L={(L1) * 1u} W={(W1) * 1u} M=M1
    M10 1OUT Q VDD VDD pmosox3 L={(0.36) * 1u} W={(0.6) * 1u} M=1
    M5 VREF 2OUT CCOUT VDD pmosox3 L={(L2) * 1u} W={(W2) * 1u} M=M2
    M2 CCOUT 1OUT VDD VDD pmosox3 L={(L1) * 1u} W={(W1) * 1u} M=M1
    XR1 VSS V+ VSS rplow lrp={(187.25) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XR2 VSS V- VSS rplow lrp={(187.25) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XR3 VSS VREF VSS rplow lrp={(206.7) * 1u} wrp={(2) * 1u} mltm=(1) s=1 paras=1
    XI5 BY<0> BY<1> BY<2> BY<3> BY<4> BY<5> BY<6> COMP2 V+ VSS TR7
    XI6 BY<0> BY<1> BY<2> BY<3> BY<4> BY<5> BY<6> COMP2 V- VSS TR7
    XQ0<1> VSS VSS RG0 pnp_vert_b
    XQ0<2> VSS VSS RG0 pnp_vert_b
    XQ0<3> VSS VSS RG0 pnp_vert_b
    XQ0<4> VSS VSS RG0 pnp_vert_b
    XQ0<5> VSS VSS RG0 pnp_vert_b
    XQ0<6> VSS VSS RG0 pnp_vert_b
    XQ0<7> VSS VSS RG0 pnp_vert_b
    XQ0<8> VSS VSS RG0 pnp_vert_b
    XQ1 VSS VSS V- pnp_vert_b
    XQ2 VSS VSS COMP2 pnp_vert_b

.ENDS
```

APPENDIX B – RESISTOR NETWORKS

Calculated values for core trimming.

#	X0	X1	X2	X3	X4	X5	X6	R Parallel [Ω]	Value [Ω]
1	0	0	0	0	0	0	0	1020.96	3320.96
2	0	0	0	0	0	0	X	1013.045581	3313.0456
3	0	0	0	0	0	X	0	1005.252923	3305.2529
4	0	0	0	0	0	X	X	997.5792366	3297.5792
5	0	0	0	0	X	0	0	990.0218182	3290.0218
6	0	0	0	0	X	0	X	982.5780451	3282.578
7	0	0	0	0	X	X	0	975.2453731	3275.2454
8	0	0	0	0	X	X	X	968.0213333	3268.0213
9	0	0	0	X	0	0	0	960.9035294	3260.9035
10	0	0	0	X	0	0	X	953.889635	3253.8896
11	0	0	0	X	0	X	0	946.9773913	3246.9774
12	0	0	0	X	0	X	X	940.1646043	3240.1646
13	0	0	0	X	X	0	0	933.4491429	3233.4491
14	0	0	0	X	X	0	X	926.8289362	3226.8289
15	0	0	0	X	X	X	0	920.3019718	3220.302
16	0	0	0	X	X	X	X	913.8662937	3213.8663
17	0	0	X	0	0	0	0	907.52	3207.52
18	0	0	X	0	0	0	X	901.2612414	3201.2612
19	0	0	X	0	0	X	0	895.0882192	3195.0882
20	0	0	X	0	0	X	X	888.9991837	3188.9992
21	0	0	X	0	X	0	0	882.9924324	3182.9924
22	0	0	X	0	X	0	X	877.0663087	3177.0663
23	0	0	X	0	X	X	0	871.2192	3171.2192
24	0	0	X	0	X	X	X	865.4495364	3165.4495
25	0	0	X	X	0	0	0	859.7557895	3159.7558
26	0	0	X	X	0	0	X	854.1364706	3154.1365
27	0	0	X	X	0	X	0	848.5901299	3148.5901
28	0	0	X	X	0	X	X	843.1153548	3143.1154
29	0	0	X	X	X	0	0	837.7107692	3137.7108
30	0	0	X	X	X	0	X	832.3750318	3132.375
31	0	0	X	X	X	X	0	827.1068354	3127.1068
32	0	0	X	X	X	X	X	821.9049057	3121.9049
33	0	X	0	0	0	0	0	816.768	3116.768
34	0	X	0	0	0	0	X	811.6949068	3111.6949
35	0	X	0	0	0	X	0	806.6844444	3106.6844
36	0	X	0	0	0	X	X	801.7354601	3101.7355
37	0	X	0	0	X	0	0	796.8468293	3096.8468
38	0	X	0	0	X	0	X	792.0174545	3092.0175
39	0	X	0	0	X	X	0	787.2462651	3087.2463
40	0	X	0	0	X	X	X	782.5322156	3082.5322
41	0	X	0	X	0	0	0	777.8742857	3077.8743
42	0	X	0	X	0	0	X	773.2714793	3073.2715
43	0	X	0	X	0	X	0	768.7228235	3068.7228
44	0	X	0	X	0	X	X	764.2273684	3064.2274
45	0	X	0	X	X	0	0	759.784186	3059.7842
46	0	X	0	X	X	0	X	755.3923699	3055.3924
47	0	X	0	X	X	X	0	751.0510345	3051.051
48	0	X	0	X	X	X	X	746.7593143	3046.7593
49	0	X	X	0	0	0	0	742.5163636	3042.5164
50	0	X	X	0	0	0	X	738.3213559	3038.3214
51	0	X	X	0	0	X	0	734.1734831	3034.1735
52	0	X	X	0	0	X	X	730.0719553	3030.072
53	0	X	X	0	X	0	0	726.016	3026.016
54	0	X	X	0	X	0	X	722.0048619	3022.0049
55	0	X	X	0	X	X	0	718.0378022	3018.0378
56	0	X	X	0	X	X	X	714.1140984	3014.1141
57	0	X	X	X	0	0	0	710.2330435	3010.233
58	0	X	X	X	0	0	X	706.3939459	3006.3939
59	0	X	X	X	0	X	0	702.596129	3002.5961
60	0	X	X	X	0	X	X	698.8389305	2998.8389
61	0	X	X	X	X	0	0	695.1217021	2995.1217
62	0	X	X	X	X	0	X	691.4438095	2991.4438
63	0	X	X	X	X	X	0	687.8046316	2987.8046

64	0	X	X	X	X	X	X	684.2035602	2984.2036
65	X	0	0	0	0	0	0	680.64	2980.64
66	X	0	0	0	0	0	X	677.1133679	2977.1134
67	X	0	0	0	0	X	0	673.6230928	2973.6231
68	X	0	0	0	0	X	X	670.1686154	2970.1686
69	X	0	0	0	X	0	0	666.7493878	2966.7494
70	X	0	0	0	X	0	X	663.3648731	2963.3649
71	X	0	0	0	X	X	0	660.0145455	2960.0145
72	X	0	0	0	X	X	X	656.6978894	2956.6979
73	X	0	0	X	0	0	0	653.4144	2953.4144
74	X	0	0	X	0	0	X	650.1635821	2950.1636
75	X	0	0	X	0	X	0	646.9449505	2946.945
76	X	0	0	X	0	X	X	643.7580296	2943.758
77	X	0	0	X	X	0	0	640.6023529	2940.6024
78	X	0	0	X	X	0	X	637.4774634	2937.4775
79	X	0	0	X	X	X	0	634.3829126	2934.3829
80	X	0	0	X	X	X	X	631.3182609	2931.3183
81	X	0	X	0	0	0	0	628.2830769	2928.2831
82	X	0	X	0	0	0	X	625.2769378	2925.2769
83	X	0	X	0	0	X	0	622.2994286	2922.2994
84	X	0	X	0	0	X	X	619.3501422	2919.3501
85	X	0	X	0	X	0	0	616.4286792	2916.4287
86	X	0	X	0	X	0	X	613.5346479	2913.5346
87	X	0	X	0	X	X	0	610.6676636	2910.6677
88	X	0	X	0	X	X	X	607.8273488	2907.8273
89	X	0	X	X	0	0	0	605.0133333	2905.0133
90	X	0	X	X	0	0	X	602.2252535	2902.2253
91	X	0	X	X	0	X	0	599.4627523	2899.4628
92	X	0	X	X	0	X	X	596.7254795	2896.7255
93	X	0	X	X	X	0	0	594.0130909	2894.0131
94	X	0	X	X	X	0	X	591.3252489	2891.3252
95	X	0	X	X	X	X	0	588.6616216	2888.6616
96	X	0	X	X	X	X	X	586.0218834	2886.0219
97	X	X	0	0	0	0	0	583.4057143	2883.4057
98	X	X	0	0	0	0	X	580.8128	2880.8128
99	X	X	0	0	0	X	0	578.2428319	2878.2428
100	X	X	0	0	0	X	X	575.6955066	2875.6955
101	X	X	0	0	X	0	0	573.1705263	2873.1705
102	X	X	0	0	X	0	X	570.6675983	2870.6676
103	X	X	0	0	X	X	0	568.1864348	2868.1864
104	X	X	0	0	X	X	X	565.7267532	2865.7268
105	X	X	0	X	0	0	0	563.2882759	2863.2883
106	X	X	0	X	0	0	X	560.8707296	2860.8707
107	X	X	0	X	0	X	0	558.4738462	2858.4738
108	X	X	0	X	0	X	X	556.0973617	2856.0974
109	X	X	0	X	X	0	0	553.7410169	2853.741
110	X	X	0	X	X	0	X	551.404557	2851.4046
111	X	X	0	X	X	X	0	549.0877311	2849.0877
112	X	X	0	X	X	X	X	546.7902929	2846.7903
113	X	X	X	0	0	0	0	544.512	2844.512
114	X	X	X	0	0	0	X	542.2526141	2842.2526
115	X	X	X	0	0	X	0	540.0119008	2840.0119
116	X	X	X	0	0	X	X	537.7896296	2837.7896
117	X	X	X	0	X	0	0	535.5855738	2835.5856
118	X	X	X	0	X	0	X	533.3995102	2833.3995
119	X	X	X	0	X	X	0	531.2312195	2831.2312
120	X	X	X	0	X	X	X	529.0804858	2829.0805
121	X	X	X	X	0	0	0	526.9470968	2826.9471
122	X	X	X	X	0	0	X	524.8308434	2824.8308
123	X	X	X	X	0	X	0	522.73152	2822.7315
124	X	X	X	X	0	X	X	520.6489243	2820.6489
125	X	X	X	X	X	0	0	518.5828571	2818.5829
126	X	X	X	X	X	0	X	516.5331225	2816.5331
127	X	X	X	X	X	X	0	514.4995276	2814.4995
128	X	X	X	X	X	X	X	512.4818824	2812.4819

Calculated values for compensation trimming.

#	X0	X1	X2	X3	X4	X5	X6	R Parallel [Ω]	Value [Ω]
1	0	0	0	0	0	0	0	1870.44	7410.44
2	0	0	0	0	0	0	X	1841.664	7381.664
3	0	0	0	0	0	X	0	1813.76	7353.76
4	0	0	0	0	0	X	X	1786.688955	7326.689
5	0	0	0	0	X	0	0	1760.414118	7300.4141
6	0	0	0	0	X	0	X	1734.90087	7274.9009
7	0	0	0	0	X	X	0	1710.116571	7250.1166
8	0	0	0	0	X	X	X	1686.030423	7226.0304
9	0	0	0	X	0	0	0	1662.613333	7202.6133
10	0	0	0	X	0	0	X	1639.837808	7179.8378
11	0	0	0	X	0	X	0	1617.677838	7157.6778
12	0	0	0	X	0	X	X	1596.1088	7136.1088
13	0	0	0	X	X	0	0	1575.107368	7115.1074
14	0	0	0	X	X	0	X	1554.651429	7094.6514
15	0	0	0	X	X	X	0	1534.72	7074.72
16	0	0	0	X	X	X	X	1515.293165	7055.2932
17	0	0	X	0	0	0	0	1496.352	7036.352
18	0	0	X	0	0	0	X	1477.878519	7017.8785
19	0	0	X	0	0	X	0	1459.85561	6999.8556
20	0	0	X	0	0	X	X	1442.266988	6982.267
21	0	0	X	0	X	0	0	1425.097143	6965.0971
22	0	0	X	0	X	0	X	1408.331294	6948.3313
23	0	0	X	0	X	X	0	1391.955349	6931.9553
24	0	0	X	0	X	X	X	1375.955862	6915.9559
25	0	0	X	X	0	0	0	1360.32	6900.32
26	0	0	X	X	0	0	X	1345.035506	6885.0355
27	0	0	X	X	0	X	0	1330.090667	6870.0907
28	0	0	X	X	0	X	X	1315.474286	6855.4743
29	0	0	X	X	X	0	0	1301.175652	6841.1757
30	0	0	X	X	X	0	X	1287.184516	6827.1845
31	0	0	X	X	X	X	0	1273.491064	6813.4911
32	0	0	X	X	X	X	X	1260.085895	6800.0859
33	0	X	0	0	0	0	0	1246.96	6786.96
34	0	X	0	0	0	0	X	1234.104742	6774.1047
35	0	X	0	0	0	X	0	1221.511837	6761.5118
36	0	X	0	0	0	X	X	1209.173333	6749.1733
37	0	X	0	0	X	0	0	1197.0816	6737.0816
38	0	X	0	0	X	0	X	1185.229307	6725.2293
39	0	X	0	0	X	X	0	1173.609412	6713.6094
40	0	X	0	0	X	X	X	1162.215146	6702.2151
41	0	X	0	X	0	0	0	1151.04	6691.04
42	0	X	0	X	0	0	X	1140.077714	6680.0777
43	0	X	0	X	0	X	0	1129.322264	6669.3223
12	0	X	0	X	0	X	X	1118.76785	6658.7679
45	0	X	0	X	X	0	0	1108.408889	6648.4089
46	0	X	0	X	X	0	X	1098.24	6638.24
47	0	X	0	X	X	X	0	1088.256	6628.256
48	0	X	0	X	X	X	X	1078.451892	6618.4519
49	0	X	X	0	0	0	0	1068.822857	6608.8229
50	0	X	X	0	0	0	X	1059.364248	6599.3642
51	0	X	X	0	0	X	0	1050.071579	6590.0716
52	0	X	X	0	0	X	X	1040.940522	6580.9405
53	0	X	X	0	X	0	0	1031.966897	6571.9669
54	0	X	X	0	X	0	X	1023.146667	6563.1467
55	0	X	X	0	X	X	0	1014.475932	6554.4759
56	0	X	X	0	X	X	X	1005.950924	6545.9509
57	0	X	X	X	0	0	0	997.568	6537.568
58	0	X	X	X	0	0	X	989.3236364	6529.3236
59	0	X	X	X	0	X	0	981.2144262	6521.2144
60	0	X	X	X	0	X	X	973.2370732	6513.2371
61	0	X	X	X	X	0	0	965.3883871	6505.3884
62	0	X	X	X	X	0	X	957.66528	6497.6653
63	0	X	X	X	X	X	0	950.0647619	6490.0648
64	0	X	X	X	X	X	X	942.583937	6482.5839
65	X	0	0	0	0	0	0	935.22	6475.22
66	X	0	0	0	0	0	X	927.9702326	6467.9702
67	X	0	0	0	0	X	0	920.832	6460.832
68	X	0	0	0	0	X	X	913.8027481	6453.8027
69	X	0	0	0	X	0	0	906.88	6446.88

70	X	0	0	0	X	0	X	900.0613534	6440.0614
71	X	0	0	0	X	X	0	893.3444776	6433.3445
72	X	0	0	0	X	X	X	886.7271111	6426.7271
73	X	0	0	X	0	0	0	880.2070588	6420.2071
74	X	0	0	X	0	0	X	873.7821898	6413.7822
75	X	0	0	X	0	X	0	867.4504348	6407.4504
76	X	0	0	X	0	X	X	861.2097842	6401.2098
77	X	0	0	X	X	0	0	855.0582857	6395.0583
78	X	0	0	X	X	0	X	848.9940426	6388.994
79	X	0	0	X	X	X	0	843.0152113	6383.0152
80	X	0	0	X	X	X	X	837.12	6377.12
81	X	0	X	0	0	0	0	831.3066667	6371.3067
82	X	0	X	0	0	0	X	825.5735172	6365.5735
83	X	0	X	0	0	X	0	819.9189041	6359.9189
84	X	0	X	0	0	X	X	814.3412245	6354.3412
85	X	0	X	0	X	0	0	808.8389189	6348.8389
86	X	0	X	0	X	0	X	803.4104698	6343.4105
87	X	0	X	0	X	X	0	798.0544	6338.0544
88	X	0	X	0	X	X	X	792.7692715	6332.7693
89	X	0	X	X	0	0	0	787.5536842	6327.5537
90	X	0	X	X	0	0	X	782.4062745	6322.4063
91	X	0	X	X	0	X	0	777.3257143	6317.3257
92	X	0	X	X	0	X	X	772.3107097	6312.3107
93	X	0	X	X	X	0	0	767.36	6307.36
94	X	0	X	X	X	0	X	762.4723567	6302.4724
95	X	0	X	X	X	X	0	757.6465823	6297.6466
96	X	0	X	X	X	X	X	752.8815094	6292.8815
97	X	X	0	0	0	0	0	748.176	6288.176
98	X	X	0	0	0	0	X	743.5289441	6283.5289
99	X	X	0	0	0	X	0	738.9392593	6278.9393
100	X	X	0	0	0	X	X	734.4058896	6274.4059
101	X	X	0	0	X	0	0	729.9278049	6269.9278
102	X	X	0	0	X	0	X	725.504	6265.504
103	X	X	0	0	X	X	0	721.133494	6261.1335
104	X	X	0	0	X	X	X	716.8153293	6256.8153
105	X	X	0	X	0	0	0	712.5485714	6252.5486
106	X	X	0	X	0	0	X	708.3323077	6248.3323
107	X	X	0	X	0	X	0	704.1656471	6244.1656
108	X	X	0	X	0	X	X	700.0477193	6240.0477
109	X	X	0	X	X	0	0	695.9776744	6235.9777
110	X	X	0	X	X	0	X	691.9546821	6231.9547
111	X	X	0	X	X	X	0	687.977931	6227.9779
112	X	X	0	X	X	X	X	684.0466286	6224.0466
113	X	X	X	0	0	0	0	680.16	6220.16
114	X	X	X	0	0	0	X	676.3172881	6216.3173
115	X	X	X	0	0	X	0	672.5177528	6212.5178
116	X	X	X	0	0	X	X	668.7606704	6208.7607
117	X	X	X	0	X	0	0	665.0453333	6205.0453
118	X	X	X	0	X	0	X	661.3710497	6201.371
119	X	X	X	0	X	X	0	657.7371429	6197.7371
120	X	X	X	0	X	X	X	654.1429508	6194.143
121	X	X	X	X	0	0	0	650.5878261	6190.5878
122	X	X	X	X	0	0	X	647.0711351	6187.0711
123	X	X	X	X	0	X	0	643.5922581	6183.5923
124	X	X	X	X	0	X	X	640.1505882	6180.1506
125	X	X	X	X	X	0	0	636.7455319	6176.7455
126	X	X	X	X	X	0	X	633.3765079	6173.3765
127	X	X	X	X	X	X	0	630.0429474	6170.0429
128	X	X	X	X	X	X	X	626.7442932	6166.7443