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Output-capacitorless segmented low-dropout voltage regulator with controlled pass transistors

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SUMMARY

This article presents a low quiescent current output-capacitorless quasi-digital complementary metal-oxide-semiconductor (CMOS) low-dropout (LDO) voltage regulator with controlled pass transistors according to load demands. The pass transistor of the LDO is segmented into two smaller sizes based on a proposed segmentation criterion, which considers the maximum output voltage transient variations due to the load transient to different load current steps to find the suitable current boundary for segmentation. This criterion shows that low load conditions will cause more output variations and settling time if the pass transistor is used in its maximum size. Furthermore, this situation is the worst case for stability requirements of the LDO. Therefore, using one smaller transistor for low load currents and another one larger for higher currents, a proper trade-off between output variations, complexity, and power dissipation is achieved. The proposed LDO regulator has been designed and post-simulated in HSPICE in a 0.18 μm CMOS process to supply a stable load current between 0 and 100 mA with a 40 pF on-chip output capacitor, while consuming 4.8 μA quiescent current. The dropout voltage of the LDO is set to 200 mV for 1.8 V input voltage. The results reveal an improvement of approximately 53% and 25% on the output voltage variations and settling time, respectively. Copyright © 2015 John Wiley & Sons, Ltd.

KEY WORDS: low-dropout (LDO); output-capacitorless; pass transistor; power management

1. INTRODUCTION

Nowadays, power management is a very important functionality in battery-supplied electronic systems. Advanced power management units for system on chip (SoC) applications need multiple voltage regulators to drive various operational blocks [1, 2]. Usually, low-dropout (LDO) voltage regulators are a part of these power management units that have less output ripple in comparison with switching counterpart circuits. However, in general, they suffer from lower efficiency. The typical structure of an LDO consists of an error amplifier, a pass transistor controlled by the aforementioned error amplifier, a feedback network, and an output capacitor. Most of conventional LDOs use a large off-chip capacitor for stability requirements which cannot be implemented as on-chip capacitors [3, 4]. Although eliminating the off-chip output capacitor carries out some important challenges such as degrading the dynamic performance of the LDO in front of fast load transients, the demand for output-capacitorless LDOs for SoC applications is inevitable [5].

Some papers in connection with output-capacitorless LDOs have been reported in recent years [6–14]. The reported LDO in [6] uses a capacitor multiplier stage to improve the dynamic performance of the

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LDO, at the expense of increasing its power consumption. The LDOs in [7, 8] have simple structure based on the flipped voltage follower (FVF). However, they suffer from weak load and line regulations. In [9], the proposal of an ultra-fast transient response LDO has the problem of significant high quiescent current of 6 mA. Thus, it is not appropriate for low power applications and battery-based devices. The LDO in [10] uses a pole-zero tracking frequency compensation technique in which an adaptive zero implemented by a variable linear resistance cancels the regulator output pole. However, mismatch can degrade the compensation strategy. Nested Miller compensation technique with a programmable capacitor array was used in [11] to provide both good phase margin and control of the damping factor. Nevertheless, the output voltage of LDO changes importantly when the load current changes. In [12], a class AB push–pull amplifier was used as error amplifier of the LDO to source and sink more current for charging and discharging the gate capacitor of pass transistor during the transient event. However, in low power mode, high output voltage deviation due to the improper operation of the error amplifier occurs in the LDO transient response. Additionally, the stability of the regulator goes down significantly for output load current less than 50 μA. The proposed regulator in [13] can switch between two and three stages with respective power transistor, depending on the load demands. Indeed, the main core of the LDO consists of two stages, an error amplifier and a pass transistor. As the load current increases, an auxiliary two-stage cascade structure is added in parallel with the pass transistor to increase the loop gain of the LDO. However, the quiescent current of the LDO is high at full-load condition, and the circuit suffers from poor load and line regulations. Finally, a low quiescent current output-capacitorless LDO regulator based on a high slew-rate current-mode transconductance error amplifier (CTA) is introduced in [14] in which the load transient characteristic of the regulator is improved by enhancing the slew-rate at the gate of pass transistor using a local common-mode feedback technique in the proposed CTA. Nevertheless, the proposed LDO has a 280 mV output voltage variation when the load current changes in a full swing manner.

In addition, recently, some digital LDOs have been reported in [15–17]. The LDO in [15] with 100 nF off-chip output capacitor can deliver only 200 μA current to the load while consuming 2.7 μA quiescent current, considering an array of 256 power transistors. On the other hand, [16] shows a digitally controlled LDO regulator in which the output voltage variation and settling time to the load transient are quite large, namely 700 mV and 1.77 ms, respectively. The quiescent current of the LDO in [17] with off-chip output capacitor of 4.5 nF is 164.5 μA that can discharge fast the battery voltage.

In typical LDO circuits, a very large size pass transistor is used to support the low dropout performance and high current demand of loads. This fact results in a large equivalent capacitance at the gate of pass transistor, thereby impairing the slew-rate at this node. Additionally, because the charge and discharge process of such a large capacitor takes a long time, the feedback loop reaction against fast load variations will be slow. Such a large size device is designed for maximum load current. However, this maximum current is not needed for all times, because the LDO is in standby mode in most of the time [10]. Therefore, it is possible to segment the pass transistor to smaller sizes and adaptively control their action according to the load demands. This paper presents an output-capacitorless LDO in which the control of the pass transistor sizes is carried out in a segmented manner. Section 2 describes the pass transistor segmentation criterion to smaller sizes. The proposed LDO architecture is presented in Section 3. Finally, circuit characterization and conclusions are in Sections 4 and 5, respectively.

2. PASS TRANSISTOR SEGMENTATION CRITERION

Using a large pass transistor creates a large capacitance at its gate terminal, which thus needs long time to charge and discharge. In addition, this capacitance degrades the stability performance at no-load conditions. Therefore, the output voltage variations to load current and/or input voltage transients will be increased; that is, the transient load and lines regulations worsen. Regarding the load transient response, a segmentation or breakdown criterion (*BC*, expressed in *mV/mA*) is defined here, as Eq. (1-a). This is obtained by evaluating the maximum output voltage transient variations due to

the load transient to different load-current variation steps for the maximum size power transistor, in order to find a suitable load-current boundary for segmenting the large pass transistor into smaller ones. The difference between *BC* and load regulation (*LR*) is shown in Figure 1 and Eqs (1-a) and (1-b). It should be noticed that although both of them have the same dimension, *LR* is a metrics for static or steady-state condition while *BC* is for dynamic or transient one.

$$BC = \frac{\text{Maximum Ouput Voltage Variations}}{\text{Load Current Variations}} = \frac{\Delta V_{out2}}{\Delta I_{out}} = \frac{V_1 - V_3}{I_2 - I_1} \tag{1-a}$$

$$\text{Load Regulation } (LR) = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{\Delta V_{out1}}{\Delta I_{out}} = \frac{V_1 - V_2}{I_2 - I_1} \tag{1-b}$$

It should be mentioned that each pass transistor needs its own control circuitry, adding more power dissipation and complexity. As a consequence, notice that a trade-off should be considered between the number of pass transistors, power consumption, and complexity.

Figure 2(a) shows a simple LDO regulator, which consists of a cascode error amplifier with a current buffer compensation scheme, a pass transistor, and a feedback network. Figure 2(b) shows the defined *BC* versus different load current steps for the LDO shown in Figure 2(a) with given transistor dimensions. As it can be seen, the maximum output voltage variation occurs at low load conditions (less than 100 μA). Therefore, this current range is selected as a boundary for segmenting the pass transistor, and one transistor is utilized to cover this current range. Additionally, with regard to Figure 2(b), other steps of load-current variations cause less variations at the output voltage, and so higher load currents can be covered by an alternative pass transistor. Consequently, the designed LDO regulator will have two pass transistors, the second one turning on when the load current is higher than 100 μA.

3. THE PROPOSED LDO ARCHITECTURE

Figure 3 shows the transistor-level schematic of the proposed LDO regulator. Transistors M_1–M_6 implement the cascode error amplifier. Capacitor C_b and transistor M_4 form a current buffer for frequency compensation. R_{f1} and R_{f2} are the feedback network resistors, and C_{out} is the output capacitor. In order to achieve high current efficiency, especially at low load currents, the proposed LDO is designed with a small bias current I_b, and extra bias currents for higher loads are provided through a dynamic biasing carried out by transistor M_7 and load-current sampling network M_8–M_9. Transistors M_{P1} and M_{P2} act as pass transistors and are responsible for delivering current to the load. Transistor M_{P1} sized to 100 μm/0.18 μm is used for low load-current step (less than 100 μA, according to the proposed *BC*), and M_{P2}, with the size of 2000 μm/0.18 μm, provides the current for

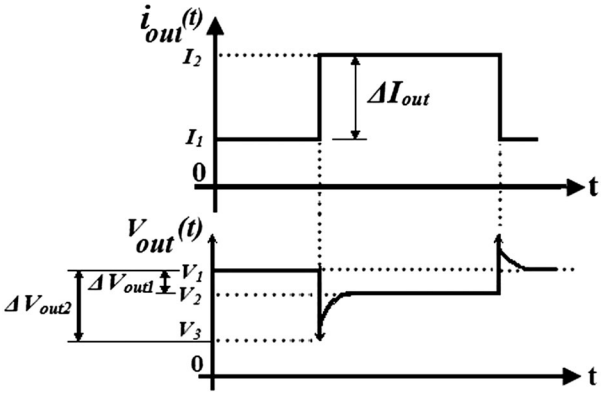
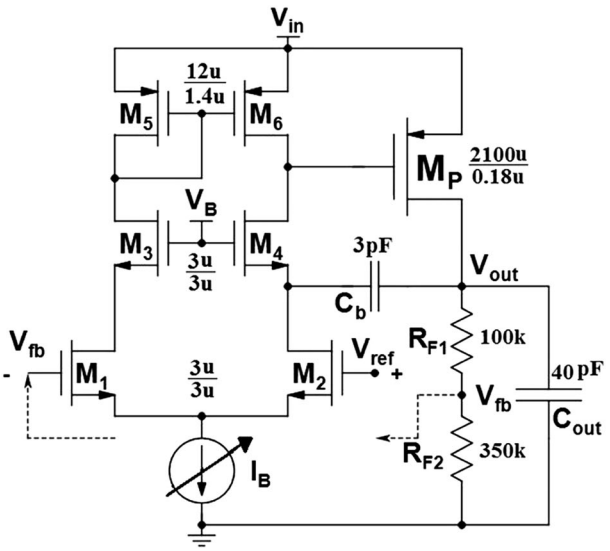


Figure 1. Distinction between breakdown criterion and load regulation.



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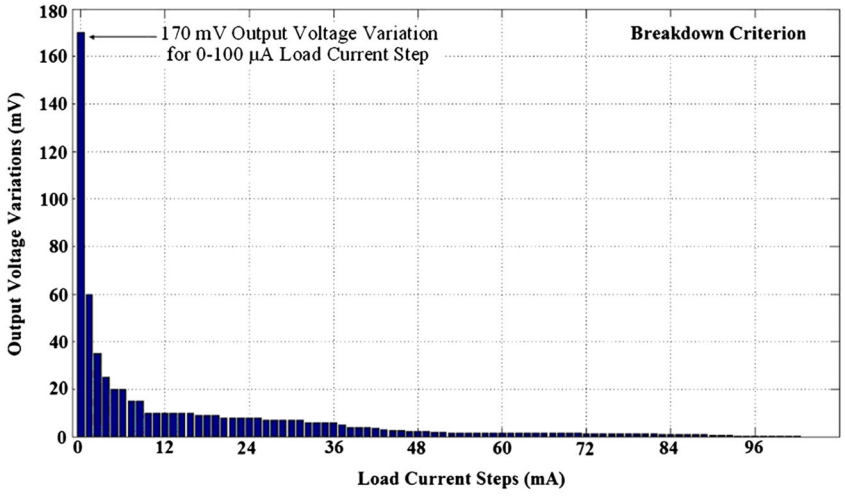


(*b*)

Figure 2. (a) Circuit schematic of the simple low-dropout (LDO) voltage regulator. (b) Breakdown criterion (*BC*) for the LDO of (a).

the loads higher than 100 µA. Transistors M_{12} and M_{13} act as a level shifter to provide a suitable control signal from the error amplifier to the pass transistor M_{P2}. Finally, transistors M_{10} and M_{11} control the second pass transistor gate voltage with respect to the output load current.

The mechanism of voltage regulation is discussed in the following. In case of load-current increase, the output voltage is prone to drop. Thus, the gate-source voltage of M_1 decreases. As a result, the drain current of M_1, M_3, M_5, and M_6 will in turn decrease and that of M_2 and M_4 will be increased, causing the gate voltage of M_{P1} to decrease and more current will source to the load. When the load current crosses the boundary, the gate voltage of M_{10} and M_{11} will be increased through the load-current sampling network (transistors M_8–M_9), and therefore, their drain voltage will drop thereby turning on the second pass transistor M_{P2} to deliver more current to the load. The higher the load current is, the lower the drain voltage of M_{10} and M_{11} will become, and as a result, sufficient current will be delivered to the load through M_{P2}. In no-load conditions, M_{10} is in triode and M_{11} is cut-off. In full-load condition, both transistors are in saturation. An analogous mechanism occurs when the load current decreases.

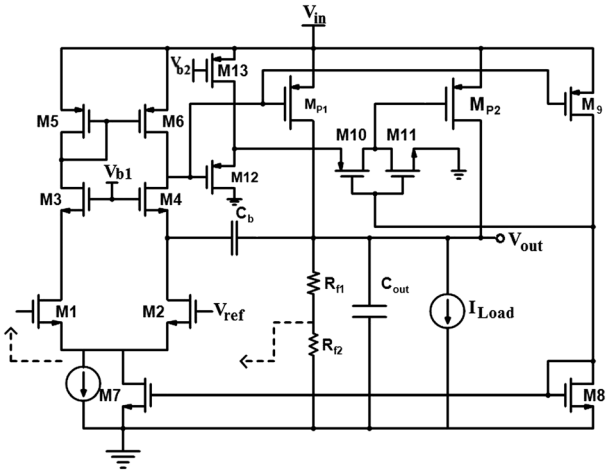


Figure 3. Schematic of the proposed low-dropout regulator.

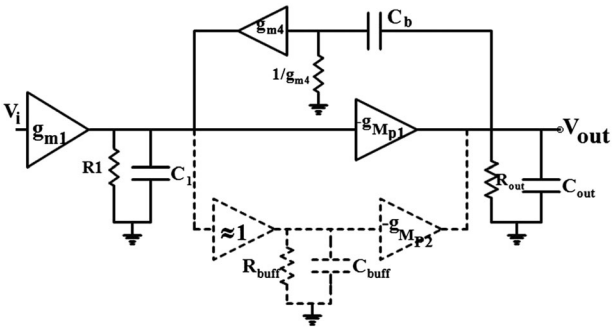


Figure 4. Small signal model of the proposed low-dropout regulator.

Figure 4 shows the small signal model of the proposed LDO regulator in which R_1 and C_1 are the output resistance and equivalent capacitance at the output node of error amplifier, respectively. R_{out} is the output resistance of the LDO which equals $R_{o2} = r_{o,M_{p1}} || (R_{f1} + R_{f2}) || R_{Load}$ for load currents lower than the border line (100 μA, in the considered case) and equals $R_{o3} = r_{o,M_{p1}} || r_{o,M_{p2}} || (R_{f1} + R_{f2}) || R_{Load}$ for larger load currents. Additionally, when the load current is lower than the threshold, the dashed line part will not operate, and, for larger load currents, this part will be added to the circuit and the pass transistor size will be increased. If the level shifter (buffer) stage is designed carefully so that its output pole is exhibited at higher frequencies, this stage can be ignored for small signal analysis, and hence, for higher load currents, the effective transconductance of pass transistors are sum of the g_{mp1} and g_{mp2} that approximately equals g_{mp2} (notice that g_{mp2} is much greater than g_{mp1}). Carrying out small signal analysis on the circuit, the transfer function is given in Eq. (2).

$$H(s) = \frac{-\beta A_0 \left(1 + s\frac{C_b}{g_{m4}}\right)}{\left(1 + sC_b g_{mp} R_1 R_{out}\right)\left(1 + s\frac{C_1 C_{out}}{C_b g_{mp}} + s^2 \frac{C_1 C_{out}}{g_{mp} g_{m4}}\right)}, \tag{2}$$

where the feedback factor (β), DC gain (A_0), pole-zero positions, and unity-gain frequency (ω_T) are as follows:

$$A_0 = g_{m1} g_{mp} R_1 R_{out} \qquad \beta = \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{3}$$

$$P_1 = -\frac{1}{g_{mp} C_b R_1 R_{out}} \qquad Z_1 = -\frac{g_{m4}}{C_b} \qquad \omega_T = \frac{g_{m1}}{C_b} \tag{4}$$

For load currents lower than the boundary, g_{mp1} and R_{o2} are represented, respectively, by g_{mp} and R_{out} in Eqs (3) and (4), while g_{mp2} and R_{o3} are represented for larger load currents. In no-load condition, the pole P_1 is dominant, while the left half plan zero Z_1 is around ω_T, which helps to improve the stability and phase margin of the LDO. Moreover, a pair of complex conjugate poles appears at higher frequencies than ω_T, with the resonance frequency and damping factor as follows:

$$\omega_n = \sqrt{\frac{g_{mp} g_{m4}}{C_1 C_{out}}} \qquad \zeta = \frac{1}{2C_b}\sqrt{\frac{C_1 C_{out} g_{m4}}{g_{mp}}} \tag{5}$$

On the other hand, in full-load condition, the pole P_1 moves slightly while still being dominant, and two other poles are located at frequencies $P_2 \approx -C_b g_{mp}/C_1 C_{out}$ and $P_3 \approx -g_{m4}/C_b$. As it can be observed, the pole P_3 and the zero Z_1 can cancel each other. In addition, the pole P_2 moves to higher frequencies by a factor of C_b/C_1, which guarantees the LDO stability.

Figure 5 shows the open loop frequency response of the proposed LDO regulator with $C_b = 3$ pF and $C_{out} = 40$ pF, confirming that the LDO is stable over the entire load-current range. The phase margins for no-load condition and the current boundary (100 µA, in this case) is the same and equals 101° and for full-load condition is 53°. Additionally, the effect of process variations for three corner cases (slow–slow (ss), typical–typical (tt), and fast–fast (ff)) on the frequency response was explored in Figure 6, and the values of phase margins are listed in Table I, indicating that the LDO has low sensitivity to the process variations. Notice one important point: Conventional LDOs with one maximum size power transistor suffer from lower stability performance and phase margin at no-load condition due to their large size pass transistor which such a large device is not needed in no-load situation (considering that, in addition, the LDO is in standby mode in most of the time). However, the proposed LDO reaches an excellent phase margin in no-load due to using the pass transistor size proportional to the load demanding while maintaining the proper phase margin at full-load condition.

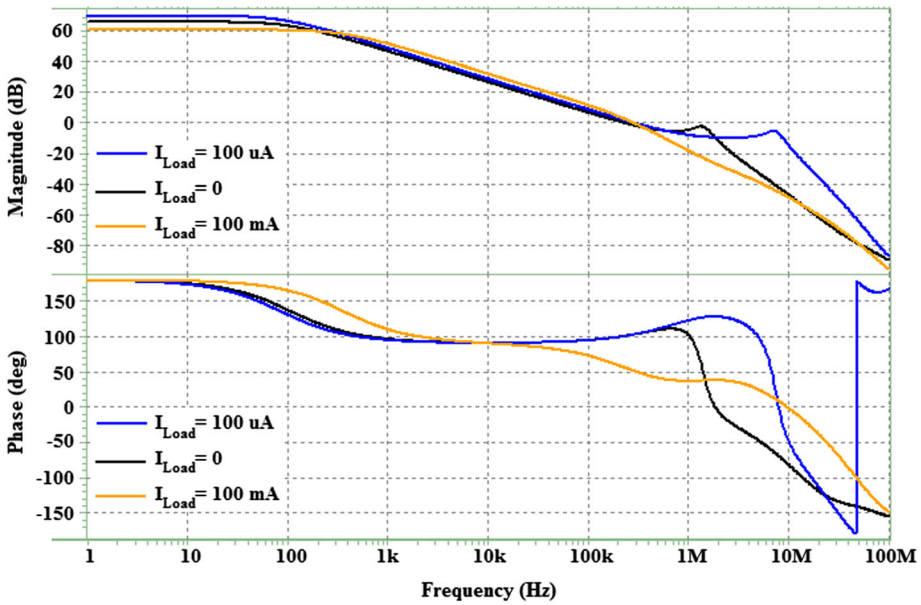


Figure 5. Open loop frequency response of the proposed low-dropout regulator.

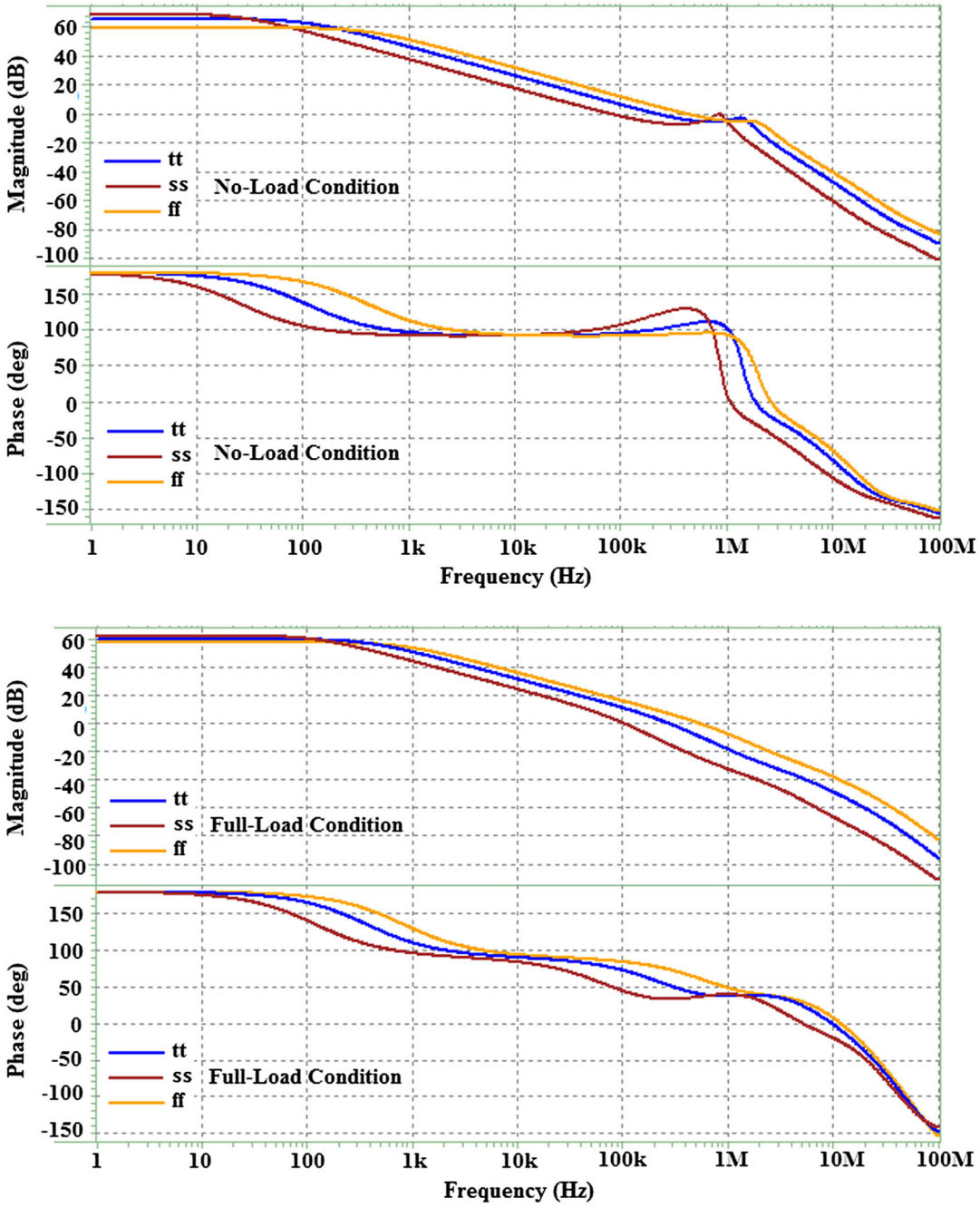


Figure 6. Effect of process variations on the low-dropout regulator stability.

Table I. Phase margin for different process variations.

	Technology		
Phase Margin (°)	ss	tt	ff
No-load	105	101	95
Full-load	47	53	62

ss, slow–slow; tt, typical–typical; ff, fast–fast.

4. POST LAYOUT PERFORMANCE CHARACTERIZATION

The proposed LDO topology has been designed and laid out, as shown in Figure 7, to source a nominal load current between 0 and 100 mA, and the obtained performance metrics correspond to HSPICE post simulations in a 0.18 μm CMOS process. Design parameter values are listed in Table II, where the input transistors sizes are chosen large to reduce the effect of flicker noise and mismatch. The core area of the chip is $369 \times 259\,\mu m^2$. The dropout voltage of the LDO was set to 200 mV for 1.8 V input voltage. The total quiescent current of the LDO at no-load and full-load conditions are 4.8 and 6 μA, respectively. The power supply ripple rejection (PSR) of the LDO at 10 kHz frequency are

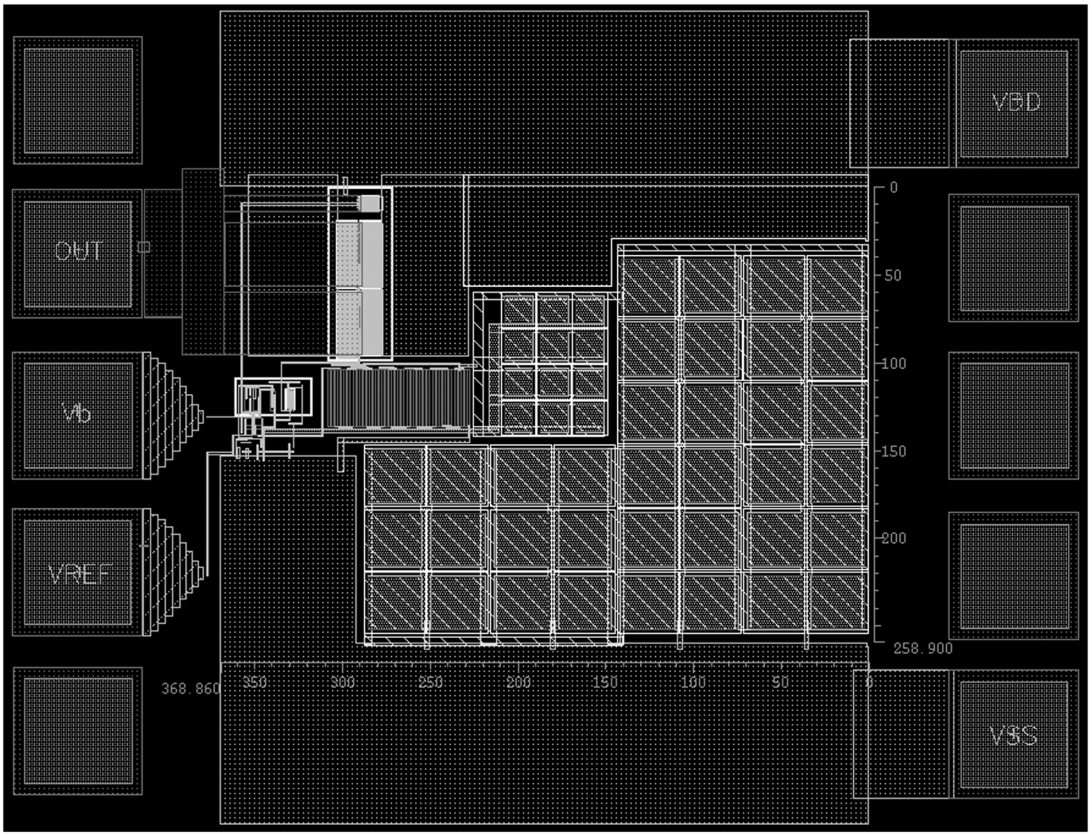


Figure 7. Layout of the proposed low-dropout regulator.

Table II. Design parameter values.

Transistors	W (μm)	L (μm)
M_1–M_4	3	3
M_5, M_6	12	1.4
M_7	2	1
M_8	1	1
M_9	0.4	1
M_{10}	30	0.35
M_{11}	1	0.35
M_{12}	10	0.5
M_{13}	1.5	0.5
M_{P1}	100	0.18
M_{P2}	2000	0.18
R_{f1} and R_{f2}	100 and 350 kΩ	

−61 and −37 dB under no-load and full-load conditions, respectively. In addition, the load and line regulations are 0.015 mV/mA and 0.2 mV/V, respectively.

Figure 8 shows the output voltage transient response of the LDO with and without applying the segmentation technique for different load-current changes. The rise and fall time for 0–100 mA load-current changes is 1 µs and that for other load-current changes is a fraction of 1 µs corresponding to the load changes. In the figures, label '1 power transistor' corresponds to the LDO without using the segmentation method that applies the maximum size power transistor needed for delivering the maximum load, while label '2 power transistors' corresponds to the proposed LDO with the segmented pass transistors. It is observed that the maximum output voltage deviation from its target is approximately 53% lower in case of using the segmentation technique, and the settling time is faster, approximately 25% with segmented pass transistors. Additionally, the load regulation has been better especially at higher load currents.

A comparison between quiescent current of the LDO with and without using the proposed technique is shown in Figure 9. It can be seen that using the proposed segmentation technique decreases the quiescent current, significantly.

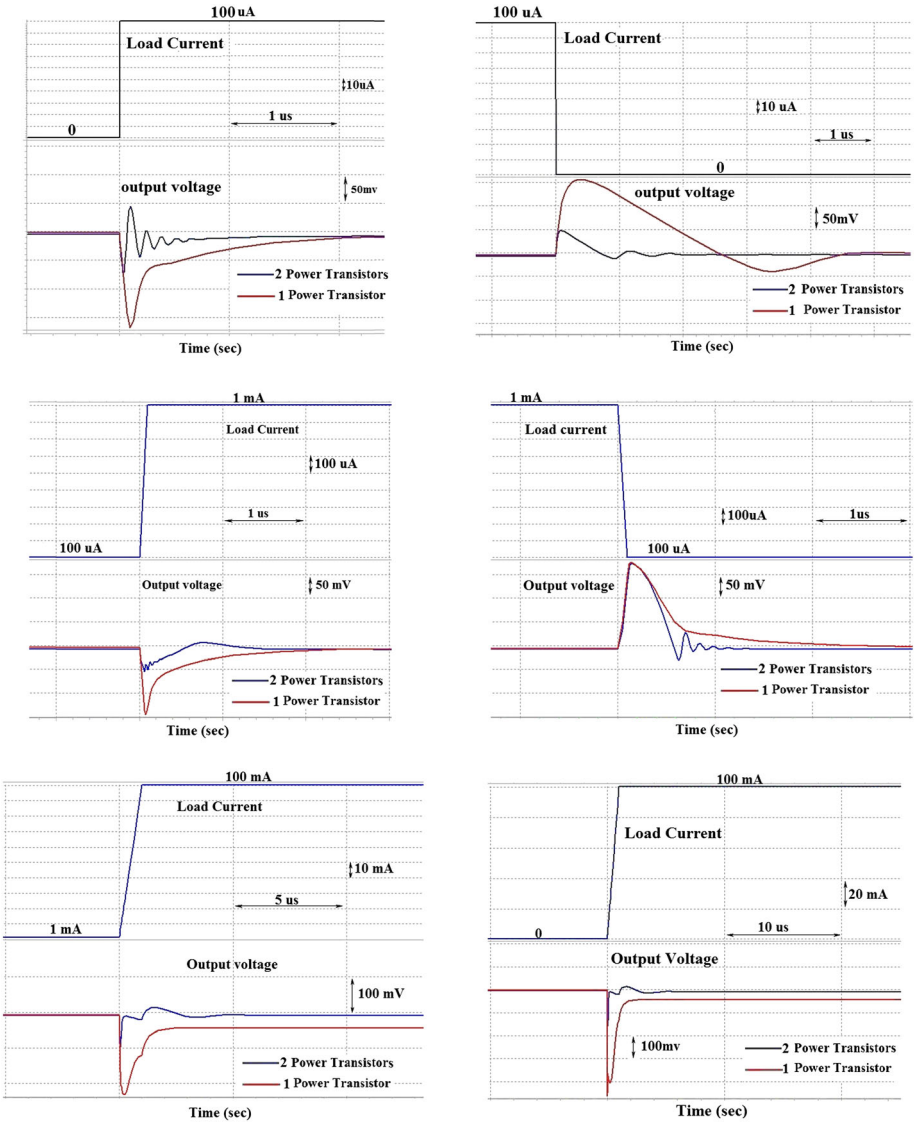


Figure 8. Load transient response of the low-dropout regulator with and without the segmentation technique for different load-current changes.

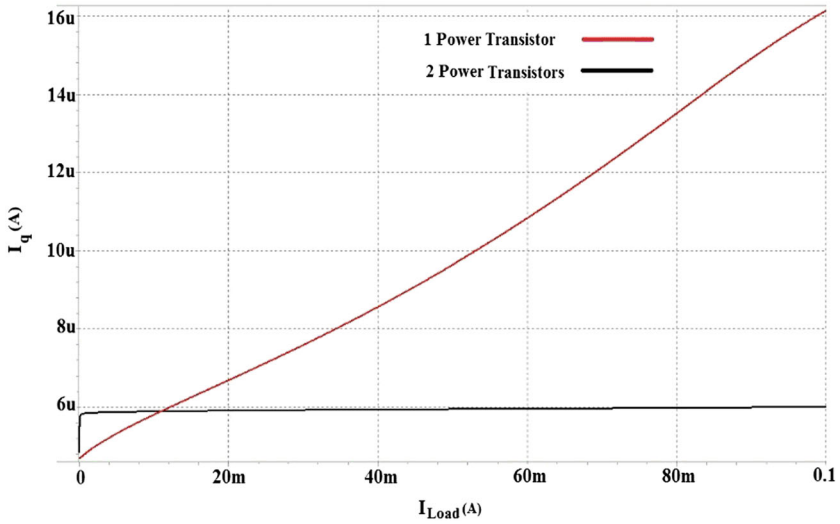


Figure 9. Comparison between quiescent current of the low-dropout regulator with and without the segmentation technique.

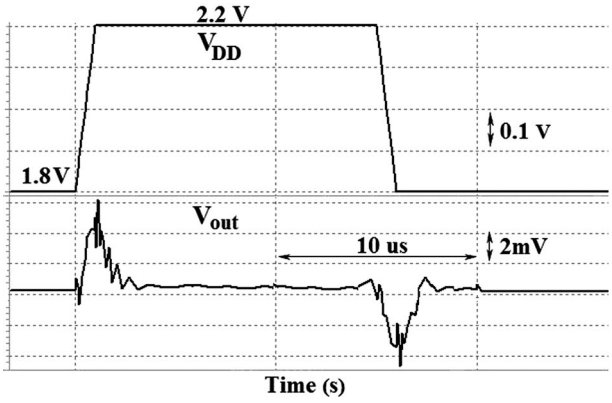
Line transient response of the proposed LDO is shown in Figure 10, in which the line voltage changes between 1.8 and 2.2 V with rise and fall times of 1 µs. It demonstrates that the maximum output voltage variation is only 6 mV in low load currents and about 140 mV in high load currents, and its maximum settling time is 2 µs.

The effect of process variations on the quiescent current, load, and line regulations of the proposed LDO are shown in Figures 11–13, respectively. Furthermore, the effect of temperature variation on the output voltage of the LDO with and without the segmented pass transistors is illustrated in Figure 14. The temperature was swept in the range of −20 to 70 °C, and, as it can be seen, under this temperature range, the output voltage variation under no-load condition is only 0.5 mV in case of using the segmentation technique that is three times lower than that without using this method.

The output noise power spectral density of the proposed LDO versus frequency is demonstrated in Figure 15. The spot noise at DC frequency is 1.3 nV^2/Hz and 960 pV^2/Hz at no-load and full-load conditions.

Monte Carlo analysis was performed on the proposed LDO in order to consider the effect of channel length mismatch between input transistors of the error amplifier and also the threshold voltage mismatch of all transistors on the output DC voltage. Figures 16 and 17 demonstrate the output DC voltage histogram for ±5% tolerance with a Gaussian distribution and 50 iterations on the channel length of input transistors of the error amplifier (M_1 & M_2) and active load of the error amplifier (M_5 & M_6), respectively. The horizontal and vertical axes indicate the deviation from the ideal output voltage and the number of iterations that a specific deviation happens, respectively. As it can be seen, ±5% tolerance on the channel length of input transistors of the error amplifier causes that 2% of samples have the maximum deviation that is equal to ±0.25% error from the ideal output voltage level. Furthermore, the maximum deviation from the ideal output voltage level due to the ±5% tolerance on the channel length of active load transistors is the same ±0.25% error which occurs on 8% of samples. Additionally, the output DC voltage histogram for a tolerance on the threshold voltage of all transistors based on the Pelgrom's model [18] with a Gaussian distribution and 50 iterations is illustrated in Figure 18, in which 6% of samples have the maximum deviation equal to ±0.56% error from the ideal output voltage level.

Dynamic power dissipation comparison of the LDO with and without the segmented pass transistors is shown in Figure 19. The power dissipation is defined as difference between the total power sunk from the supply voltage and the power delivered to the load. As it can be seen, in the steady-state condition, the power dissipation of the LDO with segmented pass transistors is less than that without segmented ones due to its less quiescent current. Furthermore, during the load transition, the LDO with segmented pass transistors saves the power dissipation of approximately 50%, which is due to its lower output voltage deviation during the load transients.



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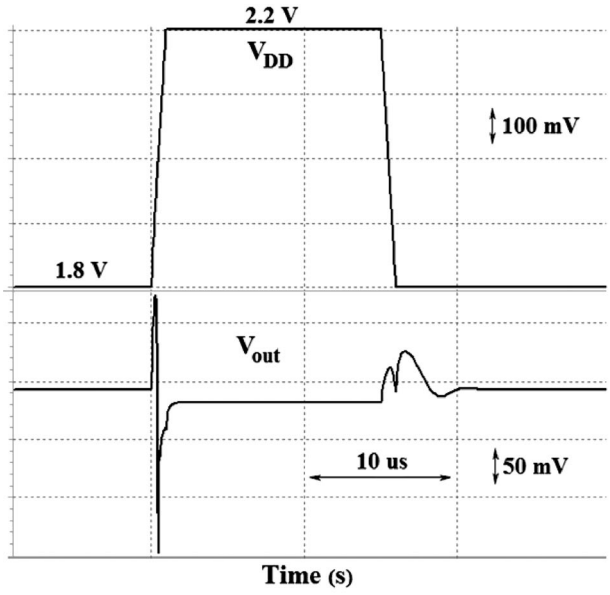

(*b*)

Figure 10. Line transient response of the proposed low-dropout regulator for (a) $I_{Load} = 100\,\mu A$ and (b) $I_{Load} = 100\,mA$.

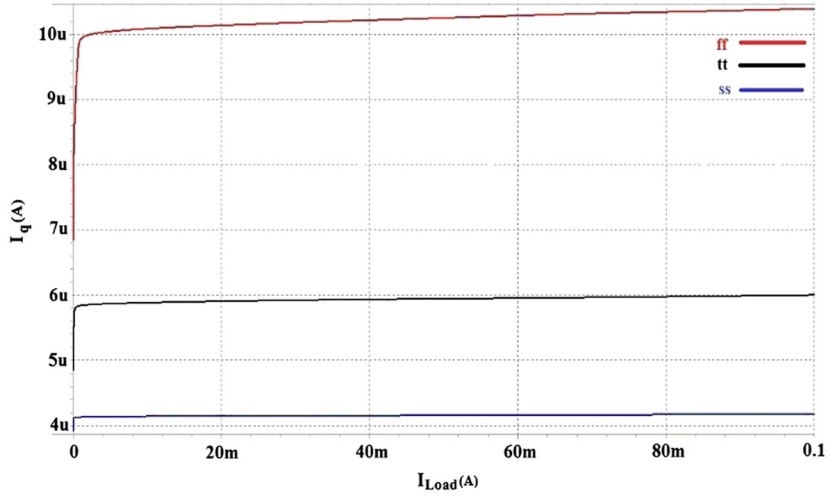

Figure 11. Effect of process variations on the quiescent current of the low-dropout regulator.

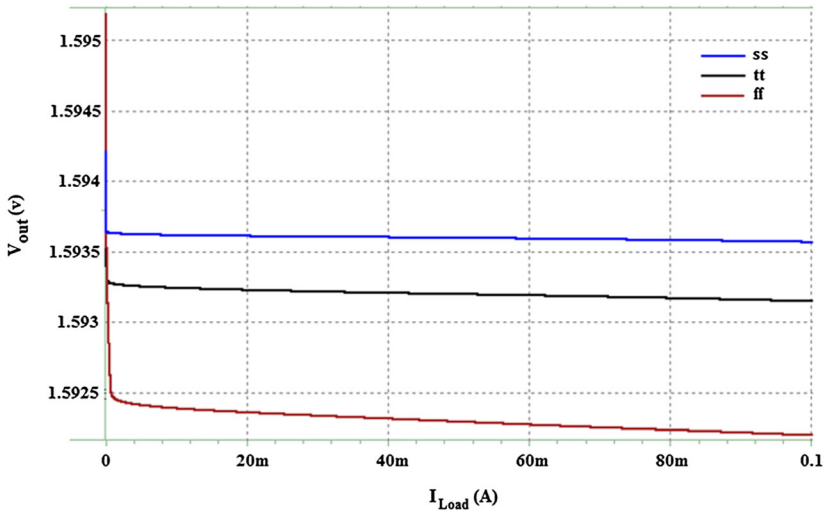

Figure 12. Effect of process variations on the load regulation of the low-dropout regulator.

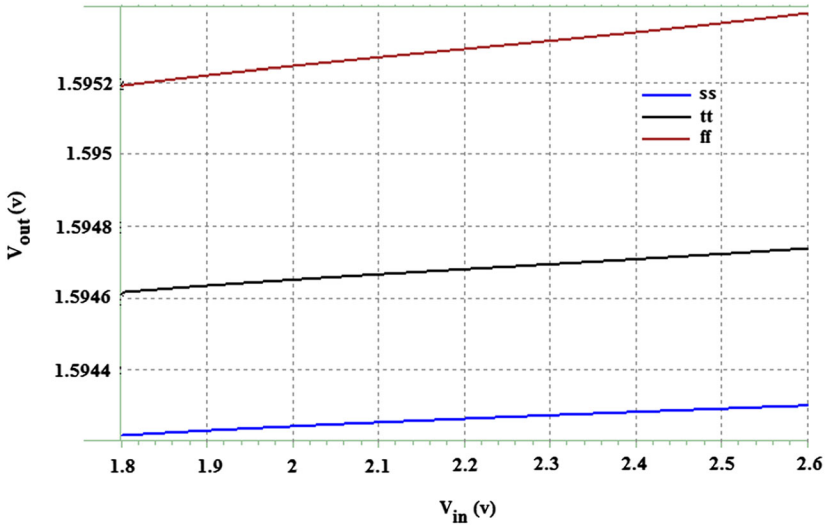

Figure 13. Effect of process variations on the line regulation of the low-dropout regulator under no-load condition.

Table III provides a benchmark performance comparison between the proposed LDO and recent works. In order to have a fair coherent comparison, other LDOs are simulated in HSPICE with the parameters mentioned in the papers, and the table results correspond to their both simulation and experimental characterization. For the proposed LDO, the results with and without controlling the pass transistor are included, and the worst case for output voltage variation (ΔV_{out}) and settling time (T_{settle}) is considered. As it can be seen, both the output voltage variation and settling time will be enhanced with controlling the pass transistor. The figure of merits ($FOM_1 = \Delta V_{out} C_{out} I_Q / I^2_{out,\max}$ and $FOM_2 = t_{settle} I_Q / I_{out,\max}$) used in [9,19], respectively, are adopted here to compare the transient response of different LDOs. Lower FOMs imply better transient operation achieved by the LDO. As it can be seen, controlling the power transistor size with regard to the load current leads to better transient performance. Furthermore, the proposed LDO with segmented power transistor has the lowest FOM_1 that is due to the segmentation technique resulting in less output voltage deviation and low quiescent current, simultaneously, while the LDOs with ΔV_{out} lower than the proposed one [6,20] have more quiescent current, or the LDOs with lower quiescent current [12,14] have higher

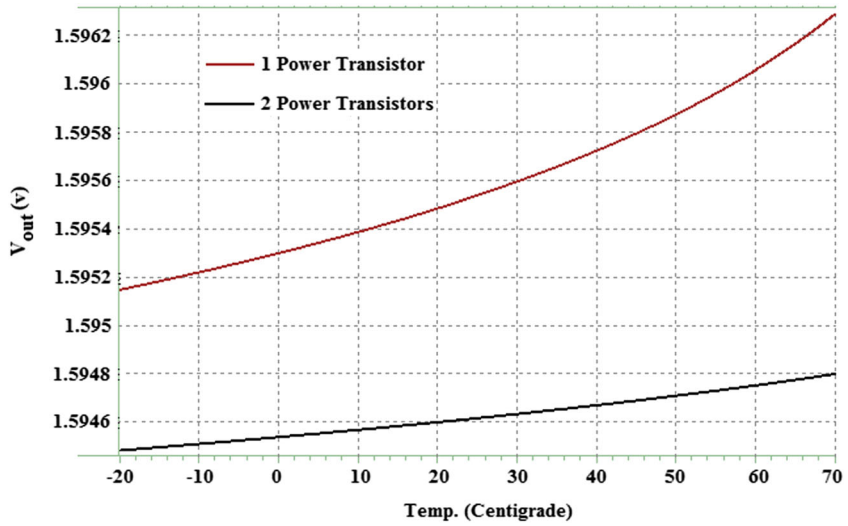

Figure 14. Effect of temperature variation on the output voltage of the low-dropout regulator under no-load condition with (2 power transistors), and without (1 power transistor) the segmentation technique.

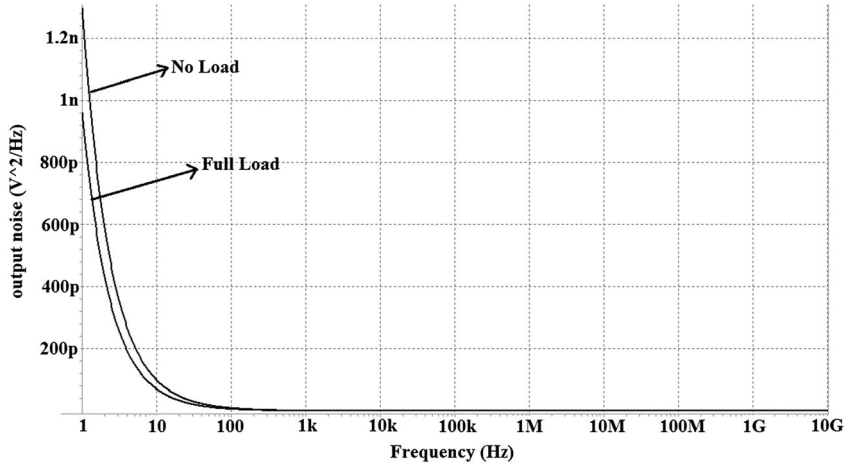

Figure 15. Noise characteristic of the proposed low-dropout regulator.

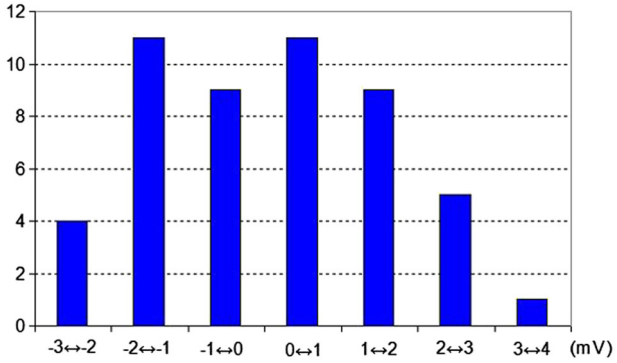

Figure 16. Histogram of the output voltage level for ±5% tolerance on the length of transistors M_1 & M_2. The horizontal and vertical axes indicate the deviation from the ideal output voltage and the number of iterations that a specific deviation happens, respectively.

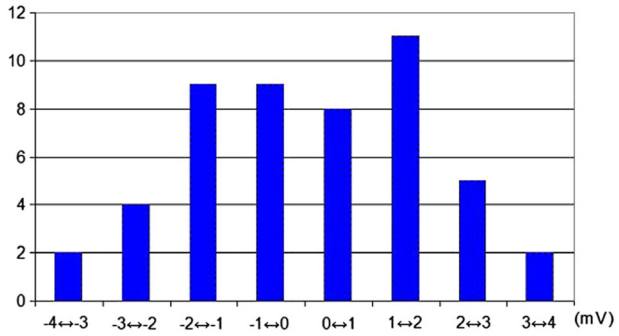

Figure 17. Histogram of the output voltage level for ±5% tolerance on the length of transistors M_5 & M_6. The horizontal and vertical axes indicate the deviation from the ideal output voltage and the number of iterations that a specific deviation happens, respectively.

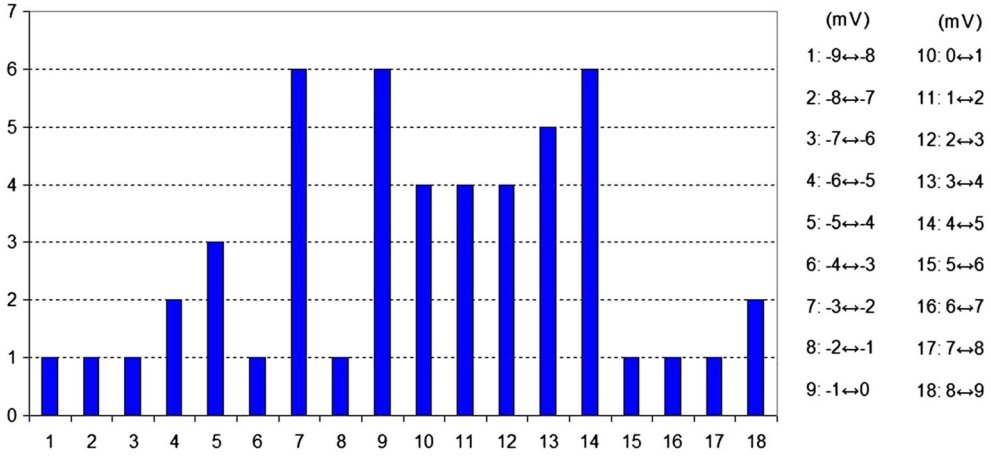

Figure 18. Histogram of the output voltage level for a tolerance on the threshold voltage of all transistors based on Pelgrom's model. The horizontal and vertical axes indicate the deviation from the ideal output voltage and the number of iterations that a specific deviation happens, respectively.

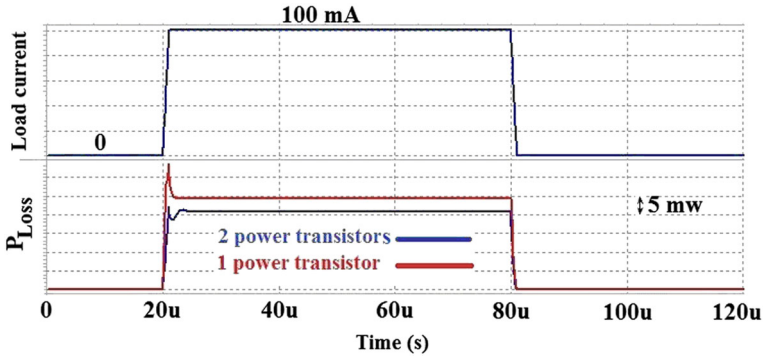

Figure 19. Comparison between dynamic power dissipation (P_{Loss}) of the low-dropout regulator with and without the proposed segmentation technique for load-current changes between 0 and 100 mA.

output voltage deviation. Additionally, the segmentation technique causes that the proposed LDO reaches one of the lowest FOM_2 due to simultaneously lower settling time and quiescent current. Just the LDO in [12] has lower FOM_2 than the proposed one due to its lower quiescent current, but its output voltage deviation is quite large, approximately 41% of its DC output voltage level.

Table III. Performance summary and comparison.

											This work	
Parameter	[6] Exp.	[6] Sim.	[7] Exp.	[7] Sim.	[12] Exp.	[12] Sim.	[14] Sim.	[16] Sim.	[20] Exp.	[20] Sim.	Without control	With control
Tech (μm)	0.35	0.35	0.35	0.35	0.18	0.18	0.18	0.35	0.35	0.35	0.18	0.18
V_{in} (V)	3	3	1.2	1.2	1.2	1.2	1.2	0.9	1.8	1.8	1.8	1.8
V_{out} (V)	2.8	2.8	1	1	1.1	1	1	0.7	1.6	1.6	1.6	1.6
I_{out} (mA)	50	50	50	50	50	50	100	50	100	100	100	100
I_Q (μA)	65	66	95	95	1.2	1.2	3.7	4.7	20	20	4.7 (no-load)	4.8 (no-load)
C_{out} (pF)	100	100	>20	20	100	100	100	100	100	100	40	40
T_{settle} (μs)	≈15	≈4	≈0.3	≈1.4	≈3	≈4.4	≈6	1.77 ms	≈9	≈8	≈4.5	≈4
ΔV_{out} (mV)	90	110	≈180	200	≈450	490	277	700	97	100	460	170
CE (%)	99.87	99.86	99.81	99.81	99.99	99.99	99.99	99.9	99.98	99.98	99.99	99.99
FOM1 (*fs*)	234	290	136	152	21.6	23.5	10.2	131.6	19.4	20	8.6	3.3
FOM2 (*ns*)	19.5	5.28	0.57	2.66	0.07	0.11	0.22	166.38	1.8	1.6	0.21	0.19

5. CONCLUSION

This paper has presented an output-capacitorless segmented CMOS LDO regulator. The pass transistor of the LDO is segmented into two smaller sizes, one for low currents and another one for high currents, based on a breakdown criterion which considers the maximum output voltage transient variations due to the load transient to different load current steps. Post-layout simulation results in a 0.18 μm CMOS process show approximately 53% and 25% improvement on the output voltage variations and settling time, respectively, in comparison with the case that the power transistor is used in its maximum size. Furthermore, a comparison between quiescent current of the LDO with and without using the proposed technique shows that using the proposed segmentation technique significantly decreases the quiescent current as a function of load current. An FOM-based comparison with other reported regulators indicate that the proposed LDO with segmented pass transistors has reached low output voltage transient deviations, settling time, and quiescent current, simultaneously with an on-chip output capacitor of 40 pF.

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