ELE539 Project
Band-Gap Reference Circuit
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Bandgap Reference Circuit

The goal of the project has been to understand the functionality of Bandgap reference circuit(s) and to verify the performance using HSPICE.

Purpose of Bandgap reference circuit:
A Bandgap reference circuit provides a constant dc voltage that is immune to temperature variations, noise, power drawn, and supply voltage fluctuations.

Motivation:

- Bandgap reference circuits operate on a very simple principle, yet has a lot of applications.
- Widely used in ADC, DAC, and voltage regulators.
- It is an essential component in data acquisitions. The conversion accuracy is dependent on the stability of the reference voltage.
- Personal interest to learn about Bandgap reference circuits

Commercial Bandgap chips available:
Several commercial Bandgap reference chips are available. The following are a few examples:

- Faraday – FXBG020H90
- Analog IP Cell
- Analog Devices ADR130
- MAXIM MAX131 - 31/2 Digit ADC with Bandgap Reference

Summary of the project:
Three topologies, shown in the following figure were implemented and verified in HSPICE, and the results are summarized in the following tables 1, 2, 3.

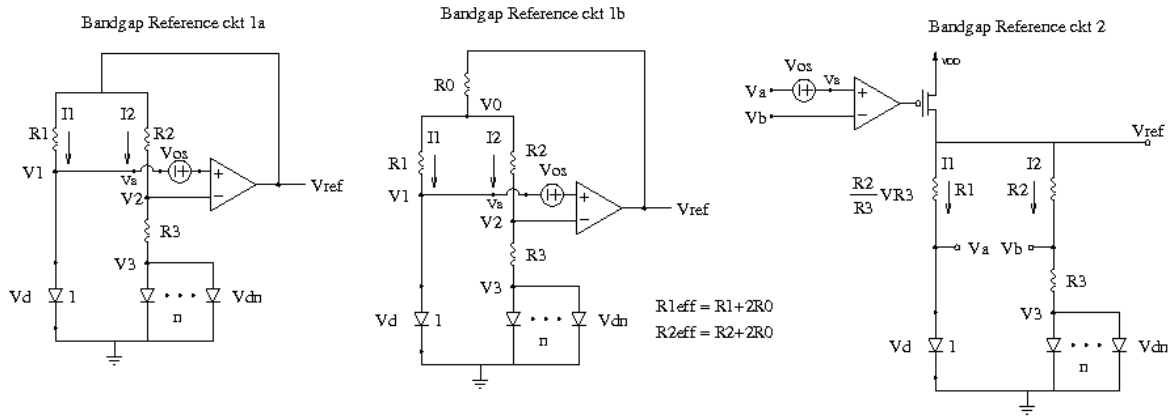


Table-1 shows the resistor and p-channel transistor values. Table-2 compares the deviations in the topologies with different parameters. Table-3 compares the performance of the topologies when resistors were halved, while keeping ratio constant.

	Values (resistor/p-channel) used				
Topology	M1 (W/L)	R0	R1	R2	R3
1(a)			400K	400K	54K
1(b)		150K	100K	100K	54K
2	60/6		400K	400K	54K

Table 1 shows the resistor and p-channel transistor values

	Deviation with respect to			
Topology	Temperature -25°C to 125 °C	Power supply 2.7V to 3.4V	Offset +269.2µV	Diode parameter Is from 10f-20f (at room temp)
1(a)	12.8mV	0.2mV	2.4mV	21mV
1(b)	12.4mV	0.25mV	3.2mV	21mV
2	20.8mV	0.3mV	2.5mV	20.4mV

Table 2 comparison of the deviations in the topologies with different parameters

		Topology 1a				Topology 1b				Topology 2			
		Deviation due to				Deviation due to				Deviation due to			
Offset voltage **	Resistors used	temperature -25 to 125°C (mV)	resistors at -25 and 125°C (mV)		Average Power over temp (µW)	temperature -25 to 125°C (mV)	resistors at -25 and 130°C*(mV)		Average Power over temp (µW)	temperature-25 to 130°C *(mV)	resistors at -25 and 130°C*(mV)		Average Power over temp (µW)
269uV	Actual version	12.8			199.21	12.4			199.21	20.8			16.8
	Halved version	23.6	16.7	27.5	199.21	21.9	16.5	25.9	199.21	32.8	16.5	28.5	22.1
538uV	Actual version	12.8				12.4				20.9			
	Halved version	23.6	16.7	27.5		21.9	16.5	25.9		32.9	16.5	28.5	

Table 3 compares the performance of the topologies when resistors were halved, while keeping ratio constant

* The upper limit value was calculated at 130°C, but the values are reasonably constat from 125°C to 130°C.
** The opamp has an offset voltage of 269uV.

When the resistance values were reduced to half, there was no change in the power of the topologies (with the resistances I used) except for topology 2. There was a power (average) difference of about 5.325µW (figure 30, page 32).

Results are shown in more detail after each plot, pages 22-33.

Comparison of the results of the three circuits:

- All the three topologies have similar performance.
- The advantage of topology 1b over 1a and 2 is: For the implemented resistance values, the total resistance of topologies 1a and 2 is 854 KΩ, where as for topology 1b it is only 404 KΩ. Hence, it is the most area efficient solution.
- The advantage of topology 2 over 1a and 1b is: The opamp has to drive only the p-channel device. In topologies 1(a) and 1(b), the opamp should drive the output load, which could be huge.
- HSPICE simulations reveal that topology 2 has less the output impedance than topologies 1a and 1b. Therefore it can be concluded that topology 2 has a better driving capability.
- The Average power of topology 2 was found to be 16μW, while topologies 1a and 1b were 199.21μW.

The Key Performance parameters of the opamp used for the project were the following:

- offset voltage: 269.2μV
- The phase margin: 52°.
- Unity Gain bandwidth: 11.8MHz
- Gain: 10K
- Poles are located at 1630Hz and 25.1MHz
- The open loop output impedance is 461KΩ

Outline of the report
Section 1: Introduction to voltage reference
Section 2: Theory of Bandgap Ref Circuit
Section 3: The topologies implemented and verified in HSPICE
Section 4: Opamp section
Section 5: HSPICE simulation results
Section 6: Summary

Section 1: Introduction to voltage reference

Reference voltage generators are used in DRAM's, flash memories, and analog devices. The generators are required to be stabilized over process, voltage, temperature variations, and also to be implemented without modification of the fabrication process.

An important part in the design of analog integrated circuits is to create reference voltages and currents with well defined values. To accomplish this on-chip, Bandgap reference circuits are commonly used. These circuits allow the design of temperature independent reference voltages. A typical application for this reference voltage is in analog to digital conversion, where the input voltage is compared to several reference levels in order to determine the corresponding digital value.

Different ways of implementing voltage reference circuits:

- The most common approach: use of a Zener diode that breaks down at a known voltage when reverse biased. Disadvantage: The breakdown voltage of the Zener diode is larger than the power supplies used in most of the modern circuits. Therefore, this approach is not popular now-a-days.
- Making use of the threshold voltage of an MOS device: The voltage generated is independent of the supply voltage, but Vt varies with temperature
- Making use of the threshold voltage between an enhancement transistor and a depletion transistor: This technique cannot be used in CMOS technology because depletion transistors are not available. Instead, threshold voltage of a p and n-channel device can be used.
- Cancelling the negative temperature dependence of a p-n Junction with a positive temp dependence (proportional to absolute temperature voltage, PTAT) circuit. (Principle of Bandgap Reference circuits)

(a) Zener diode: Making use of a Zener diode that breaks down at a specific reverse junction voltage. The following figure shows the configuration using a Zener diode.

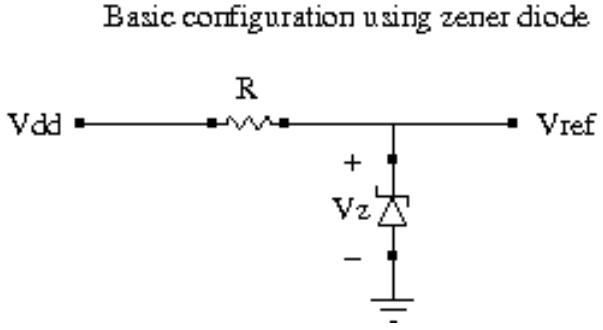


Figure 1Voltage Reference using Zener diode

Disadvantage: The breakdown voltage of the zener diode is larger than the power supplies used in most of the modern circuits. Therefore, this approach is not popular now-a-days.

(b)Making use of the threshold voltage of an MOS device. The implementation is as shown in the following figure:

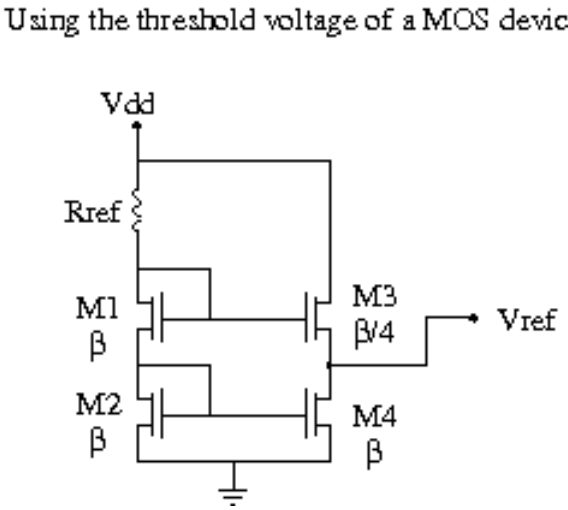


Figure 2 Voltage reference using threshold voltage of a MOS device

$$V_{ref} = V_{t1} + V_{eff1} + V_{t2} + V_{eff2} - V_{t3} - V_{eff3}$$

If the width of M3 is about 4 times smaller than the width of the other three devices

$$V_{ref} \cong V_{t1} + V_{t2} - V_{t3} \cong V_{t2}$$

Advantage: V_t is independent to the Supply voltage fluctuations
Disadvantage: V_t does vary with temperature

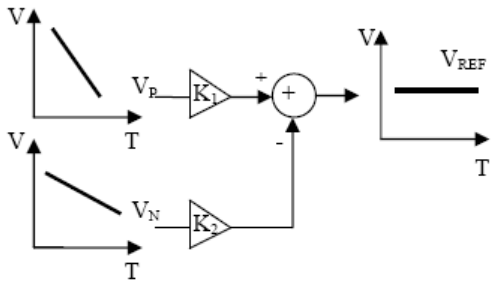
$$V_{tn} = V_{FB} + 2\Phi_{Fn} + \frac{1}{C_{ox}}\sqrt{2\Phi_{Fn} 2\varepsilon_s q N_A}$$

$$\Phi_F = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right)$$

$$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2}\left(m_n^* m_p^*\right)^{3/4} e^{-\frac{E_c - E_v}{2kT}}$$

Where k – Boltzmann constant 1.38065×10^{-23} J/°K
q- Electric charge $1.6 * 10^{-19}$ As
V_t – threshold voltage
V_{FB}-Flatband voltage
Φ_{Fn}-Fermi potential
C_{ox} – ε_{ox}/t_{ox} where t_{ox} -thickness of the oxide layer
ε_{ox}- permittivity of the oxide layer
ε_s- Relative permittivity
N_A- p-substrate doping concentration
m_n^* m_p^* - effective mass of electron and hole
h – plank's constant 6.63×10^{-34} Js
n_i – intrinsic carrier concentration of silicon ($1.5 * 10^{10}$ cm^{-3})

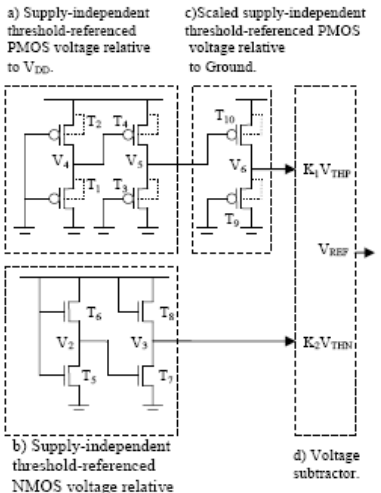
(c) Making use of the threshold voltage between enhancement transistor and a depletion transistor: This technique cannot be used in CMOS technology because depletion transistors are not available. Instead, threshold voltage of a p and n-channel devices can be used. The following figure shows the concept of this technique [9].



Voltage reference concept.

A subtraction of two threshold voltages may result in the cancellation of temperature-sensitive parameters of the threshold voltages. Therefore, threshold-voltage subtraction can be used for the design of CMOS voltage reference.

Figure 3 threshold voltage of using p and n-channel devices – concept[9]



Transistors	Size [μM/μM]
T1	98/12
T2,T6,T8,T9	12/12
T3	20.5/12
T4	36/12
T5	4/12
T7	48/12
T10	28/12

(d)The Bandgap reference (BGR) is one of the most popular reference voltage generators that generates a temperature independent voltage. This method involves the generation of a voltage with a positive temperature coefficient. The base-emitter voltage, V_{BE}, has a negative temperature coefficient. Therefore, when the two voltages are added together, the sum has a zero temperature coefficient. For silicon, this is achieved when the total voltage equals roughly 1.22V. This value is the Bandgap voltage of silicon. Hence, this method is called Bandgap reference.

Section 2: Theory – Bandgap Reference Circuit

In a conventional Band Gap Circuit, the output voltage is the sum of the built-in voltage of the forward biased (Base-emitter) diode which has a negative temperature coefficient and a voltage proportional to the absolute temperature (PTAT), which is the thermal voltage multiplied by a constant.

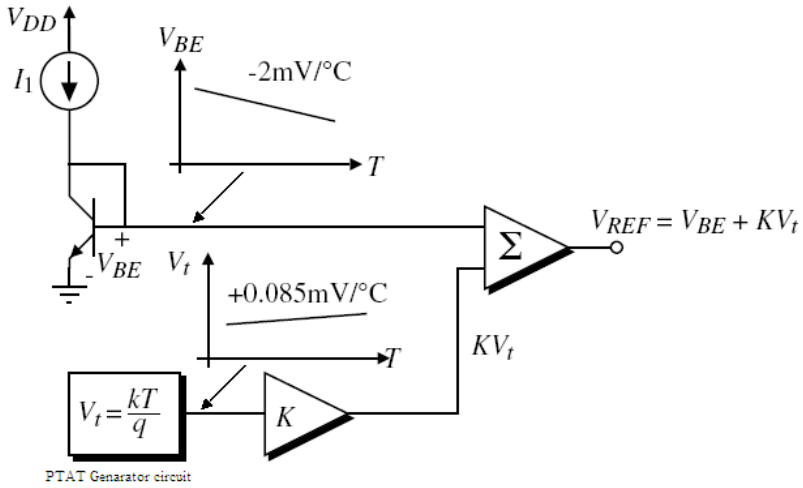


Figure 4 Basic Principle of a Bandgap Reference circuit

A forward biased base-emitter junction of a bipolar transistor is a forward biased p-n Junction. A general diode current versus voltage relation is expressed as:

$$I_d = I_s\left[e^{\left(\frac{qV_d}{KT}\right)} - 1\right]$$

$$I_d \approx I_s e^{\left(\frac{qV_d}{KT}\right)} \rightarrow (eqn1a)$$

$$V_d = \frac{kT}{q}\ln\left(\frac{I_d}{I_s}\right) \rightarrow (eqn1b)$$

Where k – Boltzmann constant 1.38065x10^{-23} J/°K

q- Electric charge 1.6*10^{-19} As

Is – Reverse saturation current

Id, Vd – diode current and voltage

Similarly for base-emitter junction

$$I_c \approx I_s e^{\left(\frac{qV_{be}}{KT}\right)}$$

$$V_{be} = \frac{kT}{q}\ln\left(\frac{I_c}{I_s}\right)$$

$$I_c = GT^{\alpha}$$

$$I_s = BT^{4-n} e^{-\frac{V_{Go}}{V_{TH}}}$$

Where V_{GO} - Bandgap voltage extrapolated to $0^oK \approx 1.2V$

n - Depends on the doping level in Base ≈ 3/2

α is typically in-between 0 and 1

V_{TH} Thermal voltage = kT/q ≈ 26mV at room temperature

G and B are proportionality constants

$$V_{be} \cong V_{TH} \ln\left(\frac{GT^{\alpha}}{BT^{4-n} e^{-\frac{V_{Go}}{V_{TH}}}}\right)$$

$$V_{be} \cong V_{TH} \ln\left(\frac{G}{B} T^{-(4-n-\alpha)} e^{\frac{V_{Go}}{V_{TH}}}\right)$$

$$V_{be} = V_{Go} - V_{TH}\left((4-n-\alpha)\ln T - \ln\left(\frac{G}{B}\right)\right) \rightarrow (eqn\,2)$$

Output voltage after summer, as shown in figure (4), is given by the following equation:

$$V_{ref} = V_{be} + V_{TH} K \rightarrow (eqn\,3)$$

By substituting equation (3) in equation (2), we get:

$$V_{ref} = V_{Go} - V_{TH}(4-n-\alpha)\ln T + V_{TH}\left(K + \ln\frac{G}{B}\right) \rightarrow (eqn\,4)$$

In order to determine the constants, such that V_{ref} is temperature independent, we should set the derivative of V_{ref} with respect to temperature to zero at $T=T_0$ $\left.\frac{dV_{ref}}{dT}\right|_{T=T_0} = 0$. The result obtained is given by the following equation:

$$V_{ref} = V_{Go} + V_{TH}(4-n-\alpha)\left[1 + \ln\frac{T_0}{T}\right] \rightarrow (eqn5)$$

In the above equation V_{GO} dominates, the second term is on the order of few mill volts. Therefore V_{ref} is approximately equal to $V_{GO,}$ the Bandgap voltage of silicon. Hence, this is called Bandgap reference circuit.

To determine the temperature dependence of the output voltage $V_{ref,}$ [from notes (page VI-3)]
Consider equation (3): $V_{ref} = V_{be} + V_{TH} K$. Since the base emitter junction is forward biased, it is the same as a forward biased p-n junction, hence V_{be} and V_d (diode voltage) can be used interchangeably.

$$\frac{dV_{ref}}{dT} = \frac{dV_{be}}{dT} + K\frac{V_{TH}}{dT} = \frac{dV_d}{dT} + K\frac{V_{TH}}{dT} \rightarrow (eqn\,6)$$

In order to obtain the temperature coefficient of the output voltage V_{ref}, the temperature coefficients of V_d and V_{TH} should be determined.
(i)To obtain dV_d/dT, consider the following. From the diode equation (1b) (page 8), we can express V_d as:

$$V_d = \frac{kT}{q}\ln\left(\frac{I_d}{I_s}\right) = V_{TH}\ln\left(\frac{I_d}{I_s}\right) \rightarrow (eqn\,7)$$

By taking the partial derivative of V_d, (equation 7) with respect to temperature, we get:

$$\frac{\partial V_d}{\partial T} = \frac{V_{TH}}{T}\ln\left(\frac{I_d}{I_s}\right) + V_{TH}\frac{I_s}{I_d}\left[\frac{\partial I_d}{I_s \partial T} - \frac{I_d}{I_s^2}\frac{\partial I_s}{\partial T}\right] \rightarrow (eqn\,8a)$$

Equation (8a) can be simplified by using equation (7) as below:

$$\frac{\partial V_d}{\partial T} = \frac{V_d}{T} + V_{TH}\left[\frac{\partial I_d}{I_d \partial T} - \frac{\partial I_s}{I_s \partial T}\right] \rightarrow (eqn\,8b)$$

I_s can also be expressed as a function of temperature according to the following equation:

$$I_s \cong I_{s0}\left(\frac{T}{T_0}\right)^{\frac{7}{2}} e^{\frac{-E_G}{kT}} \rightarrow (eqn\,9)$$

By taking the partial derivative of Is (equation 9), with respect to temperature, we get:

$$\therefore \frac{\partial I_s}{\partial T} = I_{s0}\left(\frac{T}{T_0}\right)^{\frac{7}{2}} e^{\frac{-E_G}{kT}}\left[\frac{7}{2}\frac{1}{T} + \frac{E_G}{kT^2}\right]$$

$$\Rightarrow \frac{\partial I_s}{\partial T} = I_s\left[\frac{7}{2}\frac{1}{T} + \frac{E_G}{kT^2}\right] \rightarrow (eqn\,10)$$

Substituting equation (10) in equation (8b), we get:

$$\frac{\partial V_d}{\partial T} = \frac{V_d}{T} + \frac{V_{TH}}{T}\left[\frac{T}{I_d}\frac{\partial I_d}{\partial T} - \frac{7}{2} - \frac{E_G}{kT}\right] \rightarrow (eqn\,11)$$

$$If\ I_d = I_{d0}\frac{T}{T_0}\ and\ T = 300°K\text{, using } V_d \approx 0.7V \text{ (diode voltage)}$$

$$\frac{\partial V_d}{\partial T} = \frac{V_d}{T} - \frac{V_{TH}}{T}\left[\frac{5}{2} + \frac{E_G}{kT}\right] \approx -1.8mV/^o k \rightarrow (eqn\,12)$$

(ii)Similarly, the temperature coefficient of thermal voltage at room temperature is given by:

$$\frac{\partial V_{TH}}{\partial T} = \frac{k}{q} \approx 0.085mV/^o k \rightarrow (eqn\,13)$$

Substituting the results equation (12) and (13) in equation (6), we get:

$$\frac{dV_{ref}}{dT} = \frac{dV_d}{dT} + K\frac{V_{TH}}{dT} = -1.8mV/^o k + K * 0.085mV/^o k \rightarrow (eqn\,14)$$

From the equation (14) it can be seen that in order to obtain a temperature independent voltage K has to be chosen such that the $dV_{ref}/dT = 0$.
By equating equation (14) to zero and by solving, we get $K \approx 21.17$

The Bandgap reference circuit originally proposed uses bipolar transistors. A basic CMOS compatible bipolar implementation of a Bandgap reference circuit is shown in the following figure. Here the bipolar devices are just being used a p-n junctions.

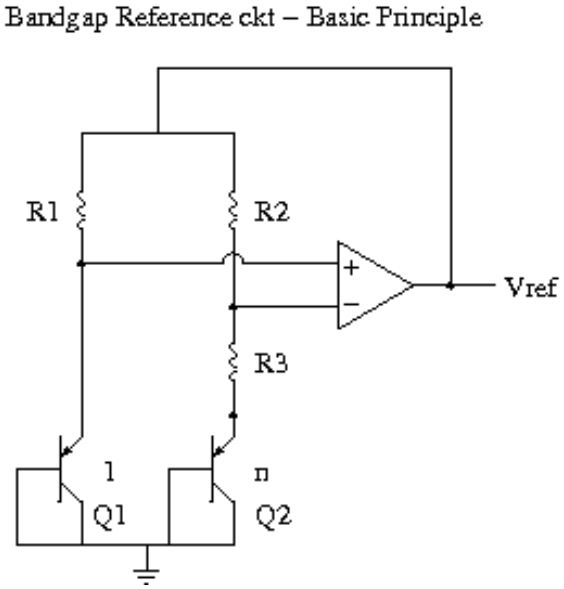


Figure 5 CMOS compatible bipolar implementation of a Bandgap reference circuit

Most of the state of the art technology uses CMOS technology; hence it is essential to implement Bandgap reference circuits compatible to CMOS technology. Figure (6) shows the diode implementation of the bipolar transistors in CMOS technology.

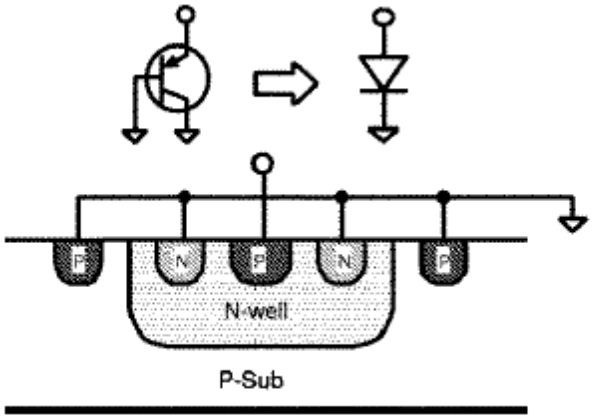


Figure 6structure of diode, fabricated by CMOS process

The resulting CMOS equivalent block diagram of figure (5) is shown in the following figure (7).

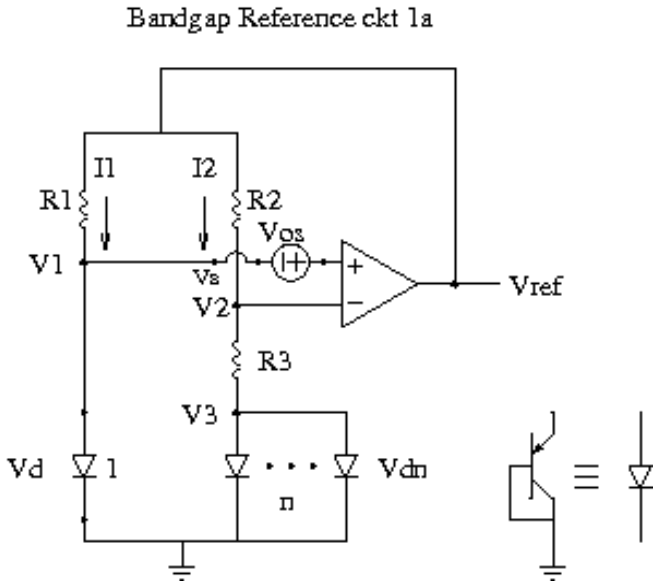


Figure 7Implementation of CMOS Bandgap reference circuit

The Bandgap reference circuits can be classified into two types:

- Voltage-mode: in this mode a voltage independent of the temperature is generated
- Current-mode: in this mode a current independent of the temperature is generated.

The topologies I implemented for this project were Voltage-mode Bandgap reference circuits. A topology depicting the current-mode is shown in the following figure:

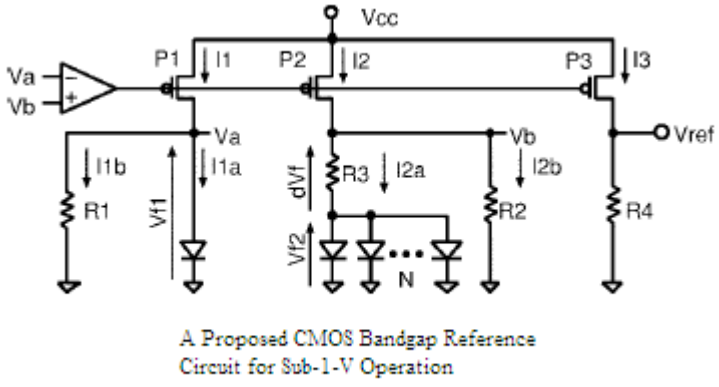


Figure 8: Current mode Bandgap reference circuit [6]

Section 3: The topologies implemented and verified in HSPICE

The following three voltage-mode Bandgap reference circuit topologies were implemented and verified in HSPICE:

Bandgap topology 1a: This topology is the CMOS equivalent of the figure (5).

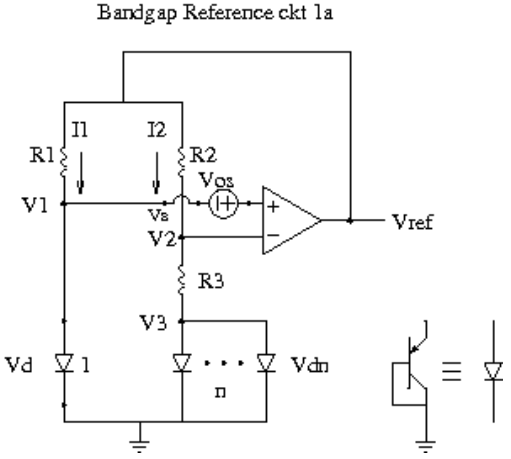


Figure 9Topology 1a

The output voltage of this topology is given by: $V_{ref} = V_d + I_1 R_1 \rightarrow (eqn15)$

If R_1 is chosen to be equal to R_2 ($R_1 = R_2$), the currents I_1 and I_2 are equal ($I_1 = I_2$). The current can be expressed as the following:

$$R_1 = R_2 \Rightarrow I_1 = I_2 = \frac{(V_2 - V_3)}{R_3} = \frac{(V_2 - V_{dn})}{R_3} \rightarrow (eqn16a)$$

Considering the opamp to be ideal, the voltage at the inputs of the opamp should be equal, therefore equation (16a) can be written as: $I_1 = I_2 = \frac{(V_1 - V_{dn})}{R_3} = \frac{(V_d - V_{dn})}{R_3} \rightarrow (eqn16b)$

$$V_1 = V_2 \Rightarrow V_d = V_{dn} + I_2 R_3 \rightarrow (eqn17)$$

Using the diode equations (1a) on page 8, the currents I_1 and I_2 can be written as:

$$I_1 = I_s e^{\left(\frac{qV_d}{KT}\right)} \Rightarrow V_d = \frac{kT}{q} \ln \frac{I_1}{I_s}$$

$$I_2 = nI_s e^{\left(\frac{qV_{dn}}{KT}\right)} \Rightarrow V_{dn} = \frac{kT}{q} \ln \frac{I_2}{nI_s}$$

Subtracting V_{dn} from V_d to compute current I_1/ I_2, we get

$$V_d - V_{dn} = \frac{kT}{q} \ln\left(\frac{I_1}{I_s}\frac{nI_s}{I_2}\right) = \frac{kT}{q} \ln(n) \rightarrow (eqn18)$$

By substituting equation (18) in equations (15) and (16b), we get:

$$V_{ref} = V_d + I_1 R_1 = V_d + \frac{(V_d - V_{dn})}{R_3} R_1 = V_d + \frac{kT}{q} \ln(n) \frac{R_1}{R_3} \rightarrow (eqn19)$$

To check the temperature dependence of the output voltage V_{ref} (equation 19), let us consider the derivative of V_{ref} with respect to temperature.

By taking the derivative of equation (19) with respect to temperature, we get:

$$\frac{dV_{ref}}{dT} = \frac{dV_d}{dT} + \frac{k}{q}\ln(n)\frac{R_1}{R_3} \rightarrow (eqn\,20)$$

To obtain a temperature independent output voltage V_{ref}, we need to choose n, R_1,R_2,R_3 such that the above equation (20) is zero.

In the simulations I chose the following values:
R1 = 400KΩ, R2, = 400KΩ, R3 = 54KΩ, n=16. Multiple diodes 'n' were chosen so that the circuit is less susceptible to the offset voltage. Also, since n is related to V_{ref} as a logarithm, an increase in n by more than 16 doesn't gain much.

By substituting the values in $\frac{k}{q}\ln(n)\frac{R_1}{R_3}$ (of equation (20)), we get:

$$\frac{k}{q}\ln(n)\frac{R_1}{R_3} \cong 0.085mV/°k * \ln(16) * \frac{400K\Omega}{54K\Omega} = 1.7457mV/°k \rightarrow (eqn\,21)$$

By substituting equation (21) and using equation (12), we get:

$$\therefore \frac{dV_{ref}}{dT} = -1.8mV/°k + 1.7457mV/°k \approx 0.054mV/°k \approx 54\mu V/°k \rightarrow (eqn\,22)$$

Hence, the resultant output voltage is approximately constant over the temperature.

Bandgap topology 1b

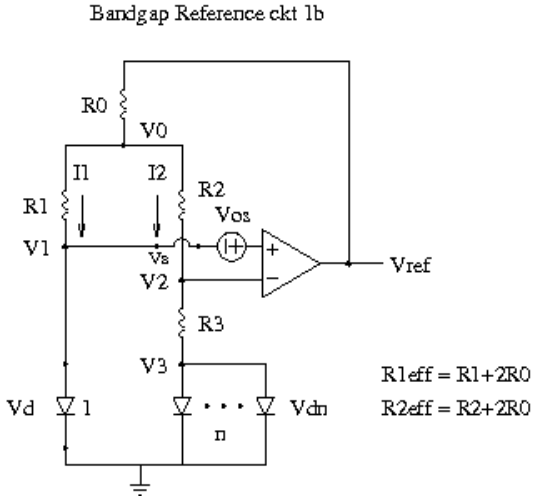


Figure 10 Topology 1(b)

This topology is similar to 1(a), except there is a resistor included in the feedback loop. Therefore, there is double the current in R_0. This current splits into half at the node V_0 if $R_1 = R_2$. The effective resistances seen at the input of the opamp are $R_{1eff} = R_1 + 2R_0$ and $R_{2eff} = R_2 + 2R_0$.

To obtain similar results as Topology 1a, I selected the following values for this topology:

- R0 = 150KΩ R1 = 100KΩ, R2, = 100KΩ (=> $R_{1eff} = R_{2eff}$ =2*150 + 100 KΩ = 400 KΩ), and R3 = 54KΩ, n=16 – (consider this as **configuration i)**

The same performance is obtained by choosing: R0 = 100KΩ R1 = 200KΩ, R2, = 200KΩ (=>R_{1eff} = R_{2eff} =2*100+200 KΩ = 400 KΩ) (consider this as **configuration ii)**

By comparing the total resistance of the different configurations (i and ii listed above) and topology 1a, it can be seen (from the following table) configuration i is the most area effective solution

	Resistance as sum	Total resistance
configuration i	(150+2*100+54) KΩ	404KΩ
configuration ii	(100+2*200+54) KΩ	554KΩ
Topology 1a	(100+2*200+54) KΩ	854 KΩ.

Apart from this difference, the principle is still the same, and all equations derived for the previous topology (1a) still apply to this topology.
Therefore, the output voltage for this topology is given by:

$$\therefore V_{ref} = V_d + \frac{kT}{q}\ln(n)\frac{R_{1eff}}{R_3} \rightarrow (eqn\,21) \text{ When } (R_1 = R_2)$$

Bandgap topology 2

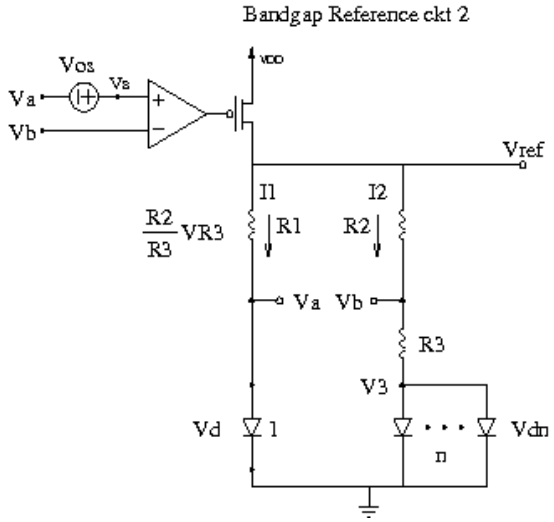


Figure 11Topology 2

This topology is similar to the previous topologies 1(a) and 1(b), except the output of the opamp is not feedback.
Advantage: The opamp has to drive only the p-channel device. In the previous topologies 1(a) and 1(b), the opamp should drive the output load which could be a large. Also, this topology has better driving capability as the output resistance is higher than previous topologies 1(a) and 1(b).
Apart from this difference, the principle is still the same, and all equations derived for the previous topology (1a) still apply to this topology.
Therefore the output voltage for this topology is given by:

$$\therefore V_{ref} = V_d + \frac{kT}{q}\ln(n)\frac{R_2}{R_3} = V_d + \frac{kT}{q}\ln(n)\frac{R_1}{R_3} \rightarrow (eqn\,22) \text{ When } (R_1 = R_2)$$

Section 4: Opamp section:

I chose a simple two stage opamp with a p-channel input differential stage. The following steps were followed:

Step1: Select a topology
Step2: Select n-channel or p-channel input differential stage
Step3: Select W/L(s) and then obtain W/L(s) of the devices
Step4: Implementation of the bias circuitry

Step1 Selecting a topology: I used a two stage opamp because of the robustness.

Step2: Selecting n-channel or p-channel input differential stage
I used a P-channel differential input stage, as the voltage at the input of the opamp is too low to keep the n-channel ON.
Consider the n-channel input differential stage shown in figure (12). The input voltage at m1 is about 0.7V (diode voltage), when m5 is in saturation the V_{ds} for m5 ≈ 0.2V*. Therefore, the voltage at the node Vs is about 0.2V. Therefore, the V_{gs} of m1 is about 0.5V; hence it is difficult to turn ON m1 as V_{tn} for an n-channel is about 0.7V
* (in-between 0.2 and 0.3V, the opamp has to be designed to meet this condition)

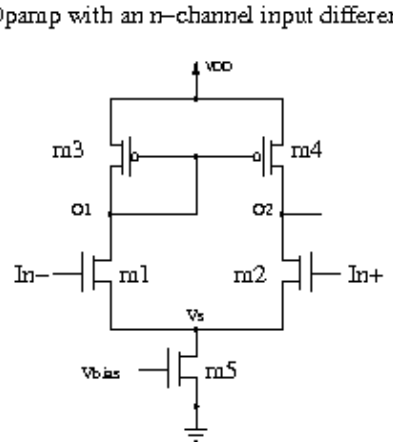


Figure 12 opamp with n-channel differential input stage

Consider the p-channel input differential stage shown in figure (13). The input voltage at m1 is about 0.7V (diode voltage), when m5 is in saturation the V_{ds} for m5 ≈ 0.2V*. Therefore, the voltage at the node Vd is about 0.2 to 0.3V below Vdd (3V). Therefore, the V_{gs} of m1 is about -2.7/-2.8V, hence there is no problem to turn m1 ON, unlike in the n-channel input differential stage, as V_{tp} for a p-channel is about -0.9V

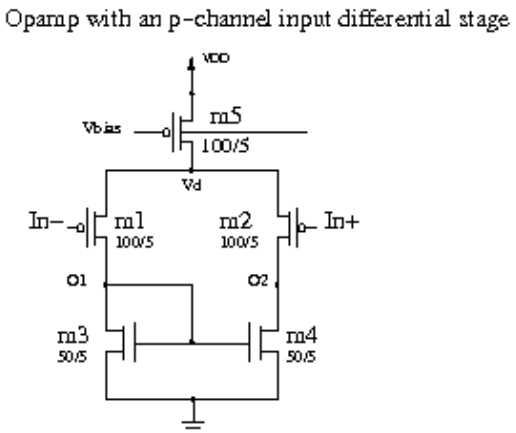


Figure 13 opamp with p-channel differential input stage

Step3: Selecting W/L(s) and then obtaining W/L(s) of the devices:

- I chose W/L = 100/5 for m5, m1, m2.
- I chose a 1:1 ratio of the current in m5 (I_{diff}) and m6 (I_{out}). Using the Systematic offset voltage condition, the W/L's of m3 and m4 are selected.

$$\frac{2(W/L)_3}{(W/L)_7} = \frac{2(W/L)_4}{(W/L)_7} = \frac{(W/L)_5}{(W/L)_6} = \frac{I_{diff}}{I_{Out}}$$

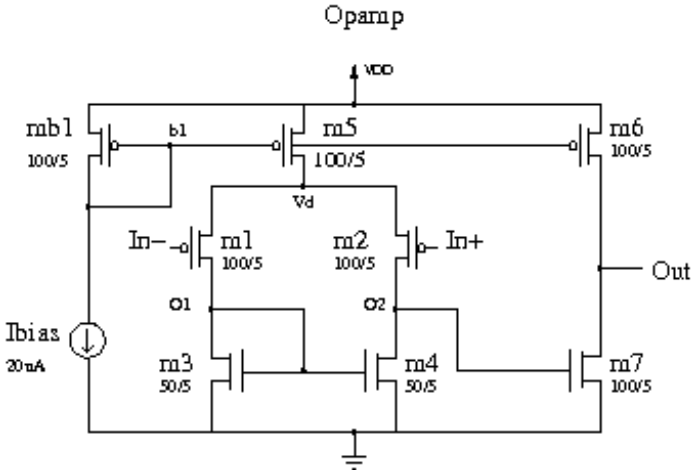


Figure 14 opamp with ideal current source

Step4: Implementation of the bias circuitry

The implementation of the bias circuitry was done in the following two stages:

- Initially using an ideal current source.
- Implementing a real bias circuitry. I selected (Supply -Independent configuration)

I chose 20μA to be the current for the opamp.

Step4 (a): Initially I used an ideal current source of 20µA and a p-channel device mb1 (W/L = 100/5) as shown in figure (14) as the bias circuitry. And the configuration was simulated in HSPICE. The phase margin of this circuit was not good, and the poles were located at 4.3 kHz and 3 MHz. Hence, a compensation circuitry was necessary.

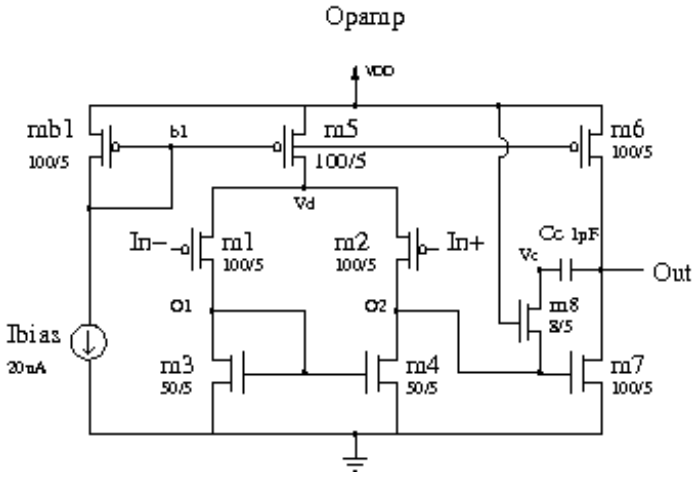


Figure 15opamp with compensation network

A compensation network, m8 and Cc as shown in the above figure (15), were included to obtain a better phase margin. By including the compensation network, the opamp has a phase margin of 50°, and the poles are now shifted to 1.6 KHz and 25 MHz, due to the pole splitting phenomenon.

Step4 (b): Implementing the Supply -Independent bias configuration
The following figure (16) shows the configuration of the biasing circuit used. The current is generated due to the small voltage drop across the resistor Rb, due to a slight mismatch in the p-channel transistor mb1 (105/5) and mb2 (100/5).

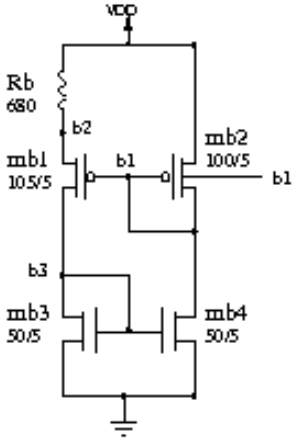


Figure 16Bias circuitry

The following equations were used to obtain the value of the Resistor Rb.

$$I_{mb1} = \frac{1}{2}\mu c_{ox}\frac{W}{L}\left(V_{b1} - V_{b2} - |V_{tp}|\right)^2 \rightarrow (eqn\,23a)$$

$$\text{Where } V_{b2} = V_{dd} - I_{bias}R_b \rightarrow (eqn\,23b)$$

$$I_{mb2} = \frac{1}{2}\mu c_{ox}\frac{W}{L}\left(V_{b1} - V_{dd} - |V_{tp}|\right)^2 \rightarrow (eqn\,23c)$$

By equating Imb2 (equation 23c) and Imb1 (equation 23a), R_b can be calculated. The following equation (24) shows the relation.

$$\frac{1}{2}\mu c_{ox}\frac{W}{L}\left(V_{b1} - V_{dd} - |V_{tp}|\right)^2 = \frac{1}{2}\mu c_{ox}\frac{W}{L}\left(V_{b1} - \left(V_{dd} - I_{bias}R_b\right) - |V_{tp}|\right)^2 \rightarrow (eqn\,24)$$

By substituting Ibias = 20µA in the above equation, R_b can be calculated. This value was then used in the HSPICE simulation to verify. It was found that when R_b was equal to 680Ω, the bias current was close to 20µA, and the biasing voltage was close to the simulation value obtained when an ideal current source was used.

Following figure (17) shows the complete opamp topology.

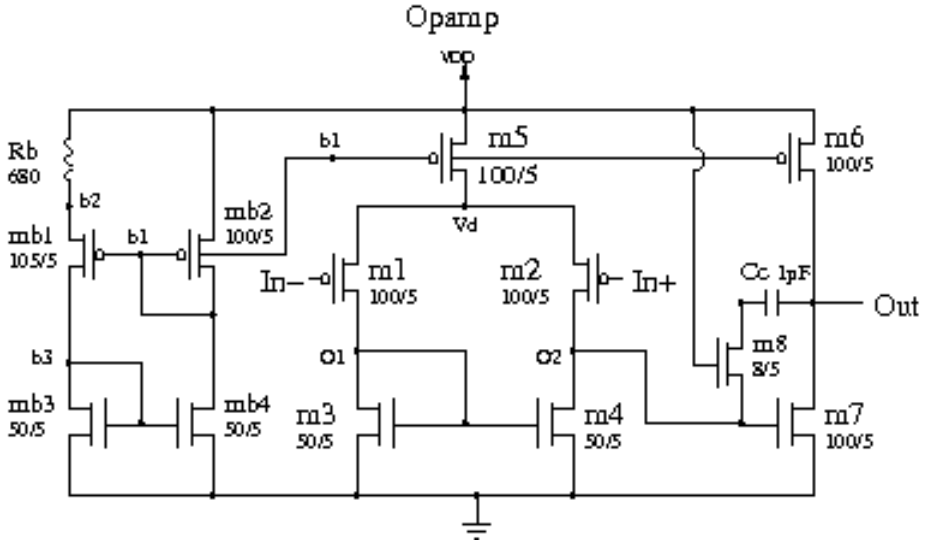


Figure 17 Complete topology of the opamp

The Performance parameters of the opamp are the following:

- offset voltage: 269.2µV
- The phase margin: 52°.
- Unity Gain bandwidth: 11.8MHz
- Gain: 10K
- Poles are located at 1630Hz and 25.1MHz
- The open loop output impedance is 461KΩ

The most important parameter in this application is the offset voltage. Since this is used to create a constant DC voltage, Slew Rate, Gain, and other parameters are not very crucial.

Opamp simulation results:

The following plot shows the result of the opamp without phase compensation. It can be seen that the poles are located at 4831Hz and 3.059MHz.
Unity Gain bandwidth: 25.12MHz
Gain: 10.6K
The phase margin was very low.

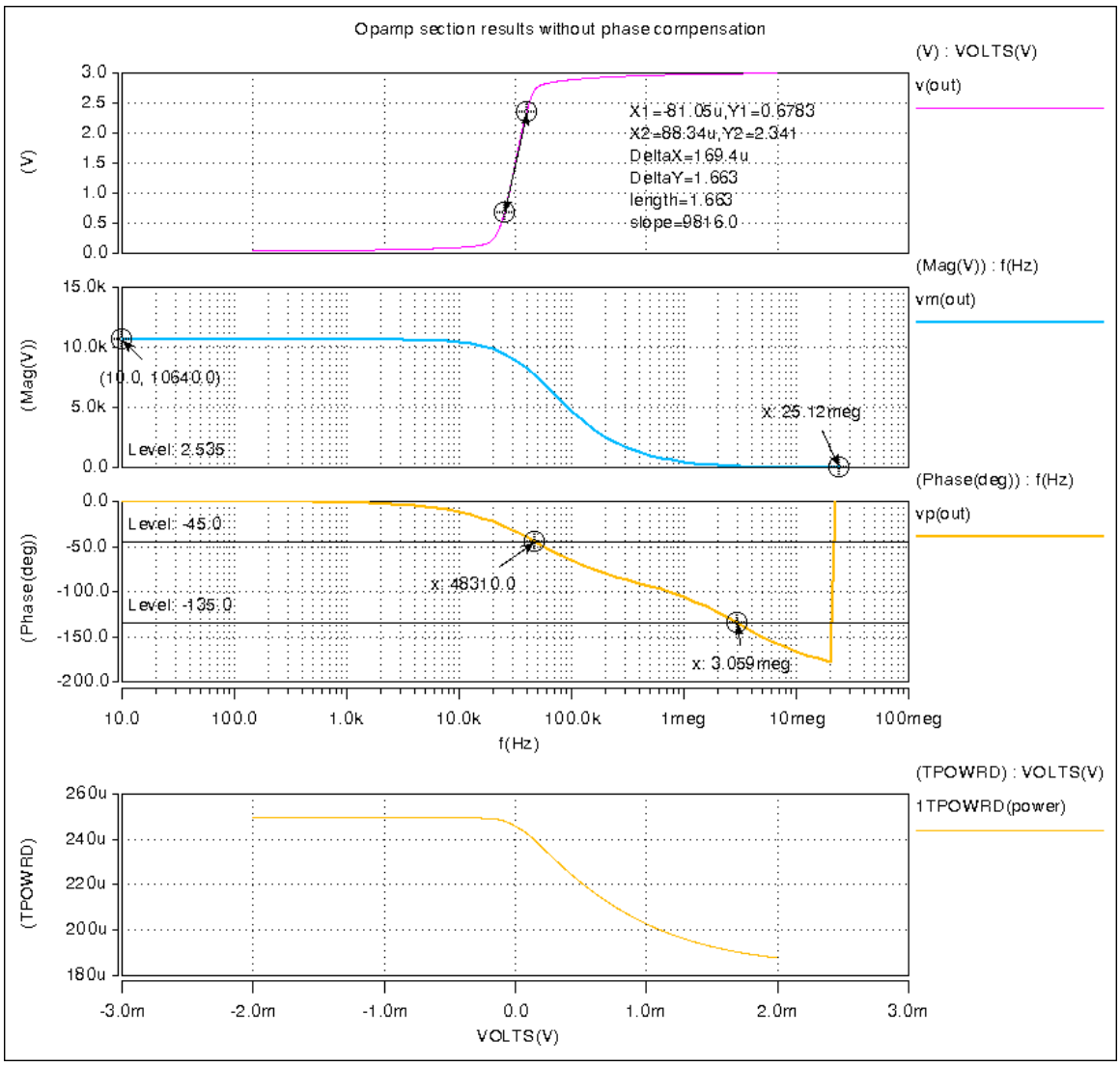


Figure 18 HSPICE simulation of opamp without compensation

The following plot shows the result of the opamp with phase compensation.
Now the poles are located at 1630Hz and 25.1MHz (pole splitting phenomenon)
The phase margin: 52°.
Unity Gain bandwidth: 11.8MHz
Gain: 10.6K

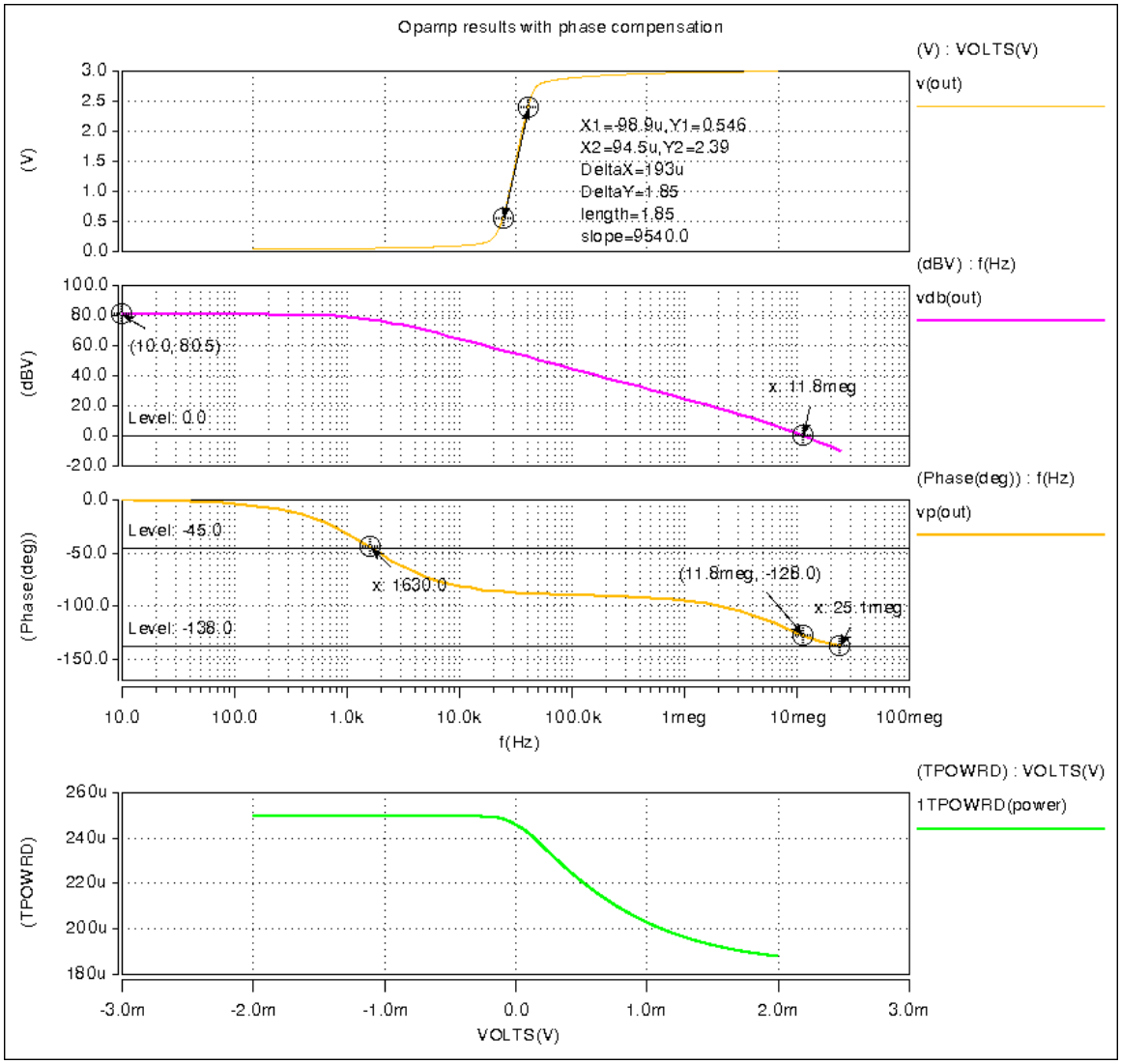


Figure 19HSPICE simulation of opamp with compensation

The pole splitting phenomenon can be clearly seen from the two plots. In the previous case the poles were located at 4831Hz and 3.059MHz. In the compensated case they are located at 1630Hz and 25.1MHz.
At the same time, the UGB is less, as this decreased from 25.12MHz to 11.8MHz.

Section 5: HSPICE simulation results of the three topologies

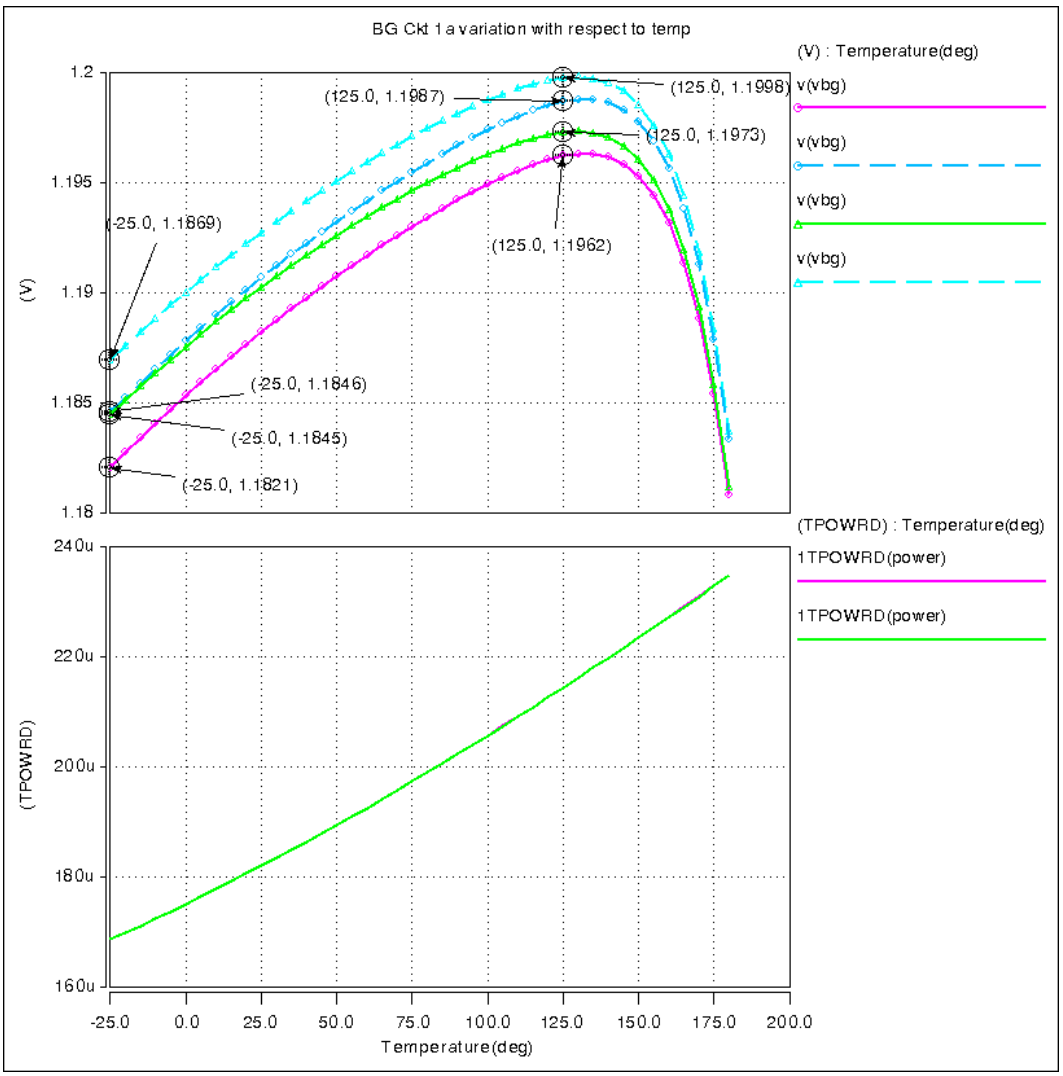


Figure 20 HSPICE simulation of Bandgap reference topology 1a, variation with temperature

Topology1a	At -25°C	At 125°C	Deviation due to temperature	Deviation due to offset-25&125°C	
				At -25°C	At 125°C
Ideal opamp no offset	1.1821	1.1962	14.1mV		
Ideal opamp with offset = 269uV	1.1845	1.1987	14.2mV	2.4mV	2.4mV
Real opamp with offset = 269uV	1.1846	1.1973	12.7mV		
Real opamp with offset = 538uV	1.1869	1.1998	12.9mV	2.3mV	2.5mV

Average power found to be 199.21µW

Power (with real opamp), simulated with different offset voltage remains the same.

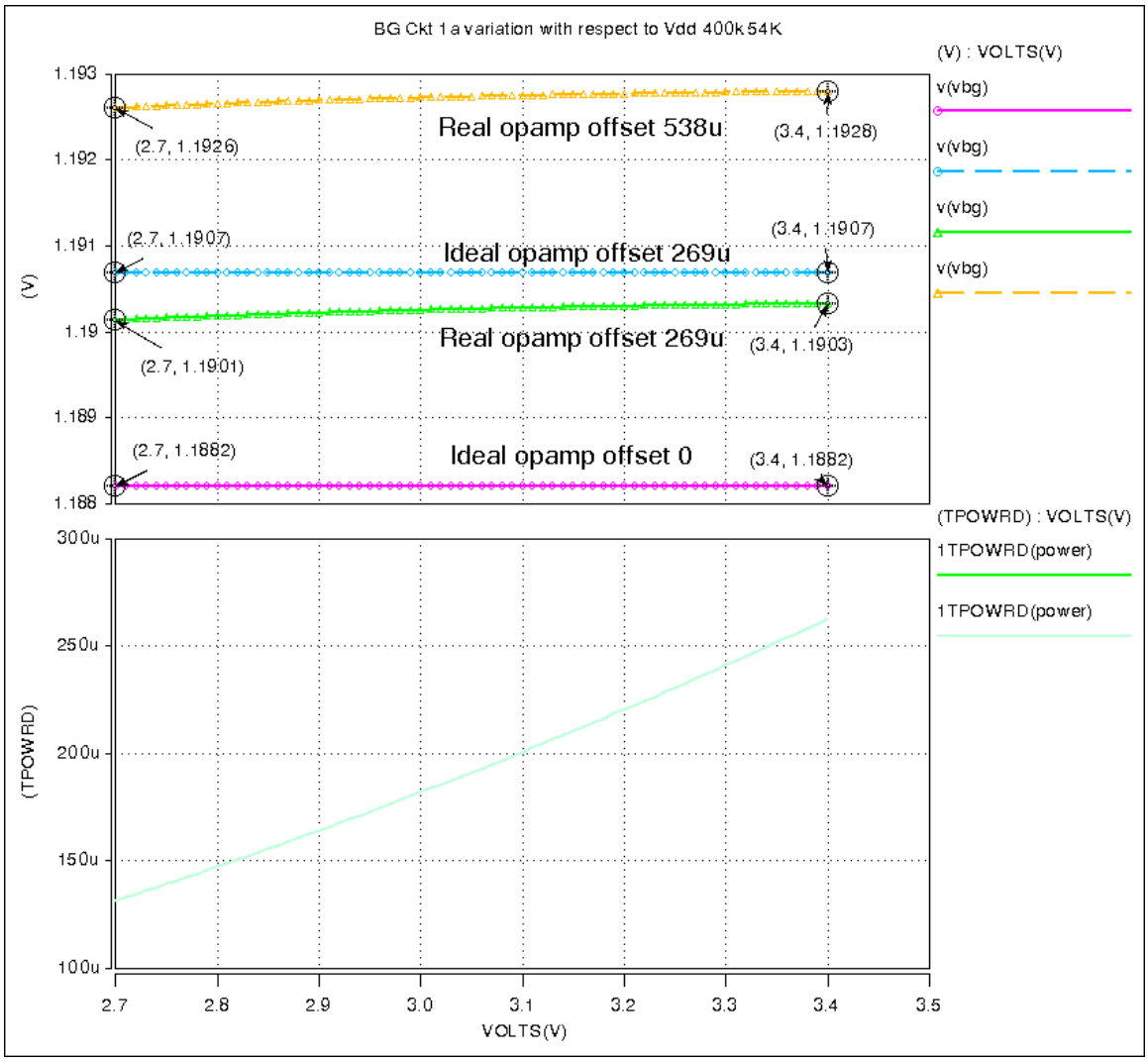


Figure 21HSPICE simulation of Bandgap reference topology 1a, variation with supply voltage

Topology1a	At 2.7V	At 3.4V	Deviation due to Vdd	Deviation due to offset	
				At 2.7V	At 3.4V
Ideal opamp no offset	1.1882	1.1882	0		
Ideal opamp with offset = 269uV	1.1907	1.1907	0	2.5mV	2.5mV
Real opamp with offset = 269uV	1.1901	1.1903	0.2mV		
Real opamp with offset = 538uV	1.1926	1.1928	0.2mV	2.5mV	2.5mV

Power, when simulated with different offset voltage (with real opamp) remains the same.

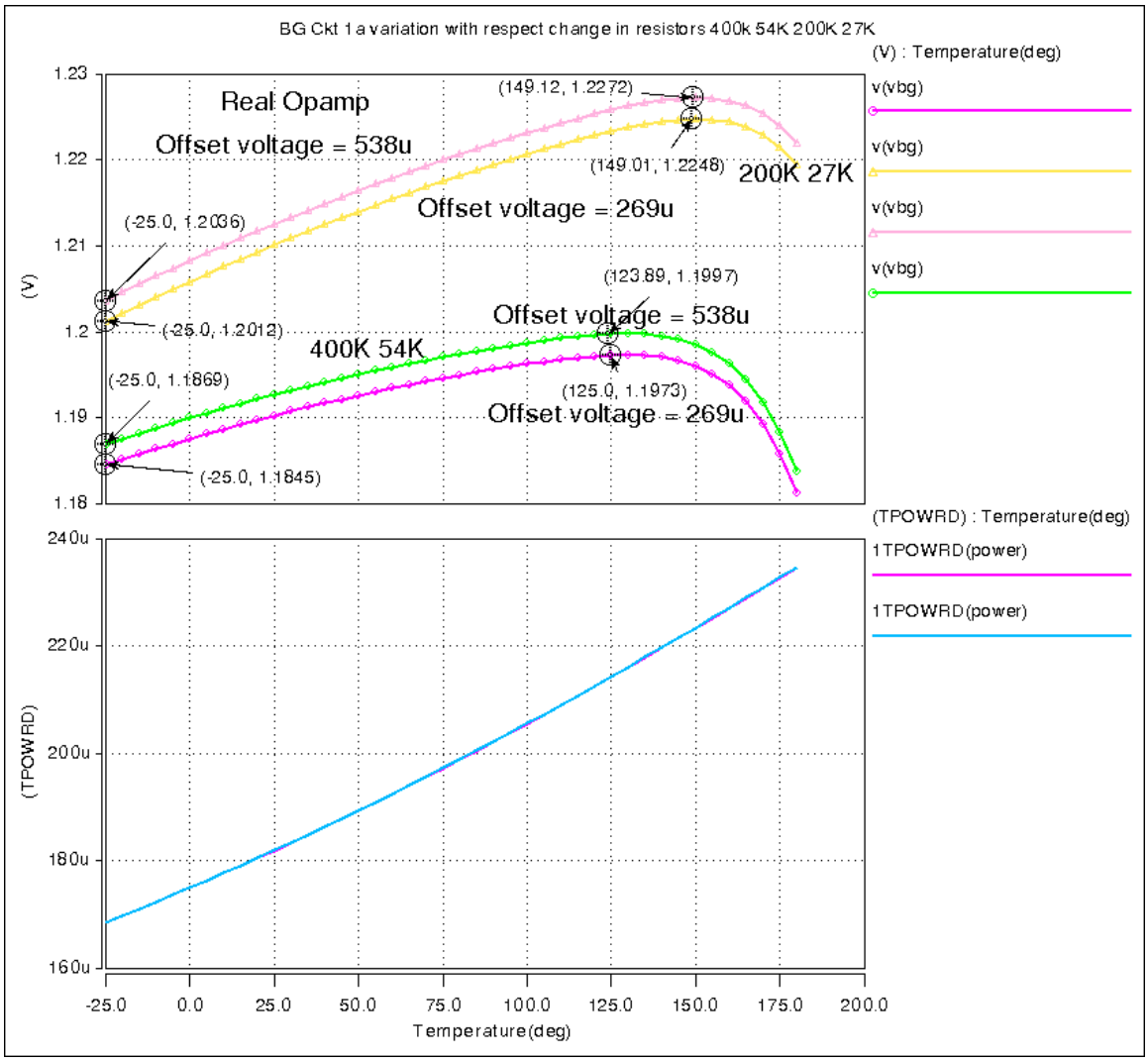


Figure 22 HSPICE simulation of Bandgap reference topology 1a, variation with change in resistors, but keeping the ratio constant

Results with real opamp

Offset voltage	Resistors used	At -25°C	At 125°C	Deviation due to temperature	Deviation due to resistors -25&125°C	
269uV	2*400K 54K	1.1845	1.1973	12.8mV		
	2*200K 27K	1.2012	1.2248*	23.6mV	16.7mV	27.5mV*
538uV	2*400K 54K	1.1869	1.1997	12.8mV		
	2*200K 27K	1.2036	1.2272*	23.6mV	16.7mV	27.5mV*

*Max values for lower resistors using 2*200K, 27K occurred at around 145°C.

Power, when simulated with different resistors and at different offset voltage remains the same.

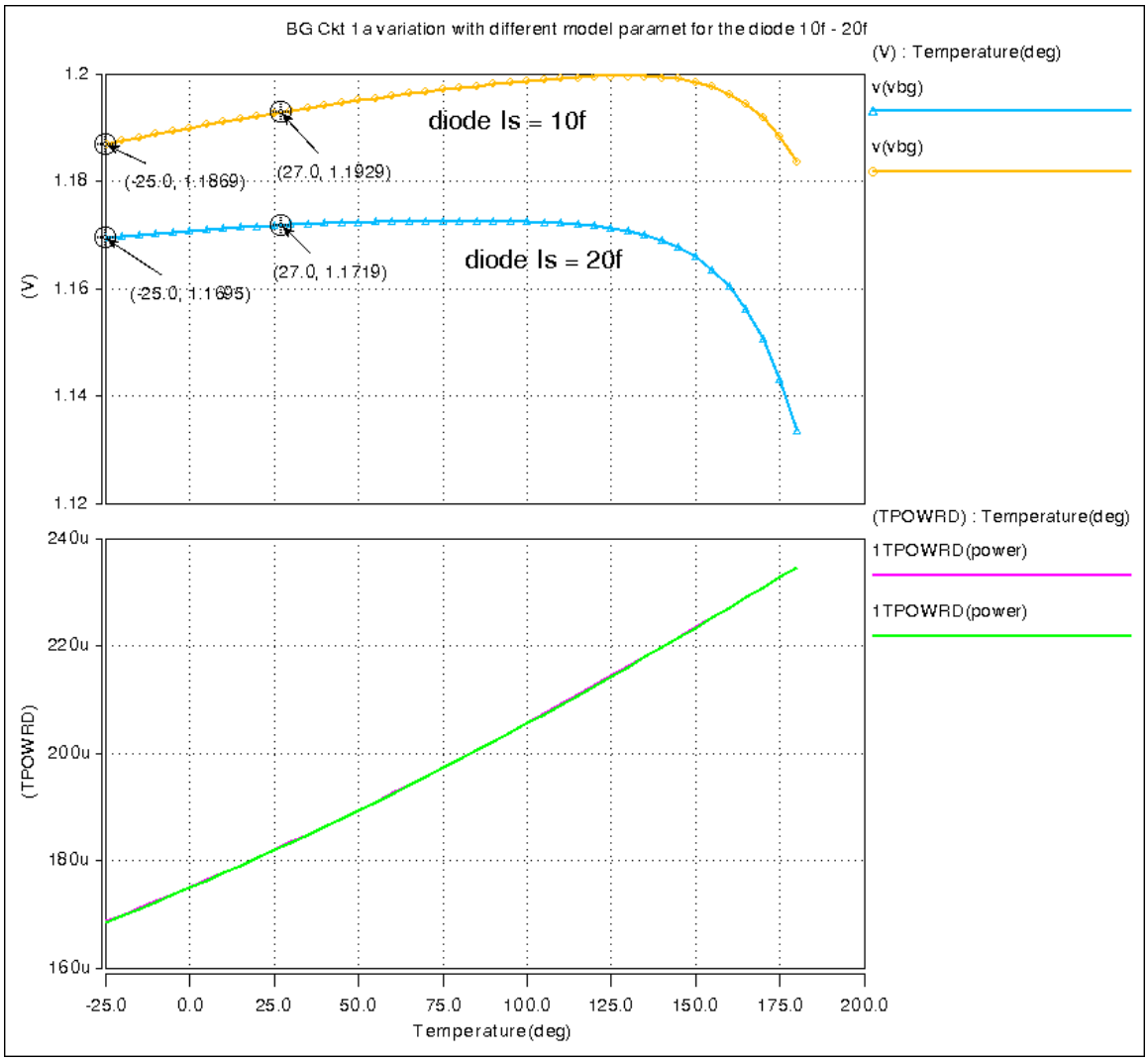


Figure 23HSPICE simulation of Bandgap reference topology 1a, variation with change in diode parameters Is 10f - 20f

The deviation with respect to change in diode parameter, at room temperature: 1.1929-1.1719 V = 21mV.

The variation should be $\ln(2)*V_{TH} = 0.69*26mV \approx 18mV$

Power, when simulated with diode remains the same

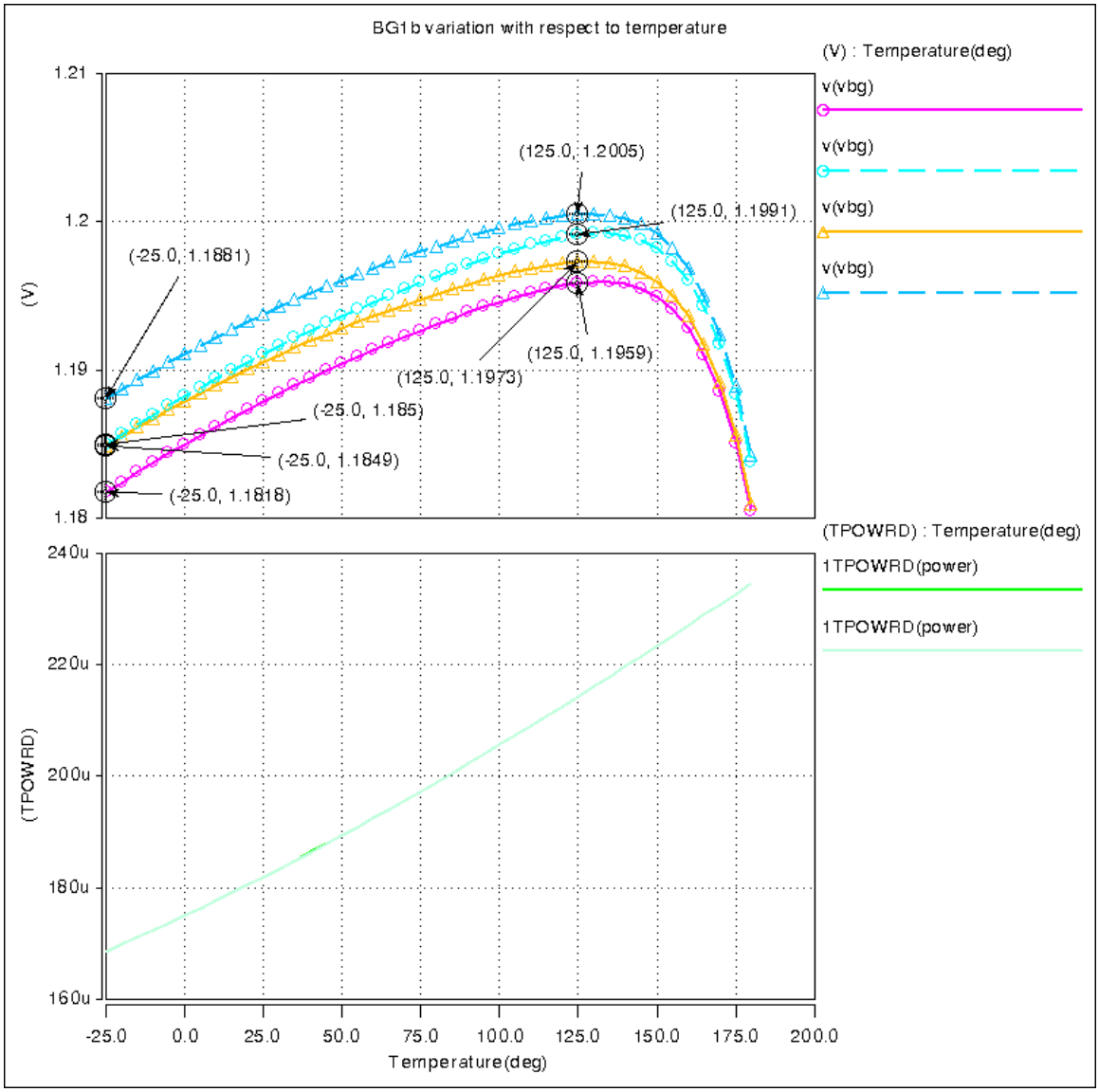


Figure 24HSPICE simulation of Bandgap reference topology 1b, variation with temperature

Topology1b	At -25°C	At 125°C	Deviation due to temperature	Deviation due to offset	
				At -25°C	At 125°C
Ideal opamp no offset	1.1818	1.1959	14.1mV		
Ideal opamp with offset = 269uV	1.185	1.1991	14.1mV	3.2mV	3.2mV
Real opamp with offset = 269uV	1.1849	1.1973	12.4mV		
Real opamp with offset = 538uV	1.1881	1.2005	12.4mV	3.2mV	3.2mV

Average power found to be 199.21µW

Power (with real opamp), simulated with different offset voltage remains the same.

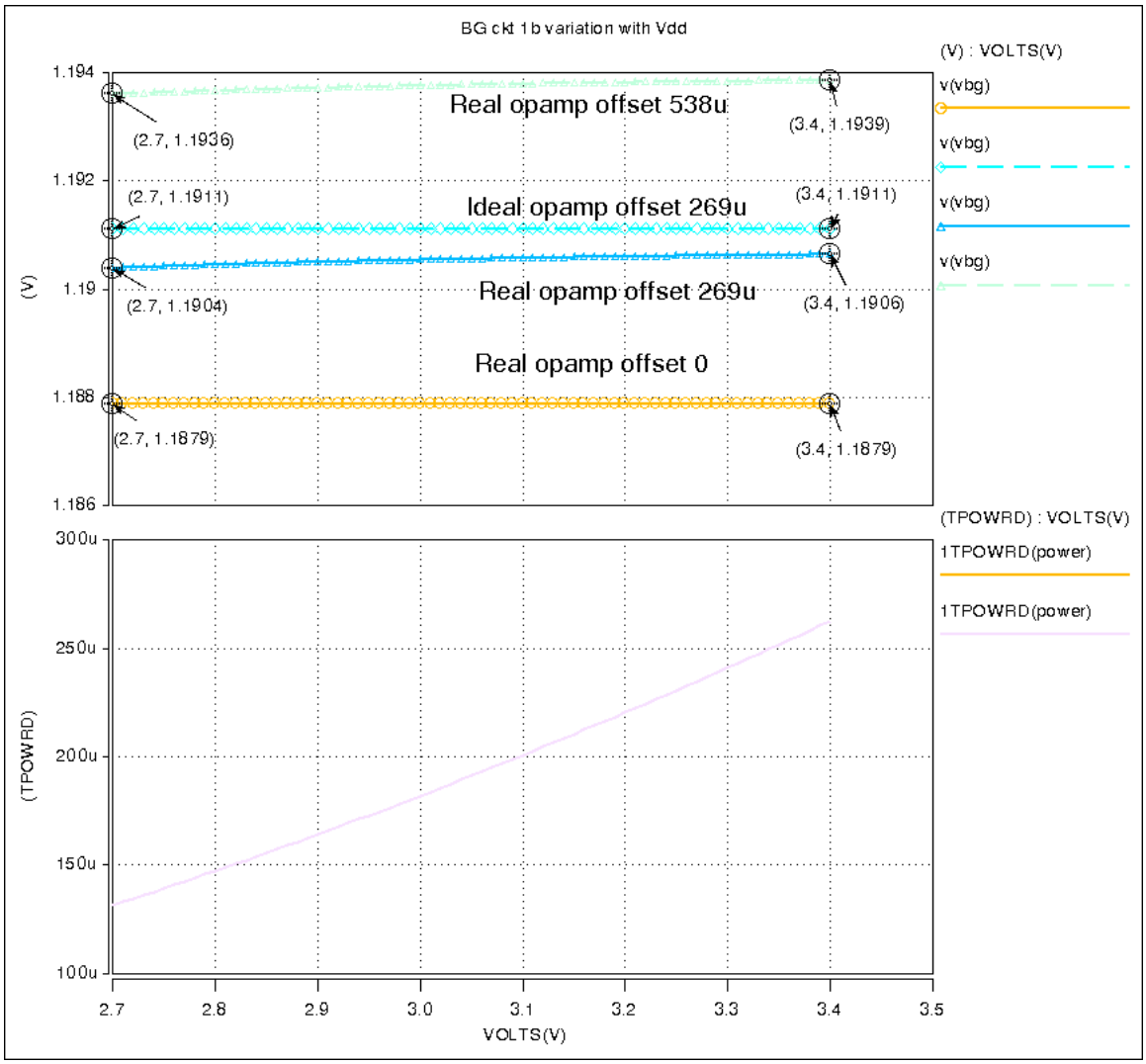


Figure 25HSPICE simulation of Bandgap reference topology 1b, variation with supply voltage

Topology1b	At 2.7V	At 3.4V	Deviation due to Vdd	Deviation due to offset	
				At 2.7V	At 3.4V
Ideal opamp no offset	1.1879	1.1879	0		
Ideal opamp with offset = 269uV	1.1911	1.1911	0	3.2mV	3.2mV
Real opamp with offset = 269uV	1.1904	1.1906	0.2mV		
Real opamp with offset = 538uV	1.1936	1.1939	0.3mV	3.2mV	3.3mV

Power, when simulated with different offset voltage (with real opamp) remains the same.

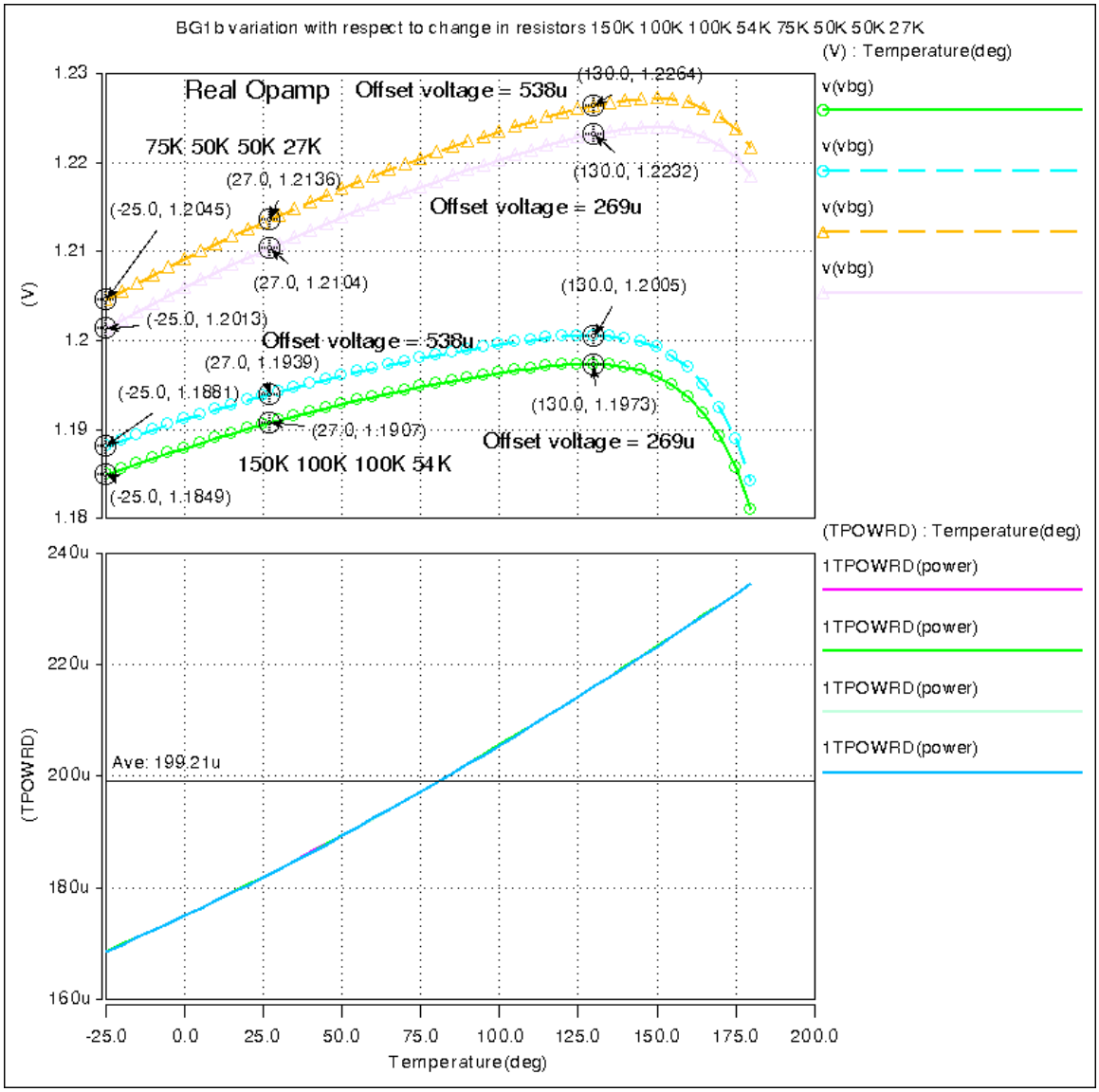


Figure 26HSPICE simulation of Bandgap reference topology 1b, variation with change in resistors, but keeping the ratio constant

Results with real opamp

Offset voltage	Resistors used	At -25°C	At 130°C	Deviation due to temperature	Deviation due to resistors -25&130°C	
269uV	150K 2*100K 54K	1.1849	1.1973	12.4mV		
	75K 2*50K 27K	1.2013	1.2232	21.9mV	16.4mV	25.9mV
538uV	150K 2*100K 54K	1.1881	1.2005	12.4mV		
	75K 2*50K 27K	1.2045	1.2264	21.9mV	18.4mV	25.9mV

Power, when simulated with different resistors and at different offset voltage remains the same, 199.21µW.

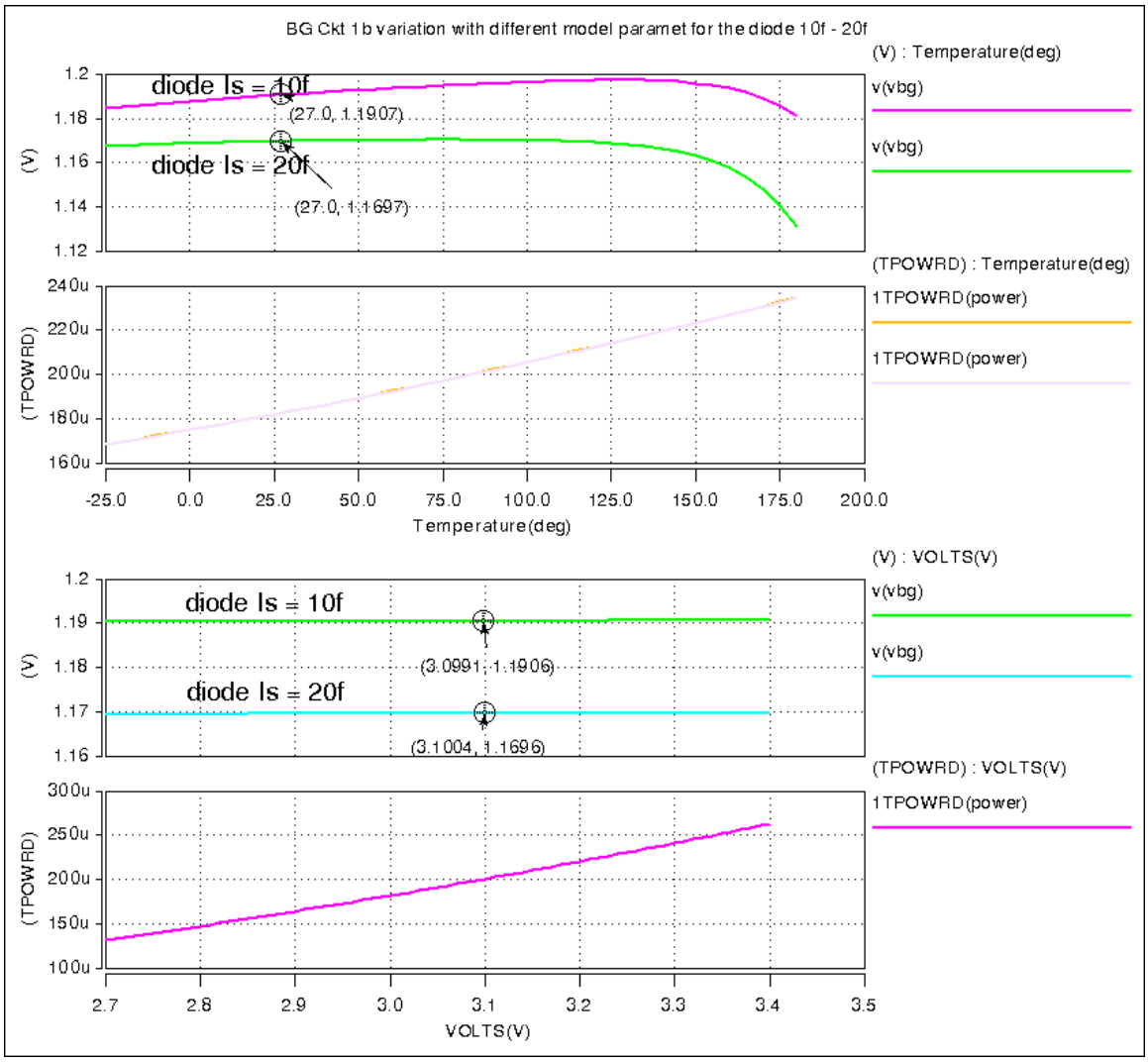


Figure 27HSPICE simulation of Bandgap reference topology 1b, variation with change in diode parameters Is 10f - 20f

The deviation with respect to change in diode parameter, at room temperature: 1.1907-1.1697 V = 21mV.

The variation should be $\ln(2)*V_{TH} = 0.69*26mV \approx 18mV$

Power, when simulated with diode remains the same

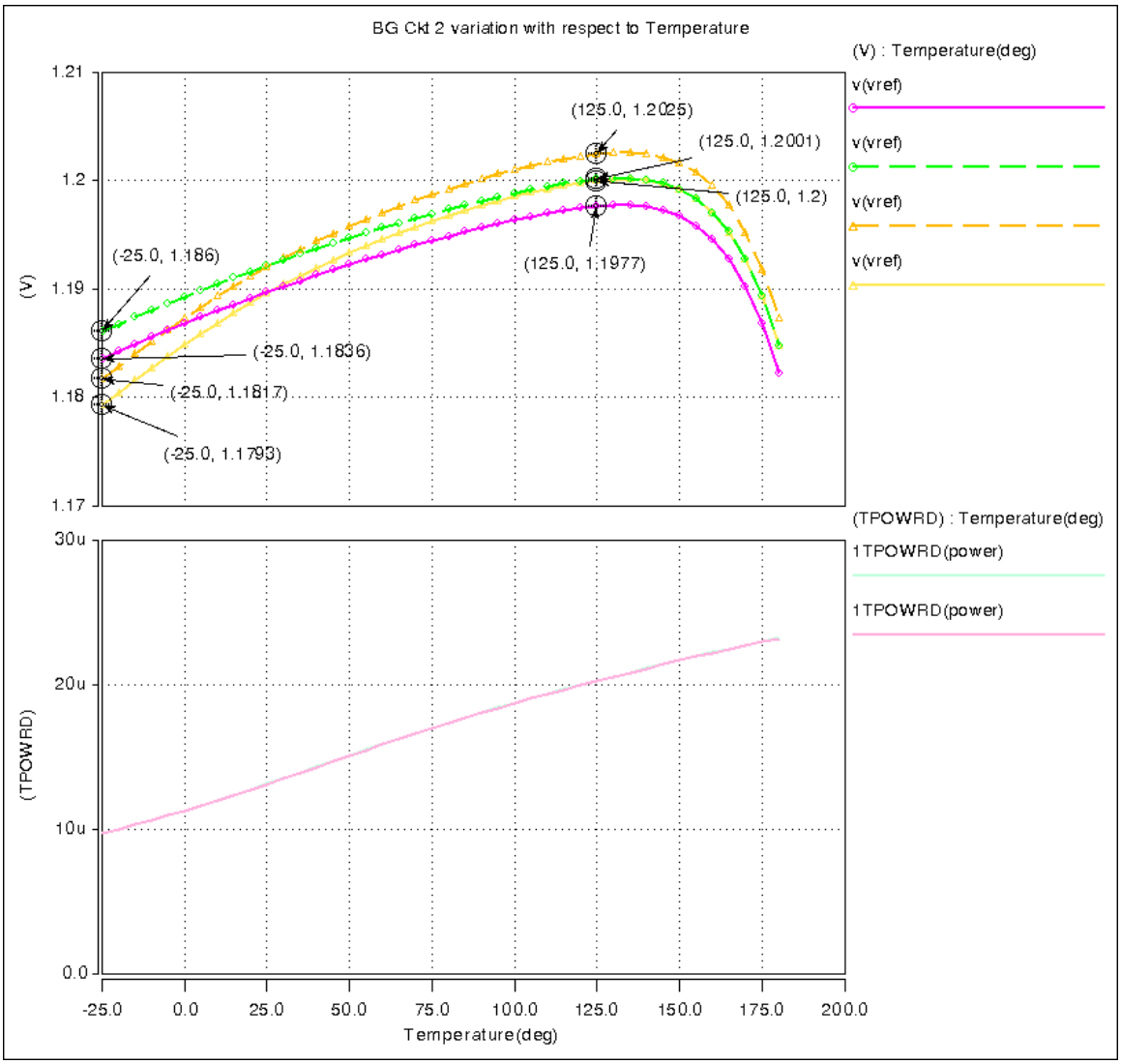


Figure 28HSPICE simulation of Bandgap reference topology2, variation with temperature

Topology2	At -25°C	At 125°C	Deviation due to temperature	Deviation due to offset	
				At -25°C	At 125°C
Ideal opamp no offset	1.1836	1.1977	14.1mV		
Ideal opamp with offset = 269uV	1.186	1.2001	14.1mV	2.4mV	2.4mV
Real opamp with offset = 269uV	1.1793	1.2	20.7mV		
Real opamp with offset = 538uV	1.1817	1.2025	20.8mV	2.4mV	2.5mV

Average power found to be 16.821µW

Power (with real opamp), simulated with different offset voltage remains the same.

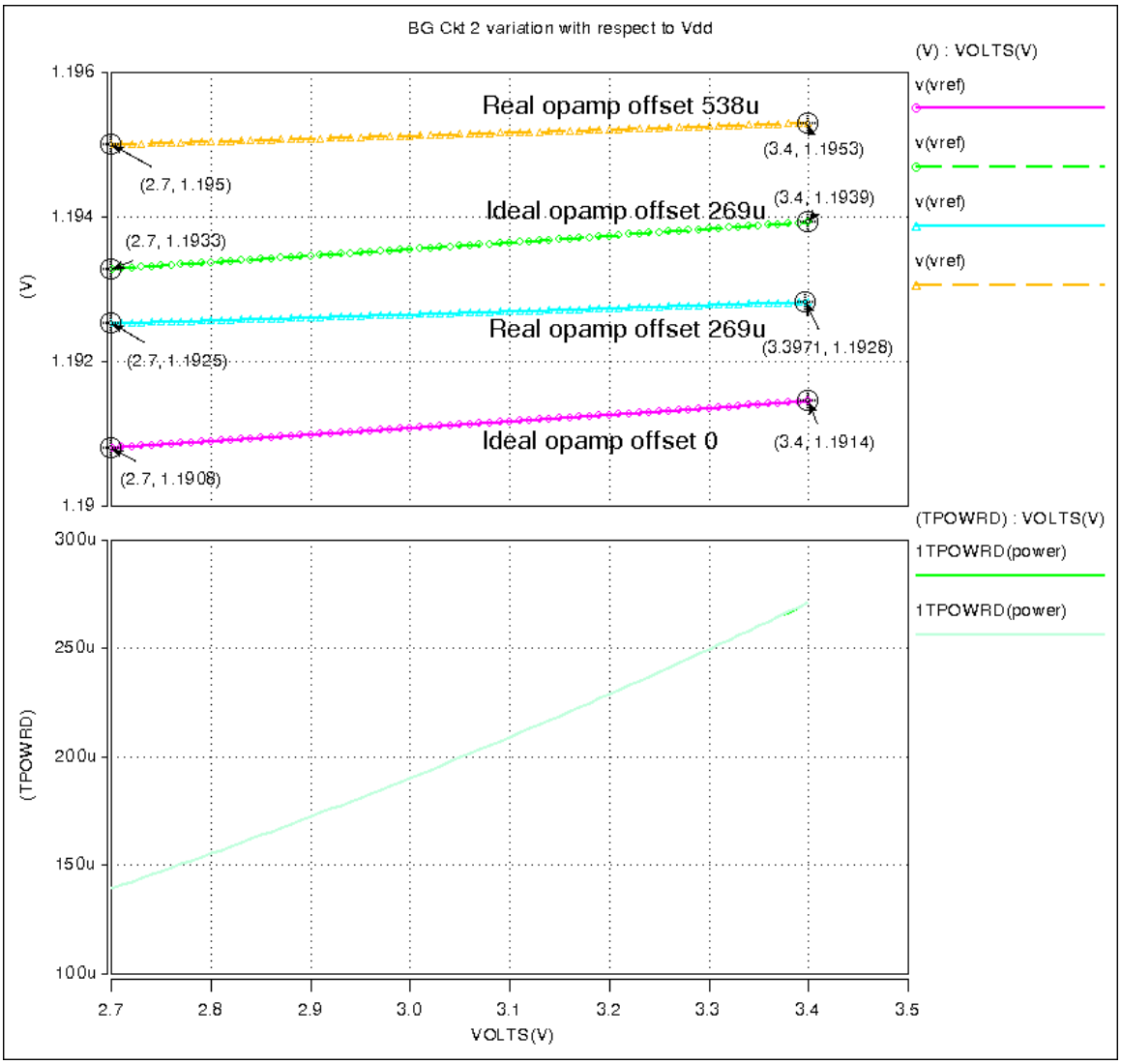


Figure 29HSPICE simulation of Bandgap reference topology 2, variation with supply voltage

Topology2	At 2.7V	At 3.4V	Deviation due to Vdd	Deviation due to offset	
				At 2.7V	At 3.4V
Ideal opamp no offset	1.1908	1.1914	0.6mV		
Ideal opamp with offset = 269uV	1.1933	1.1939	0.6mV	2.5mV	2.5mV
Real opamp with offset = 269uV	1.1925	1.1928	0.3mV		
Real opamp with offset = 538uV	1.195	1.1953	0.3mV	2.5mV	2.5mV

Power, when simulated with different offset voltage (with real opamp) remains the same.

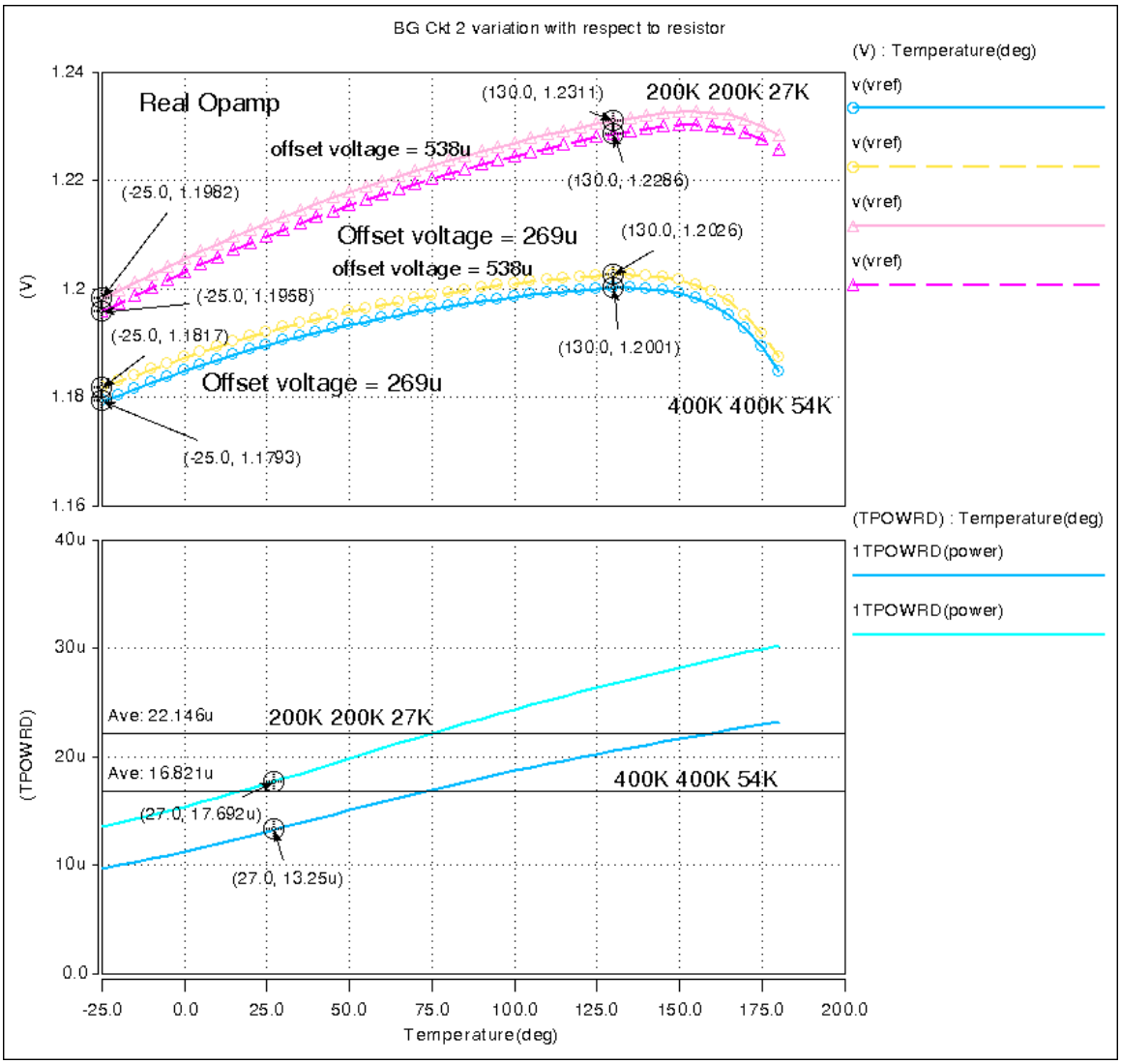


Figure 30HSPICE simulation of Bandgap reference topology 2, variation with change in resistors, but keeping the ratio constant

Results with real opamp

Offset voltage	Resistors used	At -25°C	At 130°C	Deviation due to temperature	Deviation due to resistors at-25&130°C	
269uV	2*400K 54K	1.1793	1.2001	20.8mV		
	2*200K 27K	1.1958	1.2286	32.8mV	16.5mV	28.5mV
538uV	2*400K 54K	1.1817	1.2026	20.9mV		
	2*200K 27K	1.1982	1.2311	32.9mV	16.5mV	28.5mV*

When the resistance values were reduced to half, the change in the average power = 22.146-16.821 µW = 5.325µW.

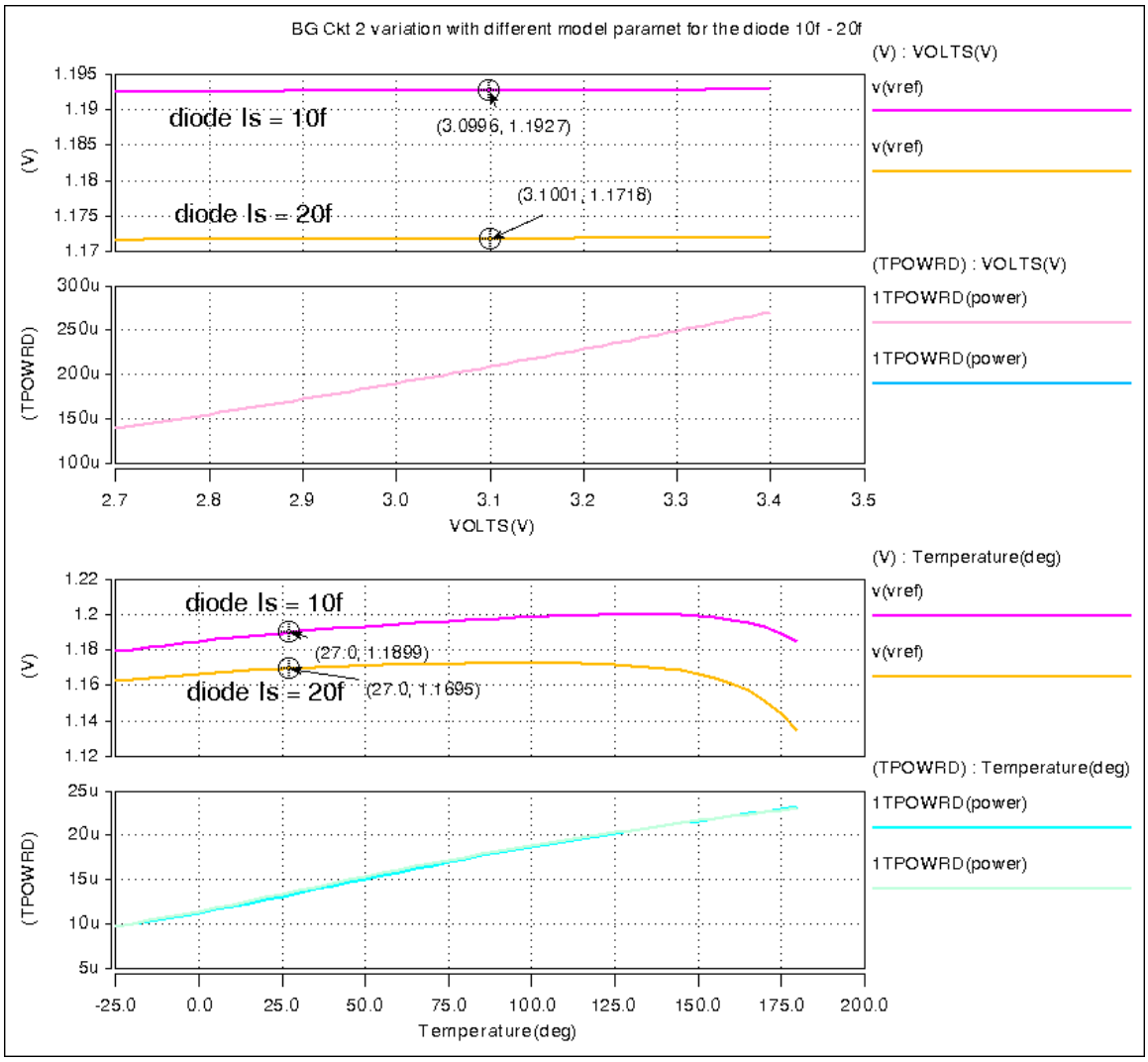


Figure 31HSPICE simulation of Bandgap reference topology 2, variation with change in diode parameters Is 10f - 20f

The deviation with respect to change in diode parameter, at room temperature: 1.1899-1.1695 V = 20.4mV.

The variation should be $\ln(2)*V_{TH} = 0.69*26mV \approx 18mV$

Power, when simulated with diode remains the same

Summary: The summary of the results (for a real opamp case) are shown in the following three tables. Table1 shows the resistor and p-channel transistor values.

Table 1

	Values (resistor/p-channel) used				
Topology	M1 (W/L)	R0	R1	R2	R3
1(a)			400K	400K	54K
1(b)		150K	100K	100K	54K
2	60/6		400K	400K	54K

Table2 compares the deviations of the topologies with different parameters.

Table 2:

	Deviation with respect to			
Topology	Temperature -25^{o}C to 125 ^{o}C	Power supply 2.7V to 3.4V	Offset +269.2µV	Diode parameter Is from 10f-20f (at room temp)
1(a)	12.8mV	0.2mV	2.4mV	21mV
1(b)	12.4mV	0.25mV	3.2mV	21mV
2	20.8mV	0.3mV	2.5mV	20.4mV

Table3 compares the performance of the topologies when resistors were halved keeping ratio constant.

Table 3

		Topology 1a				Topology 1b				Topology 2			
		Deviation due to				Deviation due to				Deviation due to			
Offset voltage **	Resistors used	temperature -25 to 125°C (mV)	resistors at -25 and 125°C (mV)		Average Power over temp (µW)	temperature -25 to 125°C (mV)	resistors at -25 and 130°C*(mV)		Average Power over temp (µW)	temperature-25 to 130°C *(mV)	resistors at -25 and 130°C*(mV)		Average Power over temp (µW)
269uV	Actual version	12.8			199.21	12.4			199.21	20.8			16.8
	Halved version	23.6	16.7	27.5	199.21	21.9	16.5	25.9	199.21	32.8	16.5	28.5	22.1
538uV	Actual version	12.8				12.4				20.9			
	Halved version	23.6	16.7	27.5		21.9	16.5	25.9		32.9	16.5	28.5	

* The upper limit value was calculated at 130°C, but the values are reasonably constat from 125°C to 130°C.
** The opamp has an offset voltage of 269uV.

Results are shown in more detail after each plot on pages 22-33.

The Key Performance parameters of the opamp used for the project were the following:

- offset voltage: 269.2μV
- The phase margin: 52°.
- Unity Gain bandwidth: 11.8MHz
- Gain: 10K
- Poles are located at 1630Hz and 25.1MHz
- The open loop output impedance is 461KΩ

Conclusions: The three topologies function as predicted by theory. The results match with the predictions: when resistances were reduced to half and also when the diode model parameter current Is was changed from 10f to 20f.
Observations:

1. The simulations show that the results are process dependent; these results are valid for 0.5um process.
2. To achieve more accurate results, we need precise diode models.
3. The power of the opamp dominates the power in all the topologies. If a less power Bandgap circuit is needed, the current in the opamp has to be reduced.
4. When the resistance values were reduced to half, there was no change in the power of the topologies (with the resistances I used), except for topology 2. There was a power difference of about 5.325μW.
5. HSPICE simulations reveal that topology 2 has less the output impedance than topologies 1a and 1b. Therefore it can be concluded that topology 2 has a better driving capability.
6. The Average power of topology 2 was found to be 16μW, while topologies 1a and 1b were 199.21μW.

Acknowledgements:
I would like to take this opportunity to thank Dr Fischer and others who have assisted me in completing this project.

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Future work:

1. Implementing a current-mode Bandgap reference circuit. Following figure (32) shows a current-mode Bandgap reference circuit. The concept of a Current-mode Bandgap reference is to generate two currents, proportional to V_f and V_{TH}. The reference voltage is the drop across the resistor R4.

$$V_{ref} = R_4\left(\frac{V_f}{R_2} + \frac{dV_f}{R_3}\right)$$

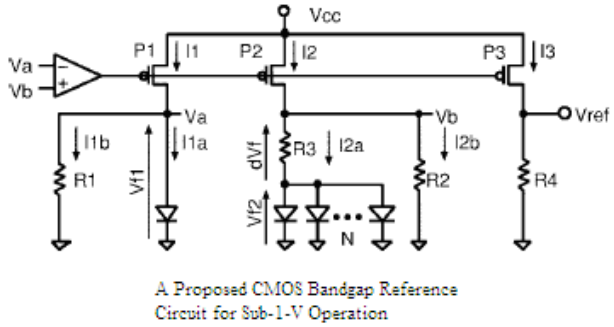

Figure 32 current-mode Bandgap reference circuits

If the resistor and diode parameters for this BGR are the same as those for the conventional Bandgap reference circuit (topology 2, figure (11)), the reference voltage can be written as:

$$V_{ref} = \frac{R_4}{R_2} V_{ref\_conventional}$$

2. Perform a Layout of a diode in magic. Simulate the topologies with the parameters obtained from the layout to see how the results are affected.
3. Perform some Noise analysis on the different topologies. The following figure shows output-noise (onoise) and input-noise(inoise) of the opamp.

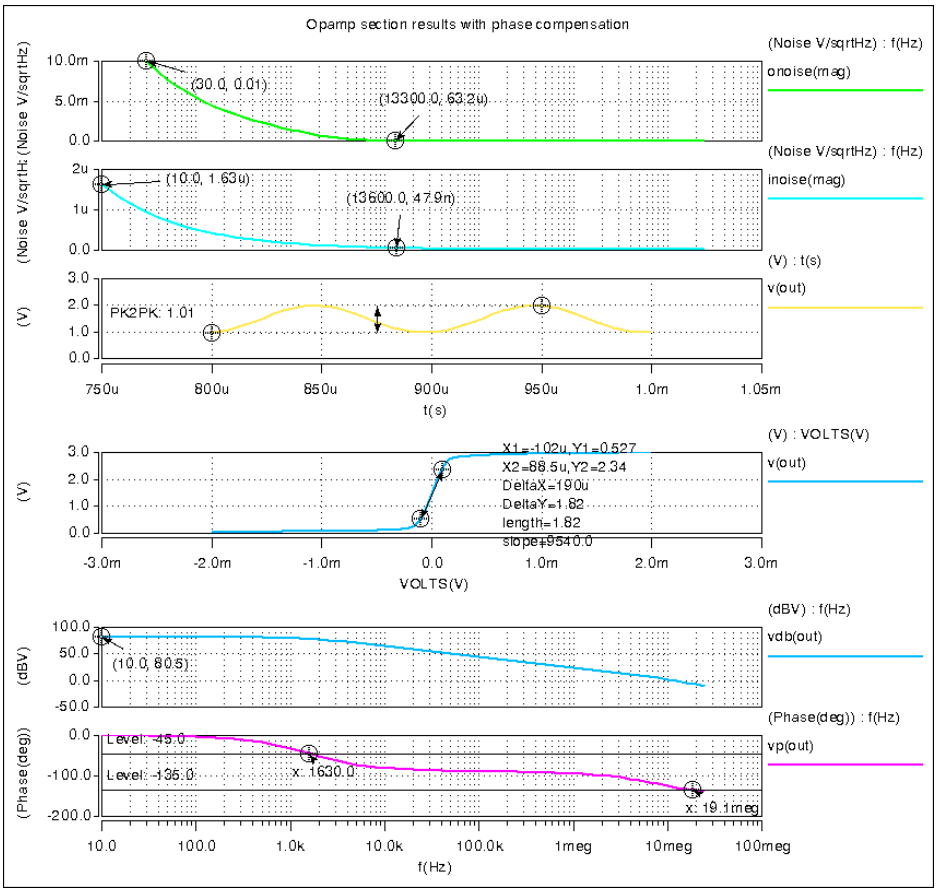

Figure 33 plots showing the performance parameters of the opamp

Implementing Bandgap Reference circuits for a wide range of temperature:
If the reader is interested in a Bandgap reference circuit which has to function over a wider range of temperature please refer to [9]. In this configuration, bipolar transistors are realized using buried doped layer. The following figure (34) shows the implementation:

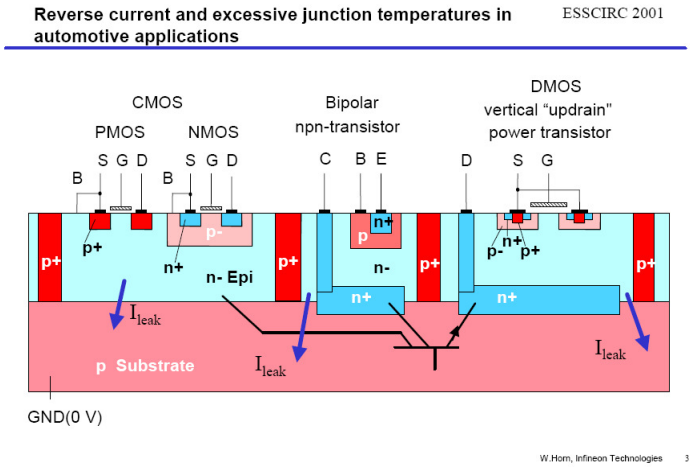

Figure 34Realizing Bipolar transistors with buried layers