A CMOS supply-insensitive with 13ppm/°C temperature coefficient current reference

Conference Paper *in* Midwest Symposium on Circuits and Systems · August 2014

DOI: 10.1109/MWSCAS.2014.6908455

CITATIONS
3

READS
478

3 authors, including:

Degang Chen
Iowa State University
284 PUBLICATIONS **3,616** CITATIONS
SEE PROFILE

Randall L Geiger
Iowa State University
207 PUBLICATIONS **2,240** CITATIONS
SEE PROFILE

A CMOS Supply-Insensitive with 13ppm/°C Temperature Coefficient Current Reference

Yen-Ting Wang, Degang Chen, Randall L. Geiger

Dept. of Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010
yentingw@iastate.edu

***Abstract*— A simple all CMOS low temperature coefficient current reference is designed. Two opposite temperature coefficient supply-insensitive self-bias reference generators that have a function of threshold voltage, mobility and resistor are utilizing to compensate the first-order and second-order temperature curvature. The proposed circuit is designed in AMI 0.5µm process with 5V supply voltage over the temperature range of -45°C to 125 °C. The proposed circuit achieves a 16µA current with temperature coefficient of 13ppm/°C, the supply variation of the designed current is ±1.2% over ±10% V_{DD} change and the accuracy over process variation is ±4.1%.**

Keywords—Current reference, temperature insensitive

I. INTRODUCTION

Voltage and current references are the most key building blocks in the analog circuitry such as amplifies, oscillators, phase-locked loops (PLLs) and analog-to-digital converters (ADCs). A reliable reference should be insensitive to supply voltage, temperature and process that is more accurate and stable than an ordinary voltage or current source. Also, the reference should be automatically on when the voltage supply switches on, so a self-bias mechanism should be a built-in characteristic. The research on designing precise reference circuits have been developed for decades and many approaches has been made in voltage or current domain[1-3], an as low power and low voltage is a trend in emerging process, most recently researches emphasis on minimize the temperature dependency.

Bandgap reference [1,2,4] is a well-known voltage reference, and a current reference can be generated from the voltage reference by applying a Ohmic component for voltage-current conversion. However, The BJT in the CMOS process is a parasitic lateral bipolar which does not have the accurate model, and also, this kind of structure normally needs an Opamp and thus increase the requirements for both power and area. Most designs without BJT are using mobility and threshold voltage to compensate the temperature dependency for each other [3]. And some other paper design the current reference in the weak-inversion for very-low power design.[6-8].

In this paper, we proposed the current reference that combines two opposite temperature coefficient current and obtain an extremely low temperature coefficient current by resistor, mobility and threshold voltage. Section II introduces a positive temperature coefficient (PTC) generator and a negative temperature coefficient (NTC) generator respectively. Section III presents the proposed reference circuit and the simulation results comes in the section IV. Section V discuss the calibration to gain a better performance. Then, a brief conclusion is given in the Section IV.

II. TEMPERATURE SENSITIVE CIRCUIT

A pure temperature insensitive reference generater circuit is difficult to obtain, but there are several temperature dependent componant that has a monotonic characteristic with temperature. PN junction in the BJT or MOS transistor, electron mobility, threshold voltage of the MOS transistor, or resistors. Some of them have PTC, and others have NTC. Therefore, a temperature insensitive current reference can be generated by combining two opposite temperature coefficient current. A PTC and NTC current generator are introduced and analyzed in the rest of section.

A. Positive Temperature Coefficient Bias Generator

The Widlar current source [1] also called Beta-multiplier reference (BMR) [9] is well known self-stabilized circuit to build a supply insensitive bias generator as shown in Fig. 1. The current is defined by the design parameter, Resistor R_3, and the ratio K between M_1 and M_2 .Assume the current ratio between M_4 and M_5 is 1 and the size ratio between M_1 and M_2 is K and channel length effect is neglected so that the current

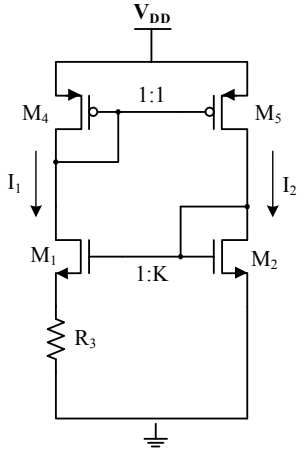

Fig. 1 Widlar bias generator

can be described as

$$I_1 = I_2 = I_{PTC} = \frac{2}{R_3^2 \mu_n C_{OX} \frac{W_2}{L_2}} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (1)$$

where I_1 and I_2 are the drain current of M_1 and M_2, R3 is a temperature dependent resistor

$$R = R_0\left[1 + \alpha(T - T_{NOM})\right] \quad (2)$$

where α is a process and material dependent parameter and has positive value and μ_n is the mobility which is a temperature dependent process parameter and is modeled by the equation

$$\mu_n = \mu_0 \left(\frac{T}{T_{NOM}}\right)^{UTE} \quad (3)$$

where UTE is the mobility temperature exponent [10], typically between -2 and -1, and μ_0 is the mobility when T_{NOM} =300K.

Take the derivative of the reference current respect to the temperature, it can be described as

$$\begin{aligned} \frac{dI_{PTC}}{dT} &= \frac{d}{dT} \cdot \left[\frac{2\left(1 - \frac{1}{\sqrt{K}}\right)^2}{\left\{R_0[1+\alpha(T-T_{NOM})]\right\}^2 \mu_0 \left(\frac{T}{T_{NOM}}\right)^{UTE} C_{OX} \frac{W_2}{L_2}} \right] \\ &= \frac{2\left(1 - \frac{1}{\sqrt{K}}\right)^2}{R_0^2 \mu_0 C_{OX} \frac{W_2}{L_2}} \cdot \left[\frac{-2\alpha \left(\frac{T}{T_{NOM}}\right)^{-UTE}}{[1+\alpha(T-T_{NOM})]^3} + \frac{-UTE\left(\frac{T}{T_{NOM}}\right)^{-UTE-1}}{[1+\alpha(T-T_{NOM})]^2} \right] \end{aligned} \quad (4)$$

Both resistor and mobility are affected by the temperature, but the temperature coefficient of the resistor could be choose to be much smaller than the temperature coefficient of the mobility, so the current is dominant by the negative UTE which eventually becomes a PTC current.

The current has a convex nonlinearity due the temperature coefficient of the resistor in the denominate term. Although the current is inherently nonlinear, it could be beneficial to the final results which will be described in detail in the simulation results.

B. Nagative Temperature Coefficient Generator

An inverse-Widlar circuit is a variation of the Widlar bias generator where the resistor has been placed in the other side and is series to the diode-connected transistor M_2 as shown in Fig. 2(a). However, it does not exist in the real world since the operating point is unstable. Base on the small signal analysis, the loop gain can be express as

$$Loop\ gain\ (a) = \frac{g_{m1}}{g_{m4}} \times g_{m5}\left(\frac{1}{g_{m2}} + R_3\right) \quad (5)$$

where g_m is the small-signal transconductance. If assuming the current ratio of M_4 and M_5 is 1, then g_{m4} equals to g_{m5} which are cancelled out, and g_{m1} has to be greater than g_{m2} to let the transistors operate in the saturation region and maintain power supply insensitivity. Therefore, the overall loop gain is greater than one, so the circuit is unstable.

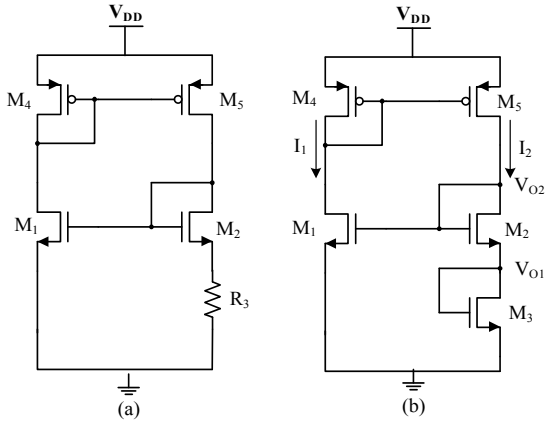

Fig. 2 Inverse-Widlar bias generator

The resistor can be replaced by a diode-connection transistor as shown in Fig.3 (b) to reduce the loop gain. This stable five-transistor inverse-Widlar circuit is used to be a threshold voltage based temperature sensor [11] since it has linear temperature coefficient. Base on the square-law model, and assume the channel length effect is ignored, analytical expressions are given below

$$I_2 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 \left(V_{O2} - V_{O3} - V_{THN}\right)^2 \quad (6)$$

$$I_2 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_3 \left(V_{O3} - V_{THN}\right)^2 \quad (7)$$

$$I_1 = I_2 = I_{NTC} \quad (8)$$

$$I_{NTC} = \frac{1}{2}\mu_n C_{OX}\left[\left(\frac{\sqrt{(W/L)_1}}{1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}} - \sqrt{\frac{(W/L)_1}{(W/L)_3}}}\right) V_{THN}\right]^2 \quad (9)$$

, and the BSIM model of threshold voltage V_{THN} [3] is also given below

$$V_{THN}(T) = V_{THN0} + (KT1 + KT1L \times \frac{L}{L_{eff}} + KT2 \times V_{bseff}) \times \left(\frac{T}{T_{NOM}} - 1\right) \quad (10)$$

where *KT1* is the temperature coefficient for threshold voltage, *KT1L* is the channel length dependence of the temperature coefficient for threshold voltage, and *KT2* is the Channel length dependence of the temperature coefficient for threshold voltage. By replacing μ_n and V_{THN} with Eq. (2) and Eq. (10), and ignore channel-length effect (*KT1L*=0) and Body effect (*KT2*=0), the current becomes

$$\begin{aligned} I_{NTC} &= \theta\left(\frac{T}{T_{NOM}}\right)^{UTE} \cdot \left[V_{THN0} + KT1 \times \left(\frac{T}{T_{NOM}} - 1\right)\right]^2 \\ &= \theta\left[\left(V_{THN0} - KT1\right)^2 \cdot \left(\frac{T}{T_{NOM}}\right)^{UTE} + 2 \cdot KT1 \cdot (V_{THN0} - KT1) \cdot \left(\frac{T}{T_{NOM}}\right)^{UTE+1} + KT1^2 \cdot \left(\frac{T}{T_{NOM}}\right)^{UTE+2}\right] \end{aligned} \quad (11)$$

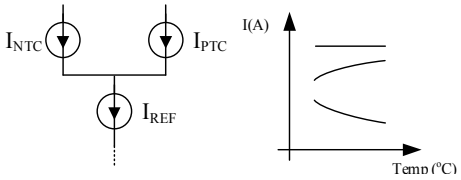

Fig. 3 Current summing diagram

where $\theta = \dfrac{\frac{1}{2}\cdot \mu_0 C_{ox}^{\ 2}}{\left(\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}} - \frac{1}{\sqrt{(W/L)_3}}\right)^2}$.

The temperature sensitivity of the current is also given

$$\frac{dI_{NTC}}{dT} = \theta \left(\begin{array}{c} UTE\left(V_{THN0} - KT1\right)^2 \left(\frac{T}{T_{NOM}}\right)^{UTE-1} + (UTE+2)KT1^2 \left(\frac{T}{T_{NOM}}\right)^{UTE+1} \\ +2(UTE+1)KT1(V_{THN0} - KT1)\left(\frac{T}{T_{NOM}}\right)^{UTE} \end{array} \right). \quad (12)$$

The temperature characteristic depends on process where some UTE equals to -1 or -2 will let some term disappear, and may contribute some convex nonlinearity but it is still dominant by a negative value.

III. Temperature Insensitive Current Reference

The temperature insensitive current reference now can be generated by adding two opposite temperature coefficient current as the block diagram shown in Fig. 3.

PTC current and NTC current are obtained from Widlar and five transistor inverse-Widlar bias generator respectively. Since PTC havs concave second-order nonlinearity, and the NTC has convex second-order nonlinearity. Summing those two current can compensate both first order and second order temperature coefficient to generate a very low temperature coefficient current. Cascode current mirror are using for both current generator to improve the power supply rejection and two additional current mirrors are added to realize the summing circuit as shown in the Fig. 4.

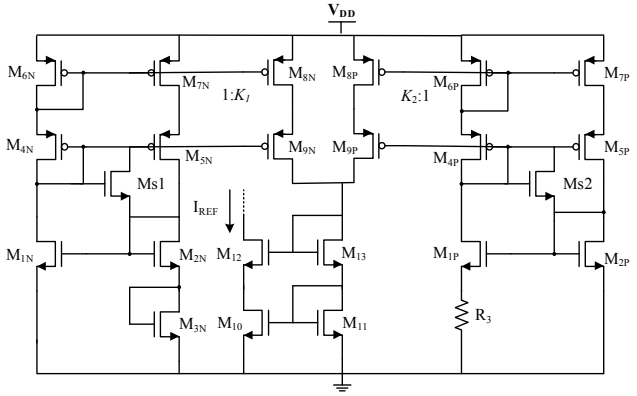

Fig. 4 Proposed current reference

The current ratio K_1 and K_2 depends on the sensitivity of each current, and the relationship

$$K_1 : K_2 = \frac{dI_{PTC}}{dT} : \frac{dI_{NTC}}{dT} \quad (13)$$

is maintained to keep the least TC of the reference current.

Startup circuits are needed for both circuits since both of them have the zero state which may not startup correctly and will let the circuit be malfunctioned unexpectedly after fabricate the chip.

IV. Simulation Results

The circuit is designed in AMI 0.5μm process, supplied by 5V and simulated from -40˚C to 125˚C. The mobility temperature exponent, *UTE*, is -1, the temperature coefficient of resistor is 1500ppm when the N^+ diffusion resistor is choosing, and *KT1* is -0.25, so the ratio of K_1 and K_2 is about 6.

A. Simulation results

The simulation results in the typical situation are shown in Fig.5. A 16μA reference current is generated by combining two opposite TC bias generator without the Opamp, As mentioned in the Section II, both PTC and NTC current are nonlinear; however, since two currents have opposite second order coefficient, the nonlinearity can be compensated, and obtained a flat, temperature insensitive current reference. The current variation is less than 35nA, and the TC is 13ppm/˚C within 165 ˚C range.

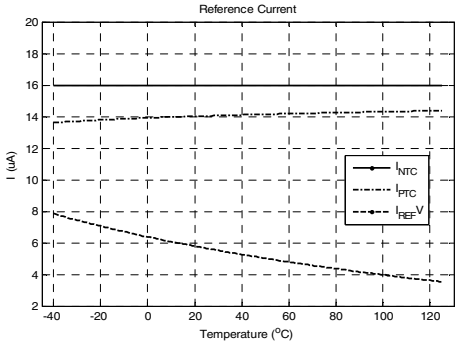

Fig. 5 Simulation results in typical

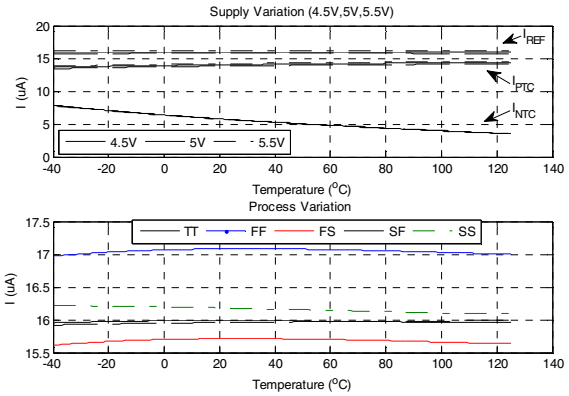

Fig. 6 Supply and process variation

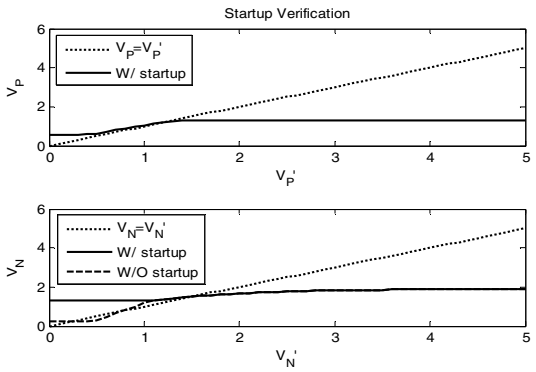

Fig. 7 Start-up verification

B. *Supply and process variation*

The supply and process variation is shown in the Fig. 6. The reference current varies about ±1.2% over the supply range of 4.5V to 5.5V, and shows about TC=20ppm/˚C at each voltage. The process variation varies ±4.1% over the all corners, and the worst case is about 40ppm/˚C in the fast NMOS slow PMOS corner.

C. *Start-up varification*

The start-up circuit is added and verified by Homotopy method [12]. For the Widlar circuit, the Homotopy method shows that there is only one operating point which means no start-up circuit is needed in the Fig. 7, yet a startup circuit is still included since the mismatch between transistors may still cause the change of the transfer curve and introduce the Trojan operating point. For the inverse-Widlar circuit, the Homotopy method shows the need of the a start-up circuit, and also show that the circuit has only one operating point after adding the start-up circuit.

V. CALIBRATION

The calibration is not needed for this circuit since the process variation is acceptable, but if the application circuit need high process insensitive requirement, then one-point trimming will improve the performance. The value of the threshold voltages and mobility changes with process variation results in the variation of the current reference, and thus degrade the performance. The simulation results show that the current may shift up or down in the different corner, and since there is no significant change of the slope and temperature coefficient, one-point calibration is sufficient to trim the current. Additional mirror array can be included to control the current mirror gain k_1 and k_2 and to increase or decrease the weighted current. As shown in the Fig. 8. The inaccuracy can be reduced to ±0.5% by one-point trim over the process corner after one-point trim at 40 ˚C.

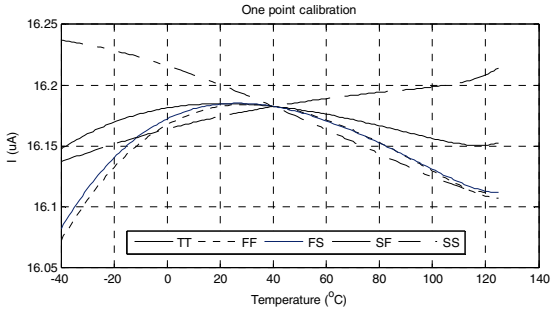

Fig. 8 One-point Calibration

VI. CONCLUSION

A current reference nearly independent on temperature and power supply variations has been proposed by using supply-insensitive self-bias reference generators as building blocks and current summing circuits to compensate the first-order and the second-order temperature effects. Temperature coefficient of 13ppm/ ˚C is obtained for a 16μA current with ±4% over process variation without trimming. This current reference is suitable for highly accuracy application.

REFERENCES

[1] R. J. Widlar, “Low-Value Current Source for Integrated Circuits” US Patent Number 03320439, Filed May 26, 1965, Granted May 16, 1967

[2] K. E. Kuijk, "A precision reference voltage source," *Solid-State Circuits, IEEE Journal of* , vol.8, no.3, pp.222,226, June 1973

[3] W.M. Sansen, F Op't Eynde, M. Steyaert, "A CMOS temperature-compensated current reference," *Solid-State Circuits, IEEE Journal of* , vol.23, no.3, pp.821,824, June 1988

[4] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation", *IEEE J. Solid-State Circuits*, vol. 34, pp.670 -674, 1999

[5] C.-H. Wang, C.-F. Lin, W.-B. Yang, Y.-L. Lo, "Supply voltage and temperature insensitive current reference for the 4 MHz oscillator," *Integrated Circuits (ISIC), 2011 13th International Symposium on* , vol., no., pp.35,38, 12-14 Dec. 2011

[6] Hande, V.G.; Baghini, M.S., "Design of voltage reference with low sensitivity to process, supply voltage and temperature variations," *Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on* , vol., no., pp.89,92, 4-7 Aug. 2013

[7] T. Shima, "Temperature insensitive current reference circuit using standard CMOS devices," *Circuits and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium on* , vol., no., pp.181,184, 5-8 Aug. 2007

[8] J. Lee, S. Cho, "A 1.4-μW 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18-μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol.47, no.10, pp.2527,2533, Oct. 2012

[9] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., Wiley, 2010, pp.624–625.

[10] X. Xi, M. Dunga, J. He, W.Liu and C. Hu, BSIM4.3.0 MOSFET Model Users’ Manual. Berkeley, CA: Univ. California, 2001, pp. 12-1

[11] C. Zhao, Y.-T. Wang, D. Genzer, D. Chen, R. Geiger, "A CMOS on-chip temperature sensor with −0.21°C 0.17 °C inaccuracy from −20 °C to 100 °C," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.2621,2625, 19-23 May 2013

[12] Y.-T. Wang, D. Chen, R. Geiger., "Practical methods for verifying removal of Trojan stable operating points," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.2658,2661, 19-23 May 2013