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A Fully-Integrated CMOS LDO Regulator for Battery-Operated On-Chip Measurement Systems

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Abstract

This paper presents a fully-integrated 0.18 µm CMOS low drop-out (LDO) regulator designed to drive on-chip low power front-end sensor nodes. The proposed LDO is based on a simple telescopic amplifier stage with internal cascode compensation driving a PMOS pass-device, providing a high precision 1.8 V output voltage for input voltages from 3.6 V to 1.92 V up to a 50 mA load current with only 22 µA quiescent current. Line and load regulation are respectively better than 0.017 mV/V and 0.003 mV/mA, while recovery times are below 4 µs over a (-40 ºC, 120 ºC) temperature span.

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Keywords: Voltage regulator; low drop-out (LDO); CMOS design; System-on-Chip (SoC); power management; portable sensing devices.

1. Introduction

The portable sensor market is pushing towards complete system-on-chip (SoC) solutions. To achieve this, one increasingly important subsystem, especially in autonomous battery powered sensing devices is the power management unit (Fig.1 a), where low drop-out regulators play a key role: they must deliver a stable power supply V_{out} under variations of load current I_{Load} and battery voltage V_{BAT}. This work presents the design in a 0.18 µm CMOS technology of a fully integrated LDO regulator to power both the read out and actuation electronics of a battery-compatible front-end sensor interface based on phase-sensitive detection (PSD) [1]. Accordingly, design specifications

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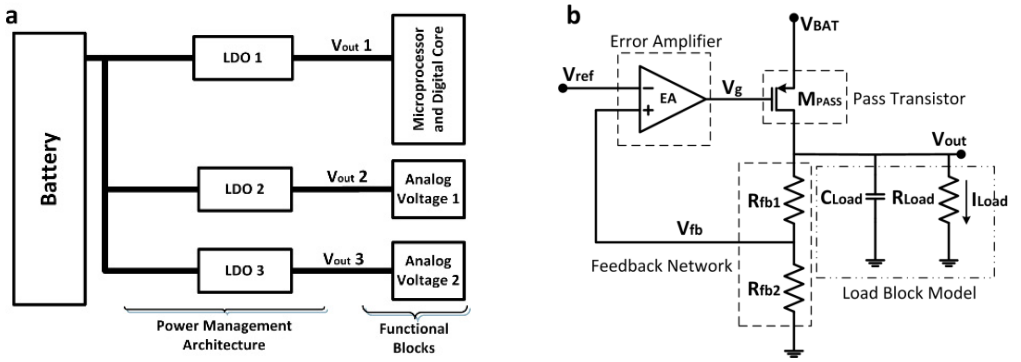

Fig. 1. (a) Block diagram of a typical power delivery system; (b) Conventional topology of a LDO voltage regulator.

are: an output voltage of 1.8 V from a 3.6 V – 2.1 V battery-compatible input voltage range, with a maximum load current of 50 mA over a 50 pF maximum capacitive load. Besides, it must comply with the two critical requirements of portable systems, i.e. reduced area and quiescent current, while maintaining good regulating performance, stability and fast response times, a challenging task with an on-chip approach avoiding the use of an external compensation capacitor [2]. The paper is organized as follows. Section 2 presents the proposed CMOS LDO architecture satisfying the specifications given by our target application. Section 3 summarizes the main achieved performances. Finally, conclusions are drawn in Section 4.

2. LDO Architecture

Fig. 1 b shows the classical topology of a CMOS LDO regulator, which provides a stable voltage V_{out} from a variable power supply V_{BAT} to properly bias the corresponding electronic system, modeled by a load current I_{Load} and a load capacitor C_{Load}. It consists of a voltage reference V_{ref}, an error amplifier (EA), a PMOS transistor as the pass element between the variable voltage V_{BAT} and the stable voltage V_{out}, and a resistive feedback network $R_{fb1} - R_{fb2}$ [3]. The circuit operates as follows: the feedback network samples the output voltage V_{out}; the error amplifier compares this feedback signal V_{fb} with a bandgap reference voltage V_{ref}, and generates an error signal that continuously drives the gate of the pass transistor to keep a constant V_{out} independently of V_{BAT} and I_{Load}:

$$V_{out} = \left(1 + \frac{R_{fb1}}{R_{fb2}}\right) V_{ref} \tag{1}$$

Following this scheme, the proposed LDO voltage regulator is shown in Fig. 2. It has been implemented in the UMC 0.18 μm 1P-6M CMOS technology. The design of the main blocks at transistor level is next discussed, except for the voltage reference $V_{ref,}$ which is provided by an external 1.2 V bandgap reference.

2.1. Pass Transistor

Pass transistor size is a critical parameter determined by the maximum load current and the minimum dropout voltage V_{do} = ($V_{in,min}$ - V_{out}) requirements, resulting in a device requiring very large silicon area. With our specifications, its size results (W/L) = (9480 μm / 0.34 μm) to keep the transistor working in saturation for I_{Load} = 50 mA with V_{do} = 300 mV.

2.2. Feedback Network

Assuming, for I_{Load} = 0, a quiescent current through the PMOS pass transistor $I_{Rfb} = V_{out} / (R_{fb1} + R_{fb2})$ =10 μA to keep bounded the overall static power consumption, and with a 1.8 V output voltage (eq. 1), it is obtained R_{fb1} = 60 kΩ and R_{fb2} = 120 kΩ. These resistances are implemented as active resistances using three identical PMOS transistors in diode configuration to optimize area: this solution reduces in a factor 3 the conventional passive solution using a high resistive polysilicon layer given by the technology ($R_{□}$ = 1039 Ω/square, W = 1 μm, L = 166.1 μm).

2.3. Error Amplifier

The EA must meet as specifications a high DC open loop gain, as the LDO line and load regulation are inversely proportional to the EA gain, and a low static current to minimize the power consumption [4]. The minimum gain required in order to have 0.1% output voltage accuracy is 60 dB. Besides, a maximum EA current budget of 10 µA is set as design specification. The configuration used is a telescopic OTA that provides a gain above 75 dB over all the operating 3.6 V – 2.1 V supply with a simple single-stage architecture, also characterized by a GBW > 330 kHz and PM = 90 ^{0} for a load capacitor determined by the parasitic pass transistor C_{gs} (12 pF – 20 pF).

2.4. Compensation Network

To obtain an on-chip solution it is necessary the use of internal compensation techniques. In this work, cascode compensation, using a single C_c = 8.5 pF capacitor as shown in Fig. 2, is adopted, thus achieving higher speed and power supply rejection (PSR) compared to the commonly used Miller compensation.

2.5. Transient behavior improvement

To enhance the transient behavior, a dynamically biased current sink path formed by a quasi-floating gate transistor M_{SINK} is added, which is only active when the load current varies from high to low, helping to discharge the path formed by (R_{fb1} + R_{fb2}) and C_{Load}.

3. Simulation Results

The regulation region ranges from V_{in} = 1.92 V to 3.6 V, i.e. the LDO has a dropout voltage of 120 mV over a (-40 ºC to 120 ºC) span. Fig. 3 shows the line regulation for I_{Load} = 50 mA (worst case) and Fig. 4 shows the load regulation for V_{BAT} = 2.1 V (worst case). Fig 5 shows the open loop frequency performance over all the operating conditions. Fig. 6 shows the full load transient response, with and without the proposed enhancement circuit. Table 1 summarizes the main performances of the proposed LDO regulator compared to previous implementations with similar specifications [2, 5, 6]. Our proposal attains significantly better regulation performance while keeps similar power, size and time response paramenters.

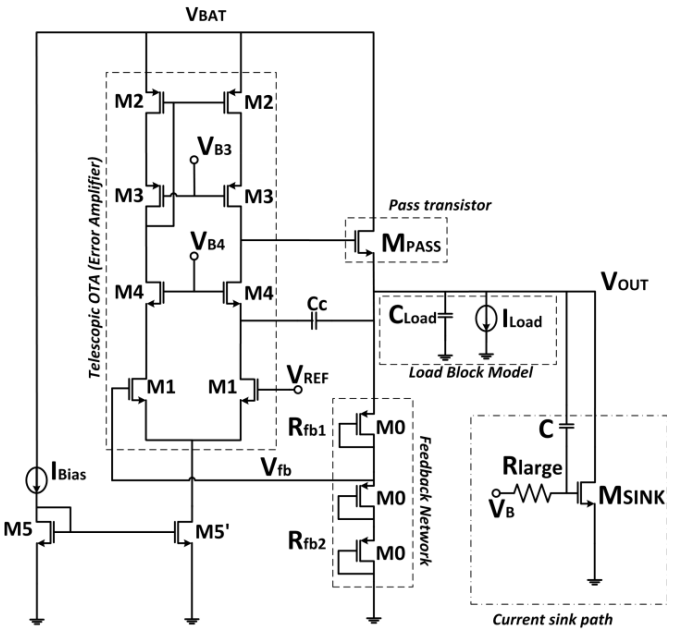

Fig. 2. Schematic of the proposed CMOS LDO.

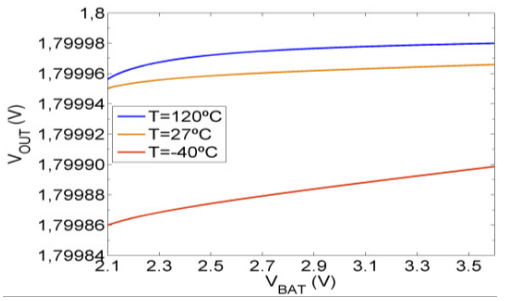

Fig. 3. Static line regulation, I_{Load} = 50 mA.

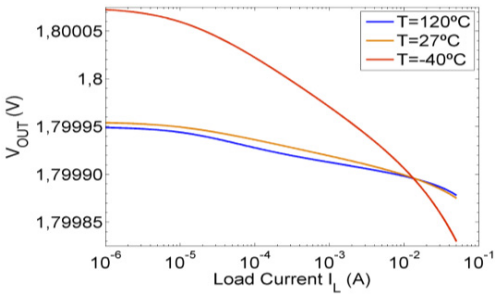

Fig. 4. Static Load regulation, V_{BAT} = 2.1 V.

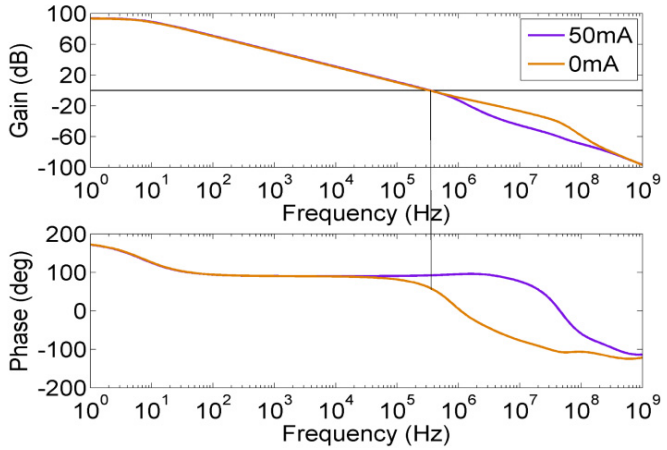

Fig. 5. Open-loop frequency response, V_{BAT} = 2.1 V.

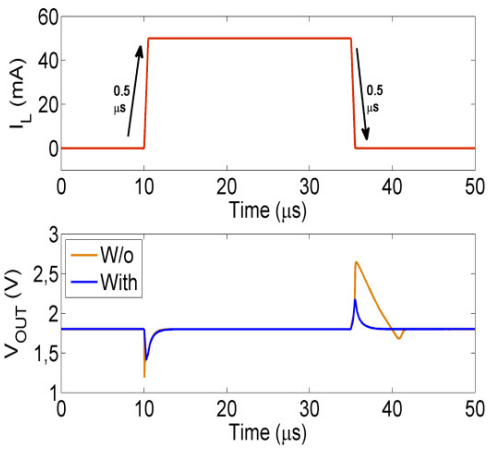

Fig. 6. Full load transient w/o and with current sink path, V_{BAT} = 3.6 V.

Table 1. Comparison of CMOS capacitor-less LDO performances.

Parameter	This work, sim	[2], 2007, exp	[5], 2011, exp	[6], 2014, sim post-layout
CMOS Technology (µm)	0.18	0.35	0.35	0.18
V_{in} (V)	1.92 – 3.6	3	1.642 – 5	2.1 – 3.3
V_{out} (V)	1.8	2.8	1.5	1.8
V_{do} (mV) @ $I_{Load,max}$	120 @ 50 mA	200 @ 50 mA	142 @ 100 mA	350 @ 70 mA
I_q (µA)	22	65	27	47
C_{Load} (pF)	50	100	100	50
Line Regulation (mV/V)	0.017	~23	1.046	0.24
Load Regulation (mV/mA)	-0.003	~0.56	0.0752	0.714
Full load settling time (µs)	4	15	1 (I_L:0 to 100 mA)	2
PSR (dB)	-62 @ 1 kHz	-57 @ 1 kHz	60.6 @ 1 kHz	-57 @ 1 kHz

4. Conclusions

A high precision low quiescent current LDO regulator to be used in portable sensing devices has been proposed and designed in a 0.18 µm CMOS process. Simulation results of its main static, dynamic and frequency properties validate the applied design strategies, successfully achieving the target specifications to attain a forthcoming SoC CMOS portable PSD measurement system.

Acknowledgements

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