A Low Voltage High Precision CMOS Bandgap Reference

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***Abstract* — In this paper, a low voltage bandgap reference with high precision is presented. Utilizing current mode structure, the minimum voltage of the proposed bandgap circuit can be reduced to 900 mV. Compensated with V_{EB} linearization technique, this bandgap reference can reach a temperature coefficient of 10 ppm/℃ in the range from 0 ℃ to 150 ℃. With 1.1-V supply voltage, the power is 47 uW and the PSRR is -55 dB at DC frequency. Occupying 0.186 mm^2 chip area, this bandgap reference has been verified in UMC 0.18um mixed mode CMOS Technology.**

I. INTRODUCTION

Since introduced in 1970s[1], [2], bandgap reference is widely used in analog and mixed-mode integrated circuits, such as data converters and DC-DC power converter. In CMOS bandgap reference design, low voltage and high precision are two important design criteria. Because of the common mode input voltage of the operational trans-conductance amplifier (OTA) and the bandgap voltage of silicon (about 1.25 V), conventional CMOS bandgap reference usually has a minimum voltage of 1.8 V. Several factors constrain the precision of bandgap reference, such as non-linearization of the emitter-base voltage (V_{EB}) in BJT, the offset of the OTA and the non-zero temperature coefficient of resistors. So the temperature coefficient of bandgap reference without curvature compensation is usually greater than 30ppm/℃. To solve the first problem, lots of researchers developed different kinds of method. Yueming Jiang and Edward K. F. Lee took the place of OTA with a operational trans-impedance amplifier[3], without the constraint of common mode input voltage of OTA, the circuit could work with a supply voltage of 1.2 V. H. Banba etc. and Ka Nang Leung etc. presented two different current mode structures which transformed the addition of two voltage to an addition of two current[4],[5]. The reference voltage generated by sum current is adjustable, breaking the constraint of bandgap voltage. To improve the precision, several high order curvature compensations have been introduced. Ka Nang Leung etc. developed a second-order curvature compensation utilizing resistors having opposing temperature coefficient[6]. Audy further proposed a third order curvature compensation based on series and parallel combinations of two kinds of resistors [7]. P. Malcovati etc. introduced a new method, which generated a nonlinear current to compensate the nonlinear V_{EB} of BJT[8].

The presented bandgap reference adopts current mode structure which can reduce supply voltage effectively. To get high precision, the V_{EB} linearization technique is applied to the bandgap reference. To reduce the systemic offset of the feedback OTA further, symmetric OTA is chosen.

This paper is organized as follows, section Ⅱ describes the basic principle and design challenges of CMOS bandgap reference. The section Ⅲ presents the low supply voltage high precision bandgap reference. In section Ⅳ, simulation and measurement results are presented, which is further compared with other bandgap references. Section Ⅴ is the conclusion of the paper.

II. PRINCIPLE AND DESIGN CHALLENGES OF CMOS BANDGAP REFERENCE

A. *Principle of CMOS bandgap reference*

The basic principle of CMOS bandgap reference is to compensate the negative-temperature-coefficient V_{EB} of BJT with a positive-temperature-coefficient voltage. The difference of V_{EB} of BJTs with different current density is proportional to absolute temperature (PTAT). A typical CMOS implementation is shown in figure 1. The output reference can be written as:

$$V_{REF} = V_{EB1} + (1 + \frac{R2}{R1}) \frac{KT}{q} \ln N . \quad (1)$$

Where R2A=R2B=R2, n is the ratio of emitter areas of Q1 and Q2, if the resistor ratio is proper, the second term which has positive temperature coefficient can cancel the negative temperature coefficient of V_{EB}.

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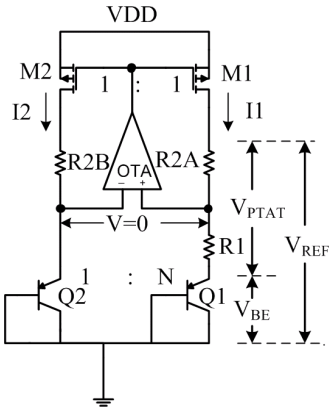

Fig. 1. A conventional CMOS bandgap circuit

B. Design challenge of CMOS bandgap reference

The V_{REF} is about 1.25 V when it is independent of temperature, so the minimum supply voltage is

$$\min\{V_{DD}\} = V_{REF} + V_{SDsat1} \qquad (2)$$

The common mode input range of the OTA also decides the supply voltage. When the OTA has a NMOS input stage:

$$\min\{V_{DD}\} = V_{EB2} + V_{DSsat} + V_{R2} \qquad (3)$$

When the input stage is PMOS:

$$\min\{V_{DD}\} = V_{EB2} + |V_{THP}| + 2V_{SDsat} \qquad (4)$$

Actually, the V_{EB} of BJT is nonlinear [8]:

$$V_{EB} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + (\eta - m)\frac{kT}{q}\ln\frac{T_r}{T} \qquad (5)$$

Where T is the absolute temperature, Tr is a reference temperature, V_G is the bandgap voltage of silicon, η is a constant depending on doping level, m is a constant depending on the temperature character of emitter current in BJT. So the output reference can not be purely temperature independent [5]. In CMOS technology, the offset of the OTA can reach 30 mV, which can not be neglected in circuit design. Counting offset in, the reference voltage can be modified to be [9]:

$$V_{ref} = V_{EB1} + \frac{R_1 + R_2}{R_1}(V_T \ln n - V_{OS}) \qquad (6)$$

Some other factors like non-ideal resistor, non-zero base current in BJT and mismatch between resistors also constrain the precision of output reference[10].

III. LOW VOLTAGE HIGH PRECISION BANDGAP REFERENCE

A. Current Mode and V_{EB} Linearization

To conquer the challenges described above, some new techniques must be applied to conventional bandgap reference. Current mode structure is a simple and effective method to reduce the supply voltage, the adjustable output reference is another advantage. The implementation is shown in the middle of figure 2 [4]. Because of the feedback loop, the nodes A and B have the same voltage, so the difference between V_{EB} of Q1 and Q2 is applied

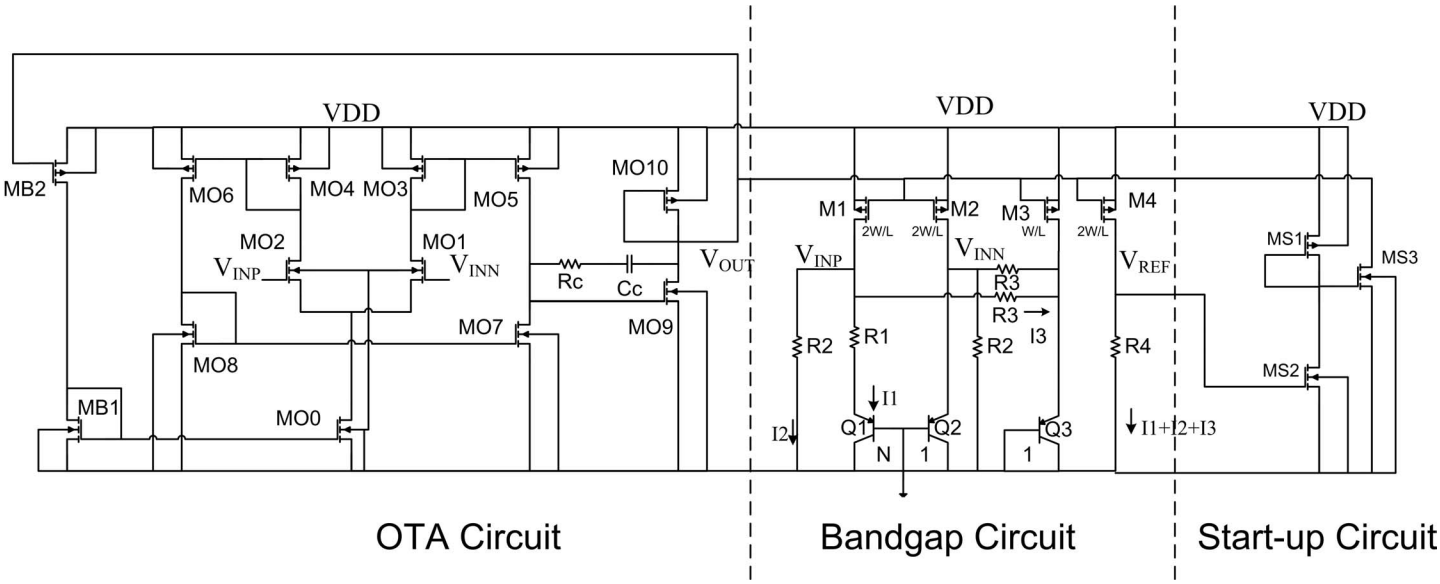

Fig. 2. The complete schematic of the proposed low voltage high precision bandgap reference

to R1. The current I1 is PTAT. Current I2 is proportional to V_{EB2}, which is approximately complementary to absolute temperature (CTAT). With a proper ratio of R1 to R2, the drain currents of M1~M4 are temperature independent. With a PTAT bias current, the V_{EB} of Q1 and Q2 are [8]:

$$V_{EB2} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + (\eta - 1)\frac{kT}{q}\ln\frac{T_r}{T} \quad (7)$$

While the V_{EB} of Q3 is [8]:

$$V_{EB3} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + \eta\frac{kT}{q}\ln\frac{T_r}{T} \quad (8)$$

The current I3 is nonlinear, can be used to linearize V_{EB} further:

$$I3 = (V_{EB2} - V_{EB3})/R3 = -V_T \ln(T_r/T)/R3 \quad (9)$$

The output reference is the voltage drop of sum current in resistor R4:

$$V_{REF} = (I1 + I2 + I3)R4 = [\frac{V_T \ln(N)}{R1} + \frac{V_{EB2}}{R2} - \frac{V_T \ln(\frac{T_r}{T})}{R3}]R4 \quad (10)$$

A temperature independent current can be gotten through Adjusting R1- R3, the output reference is adjustable because value of R4 is variable.

B. OTA Design

The feedback OTA circuit is shown in the left of figure 2. To improve the stabilization of OTA, the bias current of OTA is a copy of the current in transistors M1-M4, which is independent of supply voltage and temperature. Reducing the offset is the most important objective in OTA design. Offset consists of two parts: systemic offset and random offset. For random offset, two methods can be used: big size for input stage, common-centroid layout design. For systemic offset, the only solution is to choose a better structure. In CMOS differential OTAs, symmetric OTA has the least offset. Because in symmetric OTA, two input transistors have the same load (a diode-connected transistor), so the difference of V_{DS} between input transistors is the smallest in all differential OTAs.

C. Resistor Selection

Nonlinear behavior of V_{EB} leads to the finite temperature coefficient of V_{REF}. When resistors are implemented by lower-temperature-coefficient material, the term ln(Tr/T)*KT/q in equation 5 is smaller, leading to a better V_{EB} stabilization [11]. So the non-salicide N+ poly resistor is selected in this design.

D. Start-Up Circuit

To prevent bandgap circuit to work on zero working point, a start-up circuit formed by MS1-MS3 is needed, as shown in the right of figure 2. When the circuit works on zero working point, V_{REF} is zero, the gate voltage of MS3 is VDD-|Vthp|, which drives MS3 on, V_{OUT} is then pulled down, the circuit starts up to the normal working point. When the circuit works on the normal working point, choosing proper sizes of MS1-MS2, the gate voltage of MS3 is lower than threshold voltage, cutting off MS3, the start-up circuit does not affect working state of bandgap circuit.

E. Output Buffer

So as to drive a heavy load, ideal voltage reference has a zero output resistor. In the presented bandgap reference, the output resistor equates to R4, which is several hundreds thousands Ohms. A simple method to reduce the output resistor is to add an output buffer to the bandgap reference. The output buffer consisted of an operational amplifier with voltage-voltage negative feedback has infinite input resistor and near-zero output resistor.

IV. MEASUREMENT RESULT

The presented bandgap reference has been fabricated in UMC 0.18-μm mixed-mode process. The threshold voltage of this process is Vthn=0.31V, |Vthp|=0.46V at 0 ℃. The micrograph of the bandgap reference die is shown in figure 3. There are two bandgap core circuits in this die, with the upper one for test. Each bandgap circuit occupies 0.186 mm^2 chip area. The measured results of supply voltage dependences of the bandgap reference at 0, 30 and 100 ℃are shown in figure 4. It can be calculated that the line regulation is about 5.2mV/V in the worst case. The reason of that output reference varies with supply voltage is the finite gain of the feedback OTA. When voltage is higher than 2.6V, the gain falls down rapidly, causing a large rise in reference voltage. The measured temperature dependences of the bandgap reference with different supply voltages are shown in figure 5. In the range from 0℃ to 150℃, the best cases are when VDD=1.1V and VDD=1.2V, with a temperature coefficient of 10ppm/℃;the case of VDD=0.9V is the worst one with a temperature of 40ppm/℃; the case of VDD=1.0V and VDD=2.0V are in the middle, the temperature coefficient of which is 20ppm/℃.

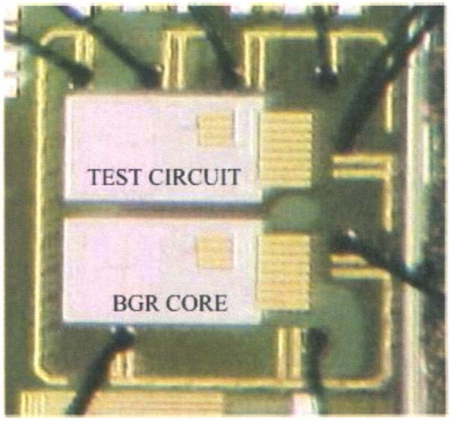

Fig. 3. The micrograph of the bandgap reference die

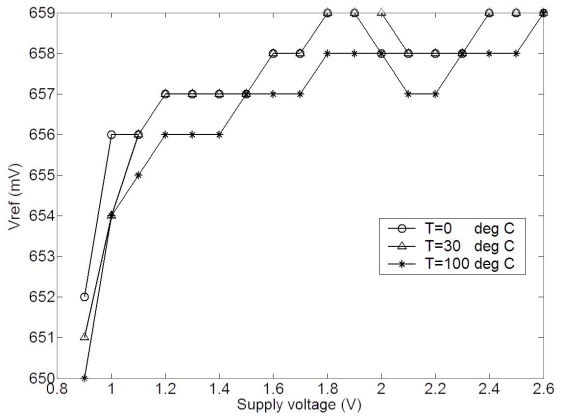

Fig. 4. Measured supply voltage dependences of the bandgap reference at 0, 30 and 100 ℃

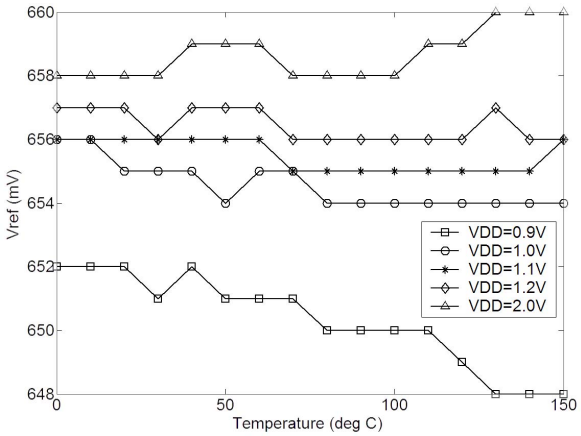

Fig. 5. Measured temperature dependences of the bandgap reference with different VDDs

The simulation and measurement performances are compared in table Ⅰ.

Table Ⅰ, Comparison of simulation and measurement performances

performance	Simulation	Measurement
Temperature coefficient	2ppm/℃-11ppm/℃	10ppm/ ℃ – 40ppm/℃
Line regulation	1.6mV/V	5.2mV/V
PSRR	-60dB@DC	-55dB@DC
Power	40uW	47uW

Table Ⅱ is a comparison with other reported low voltage, high precision bandgap references.

Table Ⅱ, Comparison of low-voltage high-precision bandgap references

	This work	Ka Nang leung etc. [5]	Malcovati etc. [8]
Process	0.18-um CMOS	0.6-um CMOS	0.8-um BICMOS
Threshold voltage	Vthn=0.31 V |Vthp|=0.46 V	Vthn=0.9 V |Vthp|=0.9 V	-
Best case voltage	1.1 V	0.98 V	0.95 V
Supply current	43 uA	18 uA	92 uA
Vref	657 mV	603 mV	536 mV
TC (best case)	10 ppm/℃	15 ppm/℃	19 ppm/℃

V. CONCLUSION

A below-1-V 10ppm/℃CMOS bandgap reference which is independent of supply voltage has been presented in this paper. Because of its low power (47uW) and high PSRR (-55dB), this bandgap reference is suitable for portable SOC applications. Since there is no special process used in this work, it is reproducible in any CMOS process. If needed, the supply voltage can be reduced further to $V_{EB}+|V_{DSsat}|$ (in this process is about 750mV). To further improve the temperature performance, carefully optimization of layout and OTA design is needed, other high order curvature compensations can also be utilized.

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