LDO REPORT

LDO DESIGN

- I designed the conventional LDO for: -

1- Output voltage of 1.8v.

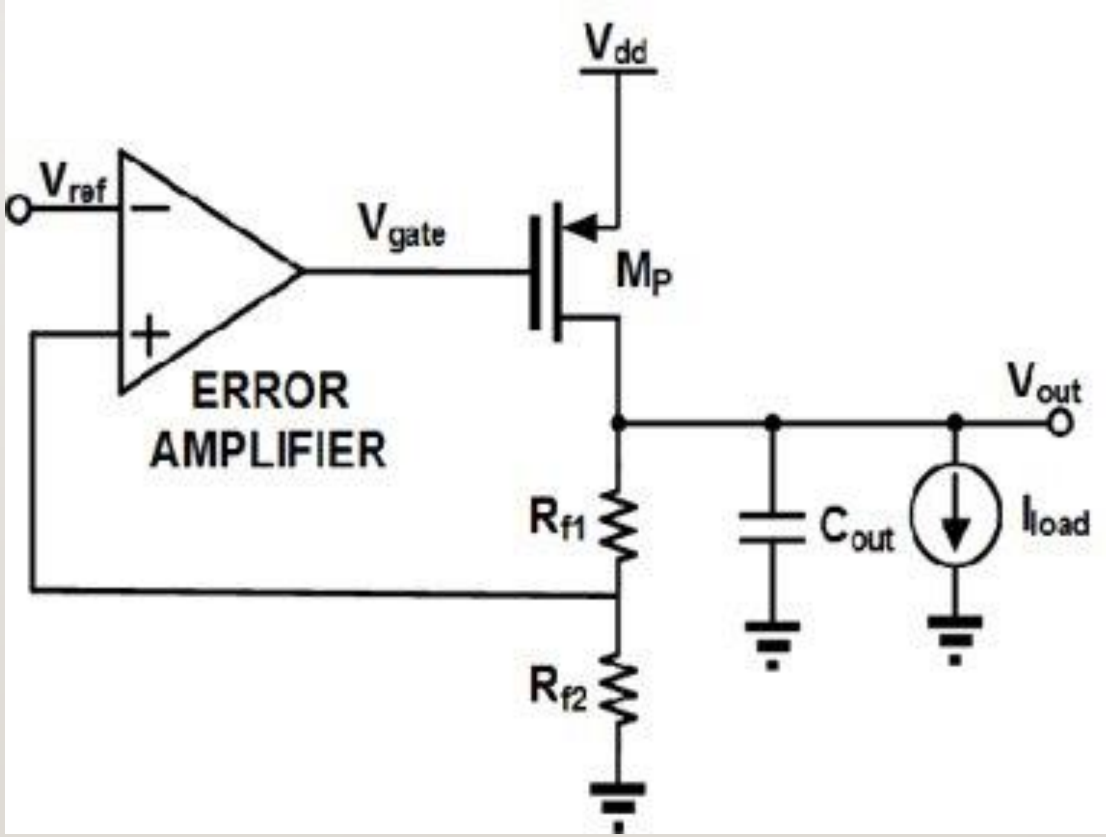
2- Input voltage from 1.8v to 2.2v.

3- Reference voltage of 1v.

4- Dropout voltage <= 0.1v

5- Maximum output current of 17mA.

6- Quiescent current of 12 uA.



LDO DESIGN STEPS

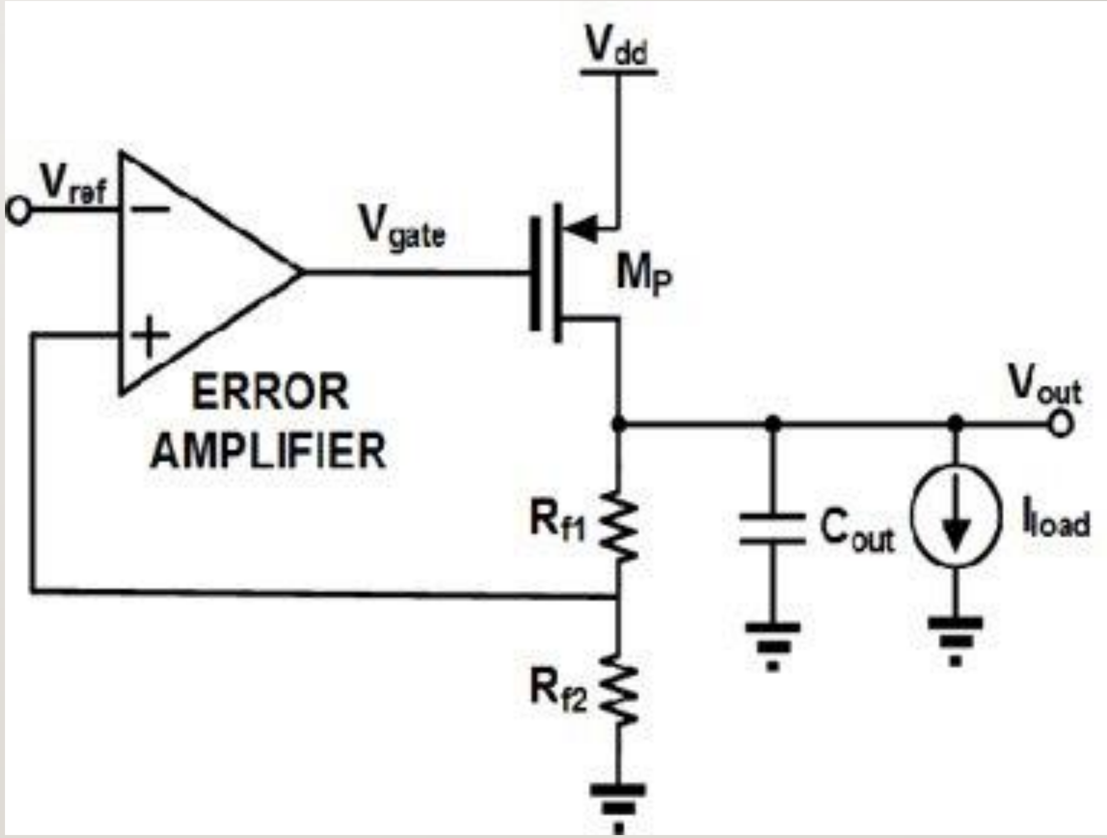
1- Feedback resistors design:

Vout = Vref (1 + Rf1/Rf2)

Vout = 1.8v and Vref =1v

so Rf1/Rf2 = 0.8

Let Rf1 = 80k and Rf2= 100k



LDO DESIGN STEPS

2- Pass transistor design: -

$$I_D = \frac{1}{2}\mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \Rightarrow \frac{W}{L} = \frac{I_D}{\frac{1}{2}\mu C_{ox} \cdot (V_{GS} - V_{TH})^2}$$

Id max = 17mA ,Vdo=0.1 and upCox = 42 u

So W/L)p = 40000

Let W=20u , L=0.5u and M= 1000

LDO DESIGN STEPS

3- Error amplifier design:-

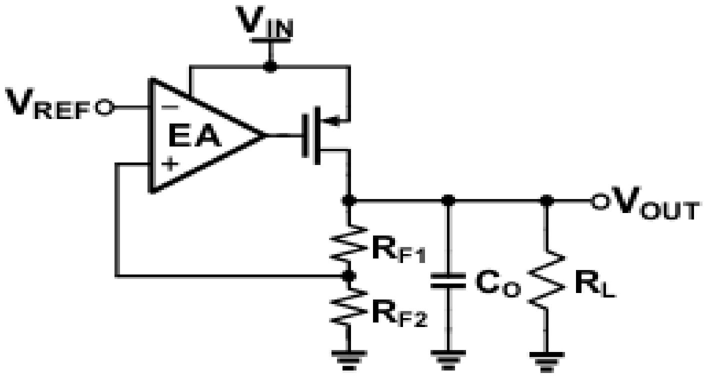
I used Two stage miller OTA.

4- Vref design:-

I used the Bandgap design to generate Vref.

LDO STABILITY

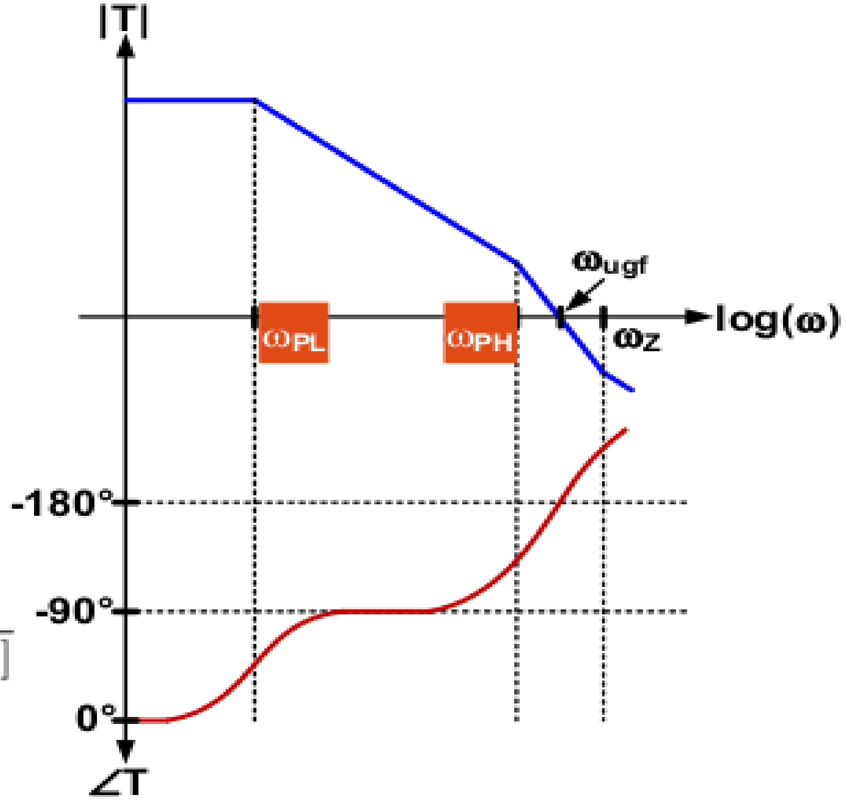
Approximate Pole Zero Locations



$$\omega_{PL} \approx \frac{1}{R_{OUT}.C_O}$$

$$\omega_{PH} \approx \frac{1}{R_{OEA}.[C_1 + g_{mp}.R_{OUT}.C_{gdp}]}$$

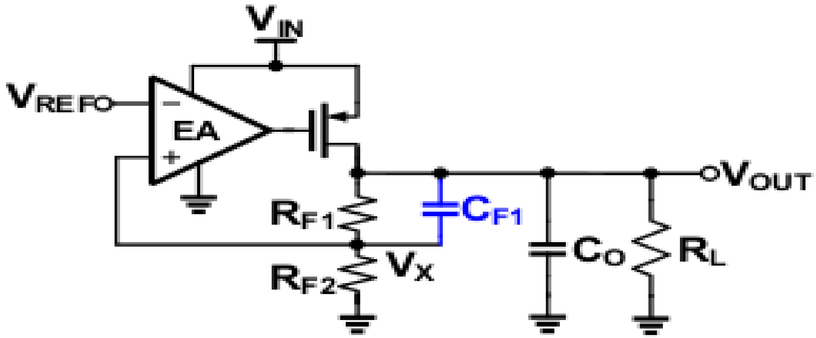
$$\omega_Z \approx \frac{g_{mp}}{C_{gdp}}$$



LDO STABILITY

Frequency Compensation – II[2]

- Introduce zero by adding feed-forward capacitor



$$\frac{V_X(s)}{V_{OUT}(s)} = \left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right)\cdot\left(\frac{1+sC_{F1}R_{F1}}{1+sC_{F1}(R_{F1}||R_{F2})}\right)$$

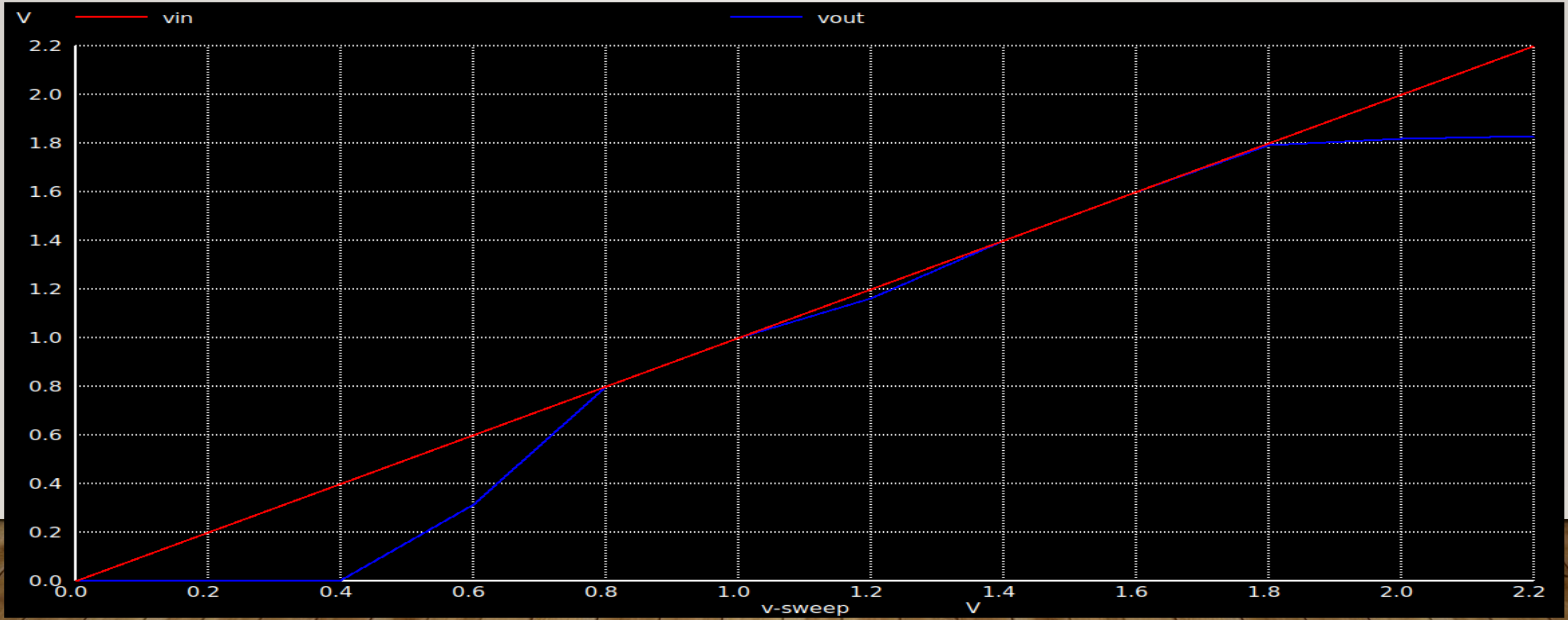
$$\boxed{\omega_{ZF} = \frac{1}{R_{F1}C_{F1}}} \qquad \boxed{\omega_{PF} = \frac{1}{(R_{F1}||R_{F2})C_{F1}}}$$

$$\frac{\omega_{PF}}{\omega_{ZF}} = 1 + \frac{R_{F1}}{R_{F2}} = \frac{V_{OUT}}{V_{REF}}$$

LDO SIMULATIONS

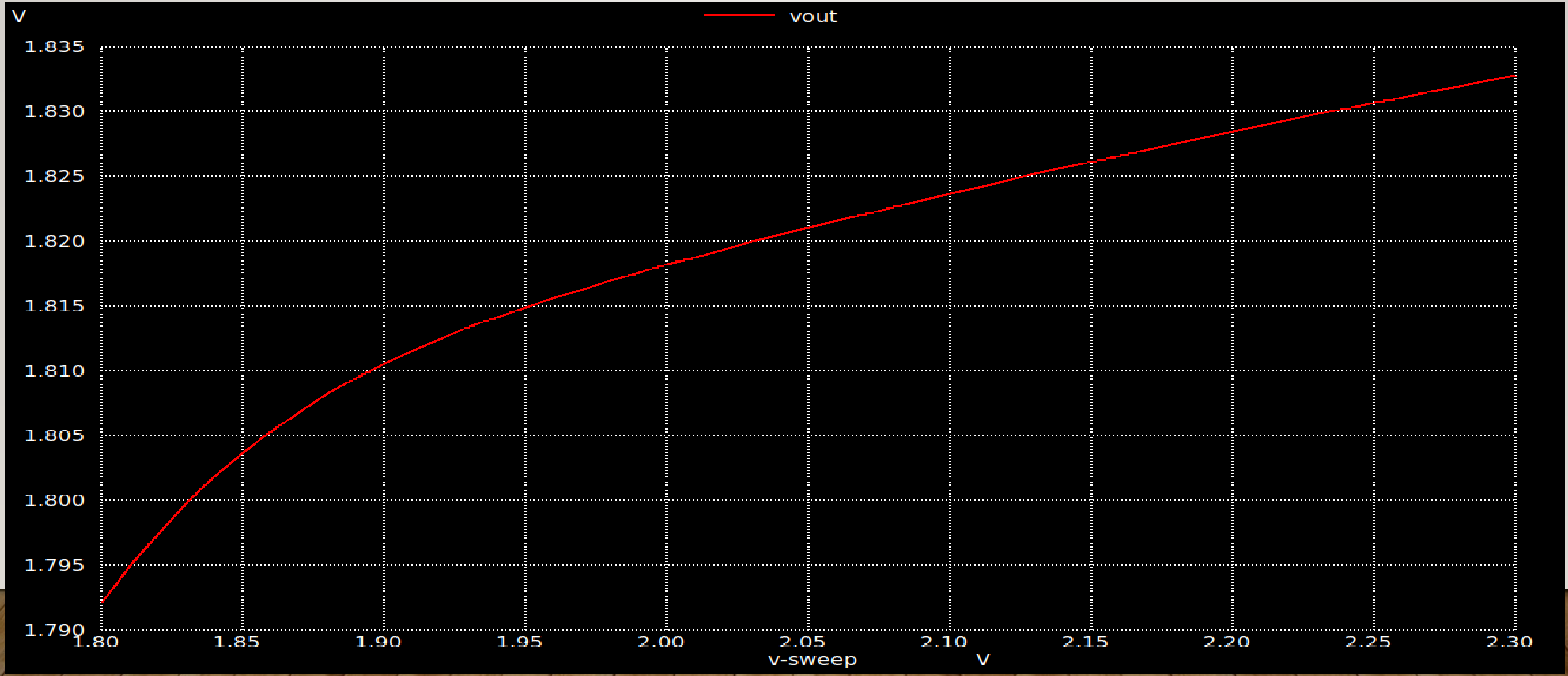
1- Dropout Voltage

Vdo achieved = 60mV



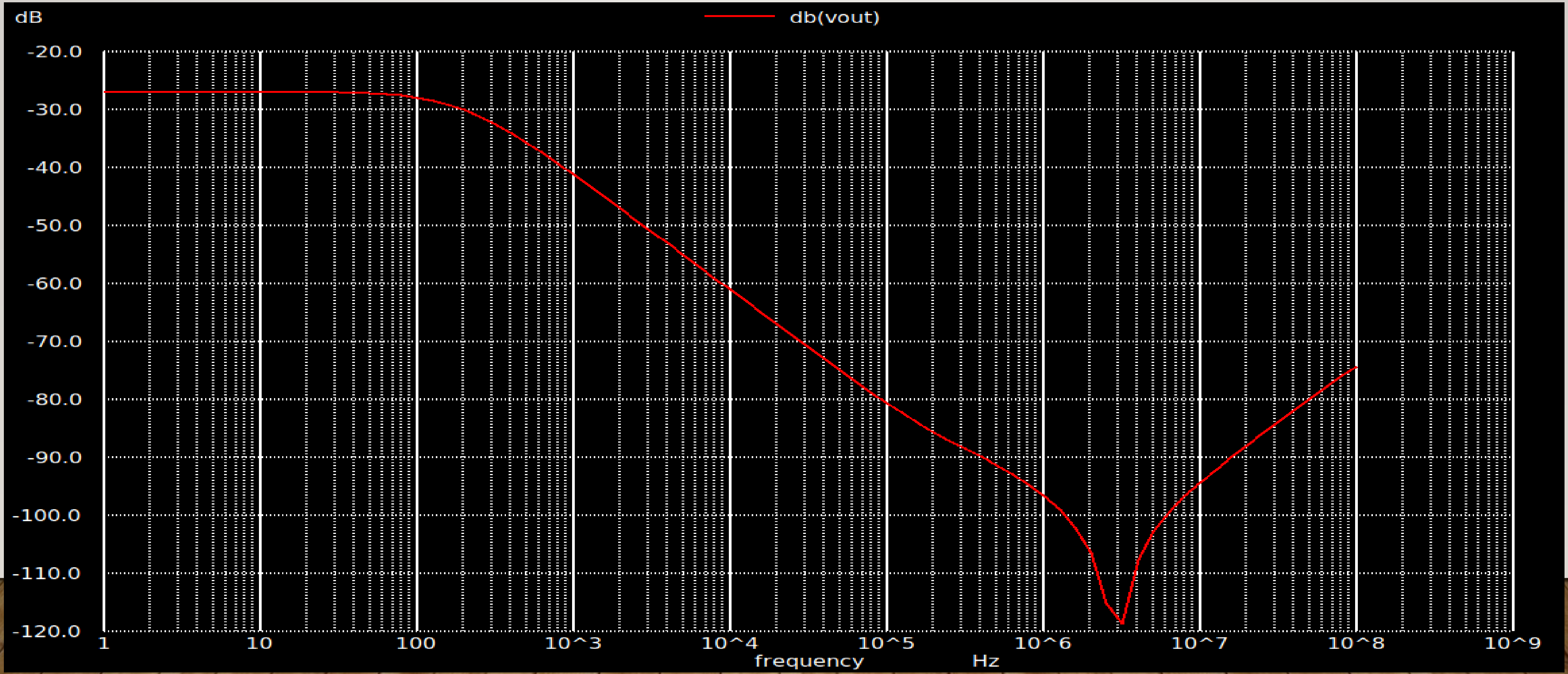
LDO SIMULATION

2- Line regulation = 90 mV/V



LDO SIMULATIONS

3- PSRR @ 1KHz = 41 dB , PSRR @ 1MHz = 97 dB



LDO SIMULATIONS

4- Line transient