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Design of CMOS Low-Dropout Voltage Regulator for Power Management Integrated Circuit in 0.18-µm Technology

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Abstract. A low-dropout (LDO) voltage regulator is the main component used in the majority of portable electronic application since it is used as power management unit in those applications. In this paper, a LDO regulator for the power management integrated circuit in 0.18-µm CMOS technology using Cadence software is presented. The error amplifier of the proposed LDO employed seven transistors for current mirror. Meanwhile, the PMOS transistor is used as a pass element transistor to control the voltage variation. The resistors are used as a feedback network circuit while the capacitor is used to minimise the variation of output voltage. The simulation results show that the proposed design provides a 2.41 V constant output voltage for the supply voltage ranges of 2.55 V to 3.55 V. The dropout voltage of 140 mV is achieved with 1.48 mW power consumption. The line regulation is 1.0 mV/V and the load regulation is 0.41 mV/A, while the layout of the proposed regulator is 27 µm x 34 µm.

INTRODUCTION

The demands for wearable and mobile devices have increased tremendously. The only voltage source for these devices is battery. However, prolong used of the battery will lead to unstable voltage level [1]. Thus CMOS linear voltage regulator was developed to overcome such problem. The CMOS linear regulator can be classified as the low dropout, low supply current, high supply current, high-speed and high voltage [2]. One of the voltage regulators used in portable devices is low-dropout voltage regulator [3]. The concept of working principle of LDO is similar to all linear voltage regulators. Therefore, a subset of linear voltage regulators is also known as low-dropout regulators.

The function of the LDO voltage regulator is to provide an output voltage which is nearly closed to the output voltage [4]. Furthermore, the low dropout regulator also used to generate a stable output voltage independent of the fluctuation of input voltage and varies the load impedance. Thus, it is very suitable for any equipment or electronic system that needs steady output voltage, while the wide fluctuations were reduced in upstream supply voltage, and the precision of the output voltage was increased with some components were needed. The advantages of a LDO voltage include a low operating bias voltage requirement, high efficiency performance, low power consumption and high heat

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dissipation [5]. The LDO regulator was available as both stand-alone packaged devices and as intellectual property (IP) core that can be integrated into a larger integrated circuit design.

LOW DROPUT VOLTAGE REGULATOR

Basic Principle

The basic LDO voltage regulator topology usually consists of error amplifier, two feedback resistors, capacitors, reference source voltage and pass transistor [6]. The PMOS based LDO regulator is shown in Fig.1. The performance of LDO voltage regulator can be verified by the dropout voltage, transient response, line regulation, efficiency, load regulation, power consumption, power supply rejection and quiescent current. Based on the previous works, researchers and designers used several techniques to improve the performance of low dropout voltage regulator [7]. The selected technique depends on the application of the device. The power supply rejection is the main factor to determine the function of low dropout voltage regulator. In addition, the frequency compensation with power supply rejection enhancer is needed to improve the performance of power supply rejection and transient response in the low dropout voltage regulator circuit [8]. The transient response of LDO voltage regulator can be improved by the frequency compensation with the power supply rejection enhancer scheme. This method will improve the performance of power supply rejection ratio. The transient response performance also can be revised by a buffer; the buffer can be added to the low dropout voltage regulator circuit between error amplifier and pass transistor [10]. The low-dropout voltage regulator can employ high pass filter to avoid the variation of power supply rejection at low frequency condition. The high pass filter consists of replica loop.

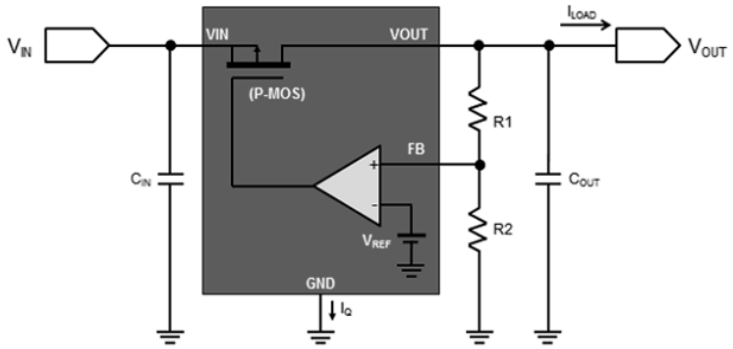

FIGURE 1. The PMOS Based Low Dropout Regulator [10]

Performance Criteria

There are some performances criteria often used to analyze the LDO such as dropout voltage, output voltage and etc. Therefore, the equation (1) to (5) is used to explain the relationship between the performance criteria and circuit parameters.

Dropout voltage (V_{do}) is the differential voltage between input voltage and output voltage is given as:

$$V_{do} = (1-n) \times V_{in} \tag{1}$$

where *n* is the ration of output voltage to input. The output voltage (V_{out}) is defined as the voltage that produced by the low dropout voltage regulator when the input voltage is applied. The V_{out} is shown in equation (2).

$$V_{out} = V_{ref} \times (1 + R_1 / R_2) \tag{2}$$

The differential current between the input current and the output current is quiescent current (I_d). It is also known as ground current. Line regulation represents the ability of the regulator to regulate the output voltage with fluctuating input voltage and its given as:

$$\text{Line regulation} = \Delta V_{out} / \Delta V_{in} \tag{3}$$

Meanwhile, the load regulation is the ability of the regulator to regulate the output voltage under different load conditions as shown in equation (4).

$$\text{Load regulation} = \frac{V_{out(\,no\ load\,)} - V_{out(\,full\ load\,)}}{I_{out(\,full\ load\,)} - 0} \tag{4}$$

Another important specification for LDO regulator is power supply rejection ratio (PSRR). Power supply rejection is defined as the ability of LDO regulator to prevent the fluctuation of the regulated output voltage. The input voltage variations will cause fluctuating voltage. PSRR is also known as ripple rejection as given in equation (5).

$$PSRR = 20\ log \frac{\Delta V_{out}}{\Delta V_{in}} \tag{5}$$

CIRCUIT IMPLEMENTATION

The proposed LDO regulator circuit was constructed in Cadence software. Figure 2 shows the schematic of the proposed LDO regulator. In the schematic diagram, the error amplifier is constructed by three PMOS transistor and five NMOS transistor. The transistors M0 to M7 are used to form the current mirror circuit. The function of current mirror structure will ensure each of the line of wire able to get same current level in this design. All the transistors are using 0.18 µm technology size. Based on the proposed design, a PMOS transistor M8 is used as a pass element transistor to control the voltage from the input to the output differential voltage. The main reason is the PMOS transistor is voltage-driven and does not require much current, thus greatly reducing the current consumed by the device itself. In addition, the voltage drop across the PMOS transistor is similar to the product of the output current and the on-resistance. The resistors R1 and R2 are used as a voltage divider network or feedback circuit. The feedback circuit structure is able to generate a feedback voltage into error amplifier. The capacitor (C_{load}) is used as a stabilizer to stabilize the output voltage and the load resistor (R_{load}) is 10 kΩ. All the parameter values are calculated based on theory.

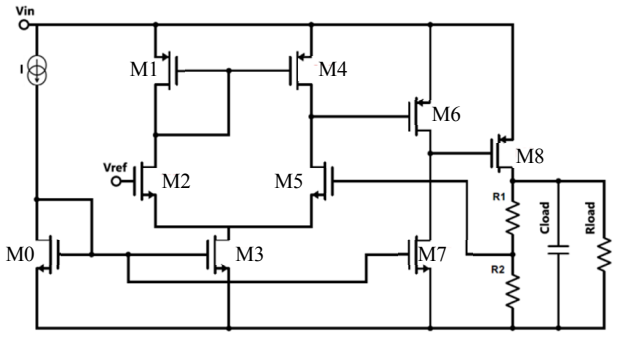

FIGURE 2. The schematic of the proposed LDO regulator

SIMULATION RESULTS

Figure 3 shows the relationship between input voltage and output voltage of LDO regulator. The output voltage of proposed design can be regulated for an input range of 2.55 V to 3.55 V. This proposed design is able to provide a 2.41 V output voltage.

For proposed LDO voltage regulator, the input range of the proposed design can be applied from 2.55 V to 3.55 V input voltage, it was able to provide a 2.41 V stable output voltage. To specify the output voltage, the two resistors played the significant role to control the output voltage. Therefore, 60 kΩ and 100 kΩ resistors are used as a feedback circuit in order to control pass transistor to generate the desired output voltage. Besides, the reference voltage is set at 1.50 V in the design. The value of the reference voltage is calculated using equation (2).

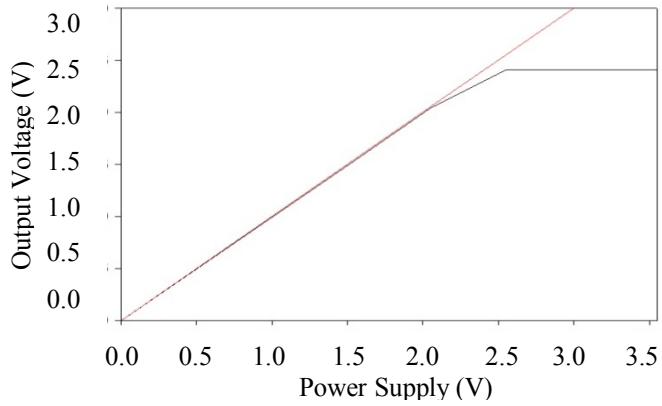

FIGURE 3. The output voltage versus input voltage of LDO Regulator

Figure 4 shows the quiescent current of LDO regulator. The quiescent current must be small enough to achieve the maximum efficiency of LDO regulator performance, The quiescent current will limit the efficiency of LDO regulator. The lower the value of quiescent current, the higher the efficiency of the low dropout voltage regulator. The output current and the input current is 256.34 µA and 241.26 µA, respectively at input voltage of 2.55 V. Therefore, the quiescent current for the proposed design is 15.08 µA.

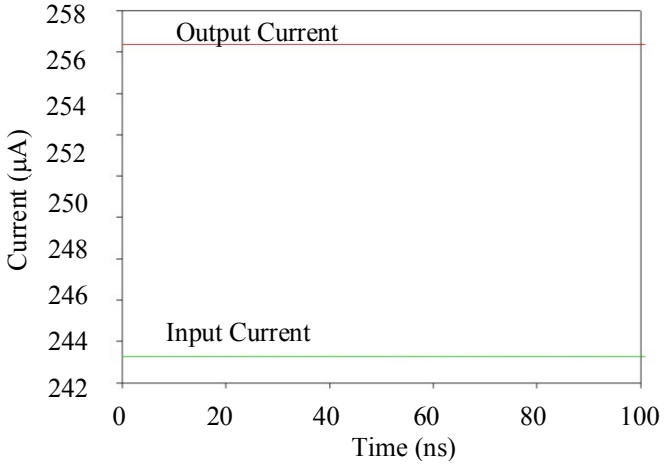

FIGURE 4. The quiescent current of LDO regulator

Figure 5 shows the results of output voltage with different input voltage. In order to measure the line regulation, the input voltage is required to increase from 2.55 V to 3.55 V by 1 V increment. The proposed LDO regulator is able to provide 2.414 V and 2.413 V output voltages at 3.55 V and 2.55 V input voltage, respectively. The line regulation of this proposed LDO regulator equal to 1 mV/V. Therefore, the proposed design required at least 1 mV/V to regulate the output voltage with the fluctuating input voltage. The lowest of the line regulation's value, the better performance of the LDO regulator circuit.

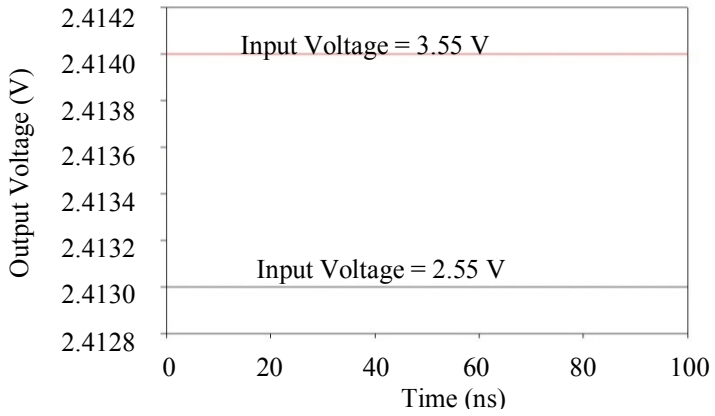

FIGURE 5. The result of output voltage with input voltage of 2.55 V and 3.55 V

Figure 6 shows the output voltage of the proposed LDO regulator with and without load. Based on Fig. 6, the output voltage of LDO regulator with load is 2.4126 V while without the load is 2.4127 V. The load regulation of this proposed LDO regulator equal to 0.41 V/A. Therefore, this low dropout voltage regulator could regulate the voltage over this acceptable load range. In addition, the regulation can change with this value.

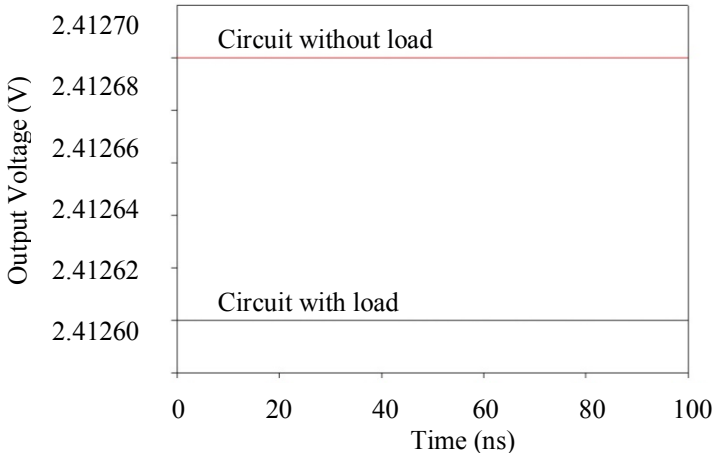

FIGURE 6. The proposed design of LDO regulator with different load setting

The magnitude of power supply rejection ratio (PSRR) of the proposed LDO regulator is shown in Fig. 7. As can be seen, the PSRR of -62.2 dB at 1 kHz frequency is achieved when the output voltage equal to 2.41 V. The PSRR indicates regulator's ability to suppress the variation of input voltage over the output voltage. Increasing the DC gain will increase the DC power supply rejection ratio of LDO regulator.

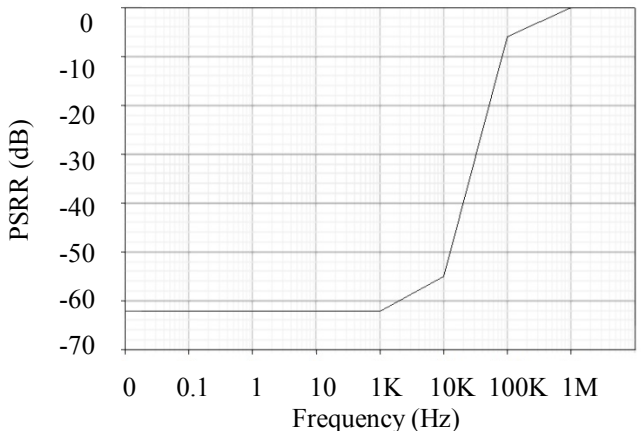

FIGURE 7. The PSRR of proposed LDO regulator

Figure 8 shows the layout of low dropout LDO voltage regulator. The layout is constructed using CMOS 0.18 µm technology. The layout of the proposed design consists of PMOS and NMOS transistors, resistors, capacitor and metal layers for transmission lines. The size of the layout is 27 µm x 34 µm. Finally, the proposed LDO drawn 582 µA current at 2.55 V supply voltage. Therefore, the power consumption of the proposed LDO is 1.48 mW.

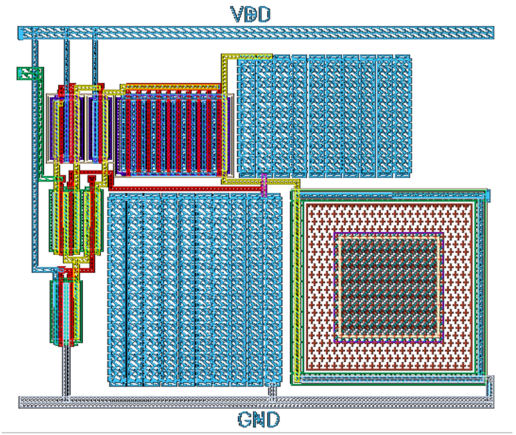

FIGURE 8. The layout of low dropout voltage regulator in 0.18 µm CMOS technology

Table I shows the comparison of performance of the proposed LDO regulator with previously published works. Even though the proposed design requires high input voltage, it is still able to provide a small value of dropout voltage. References [12] and [13] obtained low- dropout voltage due the low input voltage. Furthermore, the PSRR of -62.2 dB indicates its ability to suppress the fluctuation of the input voltage with respect to the output voltage. The performance of the PSRR of proposed design can be considered as good due to the magnitude of the PSRR is much lower than other majority references.

TABLE 1. Comparison of CMOS LDO regulator

Reference	[11]	[12]	[13]	[14]	[15]	This Work
Technology (μm)	0.18	0.18	0.18	0.13	0.18	0.18
V_{in} (V)	1.20-3.00	1.30-3.60	1.92-3.60	0.00-2.25	2.00-3.30	2.55-3.55
V_{out} (V)	1.00	1.20	1.80	1.10	1.80	2.41
V_{do} (mV)	200	120	120	200	200	140
$I_{Load,max}$ (mA)	100	50	50	95	200	241
I_q (μA)	161	5.9	22	83	1.2	15.08
C_{Load} (pF)	100	50	50	50	100	50
Load Regulation (μV/mA)	20	2	-3	1.5	400	410
Line Regulation (mV/V)	0.95	4.10	0.02	0.72	15.31	1.00
PSRR (dB)	N/A	N/A	-62.0	-45.0	N/A	-62.2
Chip size (mm^2)	N/A	N/A	N/A	0.11	0.04	0.9

CONCLUSION

The proposed low-dropout voltage regulator was successfully simulated and analysed. The proposed LDO voltage regulator is designed using the error amplifier, MOS transistors, resistors and capacitor. The proposed LDO voltage regulator ables to provide a 2.41 V stable output voltage for the input voltage range of 2.55 V to 3.55 V. The dropout voltage of 140 mV with 1.48 mW power consumption is obtained. The others performance of the proposed LDO are comparable with previously published works. Furthermore, the chip area of the LDO is 27 μm x 34 μm.

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