FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP

	File Address	P	File Address		File Address	,	File Addres
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186ł
PORTC	07h	TRISC	87h		107h		187h
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h		108h		188ł
PORTE ⁽¹⁾	09h	TRISE ⁽¹⁾	89h		109h		189ł
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Al
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18B
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18C
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18D
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽²⁾	18EI
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved ⁽²⁾	18FI
T1CON	10h		90h		110h		190l
TMR2	11h	SSPCON2	91h		111h		1911
T2CON	12h	PR2	92h		112h		192l
SSPBUF	13h	SSPADD	93h		113h		193l
SSPCON	14h	SSPSTAT	94h		114h		194
CCPR1L	15h		95h		115h		195l
CCPR1H	16h		96h		116h		196l
CCP1CON	17h		97h	General	117h	General Purpose	1971
RCSTA	18h	TXSTA	98h	Purpose Register	118h	Register	1981
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	1991
RCREG	1Ah		9Ah		11Ah		19A
CCPR2L	1Bh		9Bh		11Bh		19B
CCPR2H	1Ch	CMCON	9Ch		11Ch		19C
CCP2CON	1Dh	CVRCON	9Dh		11Dh		19D
ADRESH	1Eh	ADRESL	9Eh		11Eh		19E
ADCON0	1Fh	ADCON1	9Fh		11Fh		19FI
	20h		A0h		120h		1A0
General Purpose Register		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	
				00 27.00			455
96 Bytes		accesses	EFh F0h	accesses	16Fh 170h	accesses	1EF 1F0l
	7Fh	70h-7Fh	FFh	70h-7Fh	17Fh	70h - 7Fh	1FF
Bank 0	4 / 1 11	Bank 1	1 1 11	Bank 2	. 11111	Bank 3	

Unimplemented data memory locations, read as '0'.

^{*} Not a physical register.

Note 1: These registers are not implemented on the PIC16F876A.

^{2:} These registers are reserved; maintain these registers clear.

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TABLE 15-2: PIC16F87XA INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode			Status	Notes	
		Description		MSb			LSb	Affected	Notes
		BYTE-ORIENTED FILE REGIS	TER OPE	RATIO	NS				
ADDWF	f, d	Add W and f	1	0.0	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST	ER OPER	RATION	NS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add Literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND Literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to Address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR Literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from Interrupt	2	00	0000	0000	1001		
RETLW	k	Return with Literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from Literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR Literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

Note: Additional information on the mid-range instruction set is available in the PICmicro® Mid-Range MCU Family Reference Manual (DS33023).

^{2:} If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

^{3:} If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

15.2 Instruction Descriptions

ADDLW	Add Literal and W		
Syntax:	[label] ADDLW k		
Operands:	$0 \le k \le 255$		
Operation:	$(W) + k \to (W)$		
Status Affected:	C, DC, Z		
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.		

BCF	Bit Clear f
Syntax:	[label] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	$0 \rightarrow (f{<}b{>})$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ADDWF	Add W and f		
Syntax:	[label] ADDWF f,d		
Operands:	$0 \le f \le 127$ $d \in [0,1]$		
Operation:	(W) + (f) \rightarrow (destination)		
Status Affected:	C, DC, Z		
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.		

BSF	Bit Set f
Syntax:	[label] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW	AND Literal with W		
Syntax:	[label] ANDLW k		
Operands:	$0 \leq k \leq 255$		
Operation:	(W) .AND. (k) \rightarrow (W)		
Status Affected:	Z		
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.		

BTFSS	Bit Test f, Skip if Set		
Syntax:	[label] BTFSS f,b		
Operands:	$0 \le f \le 127$ $0 \le b < 7$		
Operation:	skip if $(f < b >) = 1$		
Status Affected:	None		
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2 TCY instruction.		

ANDWF	AND W with f		
Syntax:	[label] ANDWF f,d		
Operands:	$0 \le f \le 127$ $d \in [0,1]$		
Operation:	(W) .AND. (f) \rightarrow (destination)		
Status Affected:	Z		
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.		

BTFSC	Bit Test, Skip if Clear		
Syntax:	[label] BTFSC f,b		
Operands:	$0 \le f \le 127$ $0 \le b \le 7$		
Operation:	skip if $(f < b >) = 0$		
Status Affected:	None		
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded and a NOP is executed instead, making this a 2 Tcy instruction.		

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CALL	Call Subroutine	CLRWDT	Clear Watchdog Timer
Syntax:	[label] CALL k	Syntax:	[label] CLRWDT
Operands:	$0 \le k \le 2047$	Operands:	None
Operation:	(PC)+ 1 \rightarrow TOS, k \rightarrow PC<10:0>, (PCLATH<4:3>) \rightarrow PC<12:11>	Operation:	$00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$
Status Affected: Description:	None Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.	Status Affected: Description:	1 → PD TO, PD CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits, TO and PD, are set.
CLRF	Clear f	COMF	Complement f
Syntax:	[label] CLRF f	Syntax:	[label] COMF f,d
Operands: Operation:	$0 \le f \le 127$ $00h \to (f)$	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation.	1 → Z	Operation:	$(\bar{f}) \to (destination)$
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.	Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.
CLRW	Clear W	DECF	Decrement f
Syntax:	[label] CLRW	Syntax:	[label] DECF f,d
Operands:	None	Operands:	$0 \le f \le 127$
Operation:	$00h \rightarrow (W)$		d ∈ [0,1]
	$1 \rightarrow Z$	Operation:	(f) - 1 → (destination)
Status Affected:	Z	Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.	Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is

stored back in register 'f'.

DECFSZ	Decrement f, Skip if 0	INCFSZ	Increment f, Skip if 0
Syntax:	[label] DECFSZ f,d	Syntax:	[label] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0	Operation:	(f) + 1 \rightarrow (destination), skip if result = 0
Status Affected:	None	Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2 Tcy instruction.	Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2 Tcy instruction.
gото	Unconditional Branch	IORLW	Inclusive OR Literal with W
Syntax:	[label] GOTO k	Syntax:	[label] IORLW k
Operands:	$0 \le k \le 2047$	Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow PC < 10:0 >$	Operation:	(W) .OR. $k \rightarrow (W)$
	PCLATH<4:3> → PC<12:11>	Status Affected:	Z
Status Affected:	None	Description:	The contents of the W register a
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.		OR'ed with the eight-bit literal 'k'. The result is placed in the W register.
INCF	Increment f	IORWF	Inclusive OR W with f
Syntax:	[label] INCF f,d	Syntax:	[label] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$0 \le f \le 127$ d $\in [0,1]$
Operation:	(f) + 1 \rightarrow (destination)	Operation:	(W) .OR. (f) \rightarrow (destination)
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1' the result is placed back in	Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1' the result is placed back in

'1', the result is placed back in

register 'f'.

'1', the result is placed back in

register 'f'.

RLF	Rotate Left f through Carry
Syntax:	[label] RLF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	С
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.

SLEEP

Syntax:	[label] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → \overline{TO} , 0 → \overline{PD}
Status Affected:	TO, PD
Description:	The power-down status bit, \overline{PD} , is cleared. Time-out status bit, \overline{TO} , is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

RETURN	Return from Subroutine
Syntax:	[label] RETURN
Operands:	None
Operation:	$TOS \to PC$
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

SUBLW	Subtract W from Literal
Syntax:	[label] SUBLW k
Operands:	$0 \le k \le 255$
Operation:	$k - (W) \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

RRF	Rotate Right f through Carry
Syntax:	[label] RRF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	С
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
	C Register f

SUBWF	Subtract W from f
Syntax:	[label] SUBWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - (W) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW	Exclusive OR Literal with W
Syntax:	[label] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. $k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[label] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) \rightarrow (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

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NOTES: