CS 362: Computer Design

Homework 2

25 X 4 = 100 points

Q1) A Sequential circuit with two D flip-flops, A and B, two inputs X and Y, and one output Z is specified by the following input equations:

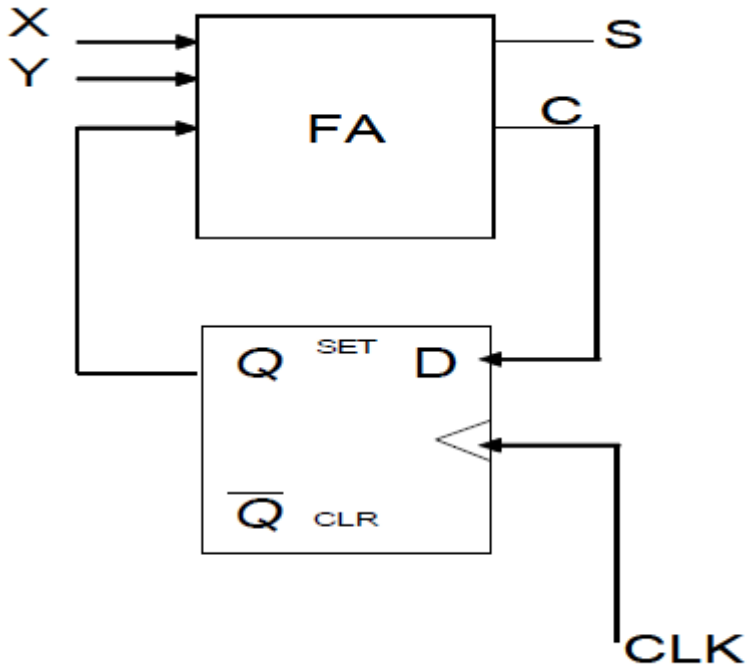
$$D_A = \bar{X}A + XY$$

$$D_B = \bar{X}B + XA,$$

$$Z = XB$$

a) Draw the logic diagram of the circuit.
b) Derive the state table.
c) Derive the state diagram.

Q2) A sequential circuit has one flip-flop Q, two inputs X and Y and one output S. It consists of a full adder circuit connected to a D flip-flop, as shown. Derive the state table and state diagram of the sequential circuit.



Q3) In many communication and networking systems, the signal transmitted on the communication lines uses a non-return-to-zero (NRZ) format. USB uses a specific version referred to as non-return-to-zero inverted (NRZI). A circuit that converts any message sequence of 0s and 1s to a sequence in the NRZI format is to be designed. The mapping for such a circuit is as follows.

a) if the message bit is 0, the NRZI format message contains an immediate change from 1to 0 or from 0 to 1, depending on the current NRZI value.
b) If the message bit is 1, then the NRZI format message remains fixed at 0 or 1, depending on the current NRZI value.

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This transformation is illustrated by the following example, which assumes that the initial value of NRZI message is 1:

Message: 10001110011010

NRZI Message: 10100001000110

Find state diagram and implementation for the circuit.

Q4) A pair of signal Request (R) and Acknowledge (A) is used to coordinate transactions between a CPU and it I/O system. The interaction of these signals is often referred to as a *"handshake".* These signals are synchronous with the clock and for a transaction, are to have their transitions always appear in the order shown below. A handshake checker is to be designed that will verify the transition order. The checker has inputs, R and A, asynchronous reset signal, RESET, and output, Error (E). If the transition is a handshake are in order E=0. If the transitions are out of order then E becomes 1 and remains at 1 until an asynchronous reset signal (RESET =1) is applied to the CPU.

Find the state diagram and implementation for the handshake checker.