Bresia Prudente, bprude2

0x00400ff8
It's a TLB hit and it will send an address of 0x900c4ff8 to the cache. This will be a cache miss since line 0xf doesn't match. It will create a new set of instructions into line 0xf and then will be changed to 0x900c4f.

0x00400ffc
This will be a TLB hit and will send an address of 0x900c4ffc to the cache. Much like the first instruction (address 0x00400ff8), it will have 0xf and 0x900c4f. However, it'll be a cache hit since the instructions dealt with the cache will miss the first instruction.

0x00401010
It'll be TLB miss and since 0x00401 isn't a part of the 0x00400 index, it will be translated into 0x900ce. Therefore, the address 0x900ce010 will sent to the cache. However, since the cache index is 0x1 and it also has an address of 0x900e0, the V-bit for 0x1 is 1. Since it matches with the address, it will have a cache hit.

Why is it helpful to know that none of the instructions being fetched are loads or stores?
This is because a TLB miss (which will trigger a page fault) can result in at least one or more processor having a chance to run.