1. DPTX Registers in Bank 0

1.1 General Control Registers

Offset	Register Name	Bit	Definition	Default
Chip Information Registers				
0x00	Vendor ID[7:0]	[7:0]	Vendor ID Low Byte (Read Only)	0x54
0x01	Vendor ID[15:8]	[7:0]	Vendor ID High Byte (Read Only)	0x49
0x02	Device ID[7:0]	[7:0]	Device ID Low Byte (Read Only)	0x51
0x03	Device ID[15:8]	[7:0]	Device ID High Byte (Read Only)	0x61
0x04	Sub-Revision ID[3:0]	[3:0]	Sub-Revision ID (Read Only)	0x0
	Major-Revision ID[3:0]	[7:4]	Major-Revision ID (Read Only)	0xA
Software Reset Registers				
0x05	RegSoftVRst	[0]	Software video clock domain reset	1
	RegSoftREFRst	[2]	Software reference clock domain reset	0
	RegSoftAUXRst	[3]	Software aux clock domain reset	0
	RegSoftSSRst	[5]	Software SDM function reset	0
		[7]		0
Interrupt Status and Clear Registers				
0x06	RHPDChgInt	[0]	HPD status change interrupt Write ‘1’ to clear this interrupt	0
	RHPDIRQInt	[1]	HPD IRQ interrupt Write ‘1’ to clear this interrupt	0
	RVidStableInt	[2]	Video stable status change interrupt Write ‘1’ to clear this interrupt	0
	RAxRqFailInt	[5]	AUX channel link training request fail interrupt Write ‘1’ to clear this interrupt	0
	RHPDIRQFailInt	[7]	AUX channel HPDIRQ request fail interrupt Write ‘1’ to clear this interrupt	0

0x07	RPCRqFailInt	[0]	AUX channel PC request fail interrupt Write ‘1’ to clear this interrupt	0
	RTrainAxFailInt	[3]	Training sequence AUX fail interrupt Write ‘1’ to clear this interrupt	0
	RPktAVIInfoInt	[4]	AVI InfoFrame packet done interrupt Write ‘1’ to clear this interrupt	0
	RPktMpgInfoInt	[6]	MPEG InfoFrame packet done interrupt Write ‘1’ to clear this interrupt	0
	RPktGenInfoInt	[7]	General InfoFrame packet done interrupt Write ‘1’ to clear this interrupt	0
0x08	RPktVidAttrInt	[0]	Video Attribute packet done interrupt Write ‘1’ to clear this interrupt	0
	RVidCTSErrInt	[2]	Video M error interrupt Write ‘1’ to clear this interrupt	0
	RLinkTrainFailInt	[4]	Link training fail interrupt Write ‘1’ to clear this interrupt	0
	RVidOvFlwInt	[5]	Video FIFO overflow interrupt Write ‘1’ to clear this interrupt	0
	R501FIFOOvInt	[6]	501 FIFO overflow interrupt Write ‘1’ to clear this interrupt	0
		[7]		
Interrupt Mask Registers				
0x09	REnHPDChgInt	[0]	‘0’: Disable interrupt event ‘1’: Enable interrupt event	0
	REnHPDIRQInt	[1]		0
	REnVidStableInt	[2]		0
	REnAxRqFailInt	[5]		0
	REnHPDIRQFailInt	[7]		0
0x0A	REnPCRqFailInt	[0]		0

	REnTrainAxFailInt	[3]		0
	REnPktAVIInfoInt	[4]		0
	REnPktMpgInfoInt	[6]		0
	REnPktGenInfoInt	[7]		0
0x0B	REnPktVidAttrInt	[0]		0
	REnVidCTSErrInt	[2]		0
	REnLinkTrainFailInt	[4]		0
	REnVidOvFlwInt	[5]		0
	REn501FIFOOvInt	[6]		0
		[7]		
System Configuration Registers				
0x0C	RegINTPol	[0]	0: Interrupt is active low 1: Interrupt is active high	0
	RegINTMode	[1]	0: Open-Drain mode 1: Push-Pull mode	0
	RegPCDrv[1:0]	[3:2]	PC I2C driving strength	10
		[4]		
	RegHPDPD	[5]	1: Enable internal pull-down	1
	RegEnHPD	[6]	0: Normal operation 1: Force HPD to High	0
		[7]		
System Status Registers				
0x0D	RINTStatus	[0]	DPTX Interrupt Status (Read Only) 0: No interrupt event 1: Interrupt is active	-
	RHPDStatus	[1]	Hot Plug Detect status (Read Only) 0: Unplug; 1: Plug	-
	RVideoStable	[2]	Video input status (Read Only) 0: Unstable; 1: Stable	-
	RU3WakeInt	[3]	U3 wakeup interrupt status (Read Only) 0: No interrupt event 1: Interrupt is active	-

	RPLL_XPLock	[4]	XPLL lock (Read Only) 0: Unlock; 1: Lock	-
	RPLL_SPLock	[5]	SPLL lock (Read Only) 0: Unlock; 1: Lock	-
	RAuxFreqLock	[6]	AUX frequency lock (Read Only) 0: Unlock; 1: Lock	-
	RMIPIINT	[7]	MIPIRX interrupt status (Read Only) 0: No interrupt event 1: Interrupt is active	-
0x0E	RefLinkState[4:0]	[4:0]	DP Link State (Read Only) [0]: Main link disable [1]: Aux channel read [2]: CR pattern [3]: EQ pattern [4]: Normal operation	00000
	RVidMuteSts	[5]	Video Mute Status (Read Only) 0: Normal operation; 1: Video mute	1
		[6]		
	RefLinkRate	[7]	DP Link Rate after training (Read Only) 0: 1.62Gbps per lane 1: 2.7Gbps per lane	0
System Debug Registers				
0x0F	RegBankSel	[0]	0: Select register Bank 0(0x00~0xFF) 1: Select register Bank 1(0x130~0x1FF)	0
	RegEnDbgDP	[1]	Select DP debug group	1
		[2]		
		[3]		
	RegEnDbg (PW)	[4]	Debug signal output 0: Disable; 1: Enable	0
	RegDbgSel[2:0]	[7:5]	Debug signal group selection	000

1.2 CLKBUF Control Registers

0x10				
	RegPDREFCLK	[4]	Power down REFCLK 0: Normal operation 1: Power down REFCLK	0

	RegPDREFCNT[1:0]	[6:5]	REFCLK power level 00: level 0 01: level 1 10: level 2 11: level 3	00
0x11	RegAutoAuxRst	[0]	Auto AXRCLK reset 0: No reset AXRCLK when AUX idle 1: Reset AXRCLK when AUX idle	1
	RegAuxFilterNum[1:0]	[2:1]	AUX signal noise filter parameter 00: 1T 01: 2T 10: 3T 11: 4T	00
	RegFixedAuxFreq	[3]	Fix AXRCLK Frequency 0: Disable, 1: Enable	0
0x12				
	Reg10bLatEdge	[6]	PHY data sampling edge 0: Positive edge; 1: Negative edge	0
	RegEnPCLKCnt	[7]		0
0x13	RPCLKCnt[7:0]	[7:0]	(Read Only)	0x--
0x14	RPCLKCnt[11:8]	[3:0]		
	RegPreDivSel[2:0]	[6:4]	Extra PCLK division counter 000: divide 1 001: divide 2 010: divide 4 … 111 divide 128	000
0x15		[0]		

	Reg_501FIFORst	[1]	20-bit to 10-bit 501 FIFO reset 0: Normal operation; 1: Reset	0
		[2]		
	RegGateRCLK	[3]	1: Enable gating RCLK	0
	RegGateAXCLK	[4]	1: Enable gating XCLK	0
	RegEnIOIDDQ	[5]	1: Enable IO IDDQ mode	0
	RegEnIntWakeU3	[6]	1: Enable INT to wakeup U3 state	0
	RegEnOSCPwd	[7]	1: Enable OSC power-down	0

1.3 Link Training Registers

0x16	RegForceLBR	[0]	Force Low Bit Rate 0: Normal operation 1: Force low bit rate	0
	RegLaneNum[1:0]	[2:1]	DisplayPort Lane Number 00: 1 Lane 01: 2 Lane 11: 4 Lane	11
	RegLaneSwap	[3]	DispalyPort Lane Swapping 0: No swapping; 1: Swapping	0
	RegSpreadAmp	[4]	DisplayPort Spread Amplitude 0: 0.0% down spread 1: 0.5% down spread	0
	RegForceCRDone	[5]	0: Normal operation; 1: Force CR Done	0
	RegForceEQDone	[6]	0: Normal operation; 1: Force EQ Done	0
	RegEnDbgLKAuxWr	[7]	Debug mode AUX write 0: Burst mode; 1: Debug mode	0
0x17	RegEnAutoTrain	[0]	Auto training mode 0: Disable; 1: Enable	0
	RegEnTxTrain	[1]	Manual training mode 0: Disable; 1: Enable	0
	RegEnReTrain	[2]	Software force re-train 0: Disable; 1: Enable	0
	RegNoAuxTrain	[3]	Link training without AUX negotiation 0: with AUX negotiation 1: without AUX negotiation	0
	RegDisVmaxChk	[4]	Link training without Vmax check 0: with Vmax check 1: without Vmax check	0

	RefStsRdDone	[5]	Link STS read done (Read only)	0
	RefCfgRdDone	[6]	Link CFG read done (Read Only)	0
	RefLCSWrDone	[7]	Link LCS write done (Read Only)	0
0x18	Reg10usRefNum[7:0]	[7:0]	Reference clock number for 10us	0x87
0x19	RegL0SwingSet[1:0]	[1:0]	Swing Set 00: Voltage swing level 0 01: Voltage swing level 1 10: Voltage swing level 2 11: Voltage swing level 3	00
	RegL1SwingSet[1:0]	[3:2]		
	RegL2SwingSet[1:0]	[5:4]		
	RegL3SwingSet[1:0]	[7:6]		
0x1A	RegL0PreEmpSet[1:0]	[1:0]	Pre-Emphasis Set 00: Without pre-emphasis 01: With pre-emphasis level 1 10: With pre-emphasis level 2 11: With pre-emphasis level 3	00
	RegL1PreEmpSet[1:0]	[3:2]		
	RegL2PreEmpSet[1:0]	[5:4]		
	RegL3PreEmpSet[1:0]	[7:6]		
0x1B	RegL0MaxSwing	[0]	Maximum Swing 0: Not maximum swing 1: Maximum swing is reached	0
	RegL1MaxSwing	[1]		
	RegL2MaxSwing	[2]		
	RegL3MaxSwing	[3]		
	RegL0MaxPreEmp	[4]	Maximum Pre-emphasis 0: Not maximum pre-emphasis 1: Maximum pre-emphasis is reached	0
	RegL1MaxPreEmp	[5]		
	RegL2MaxPreEmp	[6]		
	RegL3MaxPreEmp	[7]		
0x1C	RegL0CRDone	[0]	Clock Recovery Status (Read Only) 0: Not finish 1: CR Done	0
	RegL1CRDone	[1]		
	RegL2CRDone	[2]		
	RegL3CRDone	[3]		
	RegL0EQDone	[4]	Equalization Status (Read Only) 0: Not finish 1: EQ Done	0
	RegL1EQDone	[5]		
	RegL2EQDone	[6]		
	RegL3EQDone	[7]		
0x1D	RegL0SymLock	[0]	Symbol Lock Status (Read Only) 0: Not lock 1: Lock	0
	RegL1SymLock	[1]		
	RegL2SymLock	[2]		
	RegL3SymLock	[3]		
	RegLaneAlign	[4]	Lane Alignment (Read Only) 0: Not align 1: Align	0

	RegEnQual2Idle	[5]	Quality test state to Idle state 0: Disable; 1: Enable	1
	RegLKQualPatSet[1:0]	[7:6]	Link Quality Pattern Set (Read Only) 00: No link quality test pattern 01: D10.2 test pattern 10: SERM test pattern 11: PRBS7 test pattern	00
0x1E	RegL0SwingAdj[1:0]	[1:0]	Voltage Swing Adjust (Read Only) 00: Level 0 01: Level 1 10: Level 2 11: Level 3	00
	RegL1SwingAdj[1:0]	[3:2]		
	RegL2SwingAdj[1:0]	[5:4]		
	RegL3SwingAdj[1:0]	[7:6]		
0x1F	RegL0PreEmpAdj[1:0]	[1:0]	Pre-Emphasis Adjust (Read Only) 00: Level 0 01: Level 1 10: Level 2 11: Level 3	00
	RegL1PreEmpAdj[1:0]	[3:2]		
	RegL2PreEmpAdj[1:0]	[5:4]		
	RegL3PreEmpAdj[1:0]	[7:6]		

1.4 AUX Channel Registers

0x20	Reg_TimeBase[7:0]	[7:0]		0x28
0x21	RegEnFifoAutoRst	[0]	LS2V FIFO Auto Reset 0: Disable, 1: Enable	1
	RFifoAutoRstInt	[1]	LS2V FIFO Auto Reset Interrupt Write ‘1’ to clear this interrupt	-
	RegEnOvFlw2Rst	[2]	Video stream FIFO overflow to reset 0: Disable, 1: Enable	0
		[3]		
		[4]		
		[5]		
		[6]		
	RegEnExtStb	[7]	1: Enable external standby input	0
0x22	RegEnAuxFreqAvg	[0]	Auto AXRCLK average 0: Disable, 1: Enable	1
	RegMLOff2GatAXCLK	[1]	PSR main-link off to gate AXCLK	1
	RegEnPNSwap	[2]	DisplayPort Lane PN Swapping 0: Disable, 1: Enable	0
	RegAxPNSwap	[3]	DisaplayPort AUX PN Swapping 0: Disable, 1: Enable	0

	RegEnStandby	[4]	Standby Mode 0: Disable, 1: Enable	0
	RegEnStb2Rst	[5]	Standby to Reset 0: Disable, 1: Enable	0
	RegMLOff2GatLSCLK	[6]	PSR main-link off to gate LSCLK	1
	RegMLOff2GatSSCLK	[7]	PSR main-link off to gate SSCLK	1
0x23	Reg_EDIDFFClr	[0]	PC request FIFO clear 0: Normal operation; 1: Clear FIFO	0
	REG_MasterSel	[1]	0: Internal; 1: PC	0
	RPC_ROMAcq	[2]		0
	RPC_ReqSegment	[3]	PC request command segment	0
	Reg_TimeBase[9:8]	[5:4]		00
	Reg_EDIDNoSegW	[6]	EDID No Segment Write 0: With segment write 1: Without segment write	0
	REnAuxFIFORead	[7]	AUX channel FIFO read back 0: Disable; 1: Enable	0
0x24	RPC_ReqOffset[7:0]	[7:0]	PC request command offset	0x--
0x25	RPC_ReqOffset[15:8]	[7:0]		0x--
0x26	RPC_ReqOffset[19:16]	[3:0]		0x--
	RPC_ReqByte[3:0]	[7:4]	PC request command byte number	0x0
0x27	RPC_ReqWDOut[7:0]	[7:0]	PC request command write data byte 1	0x--
0x28	RPC_ReqWDOut[15:8]	[7:0]	PC request command write data byte 2	0x--
0x29	RPC_ReqWDOut[23:16]	[7:0]	PC request command write data byte 3	0x--
0x2A	RPC_ReqWDOut[31:24]	[7:0]	PC request command write data byte 4	0x--

0x2B	RPC_Req[3:0]	[3:0]	PC request command selection 0x0: Native Aux Read 0x4: Native Aux Write AKSV 0x5: Native Aux Write 0x6: Native Aux Write An 0x8: General I2C Start/Stop (Addr Only) 0x9: General I2C Read (Addr + DataLen) 0xA: General I2C Write (Addr + DataLen + WrData) 0xB: I2C EDID Read (Addr = 0xA0) 0xC: I2C Write 0xD: I2C Read	0x0
	AXT_AUXBusy	[5]	AUX Busy Period (Read Only)	-
	RPC_FIFOFull	[6]	(Read Only)	-
	RPC_FIFOEmpty	[7]	(Read Only)	-
0x2C	RAUXReadBack[7:0]	[7:0]	AUX Channel Read Back (Read Only) Reg0x2F is AUX FIFO read back address. . Reg0x2F <= RAUXReadBack[31:24] when(REnAuxFIFORead='0') else RPC_RFIFOData	0x--
0x2D	RAUXReadBack[15:8]	[7:0]		
0x2E	RAUXReadBack[23:16]	[7:0]		
0x2F	RAUXReadBack[31:24]	[7:0]		

1.5 HDCP Control Registers

0x30				
0x31				
0x32				
0x33				
0x34				
0x35				
0x36				

0x37				
0x38				
0x39				
0x3A				
	REG_EnIRQAct	[2]	Hardware HPD IRQ Response 0: Disable; 1: Enable	0
	REG_EnVidBlack	[3]	Video Blank Gating 0: Disable, 1: Enable	0
	RIRQActDone	[4]	Hardware HPD IRQ Done (Read Only)	-
0x3B				
0x3C				
0x3D				
0x3E				
0x3F				

1.6 HDCP Mapping Registers

0x40				
0x41				
0x42				
0x43				
0x44				
0x45				

0x46				
0x47				
0x48				
0x49				
0x4A				
0x4B				
0x4C				
0x4D				
0x4E				
0x4F				
0x50				
0x51				
0x52				
0x53				
0x54				
0x55				
0x56				
0x57				

1.7 Electrical PHY Registers

Spread Spectrum PLL				
0x58	Reg_SP_RESETB	[0]	When '0', SSCPLL_IT6019 is reset	1
	Reg_SP_PWDB	[1]	When '0', SSCPLL_IT6019 is powerdowned	1
	Reg_SP_DEI	[2]	When '1', charge pump current of SSCPLL_IT6019 is increased.	1
	~~Reg_SP_ENI2~~	~~[3]~~	~~When '1', charge pump current of SSCPLL_IT6019 is increased.~~	~~0~~
	~~Reg_SP_EC1~~	~~[4]~~	~~When '1', VCO capacitance of SSCPLL_IT6019 is increased.~~	~~0~~

	~~Reg_SP_REFSEL~~	~~[5]~~	~~Select the reference signal of SSCPLL_IT6019 between XTAL and IP_CK2S~~ ~~When '0', XTAL~~ ~~When '1', IP_CK2S~~	~~0~~
	Reg_SPTriSel	[6]	SDM module select	0
	Reg_SP_DithEn	[7]	SDM dither function 0: Disable, 1: Enable	0
Transmitter PLL				
0x59	Reg_XP_TEST[7:0]	[7:0]	Test purpose usages TXPLLTEST7: IPIG TXPLLTEST6: XPIG TXPLLTEST5: ENVC TXPLLTEST4: DEI TXPLLTEST3: DER TXPLLTEST2: ENP2 TXPLLTEST1: DISRC TXPLLTEST0: ENAC	0x00
0x5A	~~Reg_XTALPWDB~~	~~[0]~~	~~When '0', XTAL is in powerdonwn mode~~	~~1~~
	~~Reg_SP_ICKSEL~~	~~[1]~~	~~ICKSEL='0' for 108MHz output~~ ~~ICKSEL='1' for 54MHz output~~	~~0~~
		[2]		
	Reg_SP_RBR	[3]	Only valid in DP mode. (Read Only) Set RBR=0 when input clock= 270Mhz Set RBR=1 when input clock= 162Mhz Read back value = not RefLinkRate	0
		[6:4]		
	Reg_XP_ENTEST	[7]	When '1', IT6019TXPLL enter test mode	0
Transmitter PLL				
0x5B	Reg_XP_EC1	[0]	When '1', IT6019TXPLL increase VCO capacitance	0
	Reg_XP_PWDI	[1]	When '0', IT6019TXPLL current bias is not in powerdown mode. When '1', IT6019TXPLL current bias in powerdown mode, no current source available for all other blocks such as IT6019TIPLL. Normally, XP_PWDI should always be set to 0.	0

	Reg_XP_RESETB	[2]	When '0', IT6019TXPLL is reset	1
	Reg_XP_ER0	[3]	When '1', filter resistance is increased If XP_GAINBIT = '0', set XP_ER0 = '1'	0
	Reg_XP_ENI	[4]	When '1', charge pump current of IT6019TXPLL is increased.	0
	Reg_XP_PWDPLL	[5]	When '1', IT6019TXPLL is in powerdown mode	0
	Reg_XP_GAINBIT	[6]	set TXPLL_GAINBIT=1, TXPLL_ER0=0	1
	Reg_XP_SELP	[7]	VFILT PBS/PBS2 option '0': select PBS, '1': select PBS2	0
Main DisplayPort Driver				
0x5C	Reg_DRV_RSTB	[0]	Reset signal for DPTX_DRV. When '0', all flip-flops in the transmitter are reset.	1
	Reg_DRV_HS	[1]	Switch to low-swing 4-to-1 MUX Set to '1' when HBR (DP) or >165MHz (HDMI) Set to '0' when RBR (DP) or <165MHz (HDMI)	1
		[2]		
		[3]		
	Reg_DRV_LNPWDB[3:0]	[7:4]	Powerdown signal for Lane3~0 of dptx_drv	0000
0x5D	Reg_DRV_LN0DSEL	[0]	Input data selection for Lane0 0: from APR, 1: from PatGen	0
	Reg_DRV_LN1DSEL	[1]	Input data selection for Lane1	0
	Reg_DRV_LN2DSEL	[2]	Input data selection for Lane2	0
	Reg_DRV_LN3DSEL	[3]	Input data selection for Lane3	0
	Reg_PAT_SEL[1:0]	[5:4]	"00" => D10.2 "01" => 1111100000 (PCLK-like) "10" => Undefined "11" => AFE pattern gen. data (depends on PAT_SEL)	00
	RegMLOff2PwdXPLL	[6]	1: PSR main-link off to power-down XPLL	1
	RegMLOff2PwdSPLL	[7]	1: PSR main-link off to power-down SPLL	1
AUX Channel Driver and Receiver				
0x5E	Reg_AUX_VSW	[0]	When '0', $V_{AUX\text{-}DIFFp\text{-}p}$ = 400mV When '1', $V_{AUX\text{-}DIFFp\text{-}p}$ = 800mV	0
	Reg_AUX_PWDB	[1]	Powerdown signal for DPTX_AUX.	1

	Reg_AUX_HYS	[3:2]	Input hysteresis threshold 00: 70mV 01: 120mV 10: 175mV 11: 250mV	01
	Reg_AUX_IE	[4]	Input enable signal for DPTX_AUX when '0', AUX_IN = '0' when '1', AUX_IN = received aux signal	1
	Reg_PAT_EN	[5]	Enable signal for AFE pattern gen.	0
	~~Reg_PAT_SEL~~	~~[6]~~	~~Pattern selection:~~ ~~when '0', 00110011....~~ ~~when '1', PRBS7~~	~~0~~
	Reg_PAT_RSTB	[7]	Reset signal for AFE pattern gen.	0
0x5F	RegAutoSwingInc	[0]	Auto Swing Increasing during CR state 0: Disable; 1: Enable	0
	RegEnEQInCR	[1]	Change EQ value in CR phase 0: Disable; 1: Enable	1
	RegEnCRInEQ	[2]	Change CR value in EQ phase 0: Disable; 1: Enable	0
		[3]		
		[4]		
	RegDisScramble	[5]	DisplayPort Scrambling Function 0: Enable; 1: Disable	0
	RegSymErrCntSet[1:0]	[7:6]	Symbol Error Count Set 00: Disparity and Illegal Symbol Error 01: Disparity Error 10: Illegal Symbol Error 11: Reserved	00

1.8 Video Registers

Video Format Registers				
0x60				
	~~Reg_PCLKDiv2~~	~~[1]~~	~~Half input clock rate~~ ~~0: Normal PCLK frequency~~ ~~1: Original PCLK frequency/2~~	~~0~~

	Reg_InColMod[1:0]	[5:4]	Input Color Mode 00: RGB mode 01: YUV422 mode 10: YUV444 mode 11: Reserved	00
0x61				
	~~Reg_TxFFRst~~	~~[1]~~		~~0~~
	~~Reg_DualInBus~~	~~[2]~~	~~Dual-Pixel Input Mode~~ ~~0: Disable, 1: Enable~~	~~0~~
	~~Reg_ChSwap~~	~~[3]~~	~~Dual-Pixel Odd/Even Swap~~ ~~0: Disable, 1: Enable~~	~~0~~
	~~Reg_RBSwapO~~	~~[4]~~	~~Odd-Pixel R/B Swap~~ ~~0: Disable, 1: Enable~~	~~0~~
	~~Reg_RBSwapE~~	~~[5]~~	~~Even-Pixel R/B Swap~~ ~~0: Disable, 1: Enable~~	~~0~~
0x62	RegVidColDep[3:0]	[3:0]	Input video format 0000: M444B18 0001: M444B24 0010: M444B30 0011: M444B36 0100: M444B48 1001: M422B16 1010: M422B20 1011: M422B24 1100: M422B32	0001
	REGDebugMode[3:0]	[4]	Set ‘1’ when simulation	0
		[5]	Set ‘1’ when simulation	0
		[6]	when set high, force PxVidStable high	0
		[7]	1: Force PCLK stable	0
Color Space Conversion				
0x63				

	~~Reg_DualMirror~~	~~[7]~~	~~Dual-Pixel Mirror Mode~~ ~~0: Disable, 1: Enable~~	~~0~~
0x64				
0x65				
0x66				
0x67				
0x68				
0x69				
0x6A				
0x6B				
0x6C				
0x6D				
0x6E				
0x6F				
0x70				
0x71				
0x72				
0x73				
0x74				
0x75				
0x76				
0x77				
0x78				
Sync/DE Generation Registers				
0x79	Reg_GenDE	[0]	DE Generator 0: Disable; 1: Enable	0
	RegGenSync	[1]	Sync Generator 0: Disable; 1: Enable	0
	RegHSPol	[2]	Generated HSync Polarity 0: Low; 1: High	1
	RegVSPol	[3]	Generated VSync Polarity 0: Low; 1: High	1
	Reg_PGInterLaced	[4]	PG interlaced mode 0: Disable, 1: Enable	0
	Reg_DEOnlyIn	[5]	DE Only mode enable 0: Disable; 1: Enable	0

	RegEnVBlankTG	[6]	VBlank Timing Generator 0: Disable, 1: Enable	0
	RegVHTimeRec	[7]	Video H/V status register read back 0: Disable; 1: Enable	0
0x7A	Reg_PGHTotal[7:0]	[7:0]	PG horizontal total pixel count	0x--
0x7B	Reg_PGHTotal[12:8]	[4:0]		
0x7C	Reg_PGHDES[7:0]	[7:0]	PG horizontal DE start	0x--
0x7D	Reg_PGHDES[12:8]	[4:0]		
0x7E	Reg_PGHDEE[7:0]	[7:0]	PG horizontal DE end	0x--
0x7F	Reg_PGHDEE[12:8]	[4:0]		
0x80	Reg_PGHRS[7:0]	[7:0]	PG horizontal Sync start	0x--
0x81	Reg_PGHRS[12:8]	[4:0]		
0x82	Reg_PGHRE[7:0]	[7:0]	PG horizontal Sync end	0x--
0x83	Reg_PGHRE[12:8]	[4:0]		
0x84	Reg_PGVTotal[7:0]	[7:0]	PG vertical total line count When Reg0x79[7]='1', read back value = PxRec_VTotal[11:0]	0x--
0x85	Reg_PGVTotal[11:8]	[3:0]		
0x86	Reg_PGVDES[7:0]	[7:0]	PG vertical DE start (1st field) When Reg0x79[7]='1', read back value = PxRec_VDES[11:0]	0x--
0x87	Reg_PGVDES[11:8]	[3:0]		
0x88	Reg_PGVDEE[7:0]	[7:0]	PG vertical DE end (1st field) When Reg0x79[7]='1', read back value = PxRec_VDEE[11:0]	0x--
0x89	Reg_PGVDEE[11:8]	[3:0]		
0x8A	Reg_PGVDES2nd[7:0]	[7:0]	PG vertical DE start (2nd field) When Reg0x79[7]='1', read back value = PxRec_VDES2nd[11:0]	0x--
0x8B	Reg_PGVDES2nd[11:8]	[3:0]		
0x8C	Reg_PGVDEE2nd[7:0]	[7:0]	PG vertical DE end (2nd field) When Reg0x79[7]='1', read back value = PxRec_VDEE2nd[11:0]	0x--
0x8D	Reg_PGVDEE2nd[11:8]	[3:0]		
0x8E	Reg_PGVRS[7:0]	[7:0]	PG vertical Sync start (1st field)	0x--
0x8F	Reg_PGVRS[11:8]	[3:0]		
0x90	Reg_PGVRE[7:0]	[5:0]	PG vertical Sync end (1st field)	0x--
0x91	Reg_PGVRS2nd[7:0]	[7:0]	PG vertical Sync start (2nd field)	0x--
0x92	Reg_PGVRS2nd[11:8]	[3:0]		
	Reg_PGEn2ndVRRise[10:8]	**[7:5]**	When Reg_PGEn='1' or Reg_PGInterlaced='1' , this define the location of the 2nd Vsync Rise edge at the horizontal line[10:8].	**x**

0x93	Reg_PGVRE2nd[5:0]	[5:0]	PG vertical Sync end (2nd field)	0x--
	Reg_PGEn2ndVRRise[12:11]	**[7:6]**	When Reg_PGEn='1' or Reg_PGInterlaced='1' , this define the location of the 2nd Vsync Rise edge at the horizontal line[12:11].	**x**
0x94	Reg_PGEn2ndVRRise[7:0]	**[7:0]**	When Reg_PGEn='1' or Reg_PGInterlaced='1' , this define the location of the 2nd Vsync Rise edge at the horizontal line [7:0].	**xx**
Pattern Generator Registers				
0x95		[7:0]		
0x96	Reg_PGPatSel[1:0]	[1:0]	Embedded Pattern Selection 00: User Defined; 01: Color Ramp, 10: Black White; 11: Color Square	00
	Reg_PGPatMux	[4]	Embedded Pattern Multiplex 0: External Pattern, 1: Embedded Pattern	0
	RegStbPixCntSen	[5]	Stable LinePixelCnt sensitivity 0: low sensitivity, 1: high sensitivity	0
	Reg_PGVRE2nd[7:6]	[7:6]	PG vertical Sync end (2nd field)	0x--
0x97	Reg_PGEn	[0]	Pattern Generator 0: Disable; 1: Enable	0
	Reg_PGHRep2	[1]	Horizontal Repeat 1: value change every 2 pixels 0: value change every pixel	0
	Reg_PGVRep2	[2]	Vertical Repeat 1: value change every 2 pixels 0: value change every pixel	0
	Reg_PGHMD[1:0]	[5:4]	Horizontal Pattern Mode 00: Gradient Mode 01: Inversion Mode 1x: Line Mode	00
	Reg_PGVMD [1:0]	[7:6]	Vertical Pattern Mode 00: Gradient Mode 01: Inversion Mode 1x: Line Mode	00
0x98	Reg_PGColR[7:0]	[7:0]	The initial R/Cr value of pattern generation.	0x--
0x99	Reg_PGColG[7:0]	[7:0]	The initial G/Y value of pattern generation.	0x--
0x9A	Reg_PGColB[7:0]	[7:0]	The initial B/Cb value of pattern generation.	0x--
0x9B	Reg_PGColBlank[7:0]	[7:0]	Value during blank interval	0x--
0x9C	Reg_PGColBlankY[7:0]	[7:0]	Value during blank interval.	0x--

0x9D	Reg_PGCHInc[7:0]	[7:0]	Horizontal Color Value Increment in Gradient Mode.	0x--
0x9E	Reg_PGCVInc[7:0]	[7:0]	Vertical Color Value Increment in Gradient Mode.	0x--
0x9F	RAxRqFailSts[1:0]	[1:0]	AUX channel link training request fail status (Read Only) 00: No Error 01: DEFFER too many times 10: NACK 11: Timeout	00
		[4:3]		
	RHPDIRQFailSts[1:0]	[5:4]	AUX channel HPDIRQ request fail status (Read Only) 00: No Error 01: DEFFER too many times 10: NACK 11: Timeout	00
	RPCRqFailSts[1:0]	[7:6]	AUX channel PC request fail status (Read Only) 00: No Error 01: DEFFER too many times 10: NACK 11: Timeout	00
Input Video Timing Registers				
0xA0	RegDPHSyncPol	[0]	Input HSync Polarity 1: Low; 0: High RegDPHSyncPol <= PxRec_DPHSyncPol when(Reg0xA0[1]='0') else Reg0xA0[0];	-
	RegEnUsrDPHSyncPol	[1]	User defined DPHSyncPol 0: Disable; 1: Enable	0
	RegDPVSyncPol	[2]	Input VSync Polarity 1: Low; 0: High RegDPVSyncPol <= PxRec_DPVSyncPol when(Reg0xA0[3]='0') else Reg0xA0[2];	-
	RegEnUsrDPVSyncPol	[3]	User defined DPVSyncPol 0: Disable; 1: Enable	0

	RegInterLaced	[4]	Input Interlaced Mode 0: Non-Interlaced; 1: Interlaced mode RegInterLaced <= PxRec_InterLaced when(Reg0xA0[5]='0') else Reg0xA0[4];	-
	RegEnUsrInterLaced	[5]	User defined InterLaced 0: Disable; 1: Enable	0
	RegDynRange	[6]	Input Dynamic Range 0: VESA range; 1: CEA range	0
	RegColorimetry	[7]	YCbCr Colorimetry 0: ITU-R BT601-5 1: ITU-R BT709-5	0
0xA1	RegDPHTotal[7:0]	[7:0]	Input horizontal total RegDPHTotal <= PxRec_DPHTotal[12:0] when(Reg0xA2[7]='0') else (Reg0xA2[4:0]&Reg0xA1[7:0]);	0x--
0xA2	RegDPHTotal[12:8]	[4:0]		
	RegEnUsrDPHTotal	[7]	User defined DPHTotal[12:0] 0: Disable; 1: Enable	0
0xA3	RegDPHDES[7:0]	[7:0]	Input horizontal DE start RegDPHDES <= PxRec_DPHDES[12:0] when(Reg0xA4[7]='0') else (Reg0xA4[4:0]&Reg0xA3[7:0])	0x--
0xA4	RegDPHDES[12:8]	[4:0]		
	RegEnUsrDPHDES	[7]	User defined DPHDES[12:0]	0
0xA5	RegDPHDEW[7:0]	[7:0]	Input horizontal DE width	0x--
0xA6	RegDPHDEW[12:8]	[4:0]		
	RegEnUsrDPHDEW	[7]	User defined DPHDEW[12:0]	0
0xA7	RegDPHFPH[7:0]	[7:0]	Input horizontal front porch (Read Only)	0x--
0xA8	RegDPHFPH[12:8]	[4:0]		
	~~RegEnUsrDPHFPH~~	~~[7]~~	~~User defined DPHFPH[9:0] (Reserved)~~	~~0~~
0xA9	RegDPHSYNCW[7:0]	[7:0]	Input horizontal Sync width	0x--
0xAA	RegDPHSYNCW[12:8]	[4:0]		
	RegEnUsrDPHSYNCW	[7]	User defined DPHSYNCW[12:0]	0
0xAB	RegDPVTotal[7:0]	[7:0]	Input vertical total (top field)	0x--
0xAC	RegDPVTotal[11:8]	[3:0]		
	RegEnUsrDPVTotal	[7]	User defined DPVTotal[11:0]	0
0xAD	RegDPVDES[7:0]	[7:0]	Input vertical DE start (top field)	0x--

0xAE	RegDPVDES[11:8]	[3:0]		
	RegEnUsrDPVDES	[7]	User defined DPVDES[11:0]	0
0xAF	RegDPVDEW[7:0]	[7:0]	Input vertical DE height (top field)	0x--
0xB0	RegDPVDEW[11:8]	[3:0]		
	RegEnUsrDPVDEW	[7]	User defined DPVDEW[11:0]	0
0xB1	RegDPVFPH[7:0]	[7:0]	Input vertical front porch height (top field) (Read Only)	0x--
0xB2	RegDPVFPH[11:8]	[3:0]		
	~~RegEnUsrDPVFPH~~	~~[7]~~	~~User defined DPVFPH[11:0] (Reserved)~~	~~0~~
0xB3	RegDPVSYNCW[7:0]	[7:0]	Input vertical Sync height (top field)	0x--
0xB4	RegDPVSYNCW[11:8]	[3:0]		
	RegEnUsrDPVSYNCW	[7]	User defined DPVSYNCW[11:0]	0
0xB5	RegEnFieldSwap	[0]	Video Field Swap 0: Disable; 1: Enable	0
	RegSyncClock	[1]	Miscellaneous 0 Bit[0] 0: Link and stream clock asynchronous 1: Link and stream clock synchronous	0
	RegVidStereo	[3:2]	Miscellaneous 1 Bit[2:1] 00: No stereo video transported 01: Next frame is Right eye 10: Reserved 11: Next frame is Left eye	00
	RegEnUserItrVTotalEven	[4]	User defined DPVTotalEven enable 0: Disable; 1: Enable	0
	RegItrVTotalEven	[5]	User defined DPVTotalEven RegItrVTotalEven <= PxRec_DPVTotalEven when(RegB5[4]='0') else RegB5[5];	0
		[6]		0
	RegEnVidParaChgInt	[7]	1: Enable video parameter change interrupt	0
0xB6	RegVBPCompLine[2:0]	[2:0]	Vertical backporch compensation line 000: 1, 001: 2, 010: 4, 011: 8 100: 16, 101: 32, 110: Rsvd, 111: Rsvd	000
	RegColorClip	[3]	1: clip RGBY to 16~235 and CbCr to 16~240	0
		[4]		
	PxVidParaChgSts[9:7]	[7:5]	[7]: HSync Width change [8]: HDE_Start change	000

			[9]: HDE_Width change	
0xB7	PxVidParaChgSts[6:0]	[6:0]	[0]: Vtotal change [1]: VFP change [2]: VSync Width change [3]: VDE_Start change [4]: VDE_Width change [5]: Htotal change [6]: HFP change	0000000
	VidParaChgInt	[7]	Video parameter change interrupt Write ‘1’ to clear this interrupt and also clear PxVidParaChgSts[5:0]	

1.9 Audio Registers

Audio Input Control Registers				
0xB8				
0xB9				
0xBA				
0xBB				

0xBC				
0xBD				
0xBE				
0xBF				
0xC0				
0xC1				
0xC2				
0xC3				
PSR Control Register				

0xC4	LSPSRStatus[3:0]	[3:0]	PSR state (Read Only) [0]: PSR_State1 ➔ PSR inactive [1]: PSR_State2 ➔ PSR transition to active-static frame transmission [2]: PSR_State 3 ➔ PSR active – no RFB update [3]: PSR_State 5: PSR exit (Note: FW must ensure RPSRState=0x1 before entering PSR active)	0x-
	RPSREnterInt	[4]	PSR enter interrupt This interrupt is enabled by RegEnPSR and write '1' to clear	-
	RPSRExitInt	[5]	PSR exit interrupt This interrupt is enabled by RegEnPSR and write '1' to clear	-
	RPSRWakeDetInt	[6]	PSR wake detect interrupt This interrupt is enabled by RegEnPSR and write '1' to clear	-
	RPSRWakeFailInt	[7]	PSR wake fail interrupt This interrupt is enabled by RegEnPSR and write '1' to clear	-
0xC5	RegEnPSR	[0]	eDPTX PSR function 0: Disable, 1: Enable	0
	RegEnFwPSR	[1]	Firmware PSR option 0: use HW PSR, 1: use FW PSR	0
	RegSetFwPSR	[2]	0: FW PSR inactive, 1: FW PSR active	0
	RegEnIdlePat2SR	[3]	Enable Idle Pattern end to transmit SR 0: Disable, 1: Enable	0
	RegEnPSRAVMute	[4]	Enable PSR AV mute 0: Disable, 1: Enable	0
	RegExtraPSRFrame	[5]	PSR entry setup time 0: Frame n+1, 1: Frame n+2	0
	RegAutoPSRReTrain	[6]	PSR exit auto retrain 0: Disable, 1: Enable	1
	RegAutoPSRMLOff	[7]	Auto PSR main-link off 0: Disable, 1: Enable	1
0xC6	RegAuxFreqNum[7:0]	[7:0]	User Defined AUX Frequency Number	0x0C
0xC7	RefAuxFreqCnt[7:0]	[7:0]	AUX Frequency Counter (Read Only)	0x--

1.10 Misc. Control Registers

0xC8	RegFilterMax[2:0]	[2:0]	HPD Glitch Filter Timer Unit = 0.05ms	101
	RegHPDTimeOut[4:0]	[7:3]	HPD Event Timer Unit = 0.1ms	10100
0xC9	RegHPDIRQTimeMin[3:0]	[3:0]	HPD IRQ Event Minimum Timer Unit = 0.05ms	1010
	RegHPDIRQTimeMax[3:0]	[7:4]	HPD IRQ Event Maximum Timer Unit = 0.1ms	1010
0xCA	RegAuxDebugSel[7:0]	[7]& [1:0]	100/000: No delay between AUX reply and next AUX request command 001: 110 us delay between AUX_NACK/AUX_DEFER/I2C_NACK/I2C_DEFER reply and next AUX request command 101: 110 us delay between AUX reply and next AUX request command. 010: 180 us delay between AUX_NACK/AUX_DEFER/I2C_NACK/I2C_DEFER reply and next AUX request command 110: 180 us delay between AUX reply and next AUX request command. 011: 240 us delay between AUX_NACK/AUX_DEFER/I2C_NACK/I2C_DEFER reply and next AUX request command 111: 240 us delay between AUX reply and next AUX request command.	“001”
		[2]	when set high, don’t care AUX_NACK reply to I2C-over-AUX request	0
		[3]	when set high, read EDID without address only AUX command.	0
		[4]	when set high, I2C read LEN is remaining read request byte number, not Reg_I2CRdStep.	1

		[5]	when set high, PxVidStable will be low if video input H/V Sync are absent	0
		[6]	when set high, Test Pattern VCnt increase 2 each line in interlaced mode. This bit shall set high..	1
0xCB	Reg_I2CRdStep[2:0]	[2:0]	AUX to I2C Read Step	000
	Reg_DeferNo[1:0]	[4:3]	AUX Defer Number	00
	REGAuxMasterOpt	[5]	Internal Aux Request Arbitration Option 0: Gated by REG_MasterSel 1: Not gated by REG_MasterSel	1
		[7:6]		00
0xCC				
0xCD				
0xCE	RegReserved2[7:0]	[0]	RegDisMaxPktOpt	0
		[1]	RegDisMinPktOpt1	0
		[2]	RegDisMinPktOpt2	0
		[7]		0
0xCF	RegReserved3[7:0]	[0]	RegUsrDrvPre	
		[4]	RegEneDPOpt 0: DP mode, 1: eDP mode	0
		[5]	RegDisGatHPDIRQ 0: Enable hardware HPD IRQ gating 1: Disable hardware HPD IRQ gating	0
		[6]	RegHPDIRQMaxSel 0: use RegHPDIRQTimeMax[3:0] 1: use RegHPDTimeOut[4:0]	1
		[7]	RegDisGBNum 0: Enable GB, 1: Disable GB	0

1.11 Data Link Layer Registers

Main Link Registers				
0xD0	RegTUNum[5:0]	[5:0]	DisplayPort TU Number divided by 2 0x10: TU = 32 (minimum) 0x20: TU = 64 (maximum)	0x18
	RegGBNum[1:0]	[7:6]	Packet Guard Band Number Unit = 8T	0x0
0xD1	RegVSNumInt[6:0]	[6:0]	User Defined VS Number (Integer) Unit = 1TU	0x--
	RegAutoVSNum	[7]	Auto VS Calculation Mode 0: Disable; 1: Enable	1
0xD2	RegVSNumFrac[7:0]	[7:0]	User Defined VS Number (Fraction) Unit = 1/256TU	0x--
0xD3	RegEnhFraming	[0]	Enhanced Framing Mode 0: Disable; 1: Enable	0
	RegAutoVidFifoRst	[1]	Auto Video FIFO Reset 0: Disable; 1: Enable	1
	RegEnVidFifoRst	[2]	Video FIFO Reset by Manual 0: Disable; 1: Enable	0
		[3]		
	RegEnVidMute	[4]	Video Mute 0: Disable; 1: Enable	1
		[7]		
0xD4	RegEnEnhVidStmp	[0]		1
	RegEnUsrVidStmp	[1]		0
	RegStmpIntStep[1:0]	[5:4]		00
	RegEnBSSeqGat	[6]		0
		[7]		
0xD5	RegVidTimeStmpN[7:0]	[7:0]		0x00
0xD6	RegVidTimeStmpN[15:8]	[7:0]		0x80
0xD7	RegVidTimeStmpN[23:16]	[7:0]		0x00
0xD8	RegVidTimeStmpM[7:0]	[7:0]		0x--
0xD9	RegVidTimeStmpM[15:8]	[7:0]		0x--

0xDA	RegVidTimeStmpM[23:16]	[7:0]		0x--
0xDB	SysVidStmpCnt[7:0]	[7:0]	(Read Only)	0x--
0xDC	SysVidStmpCnt[15:8]	[7:0]		0x--
0xDD	SysVidStmpCnt[23:16]	[7:0]		0x--
0xDE				
0xDF				
0xE0				
0xE1				
0xE2				
0xE3				
0xE4				
0xE5				
0xE6				
0xE7	RegQueueNum[5:0]	[5:0]	User defined queue number	0x10
		[6]		
	RegAutoQueNum	[7]		1
Packet Registers				
0xE8	RegPktAVIInfoEn	[0]	AVI InforFrame Packet 0: Disable; 1: Enable	0
	RegPktMpgInfoEn	[2]	MPEG InforFrame Packet 0: Disable; 1: Enable	0
	RegPktGenInfoEn	[3]	General InforFrame Packet 0: Disable; 1: Enable	0
	RegEnVidTimeStmp	[4]	Video Time Stamp Packet 0: Disable; 1: Enable	0
		[7:6]		
AVI InfoFrame Packet				
0xE9	RegPktAVIInfoS[1:0]	[1:0]		00
	RegPktAVIInfoB[1:0]	[3:2]		00
	RegPktAVIInfoA	[4]		0
	RegPktAVIInfoY[1:0]	[6:5]		00
		[7]		
0xEA	RegPktAVIInfoR[3:0]	[3:0]		1000
	RegPktAVIInfoM[1:0]	[5:4]		00
	RegPktAVIInfoC[1:0]	[7:6]		00

0xEB	RegPktAVIInfoSC[1:0]	[1:0]		00
	RegPktAVIInfoQ[1:0]	[3:2]		00
	RegPktAVIInfoEC[2:0]	[6:4]		000
	RegPktAVIInfoITC	[7]		0
0xEC	RegPktAVIInfoVIC[6:0]	[6:0]		0x0
		[7]		
0xED	RegPktAVIInfoPR[3:0]	[3:0]		0x0
		[7:4]		
0xEE	RegPktAVIInfo06PB[7:0]	[7:0]		0x--
0xEF	RegPktAVIInfo07PB[7:0]	[7:0]		0x--
0xF0	RegPktAVIInfo08PB[7:0]	[7:0]		0x--
0xF1	RegPktAVIInfo09PB[7:0]	[7:0]		0x--
0xF2	RegPktAVIInfo10PB[7:0]	[7:0]		0x--
0xF3	RegPktAVIInfo11PB[7:0]	[7:0]		0x--
0xF4	RegPktAVIInfo12PB[7:0]	[7:0]		0x--
0xF5	RegPktAVIInfo13PB[7:0]	[7:0]		
0xF6	RegPktAVIInfoSUM[7:0]	[7:0]		
Audio InfoFrame Packet				
0xF7				
0xF8				
0xF9				
0xFA				
0xFB				
0xFC		[3:0]		
	RegVidMOffset[2:0]	[6:4]	Video Time Stamp offset [1:0]: offset value, 0 ~ 3 [2]: offset polarity, 0: +, 1: -	000
		[7]		
MIPI I2C slave port setting				
0xFD	RegMIPIPort[7:0]	[7:0]	[0]: MIPIRX I2C enable [7:1]: MIPIRX I2C slave address	0xD8
0xFE	RegCMDHold[2:0]	[2:0]	PC CMD hold option	010
	RegINTDrv[1:0]	[4:3]	INT driving strength	01

	RegMISCDrv[1:0]	[6:5]	MISC I/O driving strength	00
	RegCMDSMT	[7]	PCSCL/PCSDA Schmitt trigger option	0
0xFF	Pass Word	[7:0]		

2. DPTX Registers in Bank 1

MPEG InfoFrame Packet				
0x130	RegPktMpgInfo01PB[7:0]	[7:0]		0x--
0x131	RegPktMpgInfo02PB[7:0]	[7:0]		0x--
0x132	RegPktMpgInfo03PB[7:0]	[7:0]		0x--
0x133	RegPktMpgInfo04PB[7:0]	[7:0]		0x--
0x134	RegPktMpgInfoMF[1:0]	[1:0]		00
		[3:2]		--
	RegPktMpgInfoFR	[4]		-
0x135	RegPktMpgInfoSUM[7:0]	[7:0]		0x--
General InfoFrame Packet				
0x136	RegPktGenType[6:0]	[6:0]		0x--
		[7]		-
0x137	RegPktGen01PB[7:0]	[7:0]		0x--
0x138	RegPktGen02PB[7:0]	[7:0]		0x--
0x139	RegPktGen03PB[7:0]	[7:0]		0x--
0x13A	RegPktGen04PB[7:0]	[7:0]		0x--
0x13B	RegPktGen05PB[7:0]	[7:0]		0x--
0x13C	RegPktGen06PB[7:0]	[7:0]		0x--
0x13D	RegPktGen07PB[7:0]	[7:0]		0x--
0x13E	RegPktGen08PB[7:0]	[7:0]		0x--
0x13F	RegPktGen09PB[7:0]	[7:0]		0x--
0x140	RegPktGen10PB[7:0]	[7:0]		0x--

0x141	RegPktGen11PB[7:0]	[7:0]		0x--
0x142	RegPktGen12PB[7:0]	[7:0]		0x--
0x143	RegPktGen13PB[7:0]	[7:0]		0x--
0x144	RegPktGen14PB[7:0]	[7:0]		0x--
0x145	RegPktGen15PB[7:0]	[7:0]		0x--
0x146	RegPktGen16PB[7:0]	[7:0]		0x--
0x147	RegPktGen17PB[7:0]	[7:0]		0x--
0x148	RegPktGen18PB[7:0]	[7:0]		0x--
0x149	RegPktGen19PB[7:0]	[7:0]		0x--
0x14A	RegPktGen20PB[7:0]	[7:0]		0x--
0x14B	RegPktGen21PB[7:0]	[7:0]		0x--
0x14C	RegPktGen22PB[7:0]	[7:0]		0x--
0x14D	RegPktGen23PB[7:0]	[7:0]		0x--
0x14E	RegPktGen24PB[7:0]	[7:0]		0x--
0x14F	RegPktGen25PB[7:0]	[7:0]		0x--
0x150	RegPktGen26PB[7:0]	[7:0]		0x--
0x151	RegPktGen27PB[7:0]	[7:0]		0x--
0x152	RegPktGen28PB[7:0]	[7:0]		0x--
PSR VSC Packet				
0x153	RegPktPSRVSC00PB[7:0]	[7:0]		0x00
0x154				
0x155				
0x156				
0x157				
0x158				
0x159				
0x15A				
0x15B				
0x15C				
0x15D				
0x15E				
0x15F	RPSRWakeDone	[0]	FW PSR wakeup done (Write ‘1’ to trigger 1T pulse)	-
	RPSRWakeBusy	[1]	HW PSR wakeup busy (Read Only)	-
EMEM Control Registers				
0x160				

0x161				
0x162				
0x163				
0x164				
0x165				
0x166				
0x167				
Hardware HPD IRQ Read Back Register				
0x168	RDPCD_Reg200h	[7:0]	DPCD200H Value (Read Only)	0x--
0x169	RDPCD_Reg201h	[7:0]	DPCD201H Value (Read Only)	0x--
0x16A	RDPCD_Reg202h	[7:0]	DPCD202H Value (Read Only)	0x--
0x16B	RDPCD_Reg203h	[7:0]	DPCD203H Value (Read Only)	0x--
0x16C	RDPCD_Reg204h	[7:0]	DPCD204H Value (Read Only)	0x--
0x16D	RDPCD_Reg205h	[7:0]	DPCD205H Value (Read Only)	0x--
0x16E				
0x16F				
AFE DRV/PRE Setting Register				
0x170	RegDrv0dB400mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x40
0x171	RegPre0dB400mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x00
0x172	RegDrv3p5dB400mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x50
0x173	RegPre3p5dB400mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x21
0x174	RegDrv6dB400mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x62
0x175	RegPre6dB400mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT	0x41

			[7:3]: Driver current of de-emphasis path, T	
0x176	RegDrv9p5dB400mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x85
0x177	RegPre9p5dB400mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x85
0x178	RegDrv0dB600mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x61
0x179	RegPre0dB600mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x00
0x17A	RegDrv3p5dB600mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x7C
0x17B	RegPre3p5dB600mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x34
0x17C	RegDrv6dB600mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x96
0x17D	RegPre6dB600mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x6D
0x17E	RegDrv0dB800mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0x82
0x17F	RegPre0dB800mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x00
0x180	RegDrv3p5dB800mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0xA6
0x181	RegPre3p5dB800mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x45

0x182	RegDrv0dB1200mV	[7:0]	[2:0]: Predriver current of main path, PS [7:3]: Driver current of main path, S	0xC6
0x183	RegPre0dB1200mV	[7:0]	[2:0]: Predriver current of de-emphasis path, PT [7:3]: Driver current of de-emphasis path, T	0x07
0x184	Reg_DRV_LNPLOW[3:0]	[3:0]	Backup pull-low signals for predrivers of LN3~0	0000
		[7:4]		
0x185				
0x186				
0x187				
SSC Control Registers				
0x188	Reg_SDMMax[7:0]	[7:0]	SSC Control	0xD2
0x189	Reg_SDMMax[13:8]	[5:0]		0x21
		[6]		
		[7]		
0x18A	Reg_SDMInc[6:0]	[6:0]	SSC Control	0x4E
		[7]		
0x18C				
0x18D				
0x18E				
0x18F				
AUX Debug Function				
0x190	RegAuxDebug	[0]	AUX Debug Function 0: Disable, 1: Enable	0
	RegAuxDebugDone	[1]	AUX Debug Done Write ‘1’ to set this signal to High and it is reset by RAUXDbgIntTrg	0
		[2]		
		[3]		
	RAuxDebugTrg	[4]	AUX Debug Trigger (Read Only) 0: No Aux event, 1: New Aux event	0x-
		[7:5]		
0x191	AXT_ByteOutNoRec	[3:0]	AuxTx output byte number (Read Only)	0x-
	AXR_ByteInNoRec	[7:4]	AuxRx input byte number (Read Only)	0x-
0x192	AXT_TxByte0LH	[7:0]	AuxTx output byte 0 (Read Only)	0x--

0x193	AXT_TxByte1LH	[7:0]	AuxTx output byte 1 (Read Only)	0x--
0x194	AXT_TxByte2LH	[7:0]	AuxTx output byte 2 (Read Only)	0x--
0x195	AXT_TxByte3LH	[7:0]	AuxTx output byte 3 (Read Only)	0x--
0x196	AXT_TxByte4LH	[7:0]	AuxTx output byte 4 (Read Only)	0x--
0x197	AXT_TxByte5LH	[7:0]	AuxTx output byte 5 (Read Only)	0x--
0x198	AXT_TxByte6LH	[7:0]	AuxTx output byte 6 (Read Only)	0x--
0x199	AXT_TxByte7LH	[7:0]	AuxTx output byte 7 (Read Only)	0x--
0x19A	AXR_ByteIn0LH	[7:0]	AuxRx intput byte 0 (Read Only)	0x--
0x19B	AXR_ByteIn1LH	[7:0]	AuxRx intput byte 1 (Read Only)	0x--
0x19C	AXR_ByteIn2LH	[7:0]	AuxRx intput byte 2 (Read Only)	0x--
0x19D	AXR_ByteIn3LH	[7:0]	AuxRx intput byte 3 (Read Only)	0x--
0x19E	AXR_ByteIn4LH	[7:0]	AuxRx intput byte 4 (Read Only)	0x--
0x19F	AXR_ByteIn5LH	[7:0]	AuxRx intput byte 5 (Read Only)	0x--
0x1A0	AXR_ByteIn6LH	[7:0]	AuxRx intput byte 6 (Read Only)	0x--
0x1A1	AXR_ByteIn7LH	[7:0]	AuxRx intput byte 7 (Read Only)	0x--
0x1A2	AXR_ByteIn8LH	[7:0]	AuxRx intput byte 8 (Read Only)	0x--
0x1A3				
0x1A4				
0x1A5				
0x1A6				
0x1A7				

3. MIPIRX Registers

2.1 General Control Registers

Offset	Register Name	Bit	Definition	Default
Chip Information Registers				
0x00	Vendor ID[7:0]	[7:0]	Vendor ID Low Byte (Read Only)	0x54
0x01	Vendor ID[15:8]	[7:0]	Vendor ID High Byte (Read Only)	0x49
0x02	Device ID[7:0]	[7:0]	Device ID Low Byte (Read Only)	0x51
0x03	Device ID[15:8]	[7:0]	Device ID High Byte (Read Only)	0x61
0x04	Sub-Revision ID[3:0]	[3:0]	Sub-Revision ID (Read Only)	0x0
	Major-Revision ID[3:0]	[7:4]	Major-Revision ID (Read Only)	0xA
Software Reset Registers				
0x05	RegSoftORst	[0]	Software OCLK clock domain reset	1
	RegSoftMRst	[1]	Software MCLK clock domain reset	1
	RefSoftBRst	[2]	Software BCLK clock domain reset	1
	RefSoftNRst	[3]	Software NCLK clock domain rest	1
	RegMPSoftPRst	[4]	MP Software PCLK clock domain reset	1
	RegDPSoftPRst	[5]	DP Software PCLK clock domain reset	1
		[6]		0
		[7]		0
Interrupt Status and Clear Registers				
0x06	RPPSMVidStbChgInt	[0]	PPS MVidStb change interrupt Write ‘1’ to clear this interrupt	-
	RPPSMHSyncErrInt	[1]	PPS MHSync error interrupt Write ‘1’ to clear this interrupt	-
	RPPSMHDEErrInt	[2]	PPS MHDE error interrupt Write ‘1’ to clear this interrupt	-
	RPPSMVSyncErrInt	[3]	PPS MVSync error interrupt Write ‘1’ to clear this interrupt	-
	RPPSPVidStbChgInt	[4]	PPS PVidStb change interrupt Write ‘1’ to clear this interrupt	-
	RPPSPHSyncErrInt	[5]	PPS PHSync error interrupt Write ‘1’ to clear this interrupt	-
	RPPSPHDEErrInt	[6]	PPS PHDE error interrupt Write ‘1’ to clear this interrupt	-
	RPPSMVDEErrInt	[7]	PPS MVDE error interrupt Write ‘1’ to clear this interrupt	-

0x07	RPPSRxPSRChgInt	[0]	PPS RxPSR change interrupt Write ‘1’ to clear this interrupt	-
	RPPSDByteErrInt	[1]	PPS data byte error interrupt Write ‘1’ to clear this interrupt	-
	RFFCWRDiffInt	[2]	FIFO C W/R different interrupt Write ‘1’ to clear this interrupt	-
	RUFODecNumDiffInt	[3]	UFO decode number different interrupt Write ‘1’ to clear this interrupt	-
	RFFAWRDiffInt	[4]	FIFO A W/R different interrupt Write ‘1’ to clear this interrupt	-
	RUFOBufCFlwInt	[5]	FIFO C over/under-flow interrupt Write ‘1’ to clear this interrupt	-
	RUFOBufAFlwInt	[6]	FIFO A over/under-flow interrupt Write ‘1’ to clear this interrupt	-
	RUFOBufBFlwInt	[7]	FIFO B over/under-flow interrupt Write ‘1’ to clear this interrupt	-
0x08	RECC1bErrInt	[0]	ECC 1b error interrupt Write ‘1’ to clear this interrupt	-
	RECC2bErrInt	[1]	ECC 2b error interrupt Write ‘1’ to clear this interrupt	-
	RLMFIFOErrInt	[2]	LM FIFO error interrupt Write ‘1’ to clear this interrupt	-
	RCRCErrInt	[3]	CRC error interrupt Write ‘1’ to clear this interrupt	-
	RMCLKOffInt	[4]	MCLK off interrupt Write ‘1’ to clear this interrupt	-
	RPPIFifoOvWrInt	[5]	PPI fifo over-write interrupt Write ‘1’ to clear this interrupt	-
	RTimerInt	[6]	User timer interrupt Write ‘1’ to clear this interrupt	-
		[7]		
Interrupt Mask Registers				
0x09	REnPPSMVidStbChgInt	[0]	‘0’: Disable interrupt event ‘1’: Enable interrupt event	0
	REnPPSMHSyncErrInt	[1]		0
	REnPPSMHDEErrInt	[2]		0
	REnPPSMVSyncErrInt	[3]		0
	REnPPSPVidStbChgInt	[4]		0
	REnPPSPHSyncErrInt	[5]		0

	REnPPSPHDEErrInt	[6]		0
	REnPPSMVDEErrInt	[7]		0
0x0A	REnPPSRxPSRChgInt	[0]		0
	REnPPSDByteErrInt	[1]		0
	REnFFCWRDiffInt	[2]		0
	REnUFODecNumDiffInt	[3]		0
	REnFFAWRDiffInt	[4]		0
	REnUFOBufCFlwInt	[5]		0
	REnUFOBufAFlwInt	[6]		0
	REnUFOBufBFlwInt	[7]		0
0x0B	REnECC1bErrInt	[0]		0
	REnECC2bErrInt	[1]		0
	REnLMFIFOErrInt	[2]		0
	REnCRCErrInt	[3]		0
	REnMCLKOffInt	[4]		0
	REnPPIFifoOvWrInt	[5]		0
	REnTimerInt	[6]		0
		[7]		0
System Configuration Registers				
0x0C	RegEnUFO	[0]	1: Enable UFO function	1
	RegEnExtPSR	[1]	1: select external PSR input signal	0
		[2]		
		[3]		
	RegLaneNum[1:0]	[5:4]	00: 1-Lane, 01: 2-Lane, 10: 3-Lane, 11: 4-Lane	11
	RegEnPNSwap	[6]	MIPIRX DP/DN swap 0: Disable, 1: Enable	0
	RegEnLaneSwap	[7]	MIPIRX lane swap 0: Disable, 1: Enable	0
System Status Registers				
0x0D	RINTStatus	[0]	MIPIRX Interrupt Status (Read Only) 0: No interrupt event 1: Interrupt is active	-
		[1]		
		[2]		

	RMCLKOffSts	[3]	MCLK off status (Read Only) 0: Detect MCLK on 1: Detect MCLK off	-
	RMVidStbSts	[4]	MVidStb status (Read Only) 0: unstable, 1: stable	-
	RPVidStbSts	[5]	PVidStb status (Read Only) 0: unstable, 1: stable	-
	RxPSR	[6]	Current RxPSR status (Read Only)	-
		[7]		
0x0E		[0]		
		[1]		
		[2]		
		[3]		
		[4]		
		[5]		
		[6]		
		[7]		
System Debug Registers				
0x0F		[0]		
		[1]		
		[2]		
		[3]		
		[4]		
		[7:5]		

2.2 CLKBUF Control Registers

0x10	RegGateOCLK	[0]	'1': Power down OCLK	0
	RegGateMCLK	[1]	'1': Power down MCLK	0
	RegGateNCLK	[2]	'1': Power down NCLK	0
	RegGateBCLK	[3]	'1': Power down BCLK	0
	RegGatePCLK	[4]	'1': Power down PCLK	0
		[5]		
		[6]		
		[7]		
0x11	RegInvMCLK	[0]	'1': Inverse MCLK	1
	RegMuxMtoN	[1]	'1': NCLK/BCLK = MCLK	0
		[2]		

		[3]		
		[4]		
		[5]		
		[6]		
		[7]		
0x12	RegEnPSR2PwdMP	[0]	PSR to power-down MIPI RX 0: Disable, 1: Enable	0
	RegEnPSR2RstMP	[1]	PSR to reset MIPI RX 0: Disable, 1: Enable	0
0x13				
0x14				
0x15				
0x16	RMCLKCnt[7:0]	[7:0]	(Read Only)	0x---
0x17	RMCLKCnt[11:8]	[3:0]		
	RegPreDivSel[2:0]	[6:4]	Extra MCLK division counter	000
	RegEnMCLKCnt	[7]		0

2.3 PHY-Protocol Interface Registers

0x18	RegHSSetNum[2:0]	[2:0]	HS settle number	100
		[3]		
	RegSkipStg[2:0]	[6:4]	HS trailing skip stage	011
		[7]		
0x19	RegEnDeSkew	[0]	‘1’: Enable multi-lane deskew	0
	RegEnContCK	[1]	‘1’: Force continuous clock mode	0
		[2]		
		[3]		
	RegPPIDbgSel[2:0]	[6:4]	PPI debug selection	000
		[7]		
0x1A				
0x1B				
0x1C				
0x1D				

0x1E				
0x1F				

2.4 Lane Merge & Packet Decoder Registers

0x20	RegIgnrNull	[0]	'1': Ignore Null packet	1
	RegIgnrBlk	[1]	'1': Ignore Blank packet	1
	RegEnDummyECC	[2]	'1': Enable dummy ECC error	0
		[3]		
	RegSelLMDbg[2:0]	[6:4]	LM debug selection	000
		[7]		
0x21				
0x22				
0x23				
0x24				
0x25				
0x26	RegSelLMDbg[2:0]	[2:0]	LM debug selection	000
0x27	RegVCNum[1:0]	[7:6]	Virtual channel number	00
	RegVidType[5:0]	[5:0]	Packed Pixel Stream data type	0x3E

2.5 UFO Registers

0x28	Reg_VLC_En	[0]	'1': Enable VLC mode	0
		[5:1]		
	Reg_Block_Cnt[9:8]	[7:6]	UFO block number	01
0x29	Reg_Block_Cnt[7:0]	[7:0]		0xFF
0x2A	Reg_UFO_cfg[7:0]	[7:0]	UFO configuration [31:16]: Reserved	0x05
0x2B	Reg_UFO_cfg[15:8]	[7:0]		0x00
0x2C	Reg_UFO_cfg[23:16]	[7:0]		0x00
0x2D	Reg_UFO_cfg[31:24]	[7:0]		0x00
0x2E	RegHDEDelay[6:0]	[6:0]	UFO HDE delay number	0x34
	RegUFOFifoRst	[7]	1: UFO FIFO reset	0
0x2F	RegEnUFOReSync	[0]	1: Enable UFO re-sync	0
	RegDisUFOAutoRst	[1]	1: Disable UFO FIFO auto-reset	0
		[3:2]		
	RegUFODbgSel[2:0]	[6:4]	UFO debug selection	000
		[7]		

2.6 Packed Pixel Stream and Timing Generator Registers

0x30	RegMipi_HSS[7:0]	[7:0]	RegMipi_HSS <= PRec_HSS when(Reg0x31[7]='0') else (Reg0x31[3:0]&Reg0x30[7:0])	0x--
0x31	RegMipi_HSS[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrHSS	[7]	User defined Mipi_HSS[11:0]	0
0x32	RegMipi_HSE[7:0]	[7:0]	RegMipi_HSE <= PRec_HSE when(Reg0x33[7]='0') else (Reg0x33[3:0]&Reg0x32[7:0])	0x--
0x33	RegMipi_HSE[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrHSE	[7]	User defined Mipi_HSE[11:0]	0
0x34	RegMipi_HDES[7:0]	[7:0]	RegMipi_HDES <= PRec_HDES when(Reg0x35[7]='0') else (Reg0x35[3:0]&Reg0x34[7:0])	0x--
0x35	RegMipi_HDES[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrHDES	[7]	User defined Mipi_HDES[11:0]	0
0x36	RegMipi_HDEE[7:0]	[7:0]	RegMipi_HDEE <= PRec_HDEE when(Reg0x37[7]='0') else (Reg0x37[3:0]&Reg0x36[7:0])	0x--
0x37	RegMipi_HDEE[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrHDEE	[7]	User defined Mipi_HDEE[11:0]	0
0x38	RegMipi_HTotal[7:0]	[7:0]	RegMipi_HTotal <= PRec_HTotal when(Reg0x39[7]='0') else (Reg0x39[3:0]&Reg0x38[7:0])	0x--
0x39	RegMipi_HTotal[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrHTotal	[7]	User defined Mipi_HTotal[11:0]	0
0x3A	RegMipi_VSS[7:0]	[7:0]	RegMipi_VSS <= PRec_VSS when(Reg0x3B[7]='0') else (Reg0x3B[3:0]&Reg0x3A[7:0])	0x--
0x3B	RegMipi_VSS[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrVSS	[7]	User defined Mipi_VSS[11:0]	0
0x3C	RegMipi_VSE[7:0]	[7:0]	RegMipi_VSE <= PRec_VSE when(Reg0x3D[7]='0') else (Reg0x3D[3:0]&Reg0x3C[7:0])	0x--
0x3D	RegMipi_VSE[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrVSE	[7]	User defined Mipi_VSE[11:0]	0
0x3E	RegMipi_VDES[7:0]	[7:0]	RegMipi_VDES <= PRec_VDES	0x--

0x3F	RegMipi_VDES[11:8]	[3:0]	when(Reg0x3F[7]='0') else (Reg0x3F[3:0]&Reg0x3E[7:0])	0x-
		[6:4]		
	RegEnUsrVDES	[7]	User defined Mipi_VDES[11:0]	0
0x40	RegMipi_VDEE[7:0]	[7:0]	RegMipi_VDEE <= PRec_VDEE when(Reg0x41[7]='0') else (Reg0x41[3:0]&Reg0x40[7:0])	0x--
0x41	RegMipi_VDEE[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrVDEE	[7]	User defined Mipi_VDEE[11:0]	0
0x42	RegMipi_VTotal[7:0]	[7:0]	RegMipi_VTotal <= PRec_VTotal when(Reg0x43[7]='0') else (Reg0x43[3:0]&Reg0x42[7:0])	0x--
0x43	RegMipi_VTotal[11:8]	[3:0]		0x-
		[6:4]		
	RegEnUsrVTotal	[7]	User defined Mipi_VTotal[11:0]	0
0x44				
0x45				
0x46				
0x47				
0x48				
0x49				
0x4A				
0x4B				
0x4C				
0x4D				
0x4E	RegMipi_HSPol	[0]	0: active low, 1: active high	0
	RegMipi_VSPol	[1]	0: active low, 1: active high	0
	RegHReSyncEn	[2]	1: Enable H timing re-sync	0
	RegVReSyncEn	[3]	1: Enable V timing re-sync	0
	RegForceMCLKOn	[4]	0: Normal operation 1: Force MCLK on	0
		[5]		
		[6]		
	RegForcePPSStb	[7]	0: Normal operation 1: Force PPS stable	0
0x4F	RegWPtrSt[3:0]	[3:0]	PPS write start point	0110
	RegDBGPPSSel[2:0]	[6:4]	PPS debug selection	000
		[7]		

0x50	MRec_HSS[7:0]	[7:0]	(Read Only)	0x--
0x51	MRec_HSS[11:8]	[3:0]		0x-
		[7:4]		0
0x52	MRec_HSE[7:0]	[7:0]	(Read Only)	0x--
0x53	MRec_HSE[11:8]	[3:0]		0x-
		[7:4]		0
0x54	MRec_HDES[7:0]	[7:0]	(Read Only)	0x--
0x55	MRec_HDES[11:8]	[3:0]		0x-
		[7:4]		0
0x56	MRec_HDEE[7:0]	[7:0]	(Read Only)	0x--
0x57	MRec_HDEE[11:8]	[3:0]		0x-
		[7:4]		0
0x58	MRec_HTotal[7:0]	[7:0]	(Read Only)	0x--
0x59	MRec_HTotal[11:8]	[3:0]		0x-
		[7:4]		0
0x5A	MRec_VSS[7:0]	[7:0]	(Read Only)	0x--
0x5B	MRec_VSS[11:8]	[3:0]		0x-
		[7:4]		0
0x5C	MRec_VSE[7:0]	[7:0]	(Read Only)	0x--
0x5D	MRec_VSE[11:8]	[3:0]		0x-
		[7:4]		0
0x5E	MRec_VDES[7:0]	[7:0]	(Read Only)	0x--
0x5F	MRec_VDES[11:8]	[3:0]		0x-
		[7:4]		0
0x60	MRec_VDEE[7:0]	[7:0]	(Read Only)	0x--
0x61	MRec_VDEE[11:8]	[3:0]		0x-
		[7:4]		0
0x62	MRec_VTotal[7:0]	[7:0]	(Read Only)	0x--
0x63	MRec_VTotal[11:8]	[3:0]		0x-
		[7:4]		0
0x64				
0x65				
0x66				
0x67				
0x68				
0x69				
0x6A				

0x6B				
0x6C				
0x6D				
0x6E	PRec_HDEW[7:0]	[7:0]	(Read Only)	0x--
0x6F	PRec_HDEW[11:8]	[3:0]		0x-
		[7:4]		
0x70	RegMShift[2:0]	[2:0]	Allowable MCLK horizontal shift value	000
	RegEnMAvg	[3]	MCLK horizontal average 0: Disable, 1: Enable	1
	RegPShift[2:0]	[6:4]	Allowable PCLK horizontal shift value	011
		[7]		
0x71 ~ 0x7D				
0x7E	PFFBWStgNum[7:0]	[7:0]	(Read Only)	0x---
0x7F	PFFBWStgNum[9:8]	[1:0]		
	BUFOBufCOFlw	[2]	FIFO C over-flow (Read Only)	-
	BUFOBufCUFlw	[3]	FIFO C under-flow (Read Only)	-
	PUFOBufAOFlw	[4]	FIFO A over-flow (Read Only)	-
	PUFOBufAUFlw	[5]	FIFO A under-flow (Read Only)	-
	PUFOBufBOFlw	[6]	FIFO B over-flow (Read Only)	-
	PUFOBufBUFlw	[7]	FIFO B under-flow (Read Only)	-

2.7 AFE Registers

0x80	RegHSDivN[4:0]	[4:0]	PCLK HSCLK divided by N	00011
	RegHSMul2	[5]	PCLK HSCLK multiplied by 2	1
		[6]		
	RegRstDivN	[7]	1: Reset HSDivN	0
0x81	REGLSVHSEL[1:0]	[1:0]	Select high reference voltage of LS receiver (TT) 00: 0.85v ; 01: 0.90v 10: 0.95v ; 11: 1.00v	01
	REGLSVLSEL[1:0]	[3:2]	Select low reference voltage of LS receiver (TT) 00: 0.40v; 01: 0.45v 10: 0.50v; 11: 0.55v	01

	REGHSRS[1:0]	[5:4]	HS EQ amplifier R 11 or 10 : weak 01: middle 00: strong	11
	REGRCKD4P[1:0]	[7:6]	Clock delay options of the div4 clock path. The timing value is the same as REGHSCP.	00
0x82	REGHSCP[7:0]	[7:0]	Clock delay options of the 4 lanes. (TT) [7:6]: lane3; [5:4]: lane2 [3:2]: lane1 [1:0]: lane0 00: 140ps; 01: 240ps 10: 340ps; 11: 440ps	0x00
0x83	REGHSDP[7:0]	[7:0]	Data delay options of the 4 lanes. The timing value is the same as REGHSCP.	0x00
0x84	REGHSAMP[3:0]	[3:0]	HS amplifier stage current [3:2] [1:0] 1111: largest current 0000: smallest current	1111
	REGRTERM[2:0]	[6:4]	Select Termination value of all of the channels(TT) 000: 116 ohm; 001: 112ohm 010: 108 ohm; 011: 104ohm 100: 100 ohm; 101: 97 ohm 110: 93 ohm ; 111: 90 ohm	100
	REGHSCS	[7]	HS EQ amplifier C	1
0x85				
0x86				
0x87				
0x88				
0x89				
0x8A				
0x8B				
0x8C				
0x8D				
0x8E				
0x8F				

2.8 MISC. Registers

0x90	RegEnTimeStmp	[0]	Enable time stamp	0
		[7:1]		
0x91	Reg10usTimeInt[7:0]	[7:0]	10us time count of RCLK	0x87
0x92	RegTimerIntNum[7:0]	[7:0]	Timer interrupt count number	0x1E
0x93	RTimeStmp[7:0]	[7:0]	Time stamp, unit=100ms (Read Only)	0x--
0x94				
0x95				
0x96	RegEnFIFOCBIST	[0]	FIFO C BIST function 0: Disable, 1: Enable	0
	RegEnFIFOABIST	[1]	FIFO A BIST function 0: Disable, 1: Enable	0
	RegEnFIFOBBIST	[2]	FIFO B BIST function 0: Disable, 1: Enable	0
		[7:3]		
0x97	RFIFOCBISTDone	[0]	1: FIFO C BIST done (Read Only)	-
	RFIFOCBISTFail	[1]	1: FIFO C BIST fail (Read Only)	-
	RFIFOABISTDone	[2]	1: FIFO A BIST done (Read Only)	-
	RFIFOABISTFail	[3]	1: FIFO A BIST fail (Read Only)	-
	RFIFOBBISTDone	[4]	1: FIFO B BIST done (Read Only)	-
	RFIFOBBISTFail	[5]	1: FIFO B BIST fail (Read Only)	-
		[6]		
		[7]		
0x98	BUFO_Dbg_Info0[7:0]	[7:0]	UFO debug information 0 (Read Only)	0x--
0x99	BUFO_Dbg_Info0[15:8]	[7:0]		0x--
0x9A	BUFO_Dbg_Info0[23:16]	[7:0]		0x--
0x9B	BUFO_Dbg_Info0[31:24]	[7:0]		0x--
0x9C	BUFO_Dbg_Info1[7:0]	[7:0]	UFO debug information 1 (Read Only)	0x--
0x9D	BUFO_Dbg_Info1[15:8]	[7:0]		0x--
0x9E	BUFO_Dbg_Info1[23:16]	[7:0]		0x--
0x9F	BUFO_Dbg_Info1[31:24]	[7:0]		0x--

Note:

Interrupt	Clock Domain	Trigger Signal
RHPDChgInt	RCLK	
RHPDIRQInt	RCLK	Mask by extra RHPDIRQGat signal (DC Constant)
RVidStableInt	PCLK	PxVidStable (not 1T pulse)
RAxRqFailInt	RCLK	RAxRqFail
RHPDIRQFailInt	RCLK	RHPDIRQFail
RPCRqFailInt	RCLK	RPCRqFail
RTrainAxFailInt	RCLK	RefAxFailInt
RPktAVIInfoInt	LSCLK	LSPktAVIInfoDone
RPktMpgInfoInt	LSCLK	LSPktMpgInfoDone
RPktGenInfoInt	LSCLK	LSPktGenInfoDone
RPktVidAttrInt	LSCLK	LSSysVidAttrDone
RVidCTSErrInt	LSCLK	LSSysVidAttrInt
RLinkTrainFailInt	RCLK	RefLinkTrainFail
RVidOvFlwInt	LSCLK	LSVidOvFlwInt
R501FIFOOvInt	RCLK	R501FIFOOvRW
RPSREnterInt	LSCLK (1T pulse)	LSPSREnterInt
RPSRExitInt	LSCLK (1T pulse)	LSPSRExitInt
RPSRWakeDetInt	RCLK (Level) (generate interrupt from 0 to 1)	RPSRWakeDet
RPSRWakeFailInt	RCLK (1T pulse)	RPSRWakeFail

Note:

Interrupt	Clock Domain	Trigger Signal
RPPSMVidStbChgInt	MCLK (Level)	MVidStbInt
RPPSMHSyncErrInt	MCLK (1T)	MHSyncErrInt
RPPSMHDEErrInt	MCLK (1T)	MHDEErrInt
RPPSMVSyncErrInt	MCLK (1T)	MVSyncErrInt
RPPSPVidStbChgInt	PCLK (Level)	PVidStbInt
RPPSPHSyncErrInt	PCLK (1T)	PHSyncErrInt
RPPSPHDEErrInt	PCLK (1T)	PHDEErrInt
~~RPPSPVSyncErrInt~~	~~PCLK (1T)~~	~~PVSyncErrInt~~
RPPSVDEErrInt	MCLK (1T)	MVDEErrInt
RPPSRxPSRChgInt	PCLK (Level)	PRxPSR
RPPSDByteErrInt	MCLK (1T)	MDByteErrInt
RFFCWRDiffInt	BCLK (1T)	BFFCWRDiff
RUFODecNumDiffInt	BCLK(1T)	BUFODecNumDiff
RFFAWRDiffInt	PCLK (1T)	PFFAWRDiff
RUFOBufCFlwInt	BCLK(Level)	BUFOBufCFlw
RUFOBufAFlwInt	PCLK(Level)	PUFOBufAFlw
RUFOBufBFlwInt	PCLK(Level)	PUFOBufBFlw
RECC1bErrInt	MCLK (1T)	MECC1bErr
RECC2bErrInt	MCLK (1T)	MECC2bErr
RLMFIFOErrInt	MCLK (Level)	MLMFIFOErr
RCRCErrInt	MCLK (1T)	MCRCErr
RMCLKOffInt	RCLK (Level)	RMCLKOffSts
RPPIFifoOvWrInt	MCLK (Level)	MLxFifoOvWr
RTimerInt	RCLK (1T)	RTimerTrg