IT6151

MIPI to eDP Converter

Specification V1.00b

ITE TECH. INC.

General Description

The IT6151 is a high-performance and low-power MIPI to eDP converter, fully compliant with MIPI D-PHY 1.1, DSI 1.1 and eDP 1.3 specifications. The IT6151 supports four lanes MIPI RX and four lane eDP TX interface. The data transfer rate of MIPI RX is up to 1Gbps per lane and both RBR/HBR are supported by eDP TX interface.

To reduce the power consumption, Panel Self Refresh (PSR) function is supported by the IT6151. Various low power options are implemented to reduce the dynamic operation power when PSR function is enabled. Dedicated hardware pin or firmware control through I2C can easy set the IT6151 to standby mode which is the extremely low-power state used for no display condition. With flexible MIPI RX and eDP TX lane configurations, system can adopt the most adequate configuration for the selected display resolution. All the unused lanes can be set to power down mode to save further power.

The IT6151 provides a user-friendly firmware interface to control the eDP panel through MCCS. The DPCD registers can also be easily accessed by native AUX read/write commands. To assure the protected content is being sent to eDP panel other than a non-HDCP external DP sink, Alternative Scrambler Seed Reset (ASSR) and Alternative Framing are also supported by the IT6151. With 6x6mm small package and low power consumption, the IT6151 is suitable for mobile products nowadays.

Features

- 4-lane MIPI RX with total 4Gbps bandwidth
- 4-lane eDP TX with two link speeds, HBR(2.7Gbps) and RBR(1.62Gbps)
- Compliant with MIPI D-PHY 1.1 and DSI 1.1 specifications
- Compliant with eDP 1.3 specification
- Supporting the following 24-bit RGB 4:4:4 video formats:
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i up to 1080p
  - PC resolutions: VGA, SVGA, XGA, SXGA up to 1600x1200@60Hz, 2048x1536@60Hz
- Various Packed Pixel Stream of DSI are supported, such as:
  - 18/24/30/36-bit RGB 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 18-bit RGB 4:4:4 (Lossely)
- Mediatek Proprietary Display Stream Decompression Engine
- Compatible with Mediatek Application Processors (AP) to support up to 2048x1536@60Hz Panels

- Flexible lane swap and P/N swap configuration
- Software programmable eDP output swing and pre-emphasis level
- Embedded full-function pattern generator
- Support ASSR and Alternative Framing for content protection
- MCCS over AUX channel
- Intelligent, programmable power management
- 48-pin (6x6 mm) QFN package

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6151FN	-20~70	48-pin QFN	Green

Pin Diagram

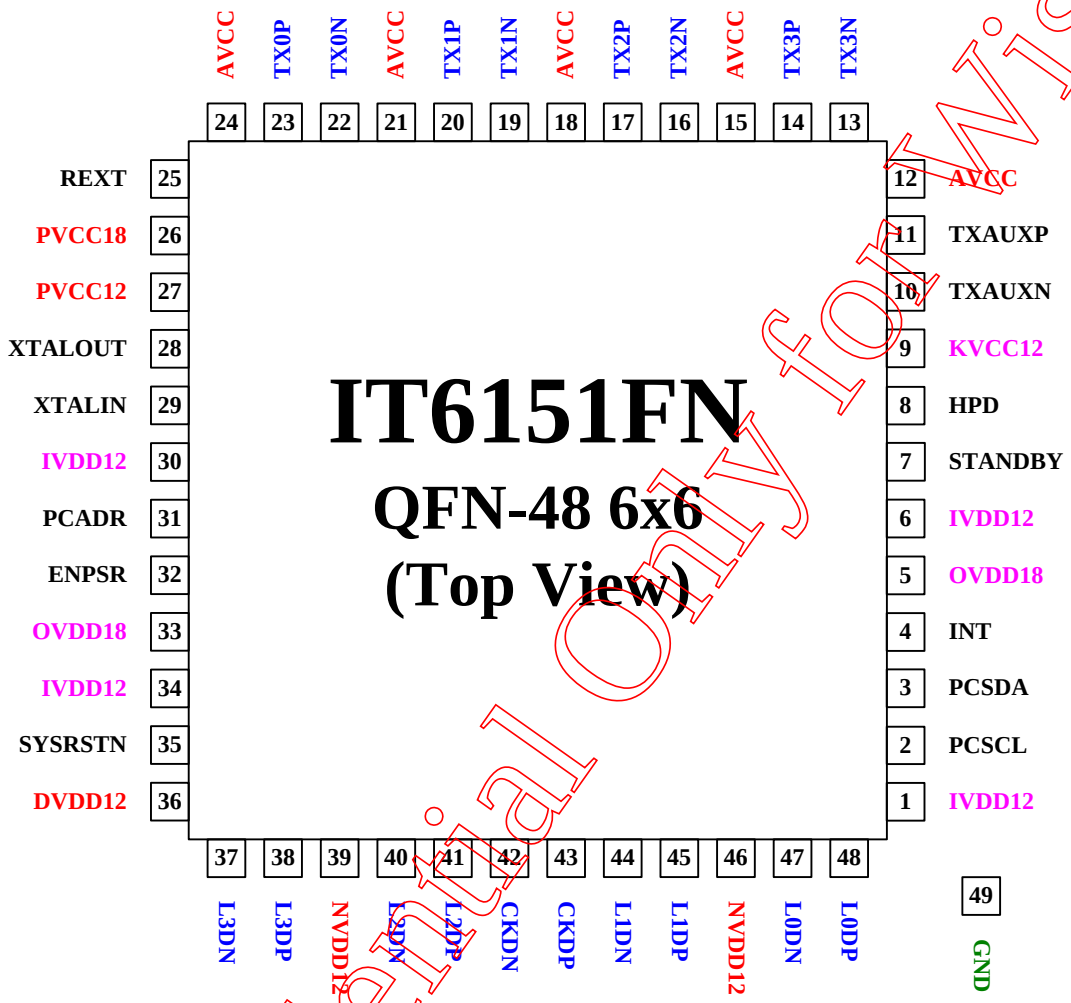


Figure 1. IT6151 pin diagram

Pin Description

MIPI RX Input Pins

Pin Name	Direction	Description	Type	Pin No.
L0DP	Analog	MIPI RX lane 0 positive signal	MIPI	48
L0DN	Analog	MIPI RX lane 0 negative signal	MIPI	47
L1DP	Analog	MIPI RX lane 1 positive signal	MIPI	45
L1DN	Analog	MIPI RX lane 1 negative signal	MIPI	44
CKDP	Analog	MIPI RX clock lane positive signal	MIPI	43
CKDN	Analog	MIPI RX clock lane negative signal	MIPI	42
L2DP	Analog	MIPI RX lane 2 positive signal	MIPI	41
L2DN	Analog	MIPI RX lane 2 negative signal	MIPI	40
L3DP	Analog	MIPI RX lane 3 positive signal	MIPI	38
L3DN	Analog	MIPI RX lane 3 negative signal	MIPI	37

eDP TX interface pins

Pin Name	Direction	Description	Type	Pin No.
TX0P	Analog	eDP TX lane 0 positive signal	DP	23
TX0N	Analog	eDP TX lane 0 negative output	DP	22
TX1P	Analog	eDP TX lane 1 positive signal	DP	20
TX1N	Analog	eDP TX lane 1 negative output	DP	19
TX2P	Analog	eDP TX lane 2 positive signal	DP	17
TX2N	Analog	eDP TX lane 2 negative output	DP	16
TX3P	Analog	eDP TX lane 3 positive signal	DP	14
TX3N	Analog	eDP TX lane 3 negative output	DP	13
TXAUXP	Analog	eDP TX AUX channel positive signal	DP	11
TXAUXN	Analog	eDP TX AUX channel negative output	DP	10
XTALIN	Analog	eDP AFE crystal input (27MHz)	Analog	29
XTALOUT	Analog	eDP AFE crystal output (27MHz)	Analog	28
REXT	Analog	External resistor for setting eDP output level. Default tied to GND via a 4.7K-Ohm SMD resistor.	Analog	25

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
PCSCL	Input	Serial Programming Clock for chip programming	Schmitt	2
PCSDA	I/O	Serial Programming Data for chip programming	Schmitt	3
INT	Output	Interrupt output. Default active-low	LVTTL	4

System Control Pins

Pin Name	Direction	Description	Type	Pin No.
SYSRSTN	Input	Hardware reset pin. Active LOW	Schmitt	35
PCADR	Input	Serial programming device address select	LVTTL	31
ENPSR	Input	External PSR function control signal	LVTTL	32
STANDBY	Input	External standby function control signal	LVTTL	7
HPD	Input	eDP Hot Plug Detection signal	LVTTL	8

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD12	Core logic supply power (1.2V)	Power	1, 6, 30, 34
OVDD18	I/O pin supply power (1.8V)	Power	5, 33
PVCC12	eDP core PLL power (1.2V)	Power	27
PVCC18	eDP core PLL power (1.8V)	Power	26
KVCC12	eDP digital frontend power (1.2V)	Power	9
AVCC	eDP analog frontend power (1.2V)	Power	12, 15, 18, 21, 24
DVDD12	MIPI digital frontend power (1.2V)	Power	36
NVDD12	MIPI analog frontend power (1.2V)	Power	39, 46
GND	Exposed ground pad	Ground	49

Functional Description

IT6151 is a MIPI RX to eDP TX converter and provides complete solutions for Mobile Industrial Processor systems to output video content to eDP panel. In addition, advanced low power function, Panel Self Refresh (PSR), is implemented to optimize the dynamic operation power, especially for still image. The following picture is the functional block diagram of IT6151, which describes clearly the data flow.

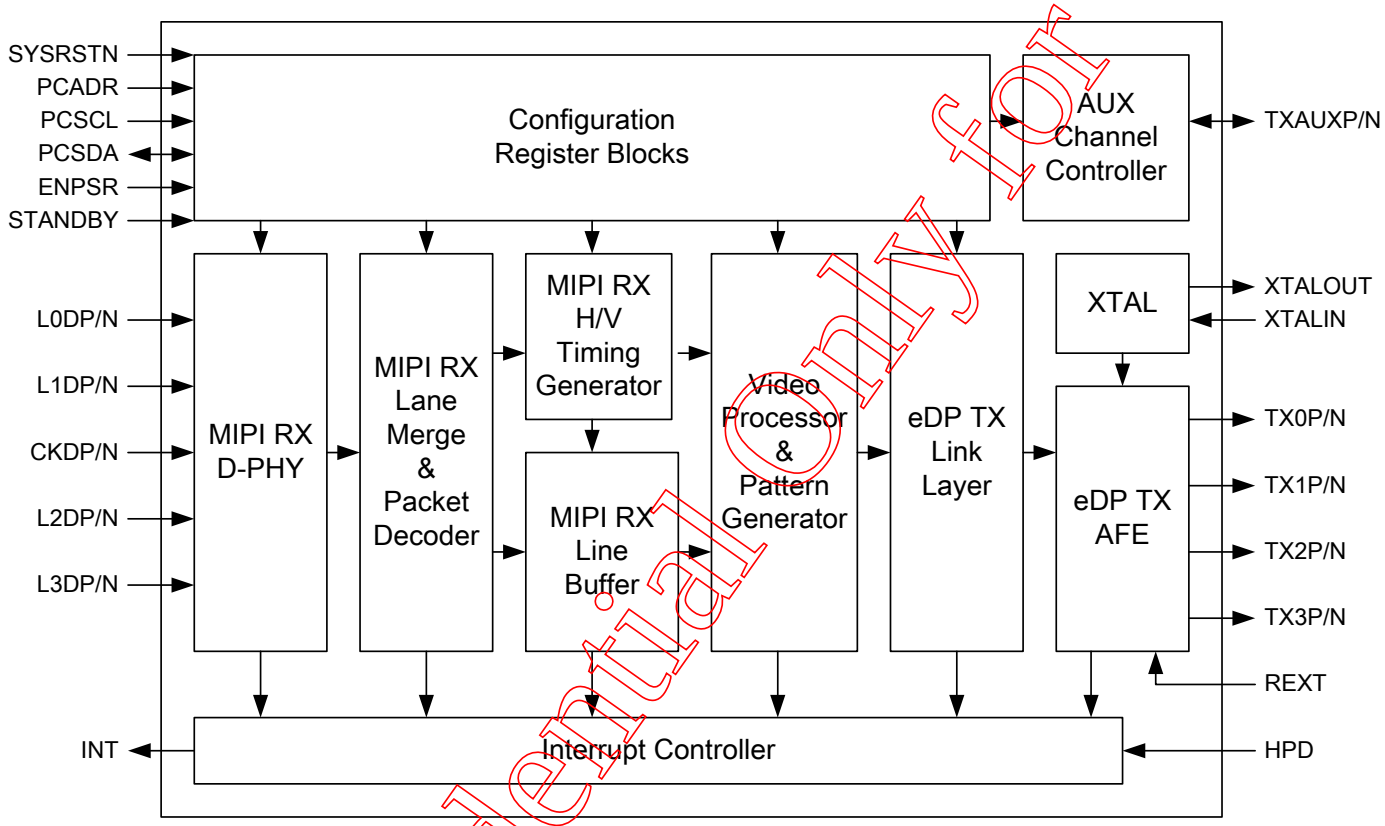


Figure 2. Functional block diagram of IT151

◆ MIPI RX D-PHY

MIPI RX D-PHY implements four unidirectional data lanes and one clock lane. The operating mode of data lane could be Control or High-Speed mode. However, the clock lane can only support continuous clock because the pixel clock for eDP is generated from this differential DDR clock. An internal PLL is used to generate the eDP pixel clock. Please refer to the IT6151 Programming Guide for the PLL setting.

◆ MIPI RX Lane Merge and Packet Decoder

Base on the video bandwidth, MIPI RX D-PHY can be configured as 1/2/3/4-lane and Lane Merge

function combines input data to a uniform 32-bit internal bus for further processing. Packet Decoder is used to check the ECC and CRC error. One-bit error in the Packet Header can be automatically corrected by the ECC function.

◆ MIPI RX H/V Timing Generator

The H/V Timing Generator uses Sync Event to generate video HSync and VSync timing. Both Sync Pulse and Sync Event mode are supported by the IT6151. The generated video timing parameters can be over-written by firmware if necessary.

◆ MIPI RX Line Buffer

The active video data of DSI protocol can be transmitted in Non-Burst or Burst mode. The IT6151 supports both modes and Line Buffer is used to hold the burst video data. With this Line Buffer, a constant data throughput can be maintained for eDP TX.

◆ Video Processor and Pattern Generator

The Video Processor uses the input H/V timing to control the video data output from Line Buffer. A Pattern Generator is embedded in the IT6151 and thus the video data and timing can be easily switched from external MIPI RX to internal pattern generator for testing.

◆ eDP TX Link Layer

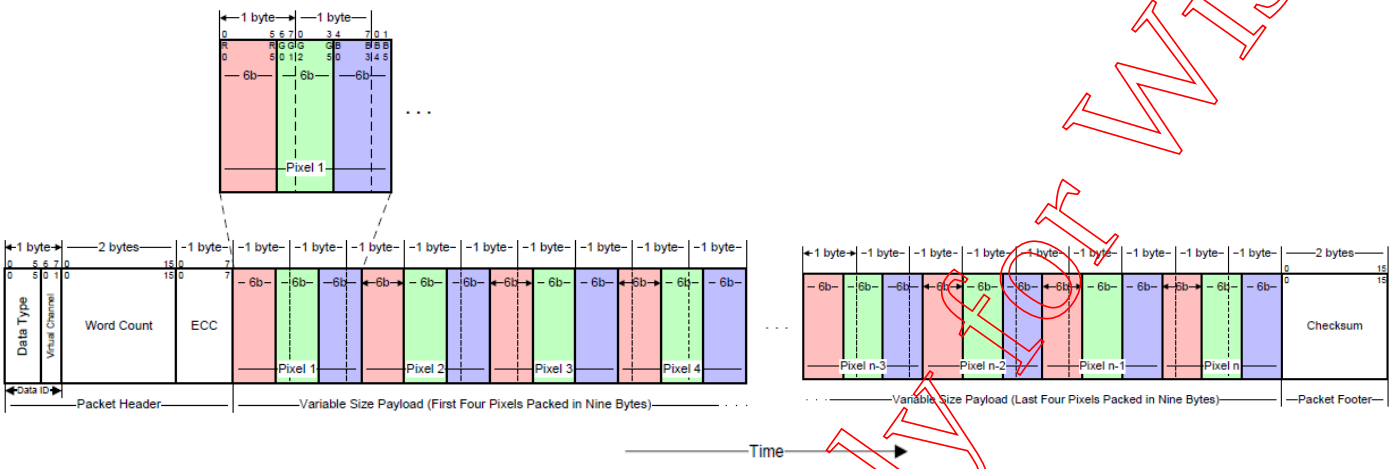
The eDP TX Link Layer receives input video data and timing to construct 10-bit symbols for transmission. The bandwidth of eDP TX is varied depends on the setting of Lane number and bit rate. The IT6151 supports 1/2/4-lane configuration and two bit rates: 2.7Gbps and 1.62Gbps per lane. User can choose the most suitable setting to reduce the power consumption. The necessary Secondary Data Packet is inserted to symbol stream by Link Layer. Please refer to IT6151 Programming Guide for detail setting.

◆ eDP TX AFE

The final step of the data processing flow is eDP TX AFE. The eDP TX driver serializes the input parallel data and drive out the proper electrical signals to the eDP panel. The output current level is controlled through connecting a precision resistor of proper value to Pin 25 (REXT).

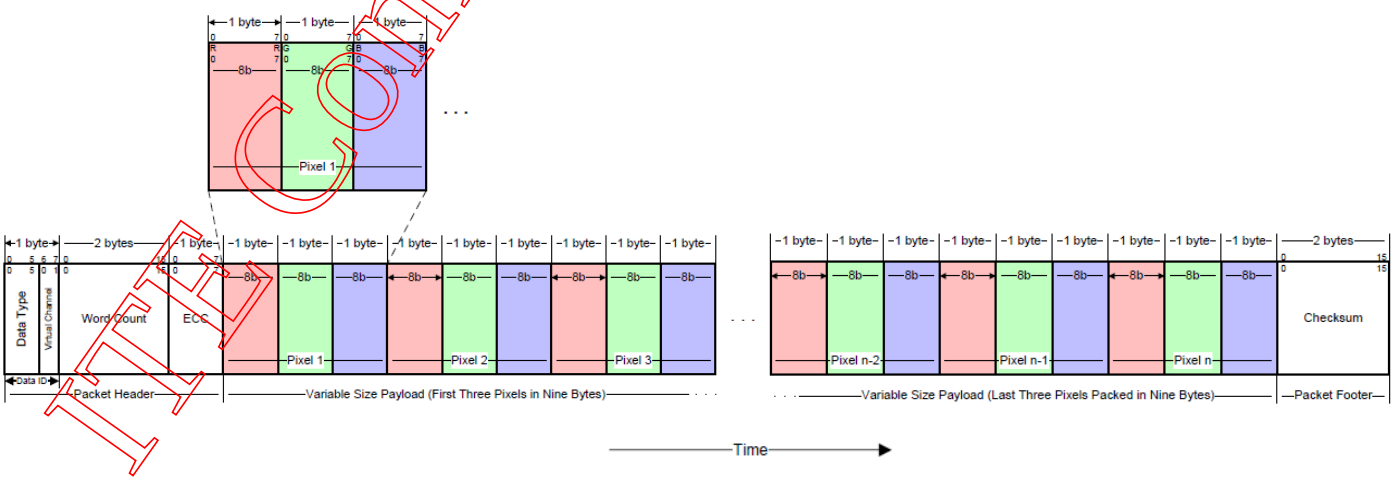
Supported Packed Pixel Steam

- 18-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x1E

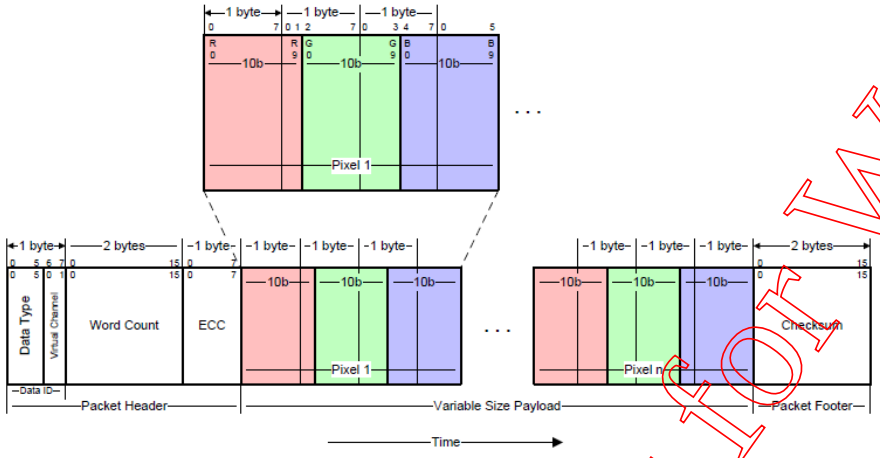


- 18-bit per Pixel (Loosely) - RGB 4:4:4, Long Packet , Data Type 0x2E

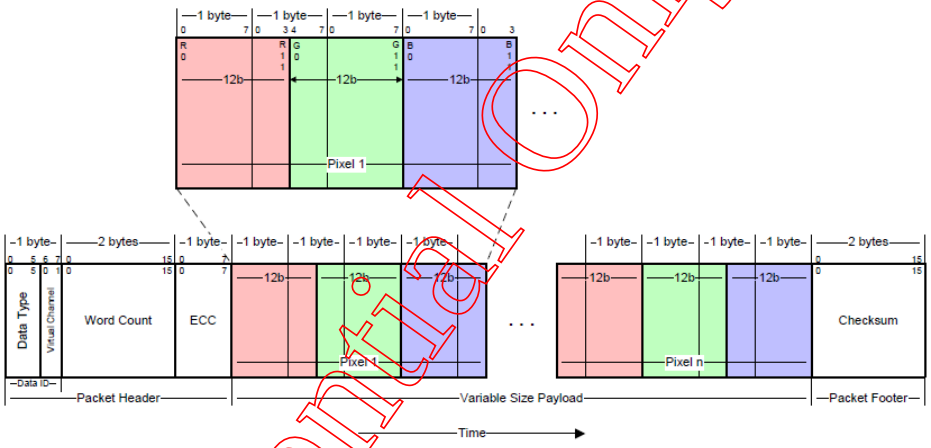
- 24-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x3E



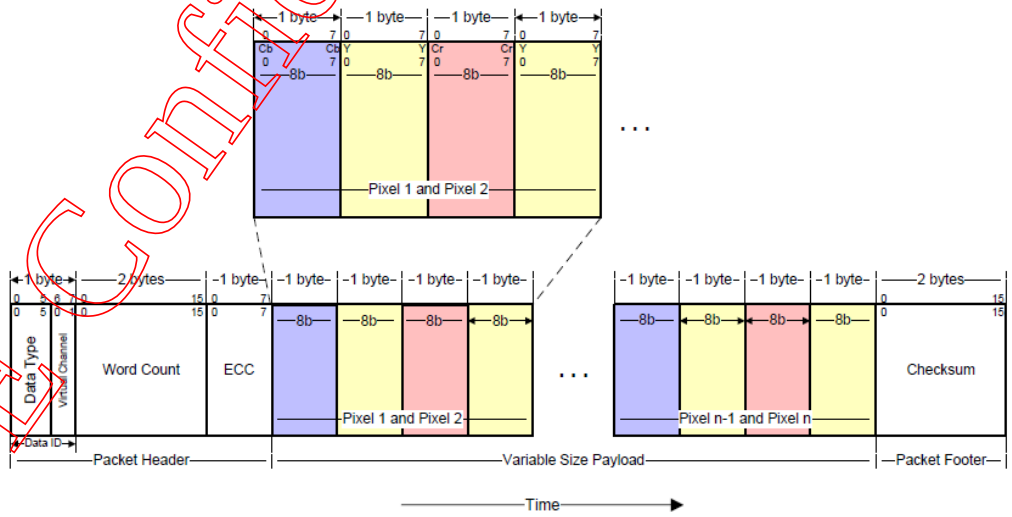
◆ 30-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x0D



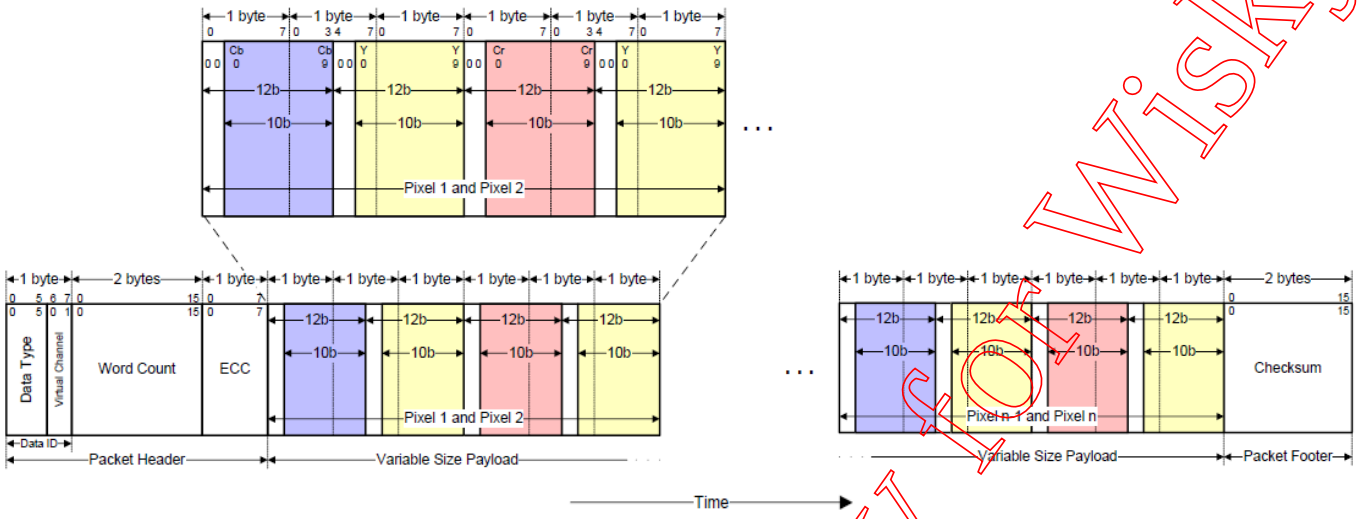
◆ 36-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x1D



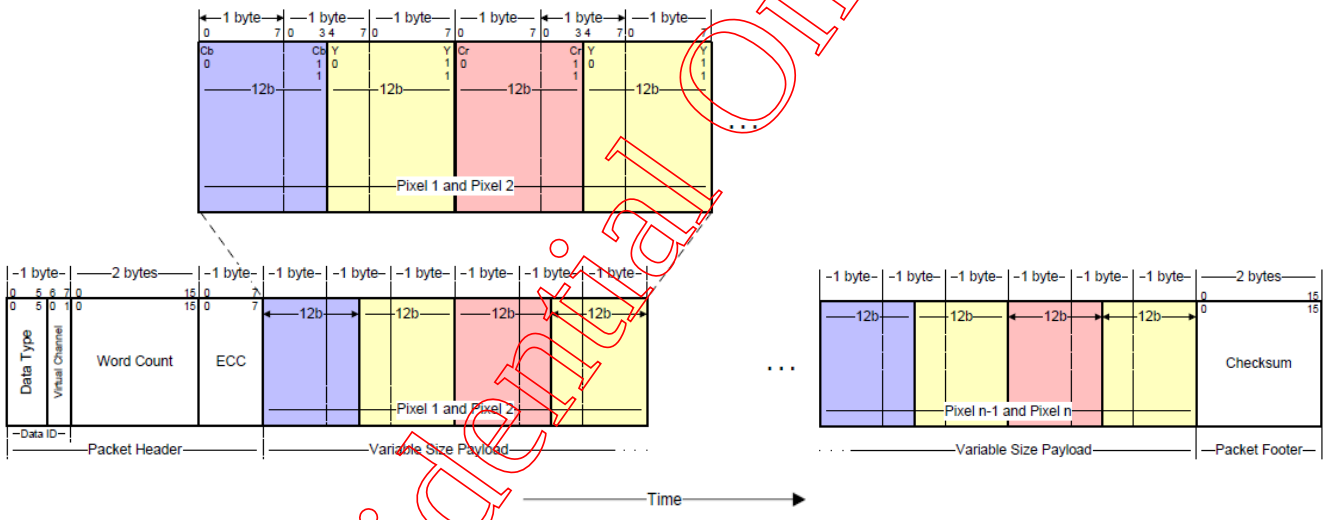
◆ 16-bit per Pixel (Packed) - YCbCr 4:2:2, Long Packet , Data Type 0x2C



◆ 20-bit per Pixel (Packed) - YCbCr 4:2:2, Long Packet , Data Type 0x0C



◆ 24-bit per Pixel (Packed) - YCbCr 4:2:2, Long Packet , Data Type 0x1C



Configuration and Function Control

The IT6151 includes one serial programming port by default for interfacing with micro-controller. This port is a slave interface, comprising PCSCL (Pin 2) and PCSDA (Pin 3). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 31). If PCADR is pulled high by the user, the eDP TX slave address is **0xBA**. If pulled low, **0xB8**. The slave address of MIPI RX is programmable and enabled by firmware. Please refer to IT6151 Programming Guide for detail.

The IT6151 allows the user to access eDP AUX channel through serial programming port. It can be used for accessing EDID or DPCD data on Sink side. For temporarily storing the acquired EDID data, the IT6151 embedded a dedicated FIFO of 16 bytes. The micro-controller may command the IT6151 to acquire 16 bytes of EDID information at a time, read them back and then continue to read the next 16 bytes until all necessary EDID information are retrieved.

The serial programming interface conforms to standard I^2C transactions and operates at up to 100kHz.

Interrupt Generation

The system micro-controller should monitor the interrupt output by the IT6151 at PIN 4 (INT). The IT6151 generates an interrupt signal with events involving various situations. This interrupt pin can be configured as push-pull or open-drain I/O with active high or active low. If the system do not use INT pin, polling interrupt status is another option. Firmware must be implemented to setup initial value of registers and handle interrupt events, otherwise the link establishment might fail. Please do follow the suggested initialization flow recommended in IT6151 Programming Guide.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Min.	Typ	Max	Unit
IVDD12	Core logic supply voltage	-0.5		1.5	V
OVDD18	I/O pin supply voltage	-0.3		2.5	V
PVCC12	eDP core PLL voltage	-0.5		1.5	V
PVCC18	eDP core PLL voltage	-0.3		2.5	V
KVCC12	eDP digital frontend voltage	-0.5		1.5	V
AVCC	eDP analog frontend voltage	-0.5		1.5	V
DVDD12	MIPI digital frontend voltage	-0.5		1.5	V
NVDD12	MIPI analog frontend voltage	-0.5		1.5	V
V_I	Input voltage	-0.3		OVDD18 +0.3	V
V_O	Output voltage	-0.3		OVDD18 +0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Description	Min.	Typ	Max	Unit
IVDD12	Core logic supply voltage	1.14	1.2	1.26	V
OVDD18	I/O pin supply voltage	1.62	1.8	1.98	V
PVCC12	eDP core PLL voltage	1.14	1.2	1.26	V
PVCC18	eDP core PLL voltage	1.62	1.8	1.98	V
KVCC12	eDP digital frontend voltage	1.14	1.2	1.26	V
AVCC	eDP analog frontend voltage	1.14	1.2	1.26	V
DVDD12	MIPI digital frontend voltage	1.14	1.2	1.26	V
NVDD12	MIPI analog frontend voltage	1.14	1.2	1.26	V
DVDD12	MHL AFE digital supply voltage	1.14	1.2	1.26	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	-20	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance			40	°C/W

Notes:
1. AVCC, NVDD12, PVCC12 and PVCC18 should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Min	Typ	Max	
V_{IH}	Input low voltage[1]	LVTTL			0.6	V
V_{IL}	Input high voltage[1]	LVTTL	1.2			V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt	0.63	0.75		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt		1.05	1.14	V
V_{OL}	Output low voltage[1]	LVTTL			0.4	V
V_{OH}	Output high voltage[1]	LVTTL	1.4			V
I_{IN}	Input leakage current[1]	all	-10		+10	µA
I_{OZ}	Tri-state output leakage current[1]	all	-10		+10	µA
I_{OL}	Serial programming output sink current[2]	Schmitt	1.25		5	mA
V_{CMRX}	Common-mode voltage HS receive mode[3]	MIPI RX	70		330	mV
V_{IDTH}	HS Differential input high threshold[3]	MIPI RX			70	mV
V_{IDTL}	HS Differential input low threshold[3]	MIPI RX	-70			mV
V_{IHHS}	HS Single-ended input high voltage[3]	MIPI RX			460	mV
V_{IHLS}	HS Single-ended input low voltage[3]	MIPI RX	-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable[3]	MIPI RX			450	mV
$V_{IH(LP)}$	LP logic high input voltage[3]	MIPI RX	880			mV
$V_{IL(LP)}$	LP logic low input voltage[3]	MIPI RX			550	mV
$V_{TX-DIFFp-p-Level1}$	Differential Peak-to-peak Output Voltage Level 1 [4]	eDP TX	340	400	460	mV
$V_{TX-DIFFp-p-Level2}$	Differential Peak-to-peak Output Voltage Level 2 [4]	eDP TX	510	600	680	mV
$V_{TX-DIFFp-p-Level3}$	Differential Peak-to-peak Output Voltage Level 3 [4]	eDP TX	690	800	920	mV

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.4V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6151 Programming Guide for proper register setting.
3. Refer to D-PHY 1.1 specification
4. Refer to DisplayPort V1.1a specification.

Operation Supply Current Specification

- **Normal Operation Mode**

RGB444 ColorBar		DP HBR 4-Lane			DP HBR 2-Lane			DP HBR 1-Lane		
	MPRX	1.2V (mA)	1.8V (mA)	PWR (mW)	1.2V (mA)	1.8V (mA)	PWR (mW)	1.2V (mA)	1.8V (mA)	PWR (mW)
720x480P60Hz (PCLK=27MHz)	1-Lane	124.01	4.37	156.68	91.61	4.37	117.79	76.21	4.37	99.30
	2-Lane	123.58	4.37	156.16	91.20	4.37	117.29	75.81	4.37	98.82
	4-Lane	127.70	4.37	161.10	95.32	4.37	122.25	79.89	4.37	103.73
	UFO	128.46	4.37	162.01	96.07	4.37	123.15	80.64	4.37	104.63
1024x768P60Hz (PCLK=65MHz)	1-Lane									
	2-Lane	136.99	4.37	172.24	104.60	4.37	133.38	89.28	4.37	114.99
	4-Lane	138.30	4.37	173.81	105.92	4.37	134.96	90.58	4.37	116.55
	UFO	140.92	4.37	176.97	108.65	4.37	138.24	93.19	4.37	119.69
1280x720P60Hz (PCLK=74.25MHz)	1-Lane									
	2-Lane	140.42	4.37	176.36	108.00	4.37	137.46	92.62	4.37	119.00
	4-Lane	140.93	4.37	176.98	108.57	4.37	138.15	93.22	4.37	119.73
	UFO	144.08	4.37	180.75	111.70	4.37	141.90	96.31	4.37	123.43
1280x1024P60Hz (PCLK=108MHz)	1-Lane									
	2-Lane									
	4-Lane	150.51	4.37	188.48	118.12	4.37	149.60			
	UFO	155.48	4.37	194.43	123.11	4.37	155.59			
1920x1080P60Hz (PCLK=148.5MHz)	1-Lane									
	2-Lane									
	4-Lane	163.01	4.37	203.48	130.98	4.37	165.03			
	UFO	171.28	4.37	213.39	138.83	4.37	174.45			
1600x1200P60Hz (PCLK=162MHz)	1-Lane									
	2-Lane									
	4-Lane	165.42	4.37	206.36	133.01	4.37	167.47			
	UFO	173.01	4.37	215.47	140.52	4.37	176.48			
2048x1536P60Hz (PCLK=209MHz)	1-Lane									
	2-Lane									
	4-Lane									
	UFO	194.52	4.37	241.29						

RGB444 ColorBar	MPRX	DP RBR 4-Lane			DP RBR 2-Lane			DP RBR 1-Lane		
		1.2V (mA)	1.8V (mA)	PWR (mW)	1.2V (mA)	1.8V (mA)	PWR (mW)	1.2V (mA)	1.8V (mA)	PWR (mW)
720x480P60Hz (PCLK=27MHz)	1-Lane	112.65	3.22	140.99	81.36	3.22	103.43	66.31	3.22	85.37
	2-Lane	112.24	3.22	140.49	80.94	3.22	102.93	65.90	3.22	84.88
	4-Lane	116.33	3.22	145.40	85.04	3.22	107.85	70.00	3.22	89.80
	UFO	117.09	3.22	146.31	85.80	3.22	108.76	70.76	3.22	90.71
1024x768P60Hz (PCLK=65MHz)	1-Lane									
	2-Lane	125.65	3.22	156.58	94.33	3.22	119.00			
	4-Lane	126.93	3.22	158.11	95.63	3.22	120.56			
	UFO	129.59	3.22	161.31	98.27	3.22	123.72			
1280x720P60Hz (PCLK=74.25MHz)	1-Lane									
	2-Lane	129.06	3.22	160.67	97.77	3.22	123.13			
	4-Lane	129.59	3.22	161.31	98.33	3.22	123.80			
	UFO	132.76	3.22	165.11	101.48	3.22	127.57			
1280x1024P60Hz (PCLK=108MHz)	1-Lane									
	2-Lane									
	4-Lane	139.20	3.22	172.85	107.80	3.22	135.16			
	UFO	144.22	3.22	178.86	112.78	3.22	141.14			
1920x1080P60Hz (PCLK=148.5MHz)	1-Lane									
	2-Lane									
	4-Lane	152.06	3.22	188.28						
	UFO	159.96	3.22	197.75						
1600x1200P60Hz (PCLK=162MHz)	1-Lane									
	2-Lane									
	4-Lane	154.14	3.22	190.76						
	UFO	161.77	3.22	199.93						
2048x1536P60Hz (PCLK=209MHz)	1-Lane									
	2-Lane									
	4-Lane									
	UFO	183.18	3.22	225.62						

Note: 1.PWR = 1.2V current x 1.2 + 1.8V current x 1.8

2. MCLK (MIPI DDR clock divided by 4) = 3/4 x PCLK (video pixel clock)
3. eDP TX SSC is enabled
4. UFO = Display Stream Decompression.

- **Standby Mode**

1.2V (mA)	1.8V (mA)	Pwr (mW)
0.746	0.334	1.4964

Note:

1. MPTX is at LP-11 state.
2. The serial programming port is enabled. (Internal XTAL is enabled)

- **Sleep Mode**

1.2V (mA)	1.8V (mA)	Pwr (mW)
0.519	0.022	0.6624

Note:

1. MPTX is at LP-11 state.
2. The serial programming port is disabled.
3. This state can be controlled by external STANDBY pin or FW. If there is no GPIO to control this STANDBY pin, AP circuit must tie STANDBY to HIGH and enter Sleep Mode by FW. If the Sleep Mode is entered by FW, it can only be wake-up by external SYSRSTN.

System Design Consideration

As a high-performance receiver/transmitter, ITE's RX/TX is capable of receiving/transmitting those signals that are attenuated and degraded by the MIPI/eDP cables. These signals are usually very small in amplitudes in addition to the distortion that the cable inflicts on them. The analog front-end of ITE's RX/TX is designed to combat environment noises as well as interference to some degree. However, to get the optimum performance the system designers should follow the guideline below when designing the application circuits and PCB layout.

- **MIPI/eDP Differential Signal**

  The characteristic impedance of all eDP differential PCB traces (RX2p/n, RX1p/n, RX0p/n, and RXCp/n) should be kept 100Ω all the way from the eDP connector to ITE's RX/TX. The characteristic impedance of all MIPI PCB traces (MIPIp, MIPIn) should be kept 100 Ohm differential, 50 Ohm single-ended per line, and 25 Ohm common-mode for both lines together. This is very crucial to the system performance at high speeds. When routing this differential transmission lines (2 single-ended lines in total), the following guidelines should be followed:

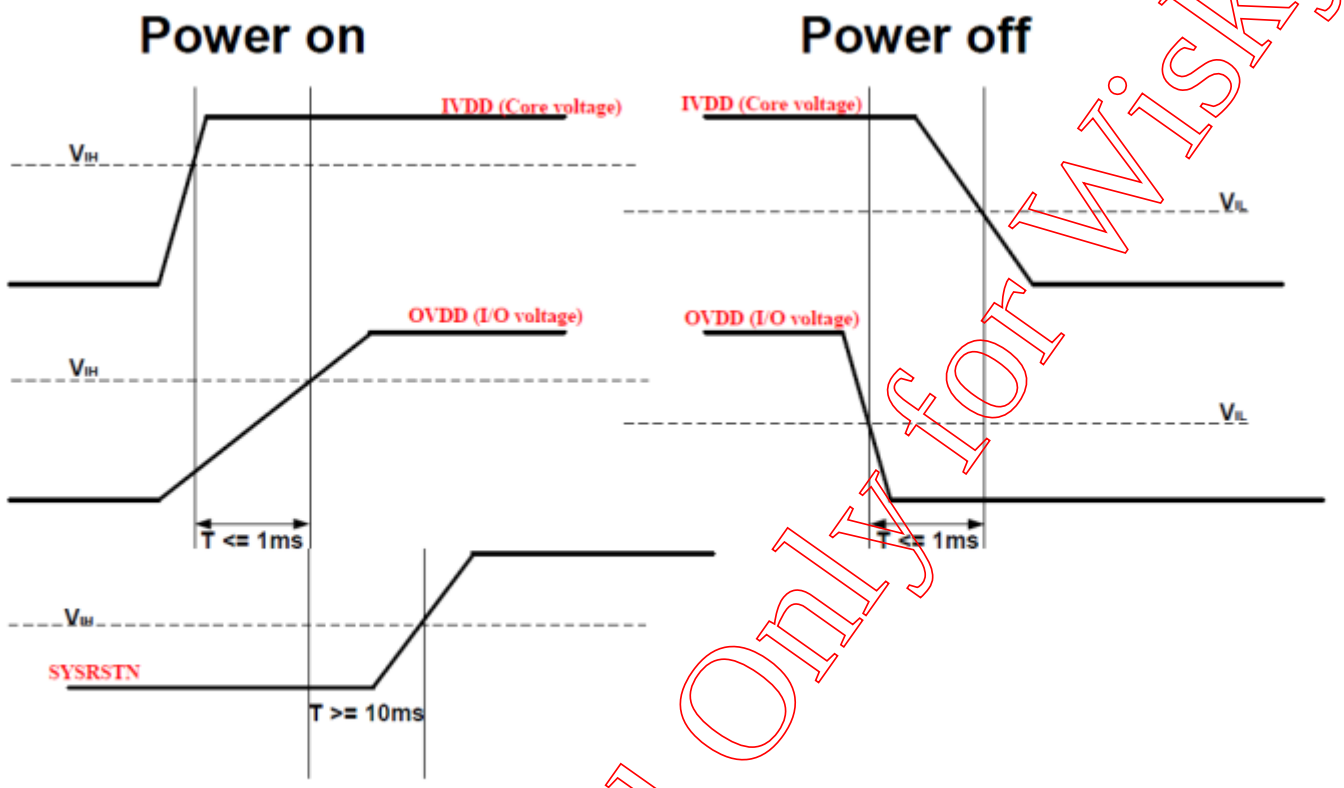
  1. The signals traces should be on the outside layers (e.g. TOP layer) while beneath it there should be a continuous ground plane in order to maintain the called micro-strip structure, giving stable and well-defined characteristic impedances.
  2. Cornering, through holes, crossing and any irregular signal routing should be avoided so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.
  3. ITE's RX/TX should be placed as close to the MIPI connector as possible. Since the differential signal pins of ITE's RX/TX perfectly match the order of the connector pins, it is very convenient to route the signal directly into the chip, without through holes or angling.
  4. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables nominal 100Ω differential, 50 Ohm single-ended per Line, and 25 Ohm common-mode impedance. Please contact us directly for technical support of this issue.
  5. The sensitive MIPI/eDP differential signals should be taken when routing. To reduce the differential unbalanced effect, it is recommended to separate at least 3 **times** the dielectric thickness between the signal layer and the reference layer to any other adjacent signal or GND plane to reduce noise inference and jitter. (or 25 mils is enough space in almost PCB stack)
  6. The MIPI/eDP IC should be located as close as possible to the output/input connector, thus minimizing noise pickup and reflections due to impedance mismatch. It is recommended that the distance between the chip and connector is less than 5 CM.

- **ESD Consideration**

  Special care should be taken when adding discrete ESD devices to all differential PCB traces (MIPIp/eDPp, MIPIn/eDPn) . ITE's RX/TX is designed to provide ESD protection for up to 4KV at these differential pins. Adding discrete ESD diodes could enhance the ESD capability, but at the same time will inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout would prevent the system from passing the SINK differential Impedance test in the MIPI/eDP Compliance Test. Besides, most general-purpose ESD diodes are relatively large in size, forcing the high-speed differential lines to corner several times and therefore introducing severe reflection. Carefully choosing an ESD diode that's designed for MIPI/eDP signaling could lead to a minimum loading as well as an optimized layout. Commercially available devices such as Semtech's RClamp0524P, RClamp0522P or CitrusCom's CS0806S that take into consideration of all aspects are recommended. (*http://www.semtech.com/products/product or http://www.citruscomsemi.com.*) A layout example is shown in Fig. 1, with referenced FR4 PCB structure included. Note that the ESD diodes should be placed as close to the MIPI/eDP connectors as possible to yield the best ESD performances.

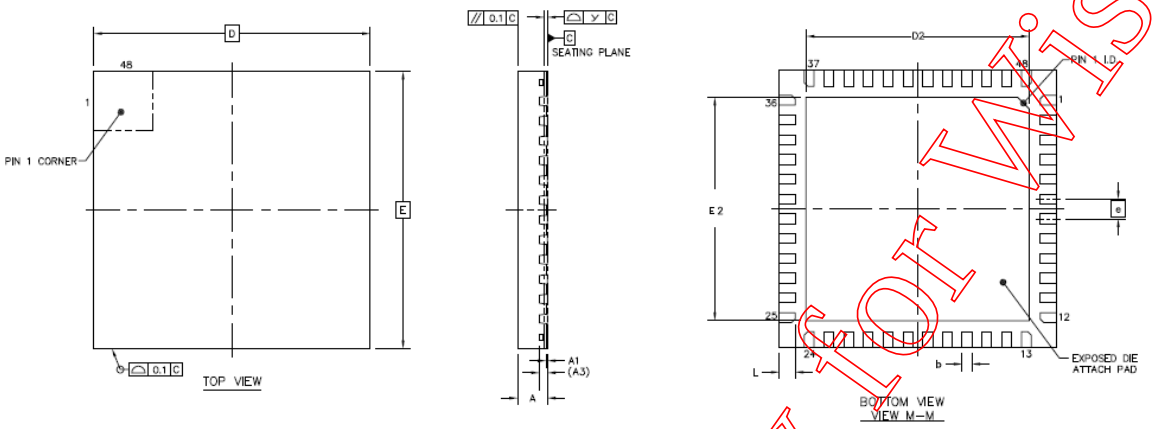
Notes: The PCB stack and material will affect differential impedance. The customer shall co-work with PCB provider to obtain the real 100 ohm differential, 50 Ohm single-ended per Line, and 25 Ohm common-mode impedance based on actual PCB stack and material.

Power Sequence



When power on, please keep IVDD go VIH before OVDD go VIH (IVDD must supply earlier than or equal to OVDD).
And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.028	0.030	0.032	0.7	0.75	0.8
A1	0	---	0.002	0	---	0.05
A3	0.008 REF			0.203 REF		
b	0.006	0.008	0.01	0.15	0.20	0.25
D	0.236 BSC			6 BSC		
D2	0.165	0.173	0.179	4.20	---	4.55
E	0.236 BSC			6 BSC		
E2	0.165	0.173	0.179	4.20	---	4.55
e	0.016			0.4 BSC		
L	0.014	---	0.020	0.35	---	0.50
y	---	---	0.003	--	--	0.08

Notes:
1. Controlling dimension：Millimeter
2. Reference document：JEDEC MO-220
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

Figure 3. 48-pin QFN Package Dimensions

Top Marking Information