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  alu.c
  - 21.11.05/BHO1
  bho1 29.12.2006
  bho1 6.12.2007
  bho1 30.11.2007 - clean up
  bhol 24.11.2009 - assembler instruction
  bhol 3.12.2009 - replaced adder with full adder
  bhol 20.7.2011 - rewrite: minimize global vars, ALU-operations are modeled wi
th fct taking in/out register as parameter
  bhol 6.11.2011 - rewrite flags: adding flags as functional parameter. Now alu
is truly a function
  bhol 26.11.2012 - remove bit declaration from op_alu_asl and op_alu_ror as th
ey are unused (this may change later)
  bho1 20.9.2014 cleaned
  GPL applies
  -->> Marco Schmid <<--
#include <stdio.h>
#include <string.h>
#include "alu.h"
#include "alu-opcodes.h"
#include "register.h"
#include "flags.h"
int const max_mue_memory = 100;
char mue_memory[100] = "100 Byte - this memory is at your disposal"; /*mue-memory
char* m = mue memory;
unsigned int c = 0;
                        /* carry bit address
unsigned int s = 1;
                        /* sum bit address
unsigned int c in = 2; /* carry in bit address */
void alu reset()
   int i;
   for(i=0;i<max_mue_memory;i++)</pre>
        m[i] = '0';
  testet ob alle bits im akkumulator auf null gesetzt sind.
  Falls ja wird 1 returniert, ansonsten 0
int zero_test(char accumulator[])
   for(i=0;accumulator[i] \neq'\0'; i++)
        if(accumulator[i]≠'0')
            return 0;
   return 1;
void zsflagging(char* flags,char *acc)
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    //Zeroflag
    if(zero test(acc))
        setZeroflag(flags);
        clearZeroflag(flags);
    //Signflag
    if(acc[0] \equiv '1')
        setSignflag(flags);
        clearSignflag(flags);
Halfadder: addiert zwei character p,g und schreibt in
den Mue-memory das summen-bit und das carry-bit.
void half_adder(char p, char q)
    char result = '0';
    char carry = '0';
    if (p \equiv '0' \land q \equiv '0')
        result = '0';
        carry = '0';
    else if(p='0' \land q='1')
        result = '1';
        carry = '0';
    else if(p\equiv'1' \land q\equiv'0')
        result = '1';
        carry = '0';
    else if(p='1' \land q='1')
        result = '0';
        carry = '1';
    m[c] = carry;
    m[s] = result;
   Reset ALU
   resets registers and calls alu_op_reset
void op_alu_reset(char reqa[], char reqb[], char accumulator[], char flags[])
    int i;
    alu_reset();
    /* clear rega, regb, accumulator, flags */
    for(i=0; i<REG_WIDTH; i++)</pre>
        rega[i] = '0';
        regb[i] = '0';
        accumulator[i] = '0';
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        flags[i] = '0';
   void adder(char pbit, char gbit, char cbit)
  Adder oder auch Fulladder:
  Nimmt zwei character bits und ein carry-character-bit
  und schreibt das Resultat (summe, carry) in den Mue-speicher
void full_adder(char pbit, char qbit, char cbit)
   half_adder(pbit, qbit);
   char carrv1 = m[c];
   half adder(m[s], cbit);
   if (carry1 ≡ '1')
        m[c] = '1';
   Invertieren der Character Bits im Register reg
  one_complement(char reg[]) --> NOT(reg)
void one_complement(char reg[])
   int i = 0;
   for (i = 7; i \ge 0; i--)
        if (req[i] \equiv '1')
            reg[i] = '0';
        else
            reg[i] = '1';
  Das zweier-Komplement des Registers reg wird in reg geschrieben
req := K2(req)
void two_complement(char reg[])
   int i = 0;
   one_complement(reg);
   m[c] = '1';
    for (i = 7; i \ge 0; i--)
        if (reg[i] \equiv '0')
            reg[i] = '1';
            m[c] = '0';
            break;
        else
            reg[i] = '0';
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   Die Werte in Register rega und Register regb werden addiert, das
   Resultat wird in Register accumulator geschrieben. Die Flags cflag,
   oflag, zflag und sflag werden entsprechend gesetzt
accumulator := rega + regb
void op add(char rega[], char regb[], char accumulator[], char flags[])
    alu reset();
    clearCarryflag(flags);
    clearOverflowflag(flags);
    int i = 0;
    for (i = 7; i \ge 0; i--)
        full_adder(rega[i], regb[i], m[c]);
        accumulator[i] = m[s];
    if ((rega[0] \equiv '1' \land regb[0] \equiv '1' \land accumulator[0] \equiv '0') \lor (rega[0] \equiv '0')
\land regb[0] \equiv '0' \land accumulator[0] \equiv '1'))
        setOverflowflag(flags);
    if (m[c] \equiv '1')
        setCarryflag(flags);
    zsflagging(flags, accumulator);
/*
  ALU_OP_ADD_WITH_CARRY
   Die Werte des carry-Flags und der Register rega und
   Register regb werden addiert, das
   Resultat wird in Register accumulator geschrieben. Die Flags cflag,
   oflag, zflag und sflag werden entsprechend gesetzt
accumulator := rega + regb + carry-flag
void op_adc(char rega[], char regb[], char accumulator[], char flags[])
    char carry;
    carry = m[c];
    op_add(rega, regb, accumulator, flags);
    if (carry \equiv '1')
        char temp[8];
        char one[8] = {'0', '0', '0', '0', '0', '0', '0', '1'};
        strcpy(temp, accumulator);
        op_add(temp, one, accumulator, flags);
   Die Werte in Register rega und Register regb werden subtrahiert, das
   Resultat wird in Register accumulator geschrieben. Die Flags cflag,
   oflag, zflag und sflag werden entsprechend gesetzt
accumulator := rega - regb = rega + NOT(regb) + 1
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void op_sub(char rega[], char regb[], char accumulator[], char flags[])
    char temp[8];
    int i = 0;
    for (i = 0; i < 8; i++)
        temp[i] = reqb[i];
    two complement(reqb);
    char carry = m[c];
   op_add(rega, regb, accumulator, flags);
    for (i = 0; i < 8; i++)
        regb[i] = temp[i];
    // Overflow for subtraction : 0 && 1 && 1 or 1 && 0 && 0
    if ((rega[0] \equiv '0' \land regb[0] \equiv '1' \land accumulator[0] \equiv '1') \lor
            (rega[0] \equiv '1' \land regb[0] \equiv '0' \land accumulator[0] \equiv '0'))
        setOverflowflag(flags);
    else
        clearOverflowflag(flags);
   if (carry \equiv '1')
        setCarryflag(flags);
   subtract with carry
   accumulator =
  a - b - !c =
  a - b - !c + 256 =
  a - b - (1-c) + 256 =
  a + (255 - b) + c =
  a + !b + c
accumulator := rega - regb = rega + NOT(regb) +carryflag
void op_alu_sbc(char rega[], char regb[], char accumulator[], char flags[])
    char carry = m[c];
   op_sub(rega, regb, accumulator, flags);
    if (carry \equiv '1')
        char temp[8];
        char one[8] = {'0', '0', '0', '0', '0', '0', '1'};
        strcpy(temp, accumulator);
        op_add(temp, one, accumulator, flags);
  Die Werte in Register rega und Register regb werden logisch geANDet,
  das Resultat wird in Register accumulator geschrieben.
  Die Flags zflag und sflag werden entsprechend gesetzt
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accumulator := rega AND regb
void op and(char rega[], char regb[], char accumulator[], char flags[])
    int i = 0;
    for (i = 0; i < 8; i++)
        if (rega[i] \equiv '1' \land regb[i] \equiv '1')
            accumulator[i] = '1';
        else
            accumulator[i] = '0';
    zsflagging(flags, accumulator);
  Die Werte in Register rega und Register regb werden logisch geORt,
   das Resultat wird in Register accumulator geschrieben.
   Die Flags zflag und sflag werden entsprechend gesetzt
accumulator := rega OR regb
void op_or(char rega[], char regb[], char accumulator[], char flags[])
    int i = 0;
    for (i = 0; i < 8; i++)
        if (rega[i] \equiv '1' \lor regb[i] \equiv '1')
            accumulator[i] = '1';
        else
            accumulator[i] = '0';
    zsflagging(flags, accumulator);
   Die Werte in Register rega und Register regb werden logisch geXORt,
   das Resultat wird in Register accumulator geschrieben.
  Die Flags zflag und sflag werden entsprechend gesetzt
accumulator := rega XOR regb
void op_xor(char rega[], char regb[], char accumulator[], char flags[])
    int i = 0;
    for (i = 0; i < 8; i++)
        if ((rega[i] \equiv '1' \land regb[i] \equiv '0') \lor (rega[i] \equiv '0' \land regb[i] \equiv '1'))
            accumulator[i] = '1';
        else
            accumulator[i] = '0';
    zsflagging(flags, accumulator);
   Einer-Komplement von Register rega
rega := not(rega)
void op_not_a(char rega[], char regb[], char accumulator[], char flags[])
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   one_complement(rega);
/* Einer Komplement von Register regb */
void op_not_b(char rega[], char regb[], char accumulator[], char flags[])
   one complement(reqb);
  Negation von Register rega
rega := -rega
void op_neq_a(char rega[], char regb[], char accumulator[], char flags[])
   two complement(rega);
  Negation von Register regb
regb := -regb
void op_neq_b(char rega[], char regb[], char accumulator[], char flags[])
   two complement(regb);
  bit ->
  carryflag <-- |
  +---+---+---
  arithmetic shift left
  asl
void op_alu_asl(char regina[], char reginb[], char regouta[], char flags[])
   int i = 0;
   if (regina[0] \equiv '1')
       setCarryflag(flags);
       clearCarryflag(flags);
   for (i = 7; i \ge 0; i--)
       int dest = i-1;
       if (dest \ge 0)
           regouta[dest] = regina[i];
   regouta[7] = '0';
  logical shift right
void op_alu_lsr(char regina[], char reginb[], char regouta[], char flags[])
   int i = 0;
   for (i = 0; i < 8; i++)
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        int dest = i+1;
        if (dest < 8)
            regouta[dest] = regina[i];
    if (getCarryflag(flags) = '1')
        regouta[0] = '1';
    else
        regouta[0] = '0';
/*
   rotate
  rotate left
void op alu rol(char regina[], char reginb[], char regouta[], char flags[])
    char temp = getCarryflag(flags);
    op alu asl(regina, reginb, regouta, flags);
    regouta[7] = temp;
/*
   rotate
  rotate left
  Move each of the bits in A one place to the right. Bit 7 is filled with the
current value of the carry flag whilst the old bit 0 becomes the new carry flag
void op_alu_ror(char regina[], char reginb[], char regouta[], char flags[])
    char temp = regina[7];
    op_alu_asl(regina, reginb, regouta, flags);
    regouta[7] = temp;
    if (temp \equiv '1')
        setCarrvflag(flags);
        clearCarryflag(flags);
/*
   Procedural approach to ALU with side-effect:
   Needed register are already alocated and may be modified
   mainly a switchboard
   alu_fct(int opcode, char reg_in_a[], char reg_in_b[], char reg_out_accu[], ch
ar flags[])
void alu(unsigned int alu_opcode, char reg_in_a[], char reg_in_b[], char reg_out
_accu[], char flags[])
    char dummyflags[9] = "000000000";
    switch ( alu_opcode ){
        case ALU OP ADD :
            op_add(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags:fla
gs);
            break;
        case ALU_OP_ADD_WITH_CARRY :
            op_adc(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:fla
gs);
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	break;
	<pre>case ALU_OP_SUB : op_sub(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:fla</pre>
gs);	op_sub(leg_in_a, leg_in_b, leg_out_accu, (liags=Nobb):uummyliags:ila
	<pre>break; case ALU_OP_SUB_WITH_CARRY :</pre>
	op_alu_sbc(req_in_a, req_in_b, req_out_accu, (flags≡NULL)?dummyflags
:flags)	
	break; case ALU_OP_AND:
,	op_and(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags:fla
gs);	break;
	case ALU_OP_OR:
s);	op_or(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:flag
5)/	break;
	case ALU_OP_XOR :
gs);	op_xor(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags:fla
1	break;
	<pre>case ALU_OP_NEG_A : op_neg_a(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:f</pre>
lags);	
	break; case ALU_OP_NEG_B:
	op_neg_b(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:f
lags);	break;
	<pre>case ALU_OP_NOT_A :</pre>
lags);	op_not_a(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags:f
iags / /	break;
	case ALU_OP_NOT_B:
lags);	op_not_b(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags:f
	break;
	<pre>case ALU_OP_ASL : op_alu_asl(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags</pre>
:flags)	;
	break; case ALU_OP_LSR:
. 61	op_alu_lsr(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags
:flags)	; break;
	<pre>case ALU_OP_ROL:</pre>
:flags)	op_alu_rol(reg_in_a, reg_in_b, reg_out_accu, (flags≡NULL)?dummyflags;
- LIAGIS /	break;
	<pre>case ALU_OP_ROR: op_alu_ror(reg_in_a, reg_in_b, reg_out_accu, (flags=NULL)?dummyflags</pre>
:flags)	
	break;
	<pre>case ALU_OP_RESET : op_alu_reset(req_in_a, req_in_b, req_out_accu, (flags≡NULL)?dummyfla</pre>
gs:flag	s);
	break; default:
]	<pre>printf("ALU(%i): Invalide operation %i selected", alu_opcode, alu_op</pre>
code);	
}	

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