Lab 4 Report

ECE 4525

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Introduction

The purpose of this lab was to design and implement an 8-bit logic/arithmetic comparator using VHDL. The comparator follows the function of the SN74AS885 chip, but without the PLE signal. The comparator inputs are controlled by DIP-switches, while the outputs are displayed on LEDs. The objectives of this lab were to review the two's complement representation of signed numbers and to design a comparator circuit for both signed and unsigned numbers. The design is first verified through behavioral and post-route simulations, then implemented on the FPGA board. Finally, a function generator and logic analyzer are used to measure the circuits longest propagation delays.

Procedure

Task One:

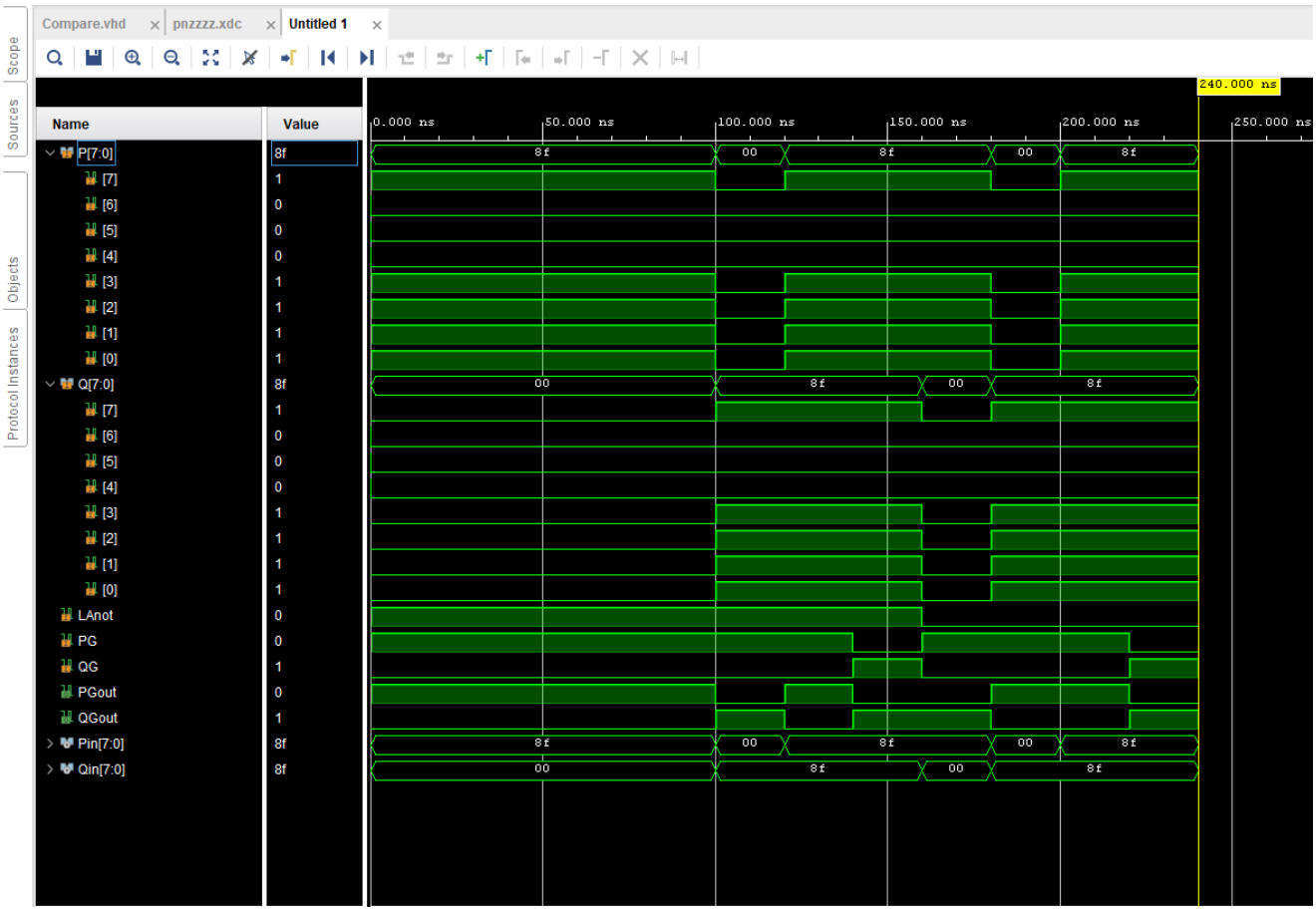

Fig 1: This shows the behavioral simulation.

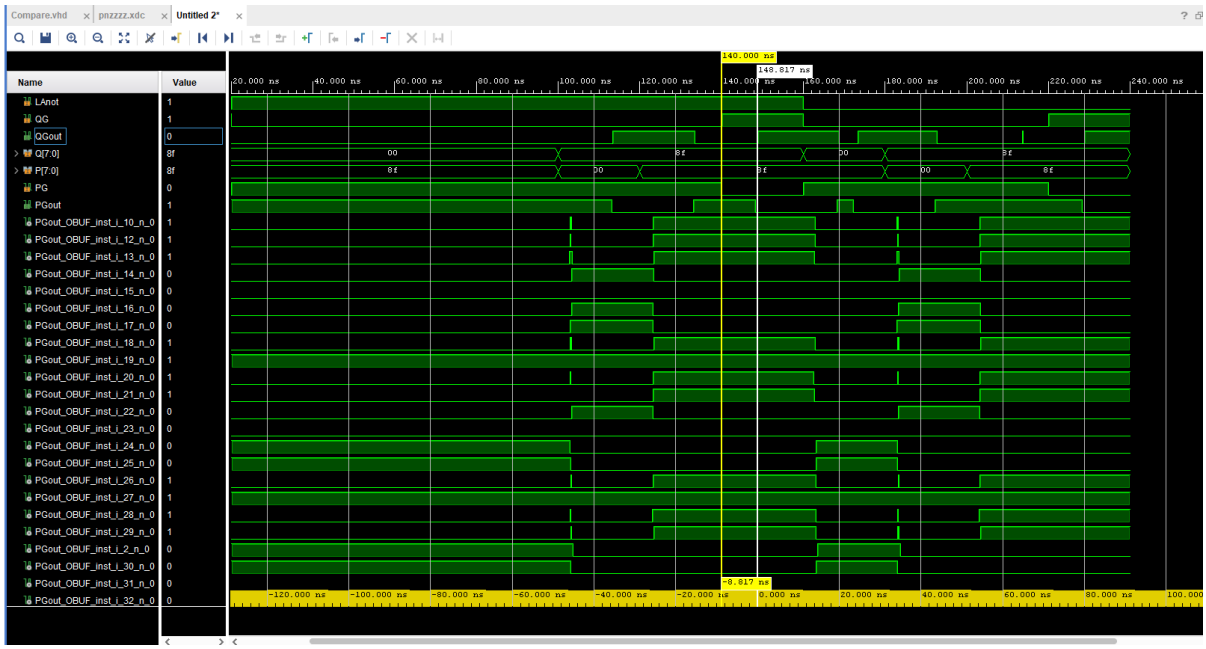

Fig 2: This is the post-route simulation showing the worst-case propagation delay. The delay we acquired was 8.817ns

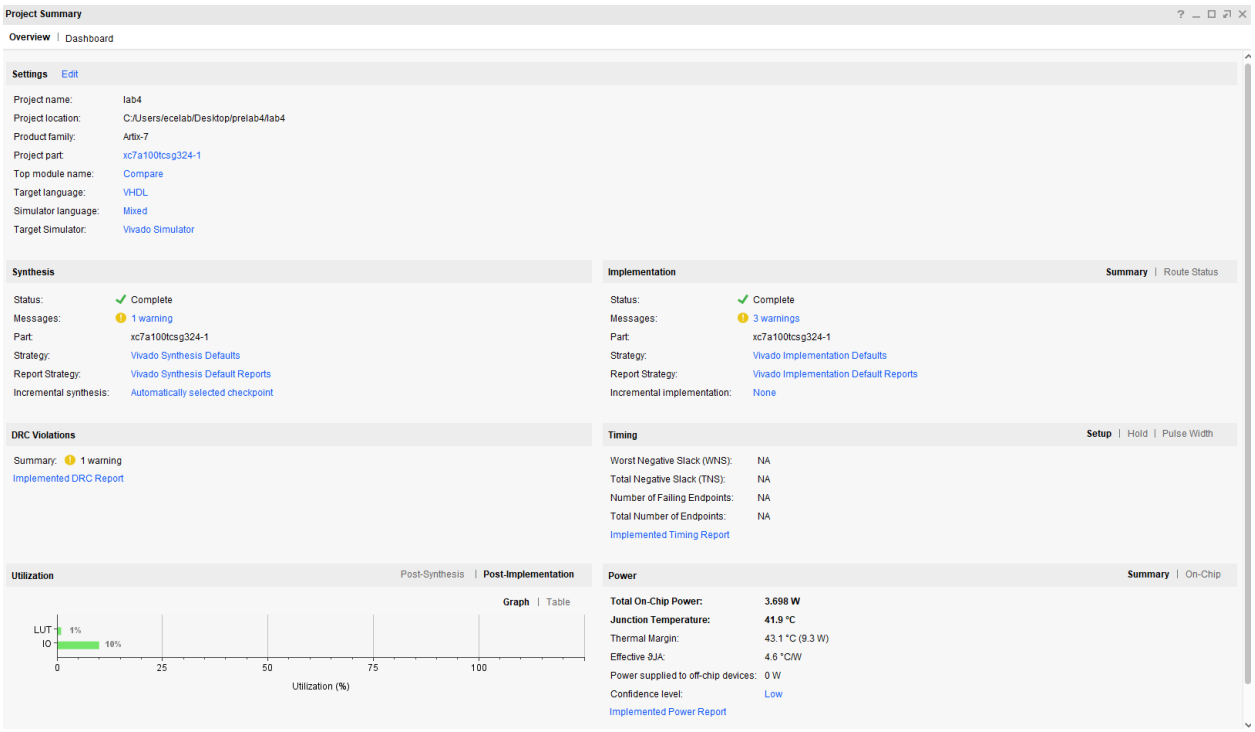

Fig 3: This is the summary report.

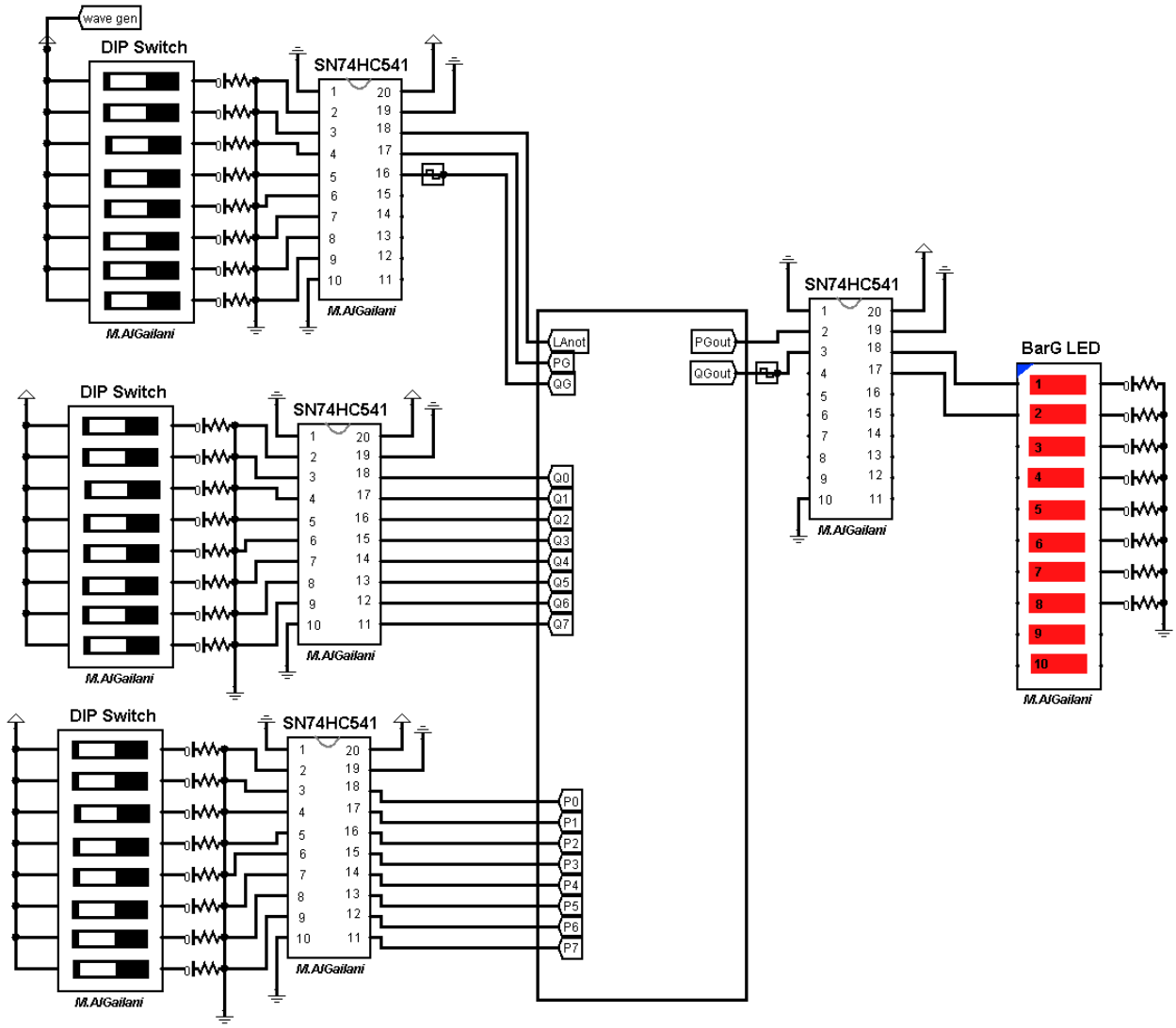

Fig 4: This shows the schematic. Q(7-0), P(7-0), LAnot, PG, and QG are set as dipswitches for inputs. PGout and QGout are set to LEDs as outputs.

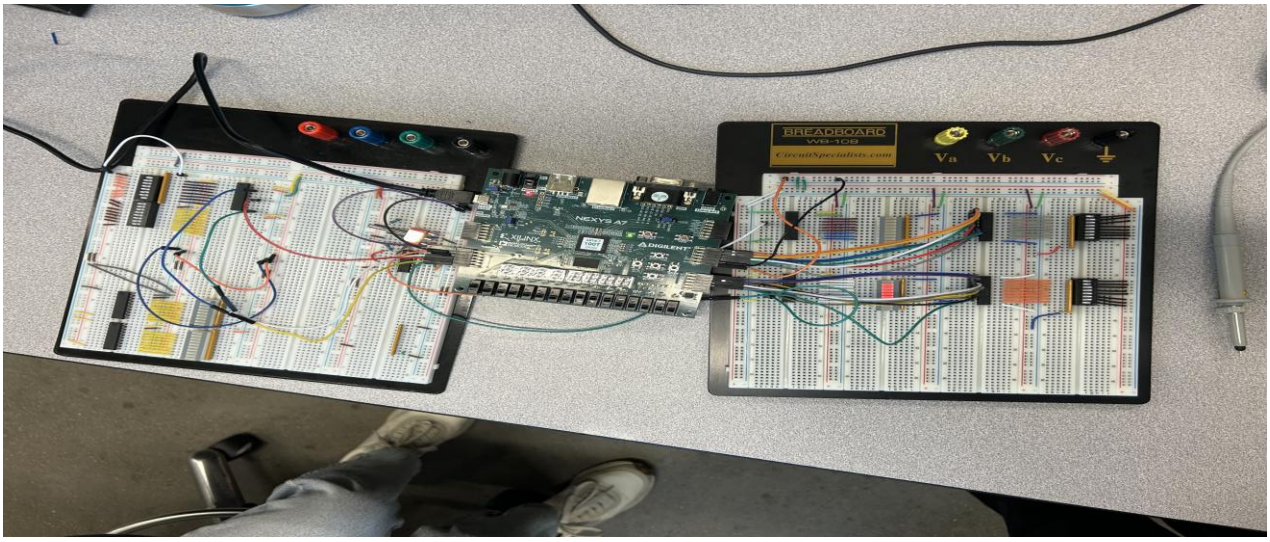

Fig 5: In this photo LA is set high, so it is logical. Q is equal to 10000011 and P is equal to 00000001 so Q is larger and QGout is set high shown on the LEDs.

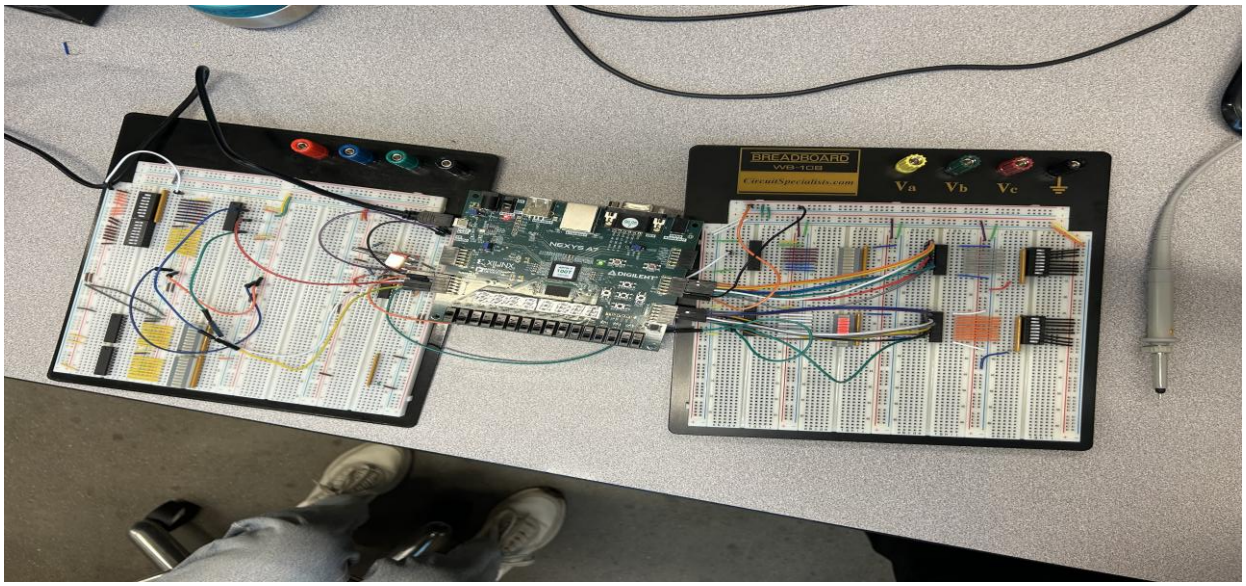

Fig 6: In this photo LA is set high, so it is logical. Q is equal to 10000011 and P is equal to 10000011 they are equal therefore QG input being high makes QGout high as shown on the LEDs.

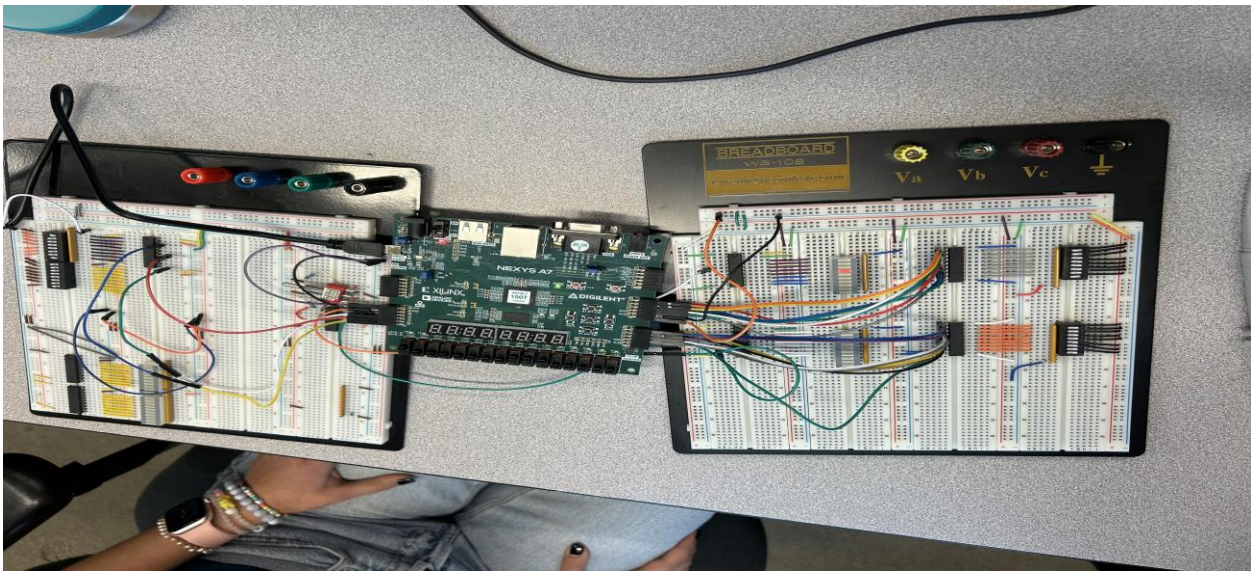

Fig 7: In this photo LA is set high, so it is logical. Q is equal to 00000000 and P is equal to 10000011 so P is larger and PGout is outputting high shown on the LEDs.

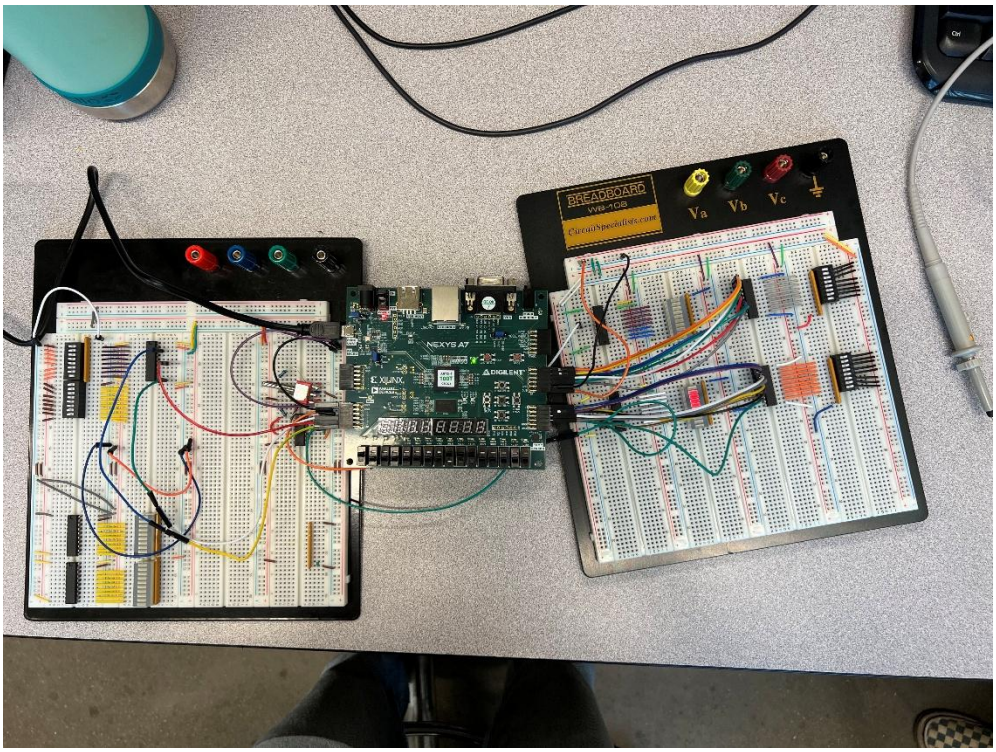

Fig 8: In this photo LA is set low, so it is arithmetical. Q is equal to (00000000) and P is equal to (10000011) so Q is larger and QGout is set high shown on the LEDs.

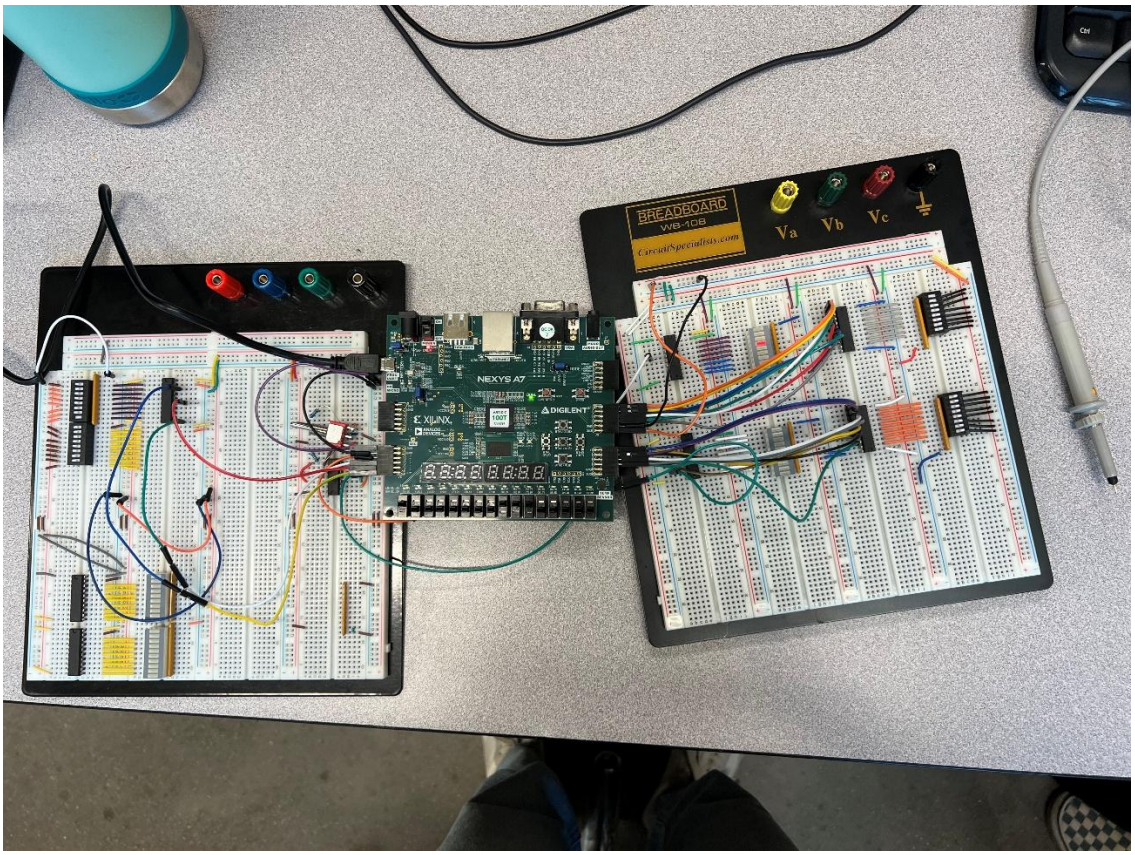

Fig 9: In this photo LA is set low, so it is arithmetical. Q is equal to (00000000) and P is equal to (00000011) so P is larger and PGout is set high shown on the LEDs.

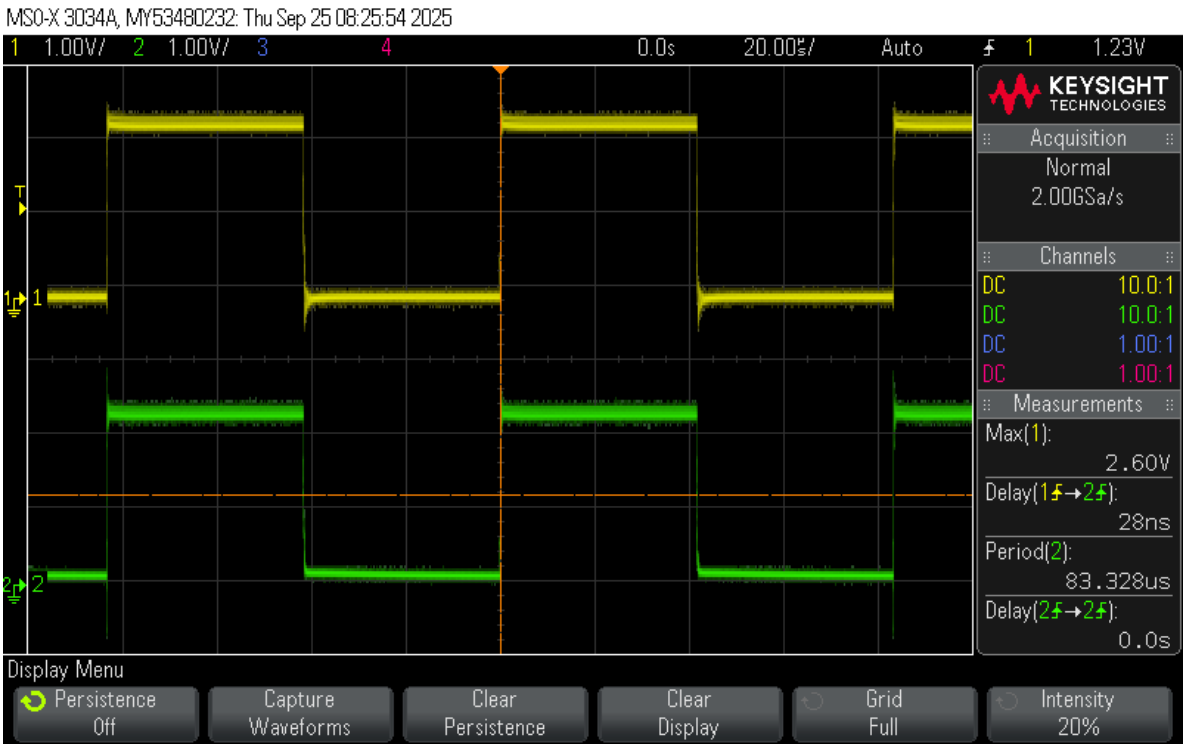

Fig 10:This shows the oscilloscope picture with the propagation delay of 28ns

Conclusion

In conclusion, the design and implementation of the 8-bit logic/arithmetic comparator provided valuable hands-on experience. The successful simulation and FPGA implementation verified the correctness of the design, while timing measurements using the function generator and logic analyzer provided insight into propagation delays and performance of the circuit. Overall, this lab reinforced key concepts, hardware descriptions, and timing analysis.

Appendix

VHD

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--use ieee.std_logic_arith.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity SN74AS885 is
  Port (
  P, Q: IN std_ulogic_vector(7 downto 0);
  LAnot,PG, QG: IN std_logic;
  PGout, QGout: OUT std_logic
  );
end SN74AS885;

architecture Behavioral of SN74AS885 is
signal Pin : signed(7  downto 0);
signal Qin: signed(7  downto 0);
begin

Pin <= signed(P);
Qin <= signed(Q);

process(LAnot,P, Q, Pin, Qin, PG, QG)

    begin

        if ((LAnot)='1') then
            if (P>Q) then
                PGout <= '1';
                QGout <= '0';
            elsif (P<Q) then
                PGout <= '0';
                QGout <= '1';
            else
                PGout <= PG;
                QGout <= QG;
            end if;
        else
            if (Pin>Qin) then
                PGout <= '1';
                QGout <= '0';
            elsif (Pin<Qin) then
                PGout <= '0';
                QGout <= '1';
            else
                PGout <= PG;
                QGout <= QG;
            end if;
        end if;
end process;

end Behavioral;
```

XDC

```
##Pmod Headers
##Pmod Header JA
set_property -dict { PACKAGE_PIN C17 IOSTANDARD LVCMOS33 } [get_ports { P[0] }];
#IO_L20N_T3_A19_15 Sch=ja[1]
set_property -dict { PACKAGE_PIN D18 IOSTANDARD LVCMOS33 } [get_ports { P[1] }];
#IO_L21N_T3_DQS_A18_15 Sch=ja[2]
set_property -dict { PACKAGE_PIN E18 IOSTANDARD LVCMOS33 } [get_ports { P[2] }];
#IO_L21P_T3_DQS_15 Sch=ja[3]
set_property -dict { PACKAGE_PIN G17 IOSTANDARD LVCMOS33 } [get_ports { P[3] }];
#IO_L18N_T2_A23_15 Sch=ja[4]
set_property -dict { PACKAGE_PIN D17 IOSTANDARD LVCMOS33 } [get_ports { P[4] }];
#IO_L16N_T2_A27_15 Sch=ja[7]
set_property -dict { PACKAGE_PIN E17 IOSTANDARD LVCMOS33 } [get_ports { P[5] }];
#IO_L16P_T2_A28_15 Sch=ja[8]
set_property -dict { PACKAGE_PIN F18 IOSTANDARD LVCMOS33 } [get_ports { P[6] }];
#IO_L22N_T3_A16_15 Sch=ja[9]
set_property -dict { PACKAGE_PIN G18 IOSTANDARD LVCMOS33 } [get_ports { P[7] }];
#IO_L22P_T3_A17_15 Sch=ja[10]

##Pmod Header JB
set_property -dict { PACKAGE_PIN D14 IOSTANDARD LVCMOS33 } [get_ports { Q[0] }];
#IO_L1P_T0_AD0P_15 Sch=jb[1]
set_property -dict { PACKAGE_PIN F16 IOSTANDARD LVCMOS33 } [get_ports { Q[1] }];
#IO_L14N_T2_SRCC_15 Sch=jb[2]
set_property -dict { PACKAGE_PIN G16 IOSTANDARD LVCMOS33 } [get_ports { Q[2] }];
#IO_L13N_T2_MRCC_15 Sch=jb[3]
set_property -dict { PACKAGE_PIN H14 IOSTANDARD LVCMOS33 } [get_ports { Q[3] }];
#IO_L15P_T2_DQS_15 Sch=jb[4]
set_property -dict { PACKAGE_PIN E16 IOSTANDARD LVCMOS33 } [get_ports { Q[4] }];
#IO_L11N_T1_SRCC_15 Sch=jb[7]
set_property -dict { PACKAGE_PIN F13 IOSTANDARD LVCMOS33 } [get_ports { Q[5] }];
#IO_L5P_T0_AD9P_15 Sch=jb[8]
set_property -dict { PACKAGE_PIN G13 IOSTANDARD LVCMOS33 } [get_ports { Q[6] }]; #IO_0_15
Sch=jb[9]
set_property -dict { PACKAGE_PIN H16 IOSTANDARD LVCMOS33 } [get_ports { Q[7] }];
#IO_L13P_T2_MRCC_15 Sch=jb[10]

##Pmod Header JC
set_property -dict { PACKAGE_PIN K1 IOSTANDARD LVCMOS33 } [get_ports { LAnot }]; #IO_L23N_T3_35
Sch=jc[1]
set_property -dict { PACKAGE_PIN F6 IOSTANDARD LVCMOS33 } [get_ports { PG }];
#IO_L19N_T3_VREF_35 Sch=jc[2]
set_property -dict { PACKAGE_PIN J2 IOSTANDARD LVCMOS33 } [get_ports { QG }]; #IO_L22N_T3_35
Sch=jc[3]
set_property -dict { PACKAGE_PIN G6 IOSTANDARD LVCMOS33 } [get_ports { PGout }]; #IO_L19P_T3_35
Sch=jc[4]
set_property -dict { PACKAGE_PIN E7 IOSTANDARD LVCMOS33 } [get_ports { QGout }]; #IO_L6P_T0_35
Sch=jc[7]
```

TCL

```
restart
add_force LAnot {1 0ns}
add_force P {10001111 0ns}
add_force Q {00000000 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 100ns
add_force LAnot {1 0ns}
add_force P {00000000 0ns}
add_force Q {10001111 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 20ns
add_force LAnot {1 0ns}
add_force P {10001111 0ns}
```

```
add_force Q {10001111 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 20ns
add_force LAnot {1 0ns}
add_force P {10001111 0ns}
add_force Q {10001111 0ns}
add_force PG {0 0ns}
add_force QG {1 0ns}
run 20ns
add_force LAnot {0 0ns}
add_force P {10001111 0ns}
add_force Q {00000000 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 20ns
add_force LAnot {0 0ns}
add_force P {00000000 0ns}
add_force Q {10001111 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 20ns
add_force LAnot {0 0ns}
add_force P {10001111 0ns}
add_force Q {10001111 0ns}
add_force PG {1 0ns}
add_force QG {0 0ns}
run 20ns
add_force LAnot {0 0ns}
add_force P {10001111 0ns}
add_force Q {10001111 0ns}
add_force PG {0 0ns}
add_force QG {1 0ns}
run 20ns
```