ECE 4525/5525
Digital Design Laboratory
Laboratory Four
8-Bit Logic/Arithmetic Comparator

Objectives:

i. To review the two's complement representation of signed numbers

ii. To design a cascadable comparator circuit for either signed or unsigned numbers

Task One

1. Devise VHDL code for an 8-bit logic/arithmetic comparator unit. The specifications you should implement are based upon the Function Table of the SN74AS885 chip by Texas Instruments but signal PLE and the internal latch for operand P are dropped. Input signals should be driven by DIP-switches and the status of the output signals should be visualized by Bar-LEDs on your solderless breadboard. You are to make the pin assignments for the input and output signals. Run the behavioral and post-route simulations to verify the correct operation of your circuit.

2. Run the implement step and download the configuration bit file to your Nexys A7 Board. Verify the correct operation.

3. With the help of a function generator and a logic analyzer obtain the longest propagation delays of the implemented circuit.

Demonstrate these tasks to your Lab TA. All circuit designs and tests should be documented by VHDL source files, a .xdc file, the top page of the Summary Report, simulation timing diagrams and logic analyzer screen shots, as appropriate. You should also furnish your schematic diagram for Task One, Part 1. All VHDL files, simulation timing diagrams and logic analyzer screen shots should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file** (scan the hard copies of the logic analyzer screen shots, as needed) through the **appropriate Drop Box in Elearning**.