ECE 4525/5250 DIGITAL DESIGN
Fall 2025
Prelab Assignment for Lab Four

Task One

Develop a behavioral VHDL code module and a proper .xdc file for Task One. All input and output signals should be routed from/to DIP Switches and Bar-LEDs, respectively, **which will be mounted on your solderless Breadboard**. **All FPGA signals involved should be buffered by suitable buffer chips**. You should also draw a schematic diagram for your circuit that will be implemented on your Breadboard. **You should make all pin assignments for the input and output signals**. The Nexys A7 Board should be represented by your FPGA and corresponding **Pmod** connector pins only.

Develop a .tcl file to verify your design by simulation.