ECE 4525/5525 DIGITAL DESIGN

FALL 2025

Homework Assignment #4

Total: 90 pts.

Due 11:30am, Friday, October 3, 2025

A **synchronous** sequential circuit is given by its state transition graph on **Page 2**. **Input X should be synchronized with respect to the falling edge of the clock**. **State changes should take place at the rising edge of the clock**. The **RESET# input** should be **active-low**. Use the available **AMD/Xilinx Vivado** software tools **to design, simulate and compile** your circuit on your **Xilinx Artix-7 FPGA** chip. However, downloading the bit file to your Nexys A7 Board is **NOT** required.

Tasks:

a) Draw an **ASM chart** for the state transition graph shown on Page 2. (10 pts.)

b) Turn in an electronic copy of the **.vhd** file for your design. (30 pts.)

c) **Map** your design to the FPGA chip specified above by running the **Implement** step. **Add** a **customized version of the Nexys A7.xdc file** to your project files such that **input X** is assigned to **SW[0], the CLK input** to the **100MHz** on-board clock, **outputs Z1 and Z2** to **LED[8]** and **LED[9]**, input RESET# to push button **BTNL** and **state designation outputs S0 through S6** are assigned to **LED[0] through LED[6]**, respectively. Turn in an **electronic copy of your .xdc file** and **only the top page of the Project Summary Report**. (10 pts.)

d) Develop a **script** (**.tcl file**) to verify the correct operation of your circuit. Make sure that **each state transition is visited at least once**. Run the **post-route simulations**. Turn in an electronic copy of your **.tcl** file along with an electronic copy of the **simulation waveforms**. **Comment on** the simulation results for full credit. (40 pts.)

Fall back position: turn in electronic copies of your **.vhd**, **.xdc** and **.tcl** files along with comments for partial credit if you couldn't compile your design due to some fatal error.

Bonus Homework Assignment #4

Total: 40 pts.

Due 11:30am, Friday, October 3, 2025

Download the **.bit** file to your Nexys A7 Board and prototype your circuit. **Create a narrated, short video clip** (**.mp4** file, up to **4mins**) to illustrate that your circuit works. Submit the mp4 file through the **appropriate Drop Box in eLearning**.

Electronic submission: submit your **single .pdf** file through the **appropriate Drop Box in eLearning**.