ECE 4525/5525 DIGITAL DESIGN
Fall 2024
Prelab Assignment for Lab Eleven

The simplified Counter has the signals as follows: inputs CKA, R0 and R5, and outputs Q_A, Q_B, and Q_C.

Task One

Part 1

Design the simplified Modulo-6 Counter as an asynchronous sequential circuit using the steps presented in class (Primitive Flow Map, Implication Table, Cover Table, Closure Table, Reduced State Table, Critical Race-Free State Assignment and Next State Equations). Develop a VHDL source code module and a proper .tcl file for simulation of Task One. The stimuli should provide for all scenarios to verify the correct operation of your counter. In addition, your .xdc file should cover the circuit inputs and outputs as outlined below.

Draw a detailed schematic diagram for Part 1. You should make your own signal assignment with respect to the Pmod JA Header pins. Map inputs R0, R5 to switches on the Nexys A7 Board, and the "y" state variables to LEDs also on the Nexys A7 Board. LEDs for counter outputs Q_A, Q_B, and Q_C and the bounce-free switch for CKA should be mounted on your solderless breadboard.