ECE 4525/5525
Digital Design Laboratory
Laboratory Eleven
Asynchronous Counter

Objectives:

i. To design an asynchronous sequential circuit from word specification

ii. To evaluate the performance of the implemented circuit

Task One

1. The link to the Data Sheets of the SN7490A Decade Counter by Texas Instruments is posted on Labs Section of the Class Web Page. Assume the specifications changes as follows: only just one R0 (Reset to 0) and R9 (Set to 9) input, respectively, is available. These inputs are active high and R9 has priority over R0. Either R0, or R9 has priority over the count function. Output Q_A is connected to CKB, that is, the CKB input is eliminated. If R9=R0=0, then the counter's contents are incremented when input CKA makes a high-to-low transition. The decade (BCD) count sequence is illustrated on Page 3 of the Data Sheets. **However, you are only required to implement a counter with states 0-to-5**. **Hence, input R9 is now revised to R5 (Set to 5).**
   Develop VHDL code for this module as an asynchronous sequential circuit. The detailed specifications are given in the Prelab Assignment, or will be decided by your Lab TA. Run **post-route simulations** to verify the correct operation of your circuit.

2. Run the implement step and download the configuration bit file to your Nexys A7 Board. The pin assignments for the input and output signals are specified in the Prelab Assignment, or determined by your Lab TA. Use switches and LEDs to verify the correct operation.

   i. Use DIP switches to verify the correct operation of the counter when inputs R0 and R5 are asserted, respectively.

   ii. Use a **bounce-free switch** to drive input CKA and verify the count sequence.

   iii. Use a bounce-free switch for CKA and DIP switches for R0 and R5 and a logic analyzer for the counter outputs to test the performance of your circuit.

   iv. Revise your VHDL code to use a **push button** on your Nexys A7 Board for CKA and again check the operation of your counter.

Demonstrate these tasks to your Lab TA by making and presenting short video clips. All circuit designs and tests should be documented by VHDL source files, the top page of the Summary Report

and post-route simulation timing diagrams. All VHDL files and simulation timing diagrams should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file** through the **appropriate Drop Box in eLearning**.