ECE 4525/5525 DIGITAL DESIGN
Fall 2025
Prelab Assignment for Lab Ten

Task One

The two inputs, X1 and X2, should be driven by bounce-free switches on your Breadboard. State variables y1, y2, and y3 and output Z should be displayed using LEDs also on your Breadboard. Draw a detailed schematic diagram for Task One. You should make your own signal assignment with respect to Pmod JB Header pins. In your schematic diagram the FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod JB Header pin numbers, respectively, that are being used.

For the reduced state table posted on the Class Web Page devise a critical race-free state assignment and the next state equations for Y1, Y2 and Y3 and the logic function for output Z. Make sure that there are no hang states.

Develop a VHDL source code module and a proper .tcl file for simulation for Task One. The simulation stimuli should guarantee that each stable state and each state transition arc is visited at least once.