ECE 4525/5525
Digital Design Laboratory
Laboratory Ten
Asynchronous Sequential Circuit

Objectives:

i. To design an asynchronous sequential circuit using VHDL

ii. To evaluate the performance of the implemented circuit

Task One

1. The **reduced state table** of an asynchronous sequential circuit is posted on the Class Web Page. Develop a **critical race-free state assignment**. Devise the **next state equations** for an implementation using **combinational logic with feedback**. **Develop VHDL code** for your circuit. The detailed specifications are given in the Prelab Assignment, or will be decided by your Lab TA. Run **post-route simulations** to verify the correct operation of the circuit.

2. Run the Implement step and download the configuration bit file to your Nexys A7 Board. The pin assignments for the input and output signals are specified in the Prelab Assignment, or determined by your Lab TA. Use switches and LEDs to verify the correct operation and to evaluate the performance of your circuit.

Demonstrate these tasks to your Lab TA by making and presenting short video clips. All circuit designs and tests should be documented by VHDL source files, the top page of the Summary Report and post-route simulation timing diagrams. All VHDL files and simulation timing diagrams should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file** through the **appropriate Drop Box in Elearning**.

x_1x_2 / y	00	01	11	10
	Y Z			
a	(a) 0	b 0	c x	(a) 0
b	(b) 0	(b) 0	d x	a 0
c	a 0	b x	(c) 1	(c) 1
d	x x	e x	(d) 1	a x
e	a 0	(e) 0	c x	x x