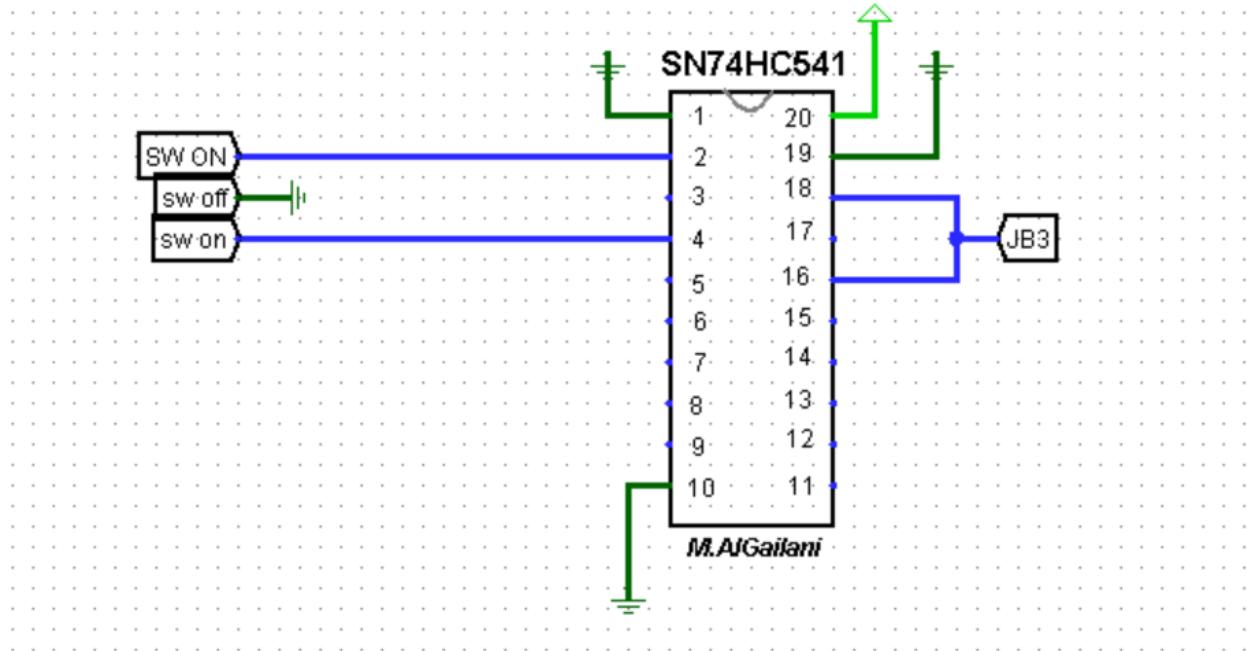


## Prelab 6

## Task1



Vhdl

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity serial is
  Port (
    CLK, RESET, A, B: in std_logic;
    CY, SUM: out std_logic
  );
end serial;

architecture Behavioral of serial is
signal c: std_logic:='0';
begin
clock: process
begin
wait until clk' event;
  if c = '0' then
    sum <= (A XOR B);
    c <= (A and B);
    cy <= c;
  end if;
end process;
end;

```

```

    else
        sum <= (a XOR b) XOR '1';
        c <= (a AND b) OR (a AND '1') OR (b AND '1');
        cy <= c;
    end if;
end process clock;

end Behavioral;

```

## Xdc

```

set_property -dict { PACKAGE_PIN E3 IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }]; #IO_L12P_T1_MRCC_35
Sch=clk100mhz

set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]

#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];

##Switches
set_property -dict { PACKAGE_PIN R17 IOSTANDARD LVCMOS33 } [get_ports { B }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN U18 IOSTANDARD LVCMOS33 } [get_ports { A }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]

## LEDs
set_property -dict { PACKAGE_PIN V14 IOSTANDARD LVCMOS33 } [get_ports { CY }]; #IO_L22N_T3_A04_D20_14
Sch=led[13]
set_property -dict { PACKAGE_PIN V11 IOSTANDARD LVCMOS33 } [get_ports { SUM }]; #IO_L21N_T3_DQS_A06_D22_14
Sch=led[15]

##Buttons
set_property -dict { PACKAGE_PIN C12 IOSTANDARD LVCMOS33 } [get_ports { RESET }]; #IO_L3P_T0_DQS_AD1P_15
Sch=cpu_resetn

##Pmod Header JB
set_property -dict { PACKAGE_PIN G16 IOSTANDARD LVCMOS33 } [get_ports { CLK }]; #IO_L13N_T2_MRCC_15 Sch=jb[3]

```

## Task 2