

ECE 4525/5525
Digital Design Laboratory
Laboratory Six
Bit-Serial Adder and Control of Shift Register

Objectives:

- i. To develop VHDL code for synchronous sequential circuits
- ii. To design control and display circuits for a shift register

Task One

1. Devise VHDL code for a bit-serial adder circuit. The ASM chart for a Moore-type bit-serial adder is posted on the Class Web Page. The detailed specifications are given in the Prelab Assignment, or will be decided by your Lab TA. A bounce-free manual clock signal should be implemented on your Breadboard for the bit-serial adder. Verify the correct operation of your bounce-free clock circuit with the help of a logic analyzer. The A and B data input signals for the two operands should be driven by switches and the status of the output signal Sum should be visualized by a LED on your Nexys A7 Board. Run behavioral and post-route simulations to verify the correct operation of your circuit.
2. Run the implement step and download the configuration bit file to your Nexys A7 Board. The pin assignments for the input and output signals are specified in the Prelab Assignment, or determined by your Lab TA. Again, verify the correct operation.

Task Two

1. Build an interface circuit to the 74HC299 shift register (or equivalent chip) that is mounted on your Breadboard using DIP-Switches, tri-state buffers, LEDs, a push button, etc. The DS₀ right shift serial input of the 74HC299 shift register should be connected to the Sum output of the bit-serial adder you have developed for Task One. The shift register's CP clock input should be connected to the proper phase of the manual clock signal you have implemented for Task One. The Mode Select information should be determined by switches on the Nexys A7 Board. The S₁ and S₀ Mode Select inputs of the shift register should be driven by outputs of the Artix-7 FPGA. Information for the asynchronous reset function should be taken from a push button on the Nexys A7 Board while the MR# Master Reset input should be driven by an output of the Artix-7 FPGA. Data for the Parallel Load function should be provided through DIP-Switches on your Breadboard. The Parallel Data outputs should be displayed using Bar-LEDs on your Breadboard.

You should develop a VHDL program to carry out the Parallel Load, Shift Right and Hold operations, respectively, of the shift register.

The detailed specifications are given in the Prelab Assignment, or will be decided by your

Lab TA. Run behavioral and post-route simulations to verify the correct operation of your circuit.

Note: you are **not** required to develop a .tcl file to simulate the 74HC299 shift register.

2. Run the implement step and download the configuration bit file to your Nexys A7 Board. The pin assignments for the input and output signals are specified in the Prelab Assignment or determined by your Lab TA. Again, verify the correct operation.

Demonstrate these tasks to your Lab TA. All circuit designs and tests should be documented by VHDL source files, a .xdc file, the top page of the Summary Report, simulation timing diagrams and logic analyzer screen shots, as appropriate. You should also furnish your schematic diagrams for Tasks One and Two. All VHDL files, simulation timing diagrams and logic analyzer screen shots should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file** (scan the hard copies the schematic diagrams) through the **appropriate Drop Box in eLearning**.