ECE 4525/5525 DIGITAL DESIGN
Fall 2025
Prelab Assignment for Lab Six

Task One

Draw a detailed schematic diagram for the **bounce-free manual clock circuit** to be mounted on your Breadboard. The **CLK** output of your circuit should be connected to **Pin 3 of Pmod connector JB** (MRCC_15 clock input). Use Switches **SW[6]** and **SW[4]** on your Nexys A7 Board to enter the two **serial operands A** and **B** to the bit-serial adder (**least significant bits first**). Use push button **CPU_RESETN** as your **asynchronous RESET** signal. You should assign a **LED** on your Nexys A7 Board to display the status of the **SUM** output. In addition, assign another LED to the signal **CY** (Carry Out) for **debug purposes**. The manual CLK signal should be buffered by suitable buffer chips. In your schematic diagram the Artix-7 FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod connector pin numbers, respectively, that are being used. Devise a suitable .xdc file for Task One.

Prepare some test data for your serial adder such that all states and state transitions will be parsed. Use your work to design your .tcl file. Develop a behavioral VHDL source code module and a proper .tcl file for Task One.

All FPGA signals involved should be buffered by suitable buffer chips. You should also draw a schematic diagram for your circuit that will be implemented on your Breadboard. **You should make all pin assignments for the input and output signals**. The Nexys A7 Board should be represented by your FPGA and corresponding **Pmod** connector pins only.

Task Two

Draw a detailed schematic diagram for Task Two. The 74HC299 Shift Register (or a compatible chip) should be mounted on your Breadboard. Your circuit should operate the 74HC299 in either of the following three modes: **Parallel Load**, **Shift Right** and **Hold**, respectively. The **serial input data** (**DS0**) to the Shift Register should be provided through the **Sum output** of your Bit Serial Adder. **Parallel load data should be provided through DIP switches on your Breadboard**. Use push button **BTNC** as a source for the shift register's **MR#** signal. The manual, bounce-free CLK signal should be used as clock source both to the Bit Serial Adder and the shift register (**CP**). This signal should also be passed as an input signal to the Artix-7 FPGA (see Task One). Keep in mind that the control signals of the shift register are

sampled with respect to the **rising edge** of its clock signal. **You should avoid potential race conditions between your Bit Serial Adder circuit and the shift register**. The **shift register outputs should be permanently displayed on a Bar-LED module on your Breadboard**. The **operating modes signals** (**S1**, **S0**) of the shift register should be determined by a combination of two signals driven by **SW[11] and SW[9]** on your Nexys A7 Board. **You should make your own decisions on the pin assignments for the signals connecting the Artix-7 FPGA to the 74HC299 chip**. All FPGA signals involved should be buffered by suitable buffer chips. In your schematic diagram the Artix-7 FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod connector pin numbers, respectively, that are being used.

Develop a simple VHDL source code module and a proper .tcl file for simulation for Task Two. **You are NOT required to simulate the 74HC299 Shift Register**.