

Example 1: A modern 1Mx1 CMOS Dynamic RAM

Motorda MCM 511000A

Advance Information

1M x 1 CMOS Dynamic RAM

The MCM511000A is a 1.0µ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM511000A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- RAS Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh

- 512 Cycle Refresh: MCM511000A = 8 ms

MCM51L1000A = 64 ms

- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection

- Fast Access Time (t_{rac}):

MCM511000A-70 and MCM51L1000A-70 = 70 ns (Max)

MCM511000A-80 and MCM51L1000A-80 = 80 ns (Max)

MCM511000A-10 and MCM51L1000A-10 = 100 ns (Max)

- Low Active Power Dissipation:

MCM511000A-70 and MCM51L1000A-70 = 440 mW (Max)

MCM511000A-80 and MCM51L1000A-80 = 385 mW (Max)

MCM511000A-10 and MCM51L1000A-10 = 330 mW (Max)

- Low Standby Power Dissipation:

MCM511000A and MCM51L1000A = 11 mW (Max, TTL Levels)

MCM511000A = 5.5 mW (Max, CMOS Levels)

MCM51L1000A = 1.1 mW (Max, CMOS Levels)

MCM511000A MCM51L1000A



P PACKAGE
PLASTIC
CASE 707A



J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822

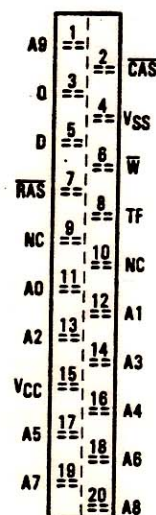


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

PIN NAMES

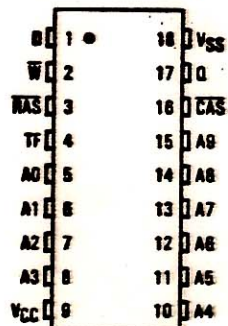
A0-A9	Address Input
D	Data Input
Q	Data Output
W	Read/Write Enable
RAS	Row Address Strobe
CAS	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground
TF	Test Function Enable
NC	No Connection

ZIG-ZAG IN-LINE



DUAL-IN-LINE

PIN ASSIGNMENT



SMALL OUTLINE

