ECE 4525/5525
Digital Design Laboratory
Laboratory Seven
Controller for Asynchronous DRAM chip

Objectives:

i. To develop VHDL code for synchronous sequential circuits

ii. To implement delays using a finite state machine

iii. To design a controller (DRAMC) for simple read and write cycles of an asynchronous DRAM chip

Task One

Devise VHDL code to control a simple read cycle for a DRAM chip. The read cycle timing diagram and the AC Parameters of the DRAM chip are posted on the Class Web Page. Detailed specifications are given in the Prelab Assignment or will be decided by your Lab TA. For this Task, your FSM will be using the 100MHz clock source on your Nexys A7 Board for the DRAM Controller (DRAMC). The read command signal that initiates the read cycle should be mapped to a switch on your Breadboard. The key DRAM control signals should be routed to your Breadboard. Detailed specifications are given in the Prelab Assignment or will be decided by your Lab TA. Run post-route simulations to verify the correct operation of your circuit. Check to see that the specified timing requirements are met. Demonstrate the implemented read cycle to the Lab TA by using a logic analyzer.

Task Two

Devise VHDL code to control a simple write cycle for a DRAM chip. The write cycle timing diagram and the AC Parameters of the DRAM chip are posted on the Class Web Page. The detailed specifications are given in the Prelab Assignment or will be decided by your Lab TA. Again, for this Part, your FSM will be using the 100MHz clock source on your Nexys A7 Board for the DRAM Controller (DRAMC). The write command signal that initiates the write cycle should be mapped to a switch on your Breadboard. The key DRAM control signals should be routed to your Breadboard. The detailed specifications are given in the Prelab Assignment or will be decided by your Lab TA. Run post-route simulations to verify the correct operation of your circuit. Check to see that the specified timing requirements are met. Demonstrate the implemented write cycle to the Lab TA by using a logic analyzer.

Task Three

Revise the VHDL programs you have developed for Tasks One and Two such that you will create a single DRAMC state machine that is capable to run either a read or a write cycle for the DRAM chip. Run post-route simulations to verify the correct operation of your revised DRAMC circuit. Demonstrate the implemented read or write cycles to the Lab TA by using a logic analyzer.

All circuit designs and tests should be documented by VHDL source files, the top page of the Summary Report and simulation timing diagrams. All VHDL files and simulation timing diagrams should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file** through the **appropriate Drop Box in eLearning**.