AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	–	70	–	85	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.