READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM511000A MCM51L1000A	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	[1]	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

NOTES:

14. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.