ECE 4525/5525 DIGITAL DESIGN
Fall 2025
Prelab Assignment for Lab Seven

Task One

Part 1.
Draw a detailed schematic diagram for Task One, Part1. The signal assignment is as follows (* stands for active-low signal):

Inputs	Location on the Pmod JB Header
R_cmd*	JB1
RESET	CPU_RESETN (on the Nexys A7 Board)

Outputs	Location on the Pmod JB Header
Mux_sel	JB3
CAS*	JB4
RAS*	JB7
W*	JB8

The CLK100MHz clock source of the Nexys A7 Board should be used to clock the DRAMC state machine on the Artix-7 FPGA chip. The R_cmd* signal should be driven by a function generator. The frequency of the R_cmd* signal should be set such that it will be negated prior to the end of the read cycle. In your schematic diagram the FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod JB Header pin numbers, respectively, that are being used.

Draw a timing diagram for the read cycle and align it with the states of your FSM. Develop a VHDL source code module, a .xdc file and a proper .tcl file for simulation for Task One, Part 1.

Part 2.
Revise your .xdc file and your schematic diagram for Part 2.

CLKIN	JB10

Task Two
Part 1.

Draw a detailed schematic diagram for Task Two, Part 1. The signal assignment is as follows (* stands for active-low signal):

Inputs	Location on the Pmod JB Header
W_cmd*	JB2
RESET	CPU_RESETN (on the Nexys A7 Board)

Outputs	Location on the Pmod JB Header
Mux_sel	JB3
CAS*	JB4
RAS*	JB7
W*	JB8

The CLK100MHz clock source of the Nexys A7 Board should be used to clock the DRAMC state machine on the Artix-7 FPGA chip. The W_cmd* signal should be driven by a function generator. The frequency of the W_cmd* signal should be set such that it will be negated prior to the end of the write cycle. In your schematic diagram the FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod JC Header pin numbers, respectively, that are being used.

Draw a timing diagram for the write cycle and align it with the states of your FSM. Develop a VHDL source code module, a .xdc file and a proper .tcl file for simulation for Task Two, Part 1.

Part 2.
Revise your .xdc file and your schematic diagram for Part 2.

CLKIN	JB10

Task Three

Develop a VHDL source code module and a proper .tcl file for simulation for Task Three.

Comments for testing

Since the circuit's outputs won't drive any loads (e.g., LEDs) you **don't need to run the output signals through TS buffers. Be careful with the hook ups of the MSO probes so you won't create short circuits between your output signals**.

Don't use a ribbon cable to connect the Pmod pins to the solderless breadboard. Ribbon cables may cause significant capacitive cross coupling effects between adjacent wires. Use single wires, instead.