

SN54ALS561A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

SDAS225A – DECEMBER 1982 – REVISED JANUARY 1995

- Carry Output for n-Bit Cascading
- Buffer-Type Outputs Drive Bus Lines Directly
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

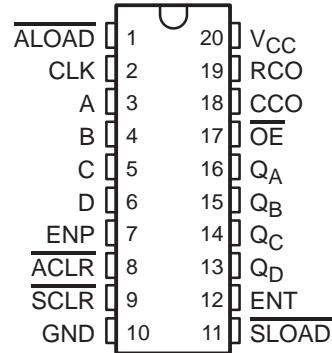
These binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either asynchronous clear (ACLR) or synchronous clear (SCLR). ACLR (direct clear) overrides all other functions of the device, while SCLR overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to asynchronous load (ALOAD) or by the combination of a low level at synchronous load (SLOAD) and a positive-going clock transition. The counting function is enabled only when enable P (ENP), enable T (ENT), ACLR, ALOAD, SCLR, and SLOAD are all high.

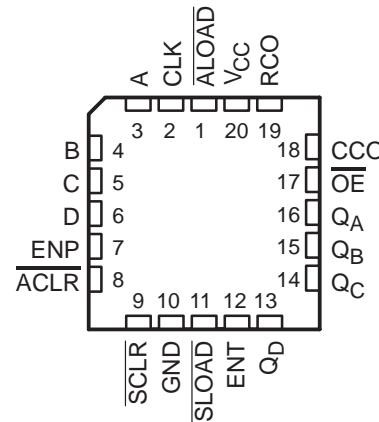
A high level at the output-enable (OE) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of OE. ENT is fed forward to enable the ripple-carry output (RCO) to produce a high-level pulse while the count is maximum (15). The clocked carry output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very high-speed counting, RCO should be used for cascading because CCO does not become active until the clock returns to the low level.

The SN54ALS561A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS561A is characterized for operation from 0°C to 70°C .

**SN54ALS561A . . . J PACKAGE
SN74ALS561A . . . DW OR N PACKAGE
(TOP VIEW)**



**SN54ALS561A . . . FK PACKAGE
(TOP VIEW)**



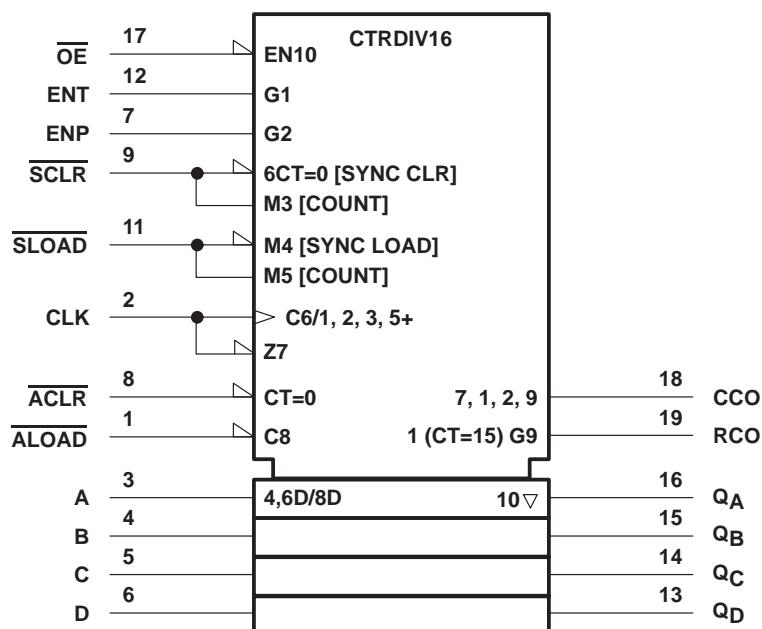
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FUNCTION TABLE

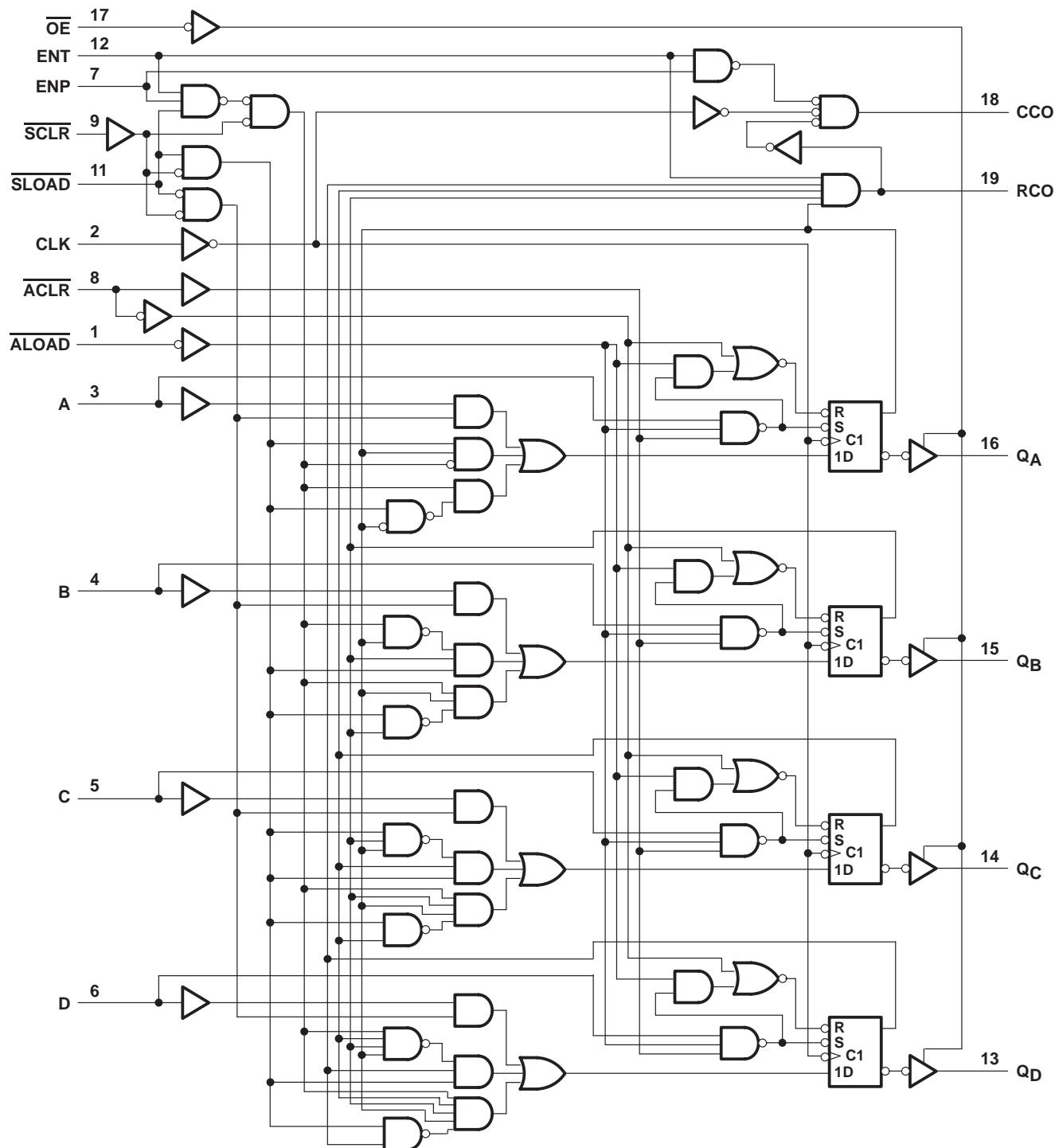
INPUTS								OPERATION
\overline{OE}	\overline{ACLR}	\overline{ALOAD}	\overline{SCLR}	\overline{SLOAD}	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	\uparrow	Synchronous clear
L	H	H	H	L	X	X	\uparrow	Synchronous load
L	H	H	H	H	H	H	\uparrow	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

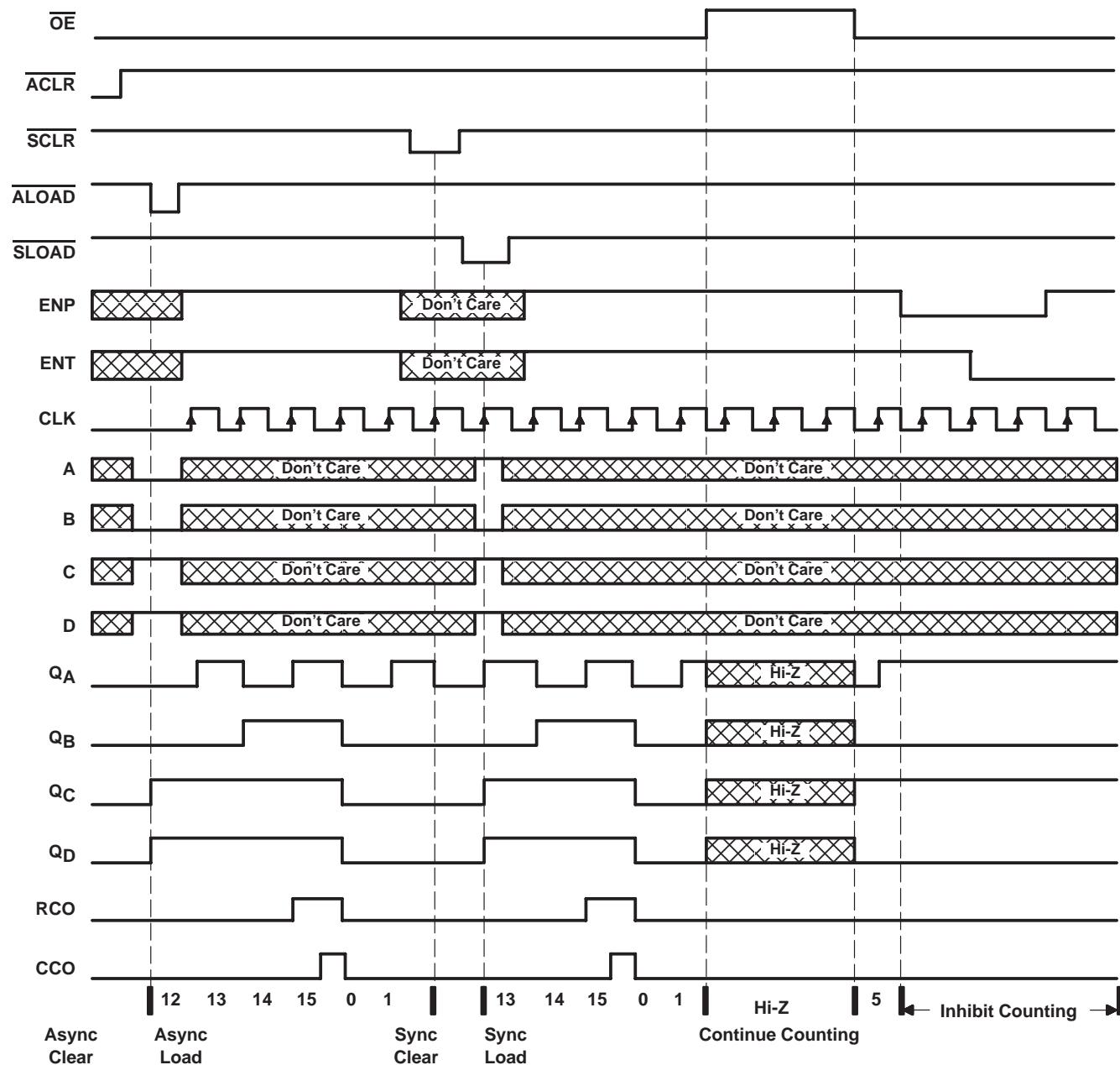
logic diagram (positive logic)



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typical load, count, and inhibit sequences



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS561A			SN74ALS561A			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage			2		2		V		
V _{IL}	Low-level input voltage			0.7		0.8		V		
I _{OH}	High-level output current	Q outputs			-1		-2.6		mA	
		CCO and RCO			-0.4		-0.4			
I _{OL}	Low-level output current	Q outputs			12		24		mA	
		CCO and RCO			4		8			
f _{clock}	Clock frequency			0	20	0	30	MHz		
t _w	Pulse duration	ACLR or ALOAD low			20		15		ns	
		CLK high			20		16.5			
		CLK low			25		16.5			
t _{su}	Setup time before CLK↑	ENP, ENT	High		25		20		ns	
			Low		25		20			
		Data at A, B, C, D			25		20			
		SCLR	Low		21		15			
			High (inactive)		35		30			
		SLOAD	Low		20		15			
			High (inactive)		35		30			
		ACLR or ALOAD inactive			12		10			
t _h	Hold time after CLK↑ for data, ENP, ENT, SCLR, or SLOAD			0		0		ns		
T _A	Operating free-air temperature			-55	125	0	70	°C		

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS561A			SN74ALS561A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2	V
	Q outputs	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.4	3.3			
V _{OL}	Q outputs		I _{OH} = -2.6 mA				2.4	3.2
	CCO and RCO	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA			0.35	0.5	
		V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	
			I _{OL} = 8 mA			0.35	0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			20			20	µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V			-20			-20	µA
I _I	ENP and ENT	V _{CC} = 5.5 V, V _I = 7 V		0.2			0.2	mA
	Other inputs			0.1			0.1	
I _{IH}	ENP and ENT	V _{CC} = 5.5 V, V _I = 2.7 V		40			40	µA
	Other inputs			20			20	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2			-0.2	mA
I _{O‡}	CCO and RCO	V _{CC} = 5.5 V, V _O = 2.25 V		-15	-70	-15	-70	mA
	Q			-20	-112	-30	-112	
I _{CC}	V _{CC} = 5.5 V	Outputs high		17	27	17	27	mA
		Outputs low		21	33	21	33	
		Outputs disabled		22	36	22	36	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 1)

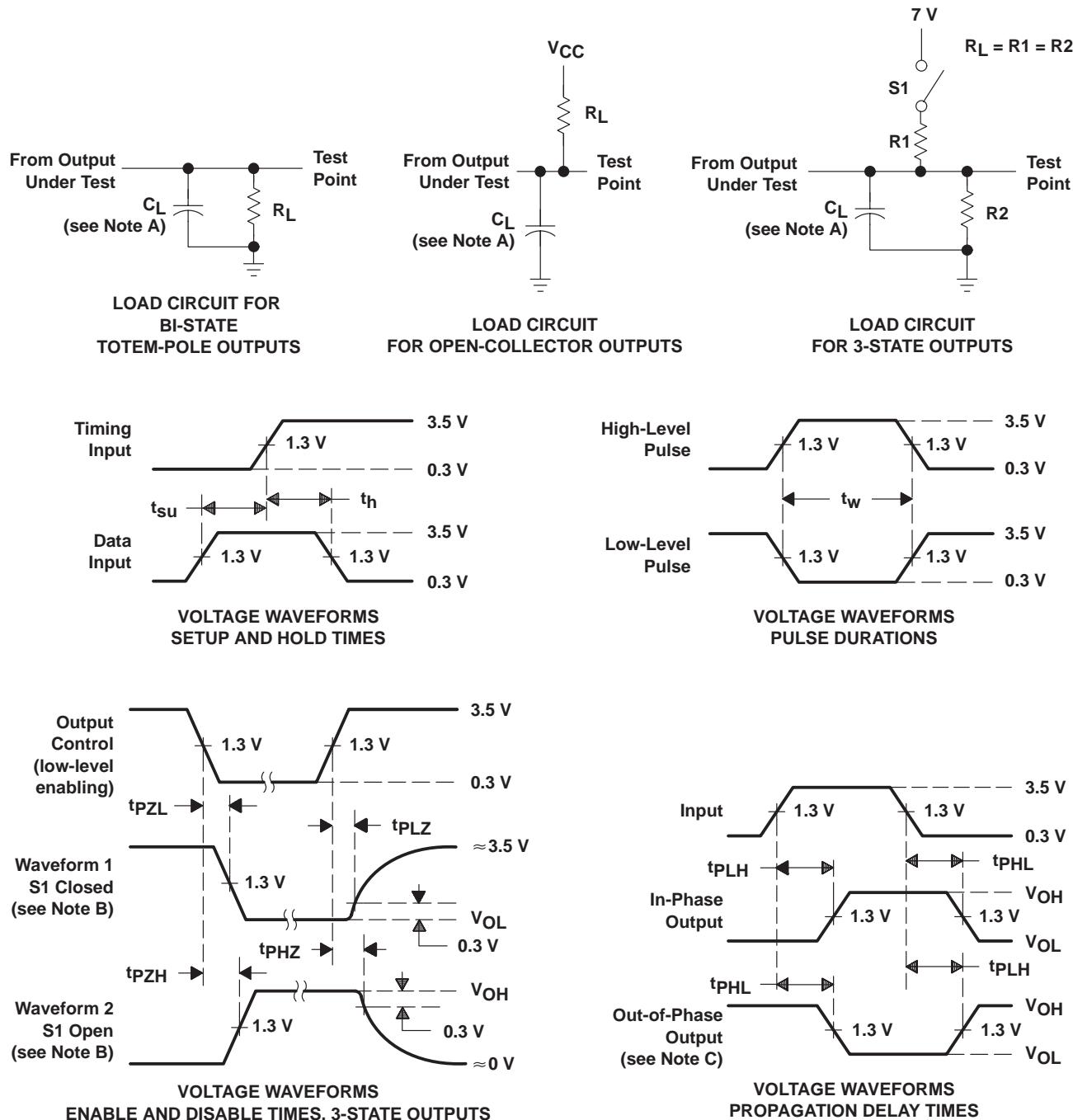
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R1 = 500\text{ }\Omega,$ $R2 = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54ALS561A		SN74ALS561A			
			MIN	MAX	MIN	MAX		
f_{max}			20	30			MHz	
t_{PLH}	CLK	Any Q	4	15	4	12	ns	
t_{PHL}			5	21	5	18		
t_{PLH}	CLK	RCO	9	35	9	29	ns	
t_{PHL}			8	29	8	24		
t_{PLH}	CLK	CCO	8	35	8	26	ns	
t_{PHL}			5	20	5	16		
t_{PLH}	$\overline{\text{ALOAD}}$	Any Q	10	38	10	35	ns	
t_{PHL}			7	27	7	23		
t_{PLH}	$\overline{\text{ALOAD}}$	RCO	15	50	15	40	ns	
t_{PHL}			12	35	12	30		
t_{PLH}	$\overline{\text{ALOAD}}$	CCO	25	65	25	55	ns	
t_{PHL}			12	42	12	33		
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns	
t_{PHL}			7	27	7	22		
t_{PLH}	ENT	RCO	5	20	5	16	ns	
t_{PHL}			4	18	4	14		
t_{PLH}	ENT	CCO	12	35	12	32	ns	
t_{PHL}			4	15	4	12		
t_{PLH}	ENP	CCO	5	22	5	18	ns	
t_{PHL}			4	14	4	12		
t_{PHL}	$\overline{\text{ACLR}}$	Any Q	7	28	7	22	ns	
t_{PZH}	$\overline{\text{OE}}$	Any Q	5	24	5	19	ns	
t_{PZL}			8	28	8	23		
t_{PHZ}	$\overline{\text{OE}}$	Any Q	2	12	2	10	ns	
t_{PLZ}			2	20	4	15		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS561AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS561ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SNJ54ALS561AJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS561A, SN74ALS561A :

- Catalog: [SN74ALS561A](#)
- Military: [SN54ALS561A](#)



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PACKAGE OPTION ADDENDUM

28-Aug-2010

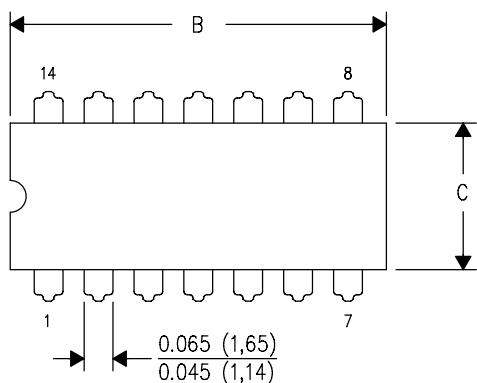
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- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

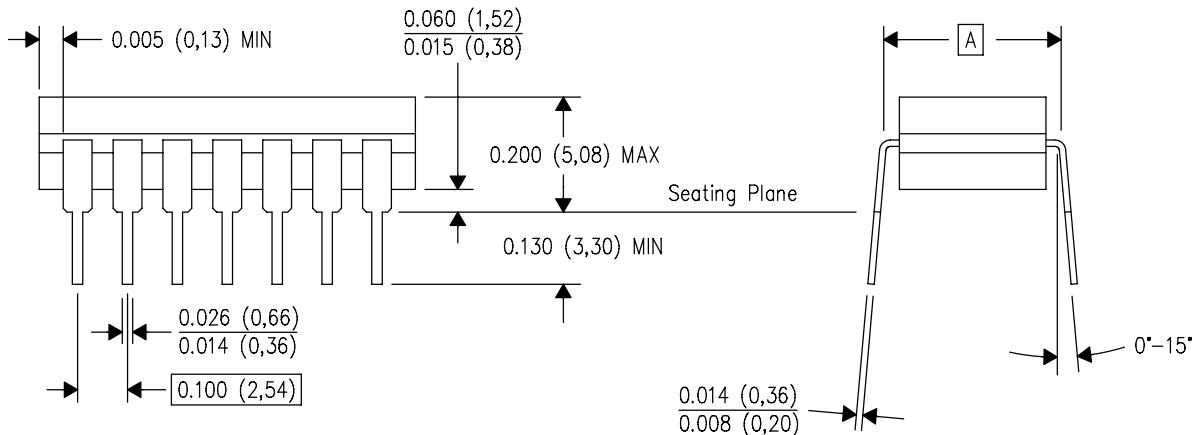
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



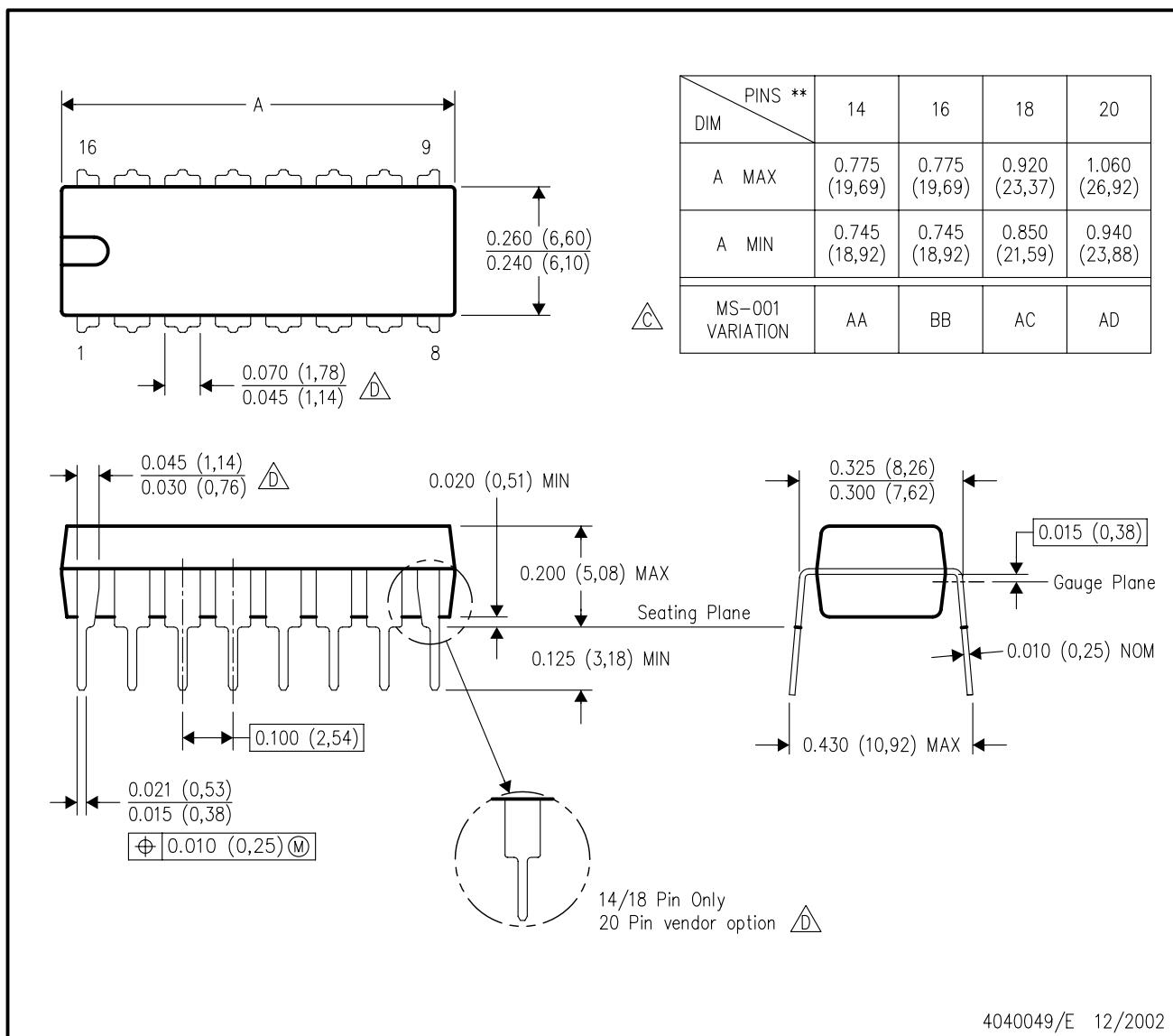
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

Symbol C: Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

Symbol D: The 20 pin end lead shoulder width is a vendor option, either half or full width.

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