ECE 4525/5525 DIGITAL DESIGN
Fall 2025
Prelab Assignment for Lab Eight

Task One

Part 1

Draw a detailed schematic diagram for the test circuit for your implementation of the **SN74ALS561 Synchronous 4-bit Binary Counter with 3-State Outputs**. Your schematics should also include a bounce-free clock circuit. The **CLK output** of your clock circuit should be connected to **Pin 3 of the JB Pmod Header** (MRCC_15 input signal of the Artix-7 FPGA). Use DIP switches and LED Bars on your solderless breadboard to design your **test circuit**. All FPGA input and output signals should be buffered by suitable buffer chips. You should make the other PMod pin assignments. In your schematic diagram the FPGA and the Nexys A7 Board should be represented by those FPGA pin numbers and Pmod Header connector pin numbers, respectively, that are being used.

In addition, develop a VHDL program for the counter, an .xdc file and a proper .tcl file for the implementation of the timing diagram given on Page 4 of the Data Sheets.