ECE 4525/5525
Digital Design Laboratory
Laboratory Eight
Synchronous 4-Bit Counter with 3-State Outputs

Objectives:

i. To develop VHDL code for synchronous sequential circuits

ii. To design a universal counter

iii. To implement 3-State outputs

Task One

1. Devise VHDL code for a circuit that is functionally equivalent to the Synchronous 4-Bit Counter with 3-State Outputs which is specified in the Prelab Assignment, or will be decided by your Lab TA. The specifications for this chip can be found on Texas Instruments Web Site (www.ti.com). The detailed specifications for this lab are given in the Prelab Assignment, or will be decided by your Lab TA. A bounce-free manual clock signal should be implemented on your Breadboard for the counter. The input signals of the counter should be driven by switches and the status of the output signals should be visualized by LEDs on your Breadboard. Run post-route simulations to verify the correct operation of your circuit.

2. Run the implement step and download the configuration bit file to your Nexys 7 Board. The pin assignments for the input and output signals are specified in the Prelab Assignment, or determined by your Lab TA. Again, verify the correct operation.

3. With the help of post-route simulation obtain the key propagation delays of your counter.

Demonstrate these tasks to your Lab TA by short video clips. All circuit designs and tests should be documented by your .vhd, .xdc, ad .do files, the top page of your Project Summary Report and simulation timing diagrams. All VHDL files and simulation timing diagrams should be **commented on for full credit**. **Submit your Lab Report as a single .pdf file**) through the appropriate **Drop Box in Elearning**.