**ECE 4525/5250 DIGITAL DESIGN**
**Fall 2025**
**Prelab Assignment for Lab Three**

**Task One**

| Inputs | Nexys A7 Board |
|---|---|
| A | SW15 |
| B | SW14 |
| | Signals on the Pmod Header JB |
| C0 | JB1 |
| Sel0 | JB2 |
| C1 | JB3 |
| Sel1 | JB4 |
| C2 | JB7 |
| Sel2 | JB8 |
| C3 | JB9 |
| Sel3 | JB10 |
| | Signal on the Pmod Header JA |
| CIN | JB7 |
| Outputs | Signals on the Pmod Header JC |
| SUM | JC1 |
| COUT | JC2 |
| Y0 | JC3 |
| Y1 | JC4 |
| Y2 | JC7 |
| Y3 | JC8 |

Develop VHDL code modules and a proper .tcl file for simulation for Task One. You should also draw a schematic diagram for your circuit. Signals CIN, C0, C1, C2, C3, Sel0, Sel1, Sel2 and Sel3 should be driven using DIP switches on your breadboard. The status of signals SUM, COUT, Y0, Y1, Y2 and Y3 should be displayed using a

bar-LED on your breadboard. All FPGA signals involved should be buffered by suitable buffer chips. The Nexys A7 Board should be represented by FPGA and corresponding JA, JB, and JC Header connector pins only.

**Task Two**

**F = AC + AB + A'C'  [F = f (A, B, C)]**

**1. Stuck-at-1 fault model (A = 1)**

| Inputs | Signals on the Pmod Header JB |
|---|---|
| A | JB7 |
| B | JB8 |
| C | JB9 |

| Outputs | Signals on the Pmod Header JB |
|---|---|
| F | JB1 |
| $F_{alpha}$ | JB3 |

**2. Bridging fault model (A = B)**

Use the pin assignments listed above.

Devise the **two $F_{alpha}$ logic functions** (the functions created by the **two fault models**, respectively, for Parts 1 and 2. Determine the input vectors for Parts 1 and 2, respectively, that can sort out the correct circuits from the ones at fault.

Develop **two** VHDL code modules and proper .tcl files for simulation for Task Two, Parts 1 and 2. You should also draw schematic diagrams for your circuits. Signals A, B and C should be driven using DIP switches on your breadboard. The status of signals F and $F_{alpha}$ should be displayed using a bar-LED on your breadboard. All FPGA signals involved should be buffered by suitable buffer chips. The Nexys A7 Board should be represented by FPGA and corresponding JB Header connector pins only.