ECE4525

Homework 5

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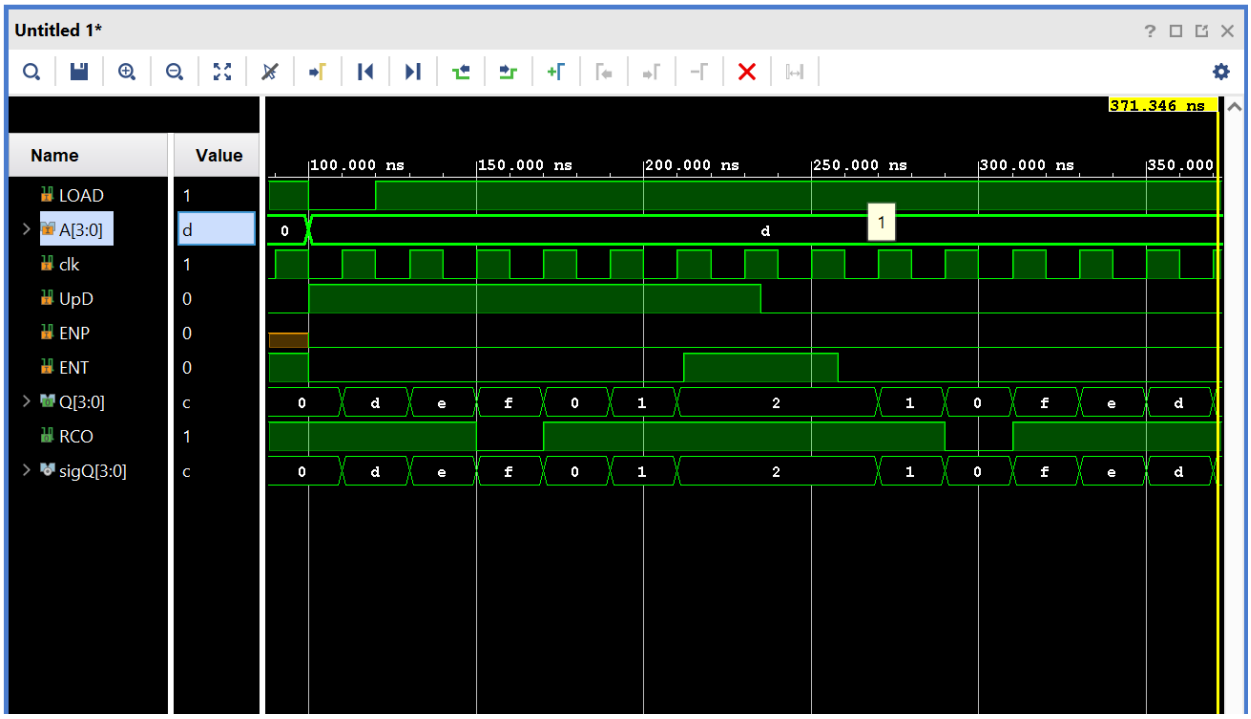
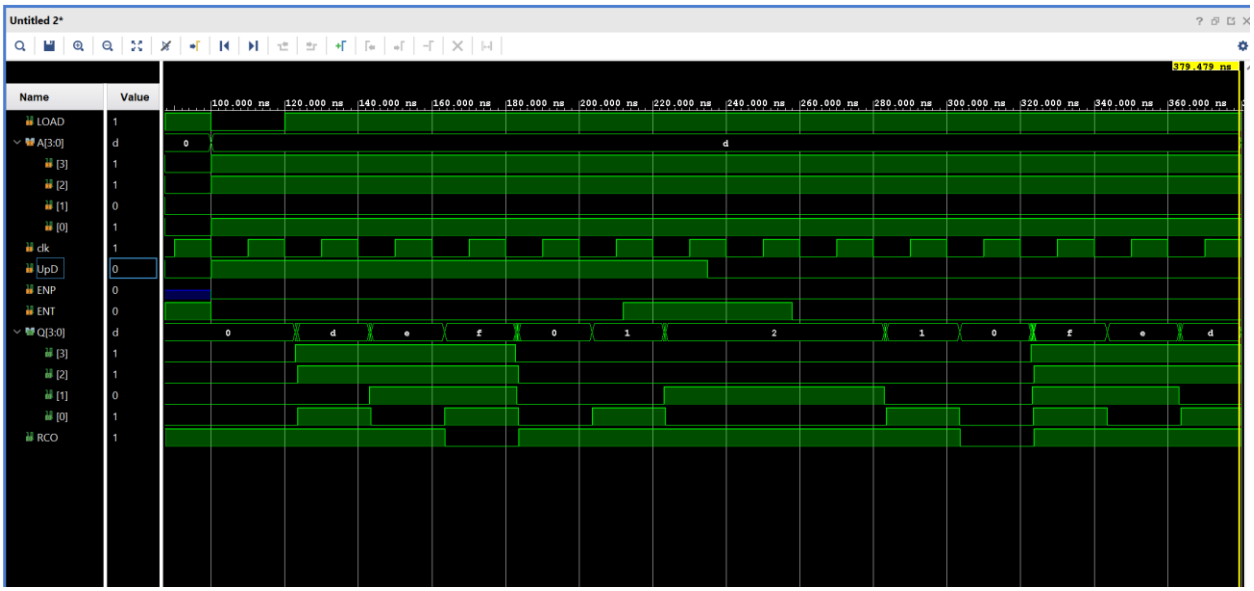
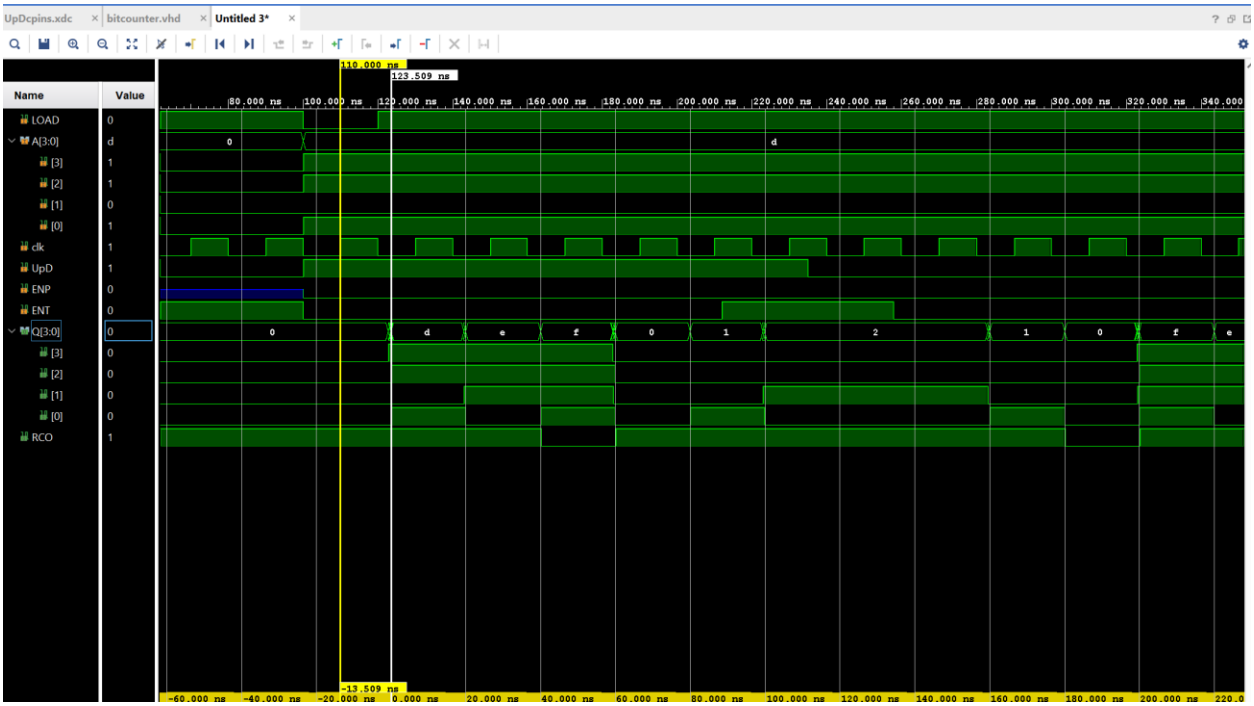
Behavioral simulation



Post route simulation



I used the exact inputs as in the datasheet for abcd, UpD, ENT and ENP input which I have saved as A vector and others. The only difference I seem to face is my inputs are flipped, D is meant to be the most significant bit and I have my D value on the first row under A vector instead of the bottom. There seems to be a delay before the Q outputs



the delay as we can see is 13.509ns, almost a whole cycle(20ns), beside that delay, I made sure to add a long delay in the beginning of the process to ensure the whole process is shown in the simulation. When I delayed 80ns, it still didn't show what I wanted to see, it needed specifically 100ns to show right outputs, similar to datasheet clock diagram.

tcl

```
restart
add_force clk {0 0ns} {1 10ns} -repeat_every 20ns

add_force LOAD {1 0ns}
add_force A {0000 0ns}
add_force UpD {0 0ns}
add_force ENT {1 0ns}
run 100ns

add_force LOAD {0 0ns}
add_force A {1101 0ns}
add_force UpD {1 0ns}
add_force ENT {0 0ns}
add_force ENP {0 0ns}
run 20ns

add_force LOAD {1 0ns}
run 92ns

add_force ENT {1 0ns}
run 23ns

add_force UpD {0 0ns}
run 23ns

add_force ENT {0 0ns}
run 122ns
```

vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity bitcounter is
  Port (
  LOAD, clk, UpD,ENP, ENT: in std_logic;
  A: in unsigned(3 downto 0);
  Q: out unsigned(3 downto 0);
  RCO: out std_logic
  );
end bitcounter;

architecture Behavioral of bitcounter is
signal sigQ: unsigned(3 downto 0):="0000";
begin
process
begin
wait until clk'event and clk = '1';
RCO <= '1';
    if LOAD = '0' then
        sigQ <= A;
    elsif (enp = '0' and ent = '0') then
        if upd = '1' then
            if sigq = "1110" then
                RCO <= '0';
                sigQ <= "1111";
            else
                RCO <= '1';
                sigQ <= sigQ + 1;
            end if;
        else
            if sigQ = "0001" then
                RCO <= '0';
                sigQ <= "0000";
            else
                RCO <= '1';
                sigQ <= sigQ - 1;
            end if;
        end if;
    else
        wait until (enp = '0' and ent = '0');
    end if;
end process;

process(sigQ)
begin
    Q <= sigq;
end process;

end Behavioral;
```

xdc

```
## Clock signal
#set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk]
```

```
#set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }];
#IO_L12P_T1_MRCC_35 Sch=clk100mhz

create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];

##Switches
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [get_ports { A[0] }];
#IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [get_ports { A[1] }];
#IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 } [get_ports { A[2] }];
#IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33 } [get_ports { A[3] }];
#IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN T13 IOSTANDARD LVCMOS33 } [get_ports { ENP }];
#IO_L23P_T3_A03_D19_14 Sch=sw[11]
set_property -dict { PACKAGE_PIN H6 IOSTANDARD LVCMOS33 } [get_ports { ENT }]; #IO_L24P_T3_35
Sch=sw[12]
set_property -dict { PACKAGE_PIN U12 IOSTANDARD LVCMOS33 } [get_ports { UpD }];
#IO_L20P_T3_A08_D24_14 Sch=sw[13]
set_property -dict { PACKAGE_PIN U11 IOSTANDARD LVCMOS33 } [get_ports { LOAD }];
#IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
#set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 } [get_ports { clk }];
#IO_L21P_T3_DQS_14 Sch=sw[15]

## LEDs
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports { Q[0] }];
#IO_L18P_T2_A24_15 Sch=led[0]
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [get_ports { Q[1] }];
#IO_L24P_T3_RS1_15 Sch=led[1]
set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 } [get_ports { Q[2] }];
#IO_L17N_T2_A25_15 Sch=led[2]
set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33 } [get_ports { Q[3] }];
#IO_L8P_T1_D11_14 Sch=led[3]
#set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVCMOS33 } [get_ports { LED[4] }];
#IO_L7P_T1_D09_14 Sch=led[4]
set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [get_ports { RCO }];
#IO_L18N_T2_A11_D27_14 Sch=led[5]
```