ECE 4525/5525 DIGITAL DESIGN

FALL 2025

Homework Assignment #2

Total: 70 pts.

Due 11:30am, Friday, September 19, 2025

You should develop a behavioral **VHDL** code for a **chip** that is **functionally equivalent** to the **TI SN74ALS151 1-of-8 Data Selectors/Multiplexers** circuit. In your program work with a "**process**" structure along with "**case**" statements. Use the available **AMD/Xilinx Vivado tools to design, simulate and map** your circuit to a **Xilinx Artix-A7 FPGA** chip (the **one** which is mounted on your **Nexys A7 Board**). The **Data Sheets** for the SNALS151 chip can be found on **Texas Instrument**'s Web Page (www.ti.com). You **don't** have to implement the **propagation delays** given in the Data Sheets.

a) Turn in an electronic copy of the **.vhd** file for your design. (30 pts.)

b) **Map** your design to the FPGA chip specified above by running the **Implement** step. **Add** a **customized version of the Nexys A7.xdc file** to your project files such that **all inputs** are assigned to **switches** and **all outputs** are assigned to **LEDs**. You make your **own choices** in assigning your inputs and outputs.
Turn in an **electronic copy of your .xdc file** and **only the top page** of the **Project Summary Report**. (20 pts.)

c) Develop a **script** (**.tcl file**) to verify the correct operation of your circuit as defined by its Function Table in the Data Sheets. You are **not required to create a fully exhaustive test regime**. Run the **post-route simulations**. Turn in an electronic copy of your **.tcl** file along with an electronic copy of the **simulation waveforms**. **Comment on** the simulation results for full credit. (20 pts.)

Fall back position: turn in electronic copies of your **.vhd**, **.xdc** and **.tcl** files along with comments for partial credit if you couldn't compile your design due to some fatal error.

Electronic submission: submit your **single .pdf** file through the **appropriate Dropbox in eLearning**.

Bonus Assignment #2

Total: 30 pts.

Due 11:30am, Friday, September 19, 2025

Generate the **.bit** file and download it to your Nexys A7 Board. **Prototype** your circuit design by manually repeating the test vectors you have used for simulations. **Create a narrated, short video clip** (**mp4** file, up to **4mins**) to illustrate that your circuit works. Submit the mp4 file through the **appropriate Dropbox in eLearning**.