module counter (

input [7:0] x,

input clk, reset,

output reg [7:0] y);

reg [7:0] r\_reg, r\_next;

always @(posedge clk, posedge reset)

if (reset)

r\_reg <= 8'b0;

else

r\_reg <= r\_next;

always@\*

if(r\_reg<x)

r\_next=r\_reg+1;

else

r\_next=x;

always@\*

y=r\_reg;

endmodule