

MX25R Extend in FSP

Rev. 1.1.0, 2023-04-24

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Introduction

Macronix MX25R series nor Flash has 3 power modes: HighPerformance Mode, LowPower Mode and DeepPowerDown Mode. However, if you want to control MX25R flash in Renesas FSP platform, you can not easily change the powermode. The MX25R Extend module based on QSPI module can provide some specific functions as follows:

- MX25R_HighPerformanceMode()
- MX25R_LowPowerMode()
- MX25R_Enter_DeepPower()
- MX25R_Exit_DeepPower()
- MX25R_Device_Reset()
- RDID()
- RDSR()
- RDSCUR()
- RDCR()

1 Hardware and Software Requirements

The RWWEE is developed and tested on Renesas RA6M3 board. User can select the same platform for quick start. The onboard NOR flash is MX25L series flash. It is recommended to add a new MX25R flash with QSPI's another CS channel (RA6M3 QSPI controller has two CS channel and can access two devices).

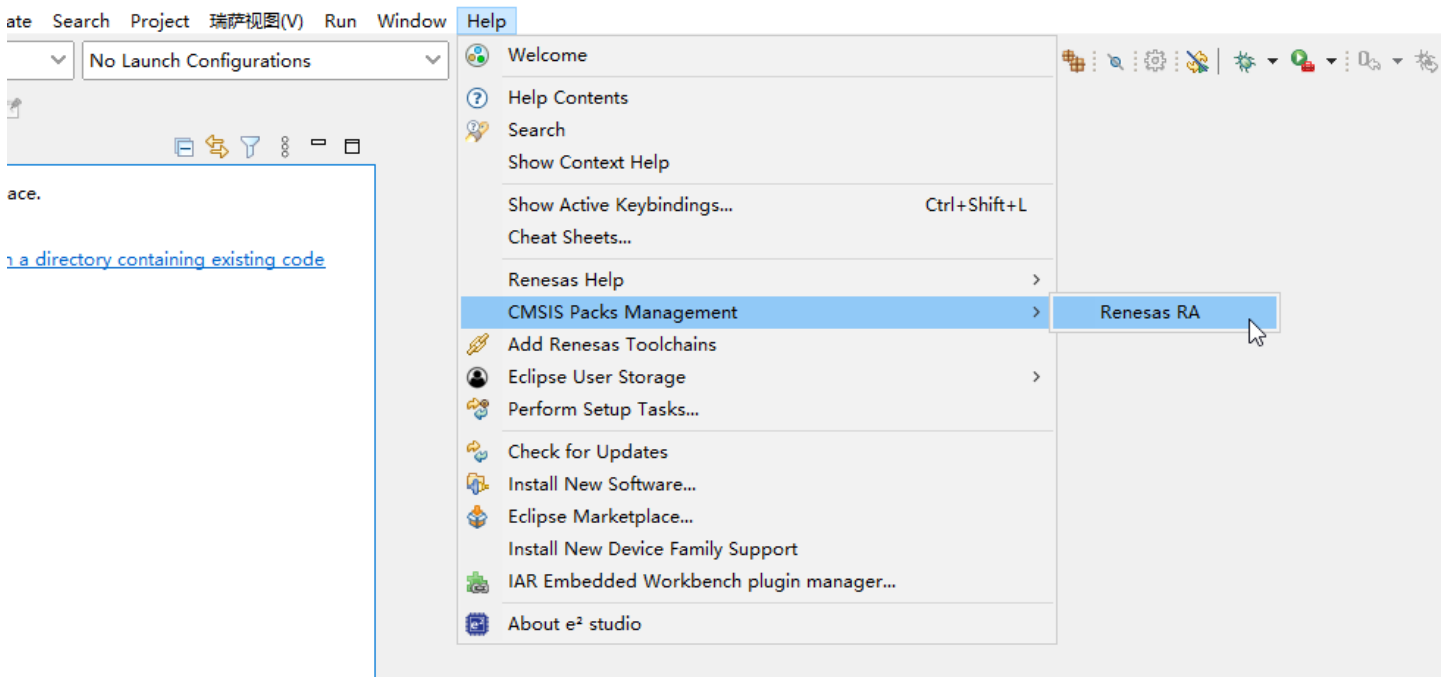
Please check if your environment can satisfy the following requirements:

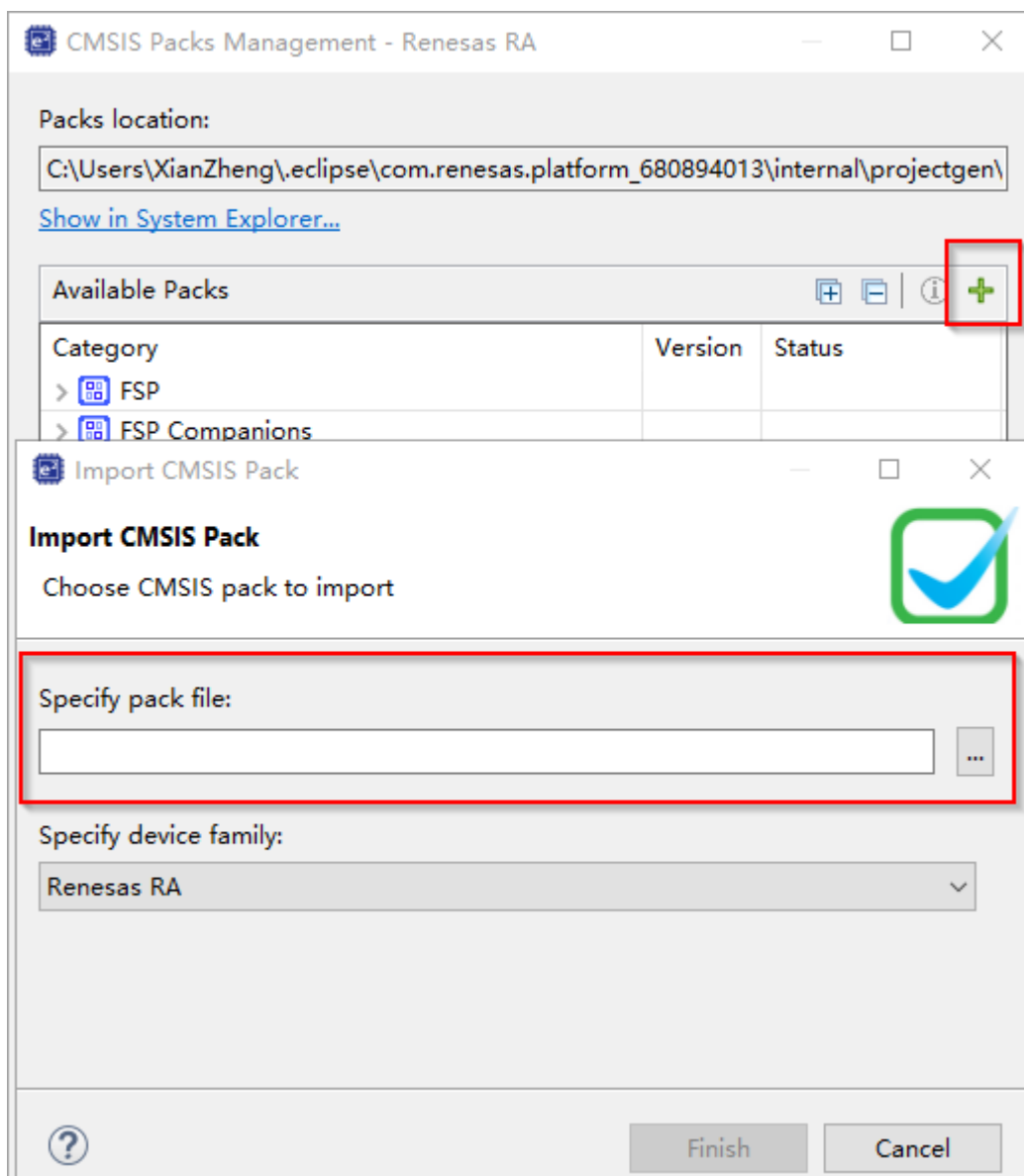
- Renesas RA6M3 Board (with MX25R flash)
- Renesas Flexible Software Package (FSP)
- J-Link RTT Viewer
- MX25R Extend Modulepack: **MXIC.MX25R_Extend.1.0.0+fsp.4.0.0.pack**
- MX25R_Extend_Sample_Project

2 Work Flow

3.1 Preparation

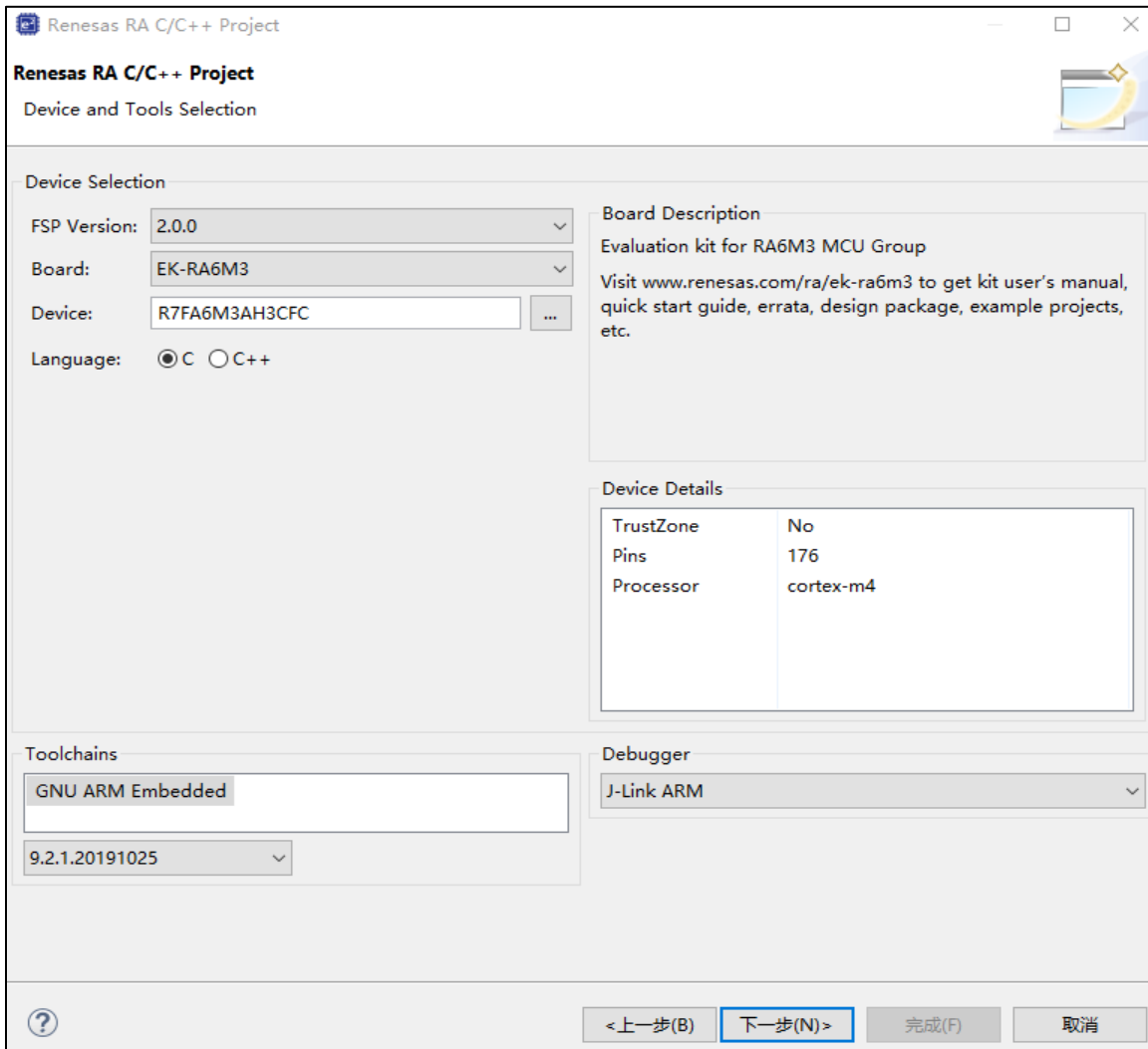
We assume that FSP is installed successfully, so you should import the pack as follows.





3.2 Build Project

Open e2studio and build a new project, here we choose **Renesas RA C/C++ Project** and device select **EK-RA6M3**:



Renesas RA C/C++ Project
Device and Tools Selection

Device Selection

FSP Version: 2.0.0
Board: EK-RA6M3
Device: R7FA6M3AH3CFC
Language: ☒ C ☐ C++

Board Description
Evaluation kit for RA6M3 MCU Group
Visit www.renesas.com/ra/ek-ra6m3 to get kit user's manual, quick start guide, errata, design package, example projects, etc.

Device Details

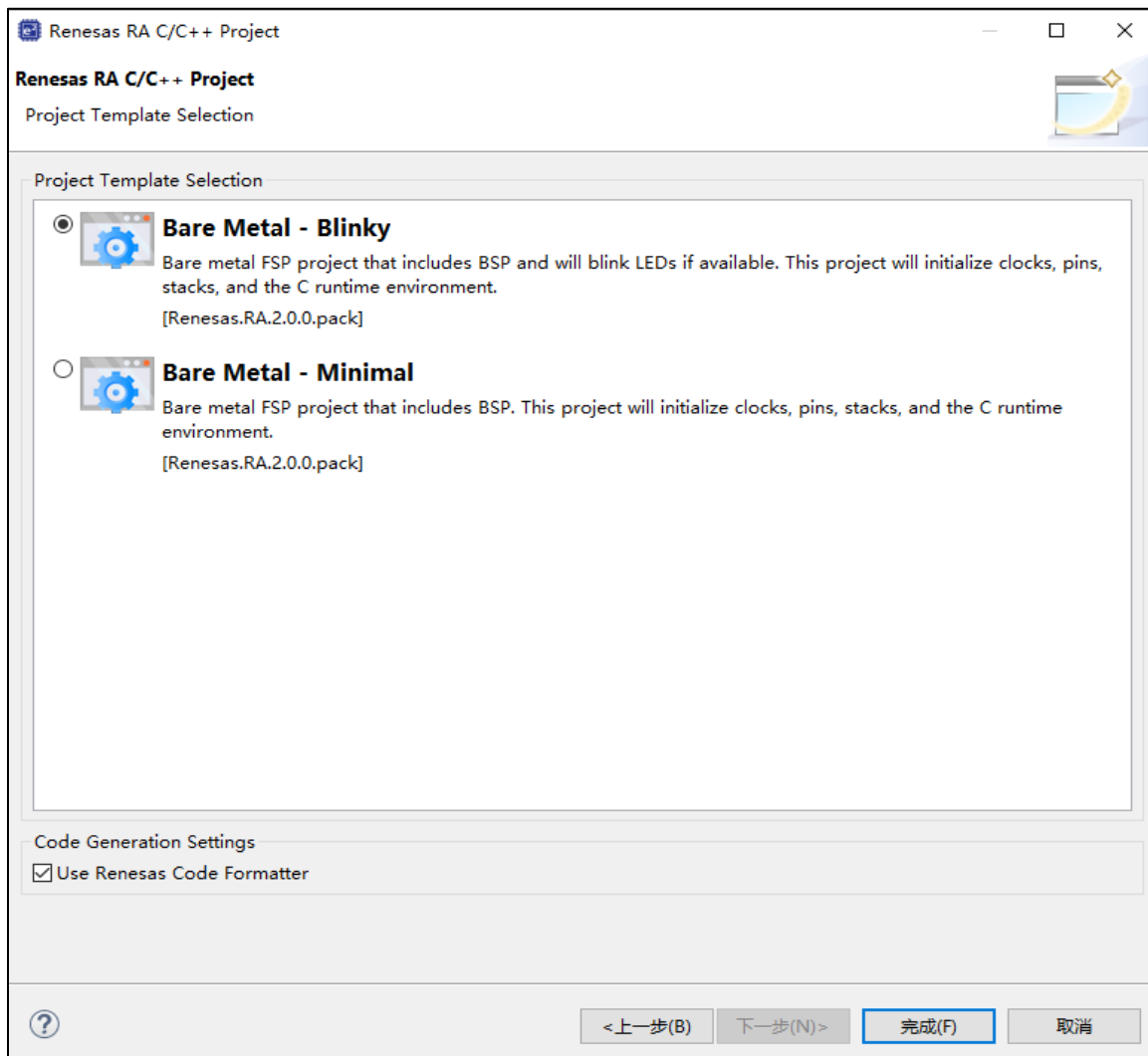
TrustZone	No
Pins	176
Processor	cortex-m4

Toolchains
GNU ARM Embedded
9.2.1.20191025

Debugger
J-Link ARM

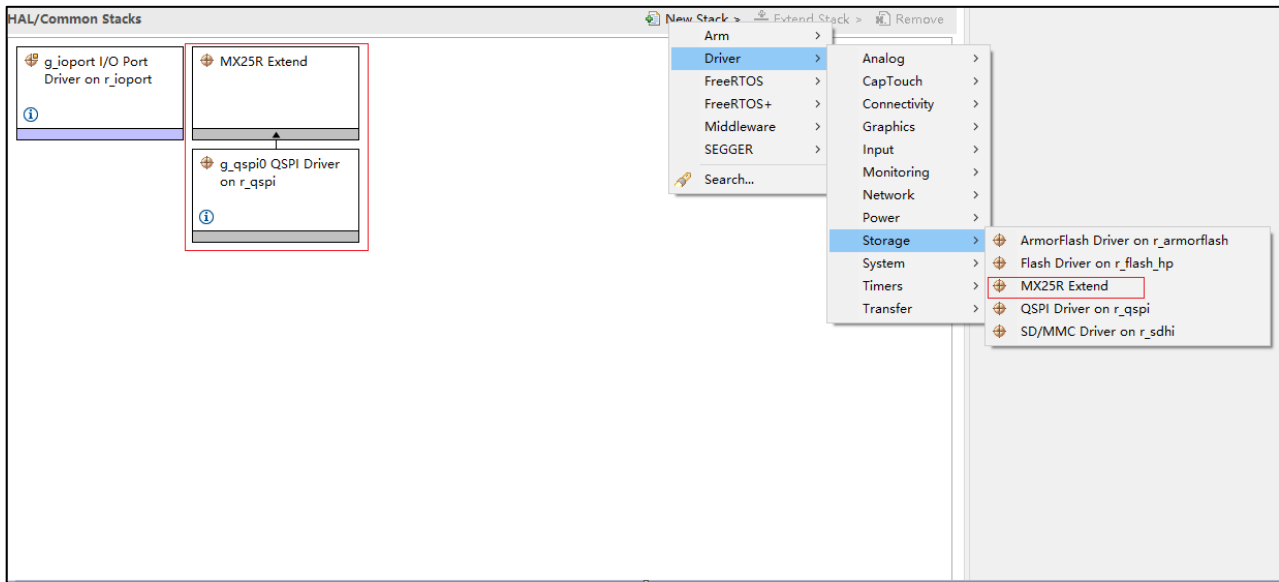
< 上一步(B) 下一步(N) > 完成(F) 取消

Then we can select **Bare Metal – Blinky** as a template:



3.3 Add Modules and set Parameters

After build project, you should add MX25 Extend module as the follow picture: **New Stack->Driver->Storage->MX25R Extend.**



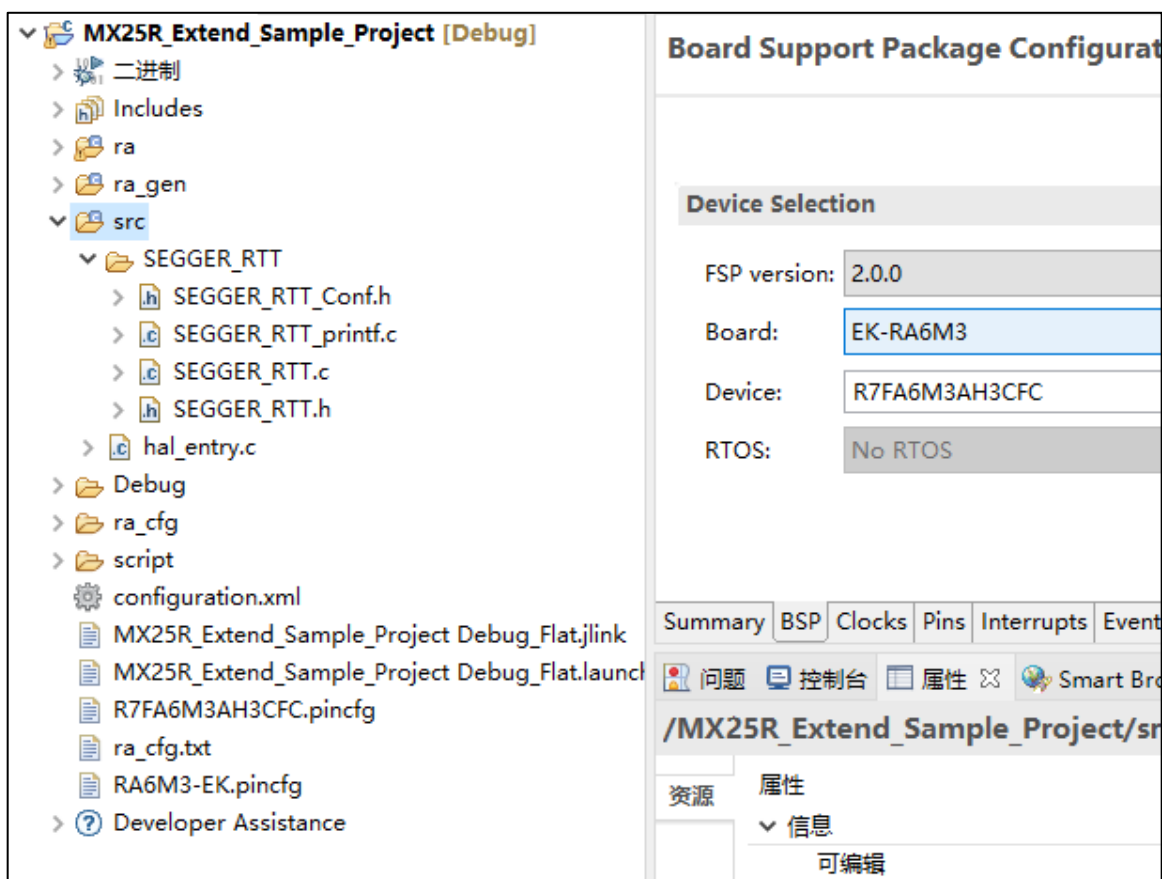
After add MX25R Module, you should set correct pins according to actual connection.

Settings	属性	值
API Info	▼ Common	
	Parameter Checking Enable	Default (BSP)
	Support Multiple Line Program in Extended SPI Mode	Disabled
	▼ Module g_qspi0 QSPI Driver on r_qspi	
	> General	
	> Command Definitions	
	> Bus Timing	
	▼ Pins	
	QSPCLK	P305
	QSSL	P207
	QIO0	P307
	QIO1	P308
	QIO2	P309
	QIO3	P310

Finally, you should set **Heap size** in **BSP->Properties**(To generate random data for testbench), then save the changes and click **Generate Project Content** button to generate code.

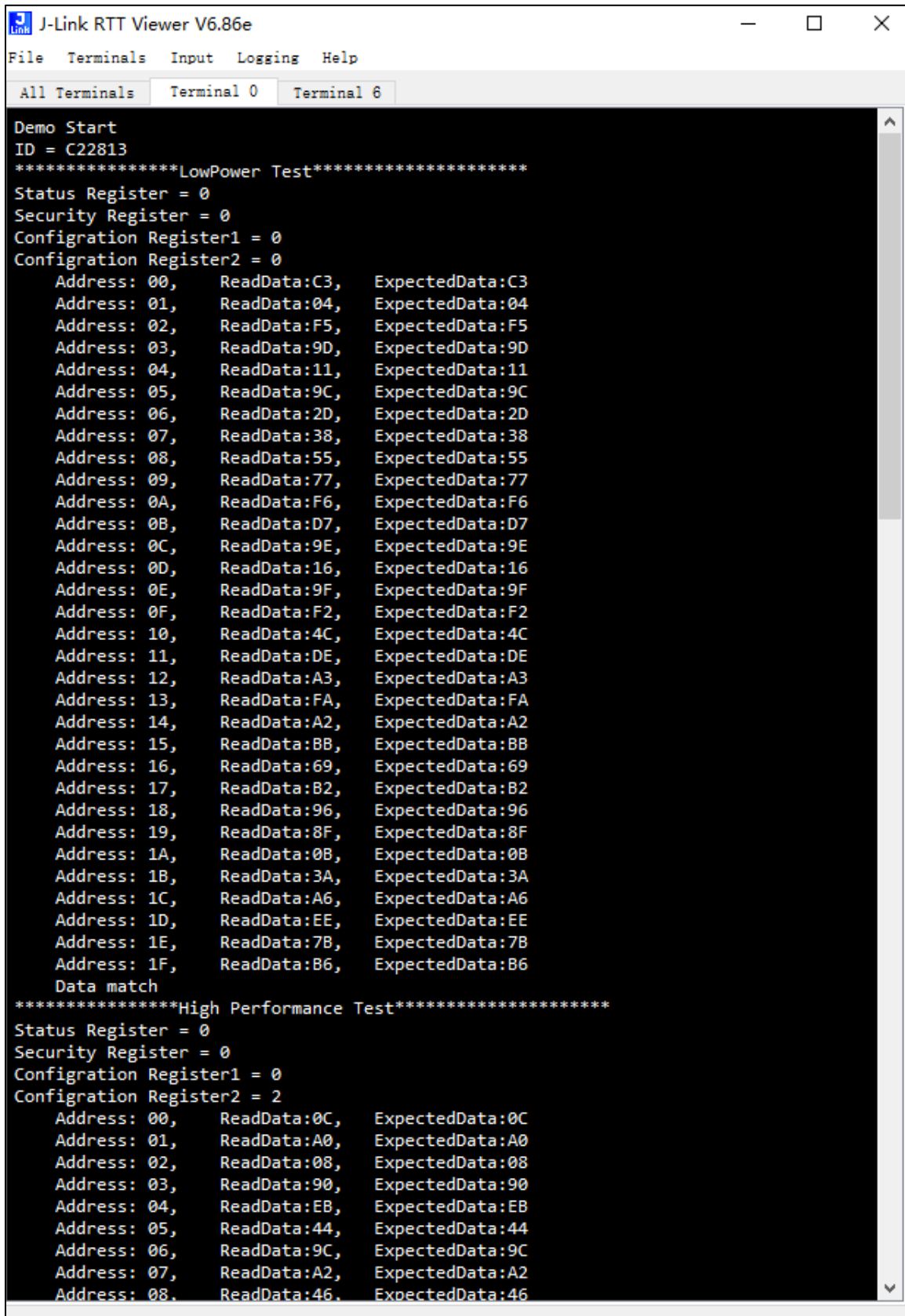
3.4 Add Testbench

You can copy **SEGGER_RTT** folder and **hal_entry.c** from **MX25R_Extend_Sample_Project** and paste to **src** folder. Then, you should click the hammer button to build the project.



3 Run Demo

Download the code to develop board, and then connect to J-Link RTT Viewer.



```

J-Link RTT Viewer V6.86e
File Terminals Input Logging Help
All Terminals Terminal 0 Terminal 6

Demo Start
ID = C22813
*****LowPower Test*****
Status Register = 0
Security Register = 0
Configuration Register1 = 0
Configuration Register2 = 0
  Address: 00,   ReadData:C3,   ExpectedData:C3
  Address: 01,   ReadData:04,   ExpectedData:04
  Address: 02,   ReadData:F5,   ExpectedData:F5
  Address: 03,   ReadData:9D,   ExpectedData:9D
  Address: 04,   ReadData:11,   ExpectedData:11
  Address: 05,   ReadData:9C,   ExpectedData:9C
  Address: 06,   ReadData:2D,   ExpectedData:2D
  Address: 07,   ReadData:38,   ExpectedData:38
  Address: 08,   ReadData:55,   ExpectedData:55
  Address: 09,   ReadData:77,   ExpectedData:77
  Address: 0A,   ReadData:F6,   ExpectedData:F6
  Address: 0B,   ReadData:D7,   ExpectedData:D7
  Address: 0C,   ReadData:9E,   ExpectedData:9E
  Address: 0D,   ReadData:16,   ExpectedData:16
  Address: 0E,   ReadData:9F,   ExpectedData:9F
  Address: 0F,   ReadData:F2,   ExpectedData:F2
  Address: 10,   ReadData:4C,   ExpectedData:4C
  Address: 11,   ReadData:DE,   ExpectedData:DE
  Address: 12,   ReadData:A3,   ExpectedData:A3
  Address: 13,   ReadData:FA,   ExpectedData:FA
  Address: 14,   ReadData:A2,   ExpectedData:A2
  Address: 15,   ReadData:BB,   ExpectedData:BB
  Address: 16,   ReadData:69,   ExpectedData:69
  Address: 17,   ReadData:B2,   ExpectedData:B2
  Address: 18,   ReadData:96,   ExpectedData:96
  Address: 19,   ReadData:8F,   ExpectedData:8F
  Address: 1A,   ReadData:0B,   ExpectedData:0B
  Address: 1B,   ReadData:3A,   ExpectedData:3A
  Address: 1C,   ReadData:A6,   ExpectedData:A6
  Address: 1D,   ReadData:EE,   ExpectedData:EE
  Address: 1E,   ReadData:7B,   ExpectedData:7B
  Address: 1F,   ReadData:B6,   ExpectedData:B6
Data match
*****High Performance Test*****
Status Register = 0
Security Register = 0
Configuration Register1 = 0
Configuration Register2 = 2
  Address: 00,   ReadData:0C,   ExpectedData:0C
  Address: 01,   ReadData:A0,   ExpectedData:A0
  Address: 02,   ReadData:08,   ExpectedData:08
  Address: 03,   ReadData:90,   ExpectedData:90
  Address: 04,   ReadData:EB,   ExpectedData:EB
  Address: 05,   ReadData:44,   ExpectedData:44
  Address: 06,   ReadData:9C,   ExpectedData:9C
  Address: 07,   ReadData:A2,   ExpectedData:A2
  Address: 08,   ReadData:46,   ExpectedData:46
  
```

4 Revision History

Table 8-1: Revision History

Revision No.	Description	Page	Date
Rev. 1.0.0	Initial Release	ALL	April 13, 2021
Rev. 1.1.0	Update	4	April 24, 2023



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