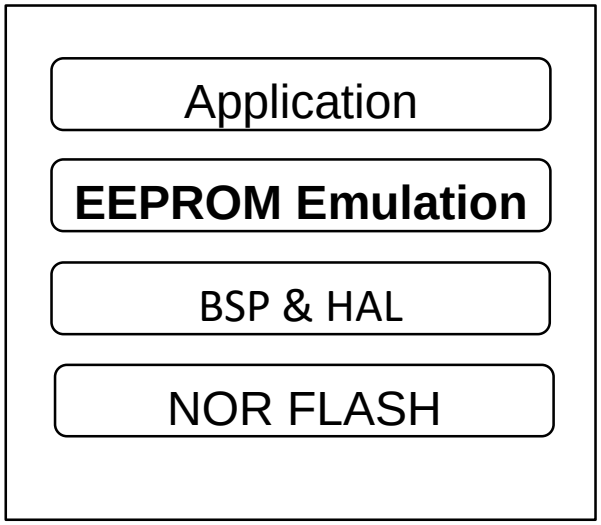
MACRONIX

MXIC vEE Introduction

2022.12

MXIC vEE Introduction

- MXIC vEE(virtual EEPROM Emulation) propose an algorithm and system architecture for implementing the EEPROM emulation on a Read-While-Write flash memory. It support to run read and write/erase operations simultaneously in multi-threaded and real-time environment. It gains about 20% increase on overall read/write performance.

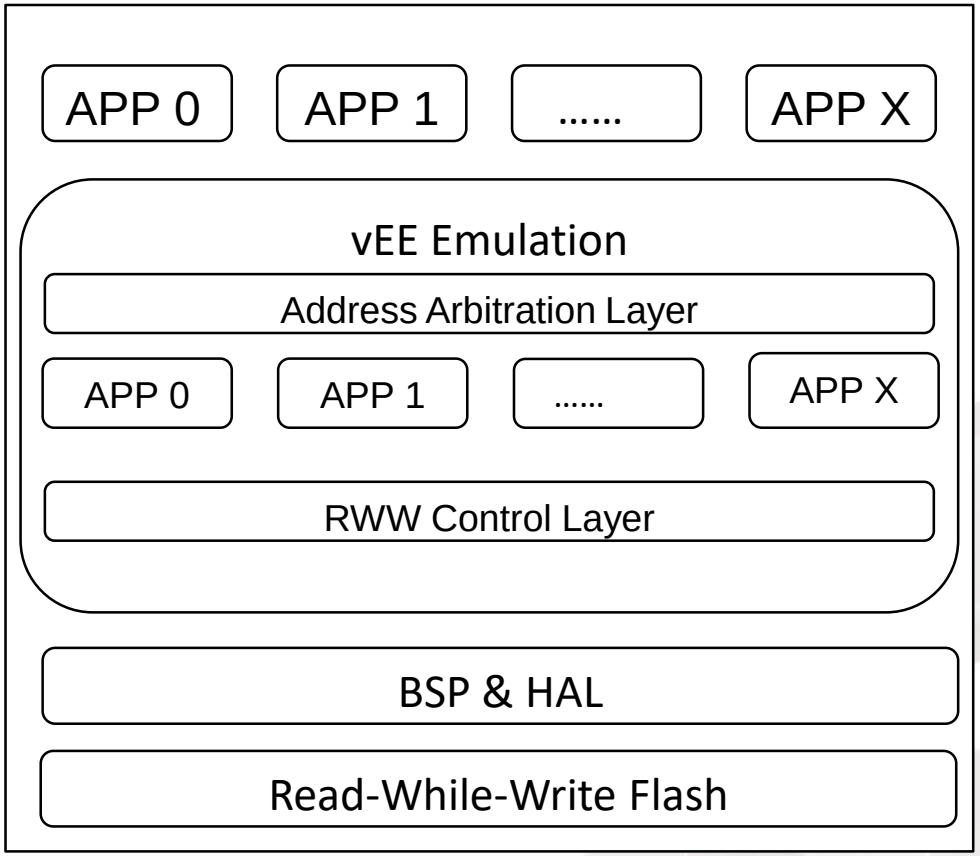


An EEPROM emulation is implement as a flash translation management layer on a NOR flash memory.
An application issues a request to the vEE, which manages to fine a target physical location in the flash and executes the requesting operation via BSP&HAL layer.

MXIC vEE Introduction

When using RWW OctaFlash, our vEE has actually achieved 20% overall performance improvement, referring to vEE's system architecture. There are three layers:

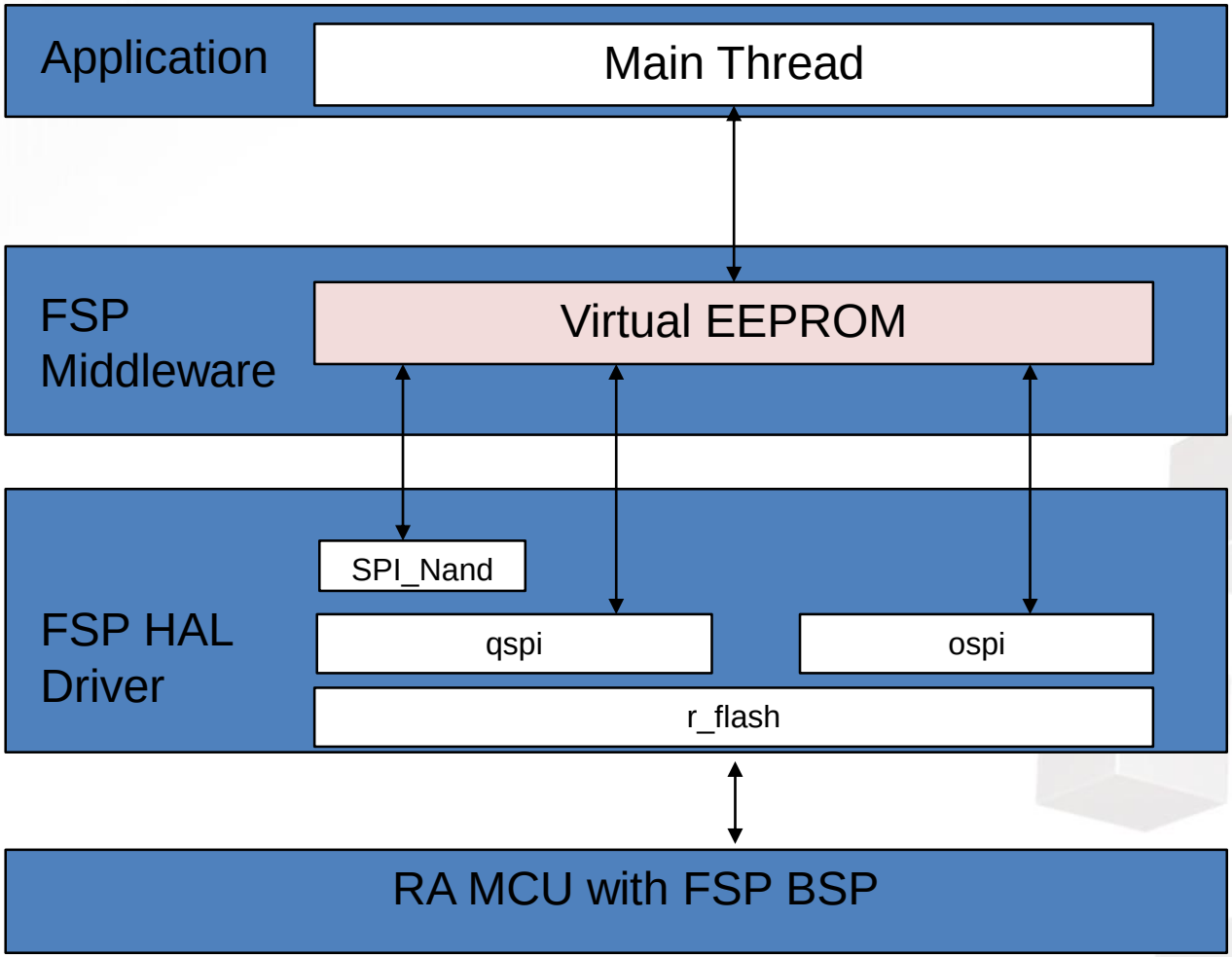
1) Address Arbitration Layer: it distributes user logical addresses into different flash memory banks to enhance parallelism of running read and write/erase operations.
2) EEPROM Emulation Layer: RWWEE is viewed as a set of identical small EEPROMs and this layer manges each of them independently.
3) RWW Control Layer: it is responsible for multi-threading management and RWW timing control.



MXIC vEE Introduction

- Although vEE is suit for Read-While-Write(RWW) Flash, it can also work on normal NOR flash by disabling the RWW feature.
- Now, MXIC vEE is suit for QSPI Nor Flash(MX25 series),OSPI Nor flash(MX25LW/MX25LM series) and SPI Nand Flash(MX31series)
- For more detail, please refer to <Read-While-Write EEPROM Emulation Introduction (FSP Version)>

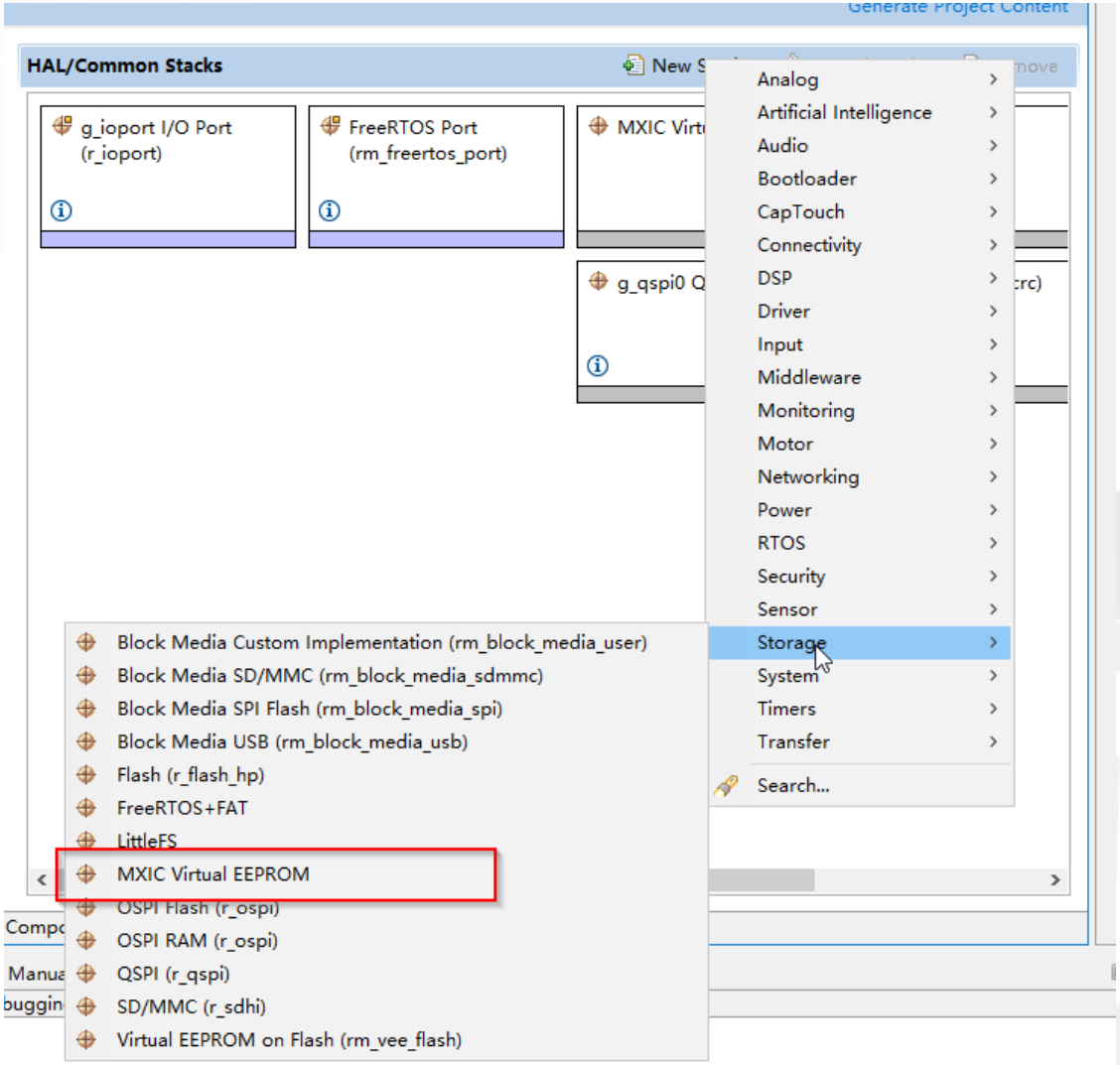
vEE Layer


Application
Main Thread
FSP
Middleware
Virtual EEPROM
FSP HAL
Driver
SPI_Nand
qspi
ospi
r_flash
RA MCU with FSP BSP

Required Resources

- MXIC vEE module pack file
- Renesas FSP v4.0 or later
- RA6M4 Development Board

MXIC vEE Module



vEE Configuration for Nor Flash

MXIC Virtual EEPROM

Settings

Property	Value
Common	
Parameter Checking	Default (BSP)
Select Flash Type	QSPI Normal Nor Flash
Select Controller	QSPI
PC_Protection	Disabled
CRC	Disabled
Read_Rollback	Disabled
Background	Disabled
ECC Check(Only for OctaFlash)	Disabled
Select Hash Type	MX_EEPROM_HASH_SEQUENTIAL
MX_FLASH_CHUNK_SIZE	0x10
MX_FLASH_PAGE_SIZE	0x100
MX_FLASH_SECTOR_SIZE	0x1000
MX_FLASH_BLOCK_SIZE	0x10000
MX_FLASH_BANK_SIZE	0x400000
MX_FLASH_TOTAL_SIZE	0x1000000
MX_EEPROM_BANKS	4
MX_EEPROM_CLUSTERS_PER_BANK	1
MX_EEPROM_SECTORS_PER_CLUSTER	16
MX_EEPROM_FREE_SECTORS	1
MX_EEPROM_ENTRY_SIZE	256
BANK_OFFSET	{0x000000, 0x400000, 0x800000, 0xc00000}
Module MXIC Virtual EEPROM	
Name	g_mx_vee0

vEE Configuration for SPI_Nand Flash

MXIC Virtual EEPROM

Settings

Property	Value
Common	
Parameter Checking	Default (BSP)
Select Flash Type	SPI_Nand Flash(Use QSPI_CONTROL)
Select Controller	QSPI
PC_Protection	Disabled
CRC	Disabled
Read_Rollback	Disabled
Background	Disabled
ECC Check(Only for OctaFlash)	Disabled
Select Hash Type	MX_EEPROM_HASH_SEQUENTIAL
MX_FLASH_CHUNK_SIZE	0x10
MX_FLASH_PAGE_SIZE	512
MX_FLASH_SECTOR_SIZE	0x1000
MX_FLASH_BLOCK_SIZE	0x10000
MX_FLASH_BANK_SIZE	0x1000000
MX_FLASH_TOTAL_SIZE	0x4000000
MX_EEPROM_BANKS	4
MX_EEPROM_CLUSTERS_PER_BANK	1
MX_EEPROM_SECTORS_PER_CLUSTER	16
MX_EEPROM_FREE_SECTORS	1
MX_EEPROM_ENTRY_SIZE	512
BANK_OFFSET	{0x000000, 0x4000000, 0x8000000, 0xc000000}
Module MXIC Virtual EEPROM	
Name	g_mx_vee0

vEE Configure Introduction

- Select Flash Type:
  Here we have four choices
  (1) QSPI Normal Nor Flash
  (2) QSPI Normal Nor Flash
  (3) QSPI RWW Nor Flash
  (4) SPI Nand Flash

- Select Controller:
  Here we can select QSPI or OSPI controller.

SPI Nand Flash is Nand flash but it can act like a Nor Flash.

QSPI/OSPI Normal Flash and SPI_Nand Flash(MX25 series)can achieve all functions.

OSPI RWW Flash can realize the Read-While-Write function in vEE.

User should choose the correct type of flash according to the actual situation.

vEE Configure Introduction

OSPI RWW Nor Flash has add RWW function comparing to OSPI Normal Flash functions.

If your flash is RWW Flash but you don’t want to use rww function, please choose OSPI Normal Nor Flash.

OSPI module’s clock should not exceed 50MHz in OSPI default setting or Command interval setting set a higher value(Command interval time exceed 40ns).

vEE Configure Introduction

- PC_Protection:

  Handle insufficient erase by sudden power cycling.

- CRC:

  Enable or Disable CRC check, if you enable crc, you should add crc module.

- Read_Rollback:

  Try to recover the old version of user data if any read error happens.

- Background:

  Put some time-consuming task to background thread to improve the response time of user request.

vEE Configure Introduction

- Select Hash Type
- MX_FLASH_CHUNK_SIZE
- MX_FLASH_PAGE_SIZE
- MX_FLASH_SECTOR_SIZE
- MX_FLASH_BLOCK_SIZE
- MX_FLASH_BANK_SIZE
- MX_FLASH_TOTAL_SIZE
- MX_EEPROM_BANKS
- MX_EEPROM_CLUSTERS_PER_BANK
- MX_EEPROM_SECTORS_PPER_CLUSTER
- MX_EEPROM_FREE_SECTORS
- MX_EEPROM_ENTRY_SIZE
- BANK_OFFSET

Please refer to <Read-While-Write EEPROM Emulation Introduction (FSP Version)> for all the above items.

vEE Configure Introduction

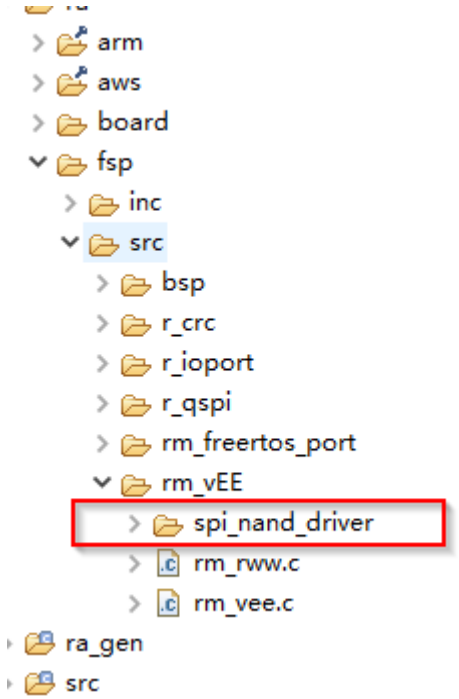
- User can use the default settings or modify the settings according to the actual Flash, ,or use the default value.

- The MX_BANK_SIZE is unique to RWW Flash(Please refer to Octa RWW Flash datasheet), but here can also be used in Normal Flash, we can artificially divide the whole chip into multiple banks and build vEE Emulation on it.

vEE Configure Introduction

- In SPI_Nand, It is a little different from nor flash:

(1)For SPI_Nand Flash, the typical value of page size is 0x800, block size is 0x20000 and sector size is ignore. In addition, MX_EEPROM_ENTRY_SIZE is 512, and BANK_OFFSET interval is 0x4000000(eg.{0x80000, 0x4080000, 0x8080000, 0xc080000}).
(2) Actually, the 'MX_FLASH_PAGE_SIZE' is 2048, however, one page can only write four times, so in vEE, we set it 512.
(3)The vEE will ignore 'MX_FLASH_SECTOR_SIZE' cause SPI_Nand don't have sectors.
(4)The 'MX_EEPROM_ENTRY_SIZE' is 512.
(5)The 'BANK_OFFSET' can refer the picture above or SPI_Nand datasheet.



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