Flash Power Manage in FSP

Rev. 1.2.0, 2023-12-1

Contents

Introduction

Usually, Nor Flash has more than one power mode, such as Normal mode and DeepPowerDown, but in FSP, it is not very easy to change Flash power mode, In this application, we introduce a middleware to manage Flash Powe rmode, and take MX25R as an example for interpretation. The Power Manage Middleware just offers some interfaces and the Flash vender should realize the interfaces according to related rules:

- power_init ()
- setNormalMode ()
- setHighPerformanceMode ()
- setLowPowerMode ()
- setSuperLowPowerMode ()
- setDeepPowerDownMode ()

power_init() is used to do some initialization work, and then vender should select some power mode according to actual Flash. Finally, the other power should return NOT_SUPPORT;

1 Hardware and Software Requirements

The RWWEE is developed and tested on Renesas RA6M3 board. User can select the same platform for quick start. The onboard NOR flash is MX25L series flash. It is recommended to add a new MX25R flash with QSPI's anther CS channel (RA6M3 QSPI controller has two CS channel and can access two devices).

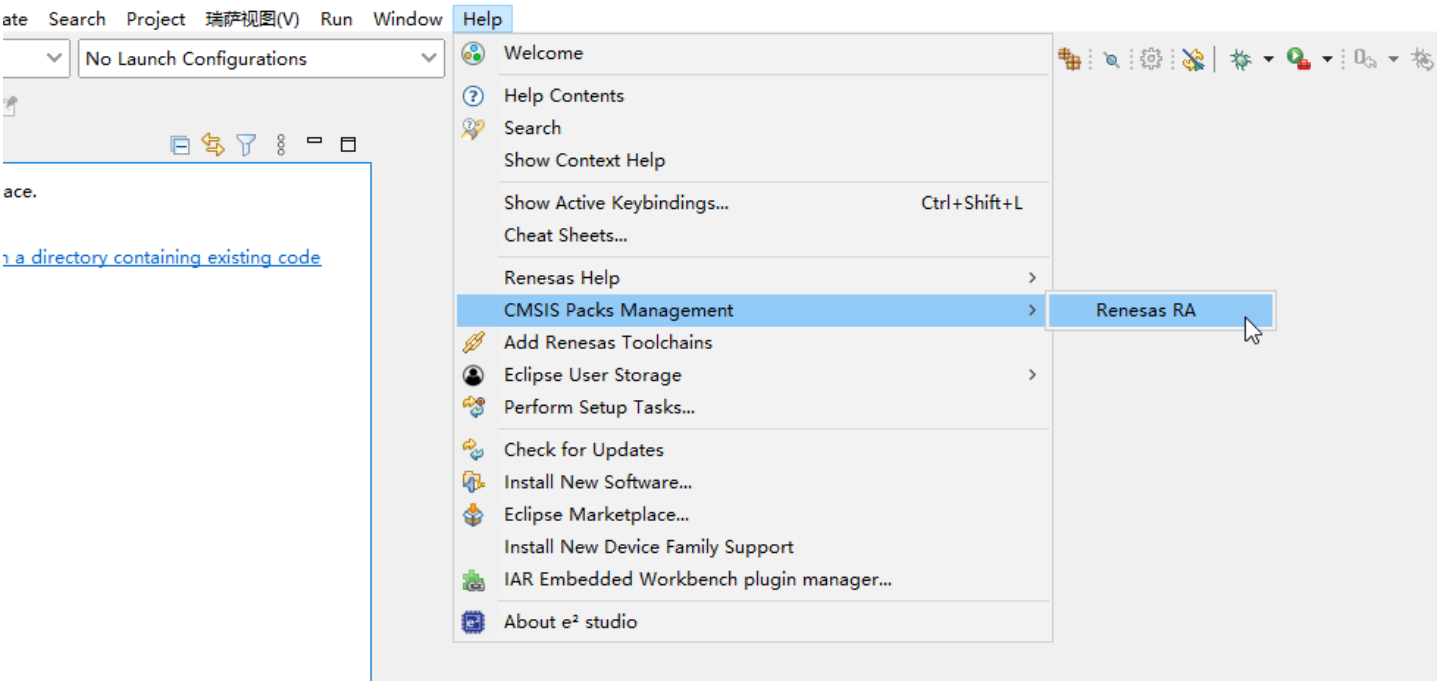
Please check if your environment can satisfy the following requirements:

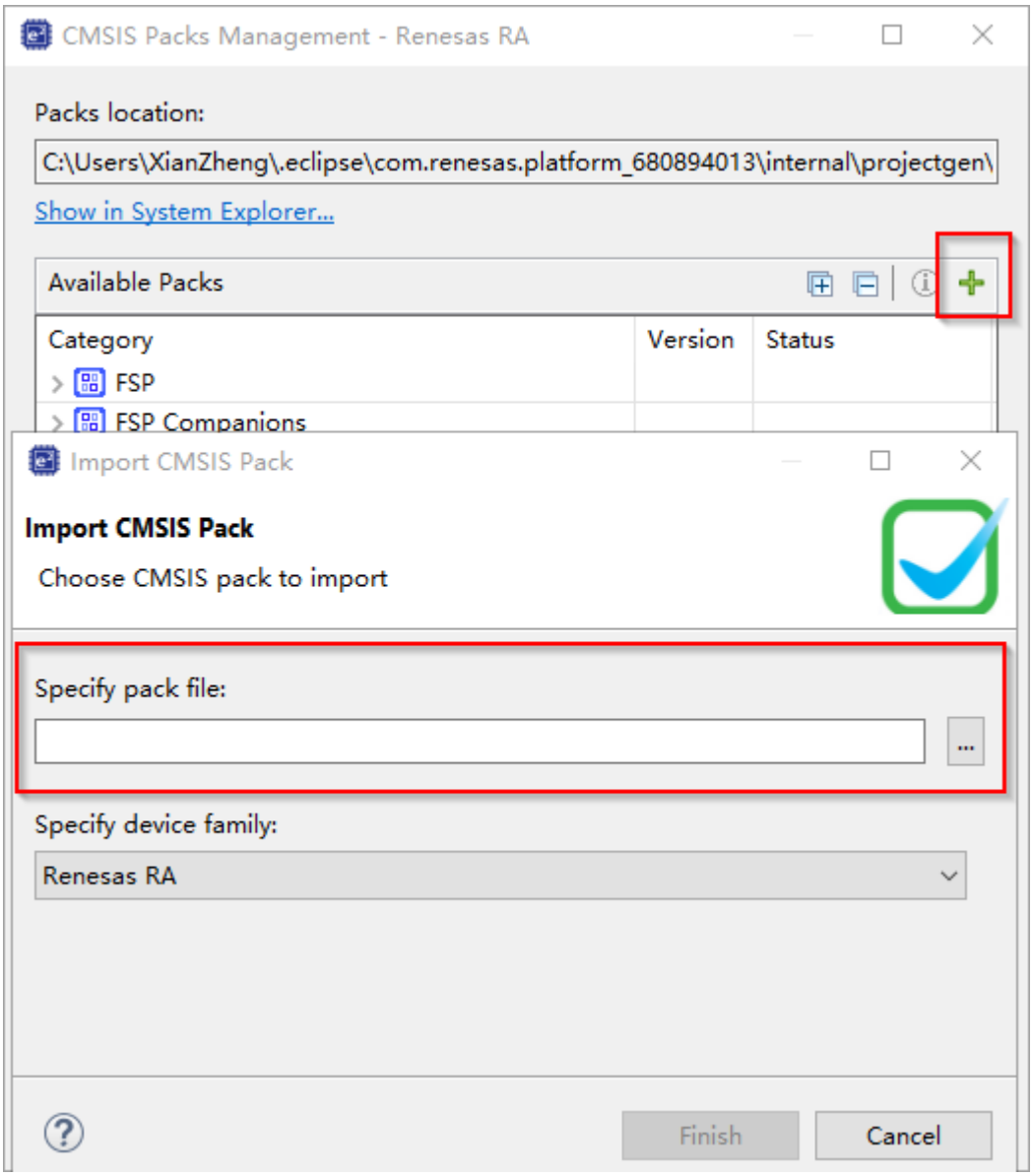
- **Renesas RA6M3 Board (with MX25R flash)**
- **Renesas Flexible Software Package (FSP)**
- **J-Link RTT Viewer**
- **MX25R Extend Modulepack: MXIC.MX25R_Extend.2.0.0.pack**
- **PowerManage Modulepack: Renesas.Flash_PowerManage.1.0.0+fsp.5.0.0.pack**
- **PowerManage_Sample_Project**

2 Work Flow

3.1 Preparation

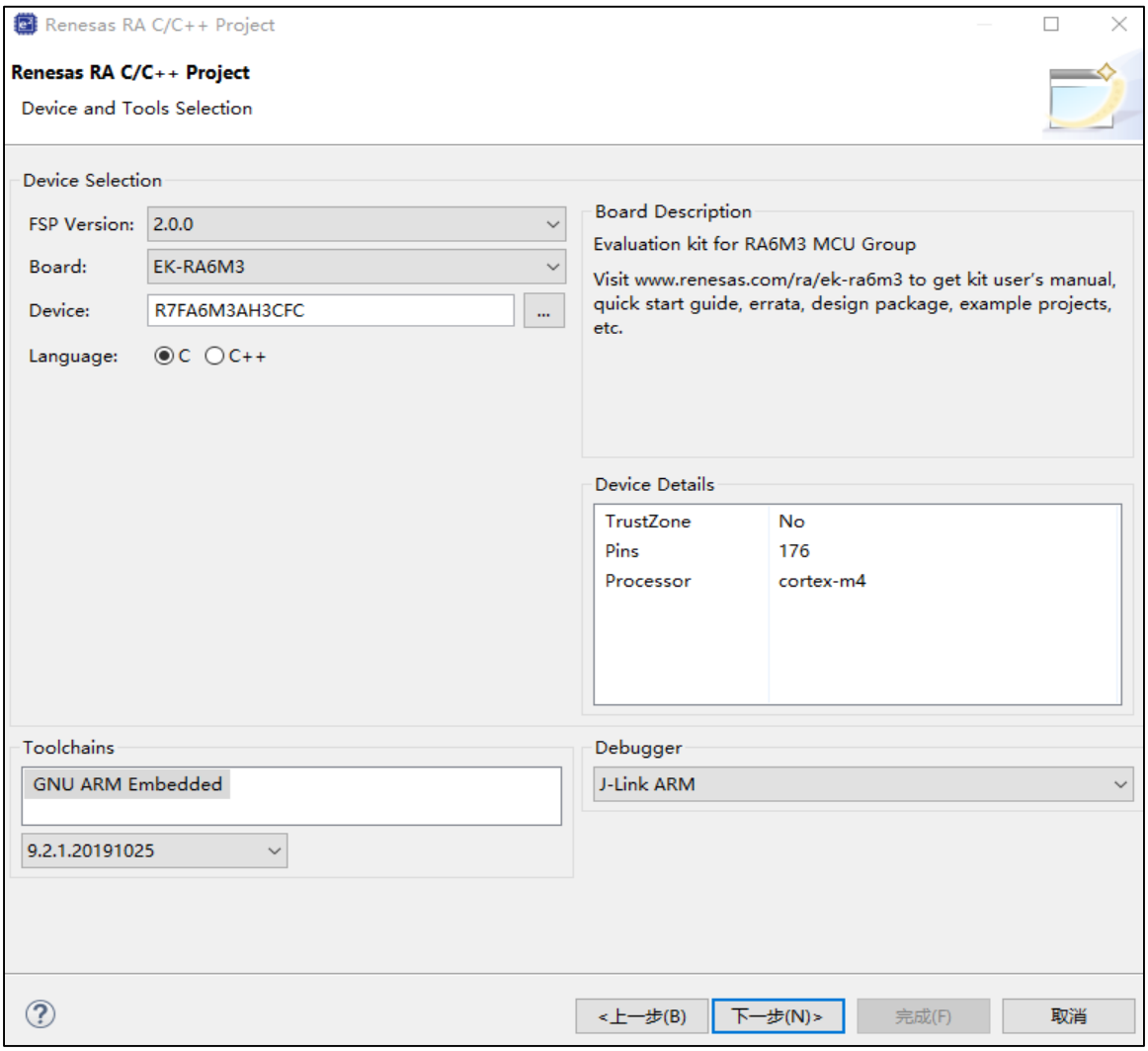
We assume that FSP is installed successfully, so you should import the pack as follows.


ate Search Project 瑞萨视图(V) Run Window Help
No Launch Configurations
ace.
a directory containing existing code
Welcome
Help Contents
Search
Show Context Help
Show Active Keybindings... Ctrl+Shift+L
Cheat Sheets...
Renesas Help
CMSIS Packs Management
Add Renesas Toolchains
Eclipse User Storage
Perform Setup Tasks...
Check for Updates
Install New Software...
Eclipse Marketplace...
Install New Device Family Support
IAR Embedded Workbench plugin manager...
About e² studio
Renesas RA

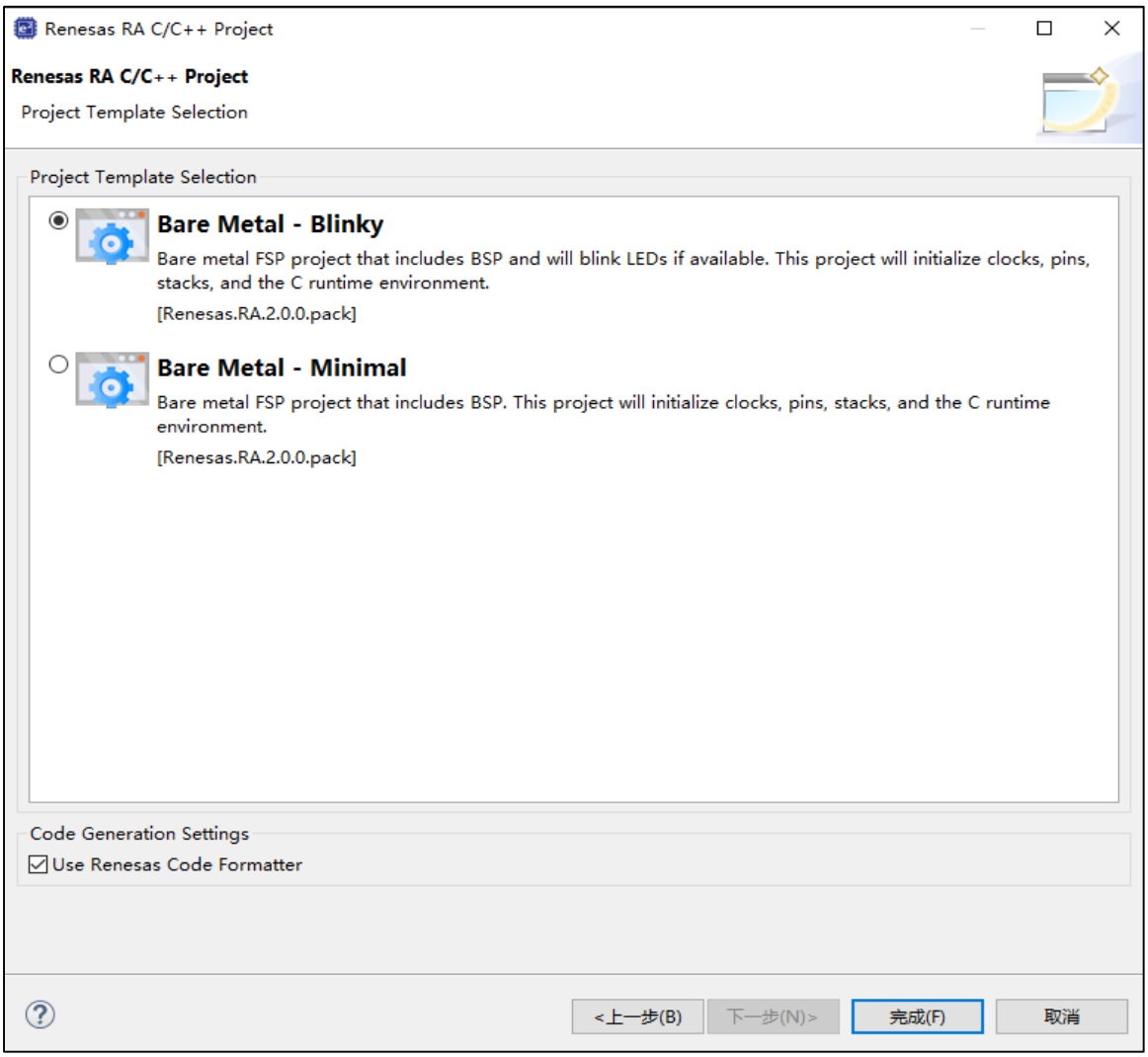


3.2 Build Project

Open e2studio and build a new project, here we choose **Renesas RA C/C++ Project** and device select **EK-RA6M3**:

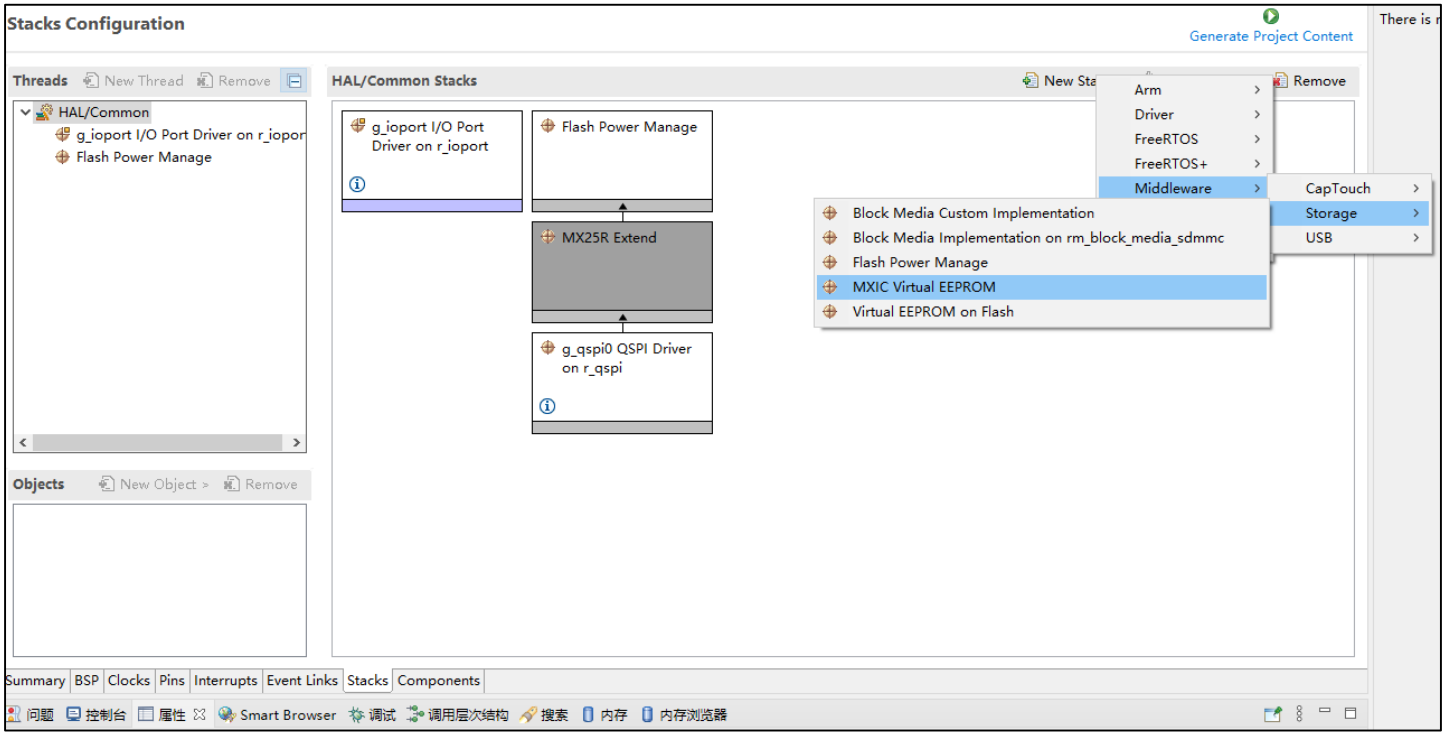


Then we can select **Bare Metal – Blinky** as a template:



3.3 Add Modules and set Parameters

After build project, you should add Power Manage module as the follow picture: **New Stack->Middleware->Storage->Flash Power manage.**

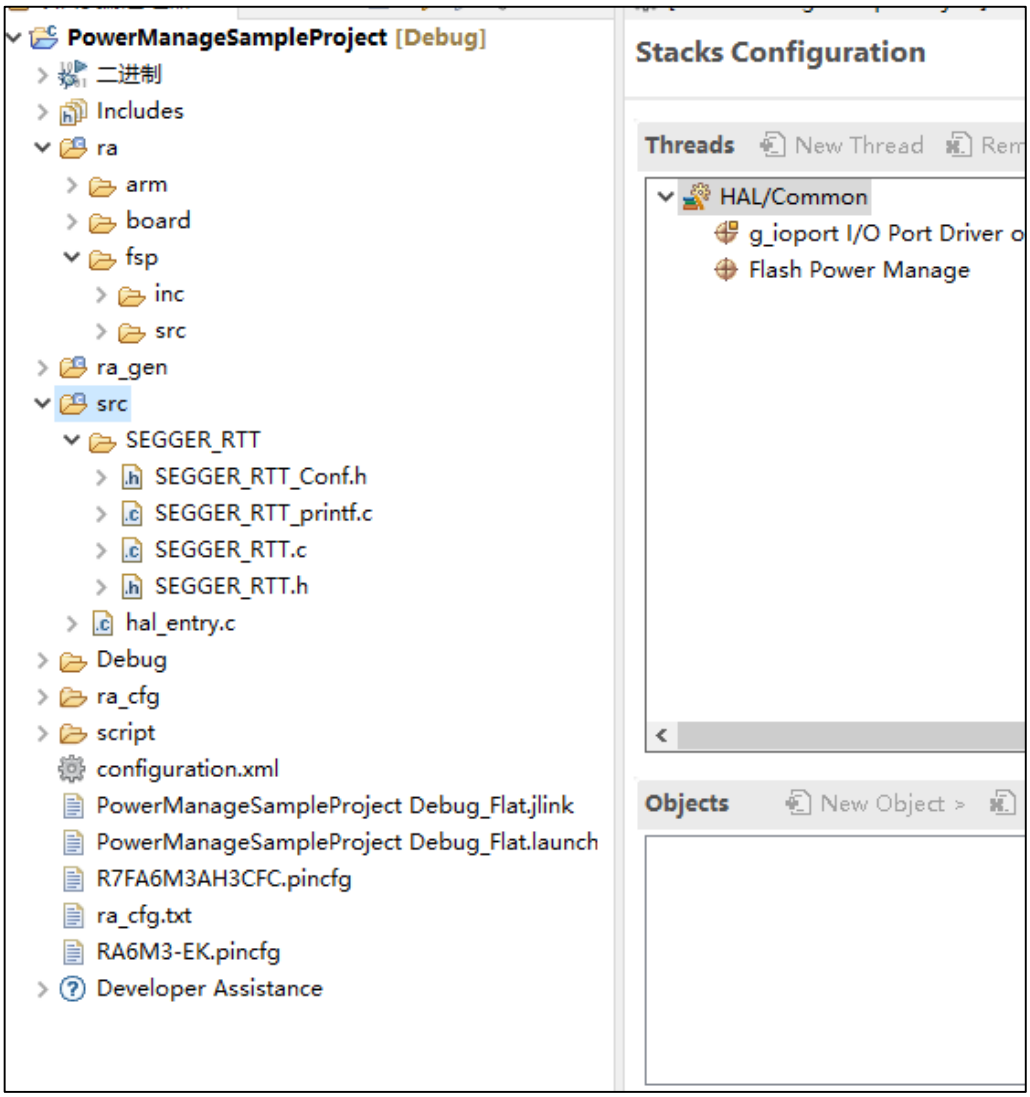


After add MX25R Module, you should set correct pins according to actual connection. For more information, Please refer to *MX25R_Extend Application Note*.

Finally, you should set **Heap size** in **BSP->Properties**(To generate random data for testbench), then save the changes and click **Generate Project Content** button to generate code.

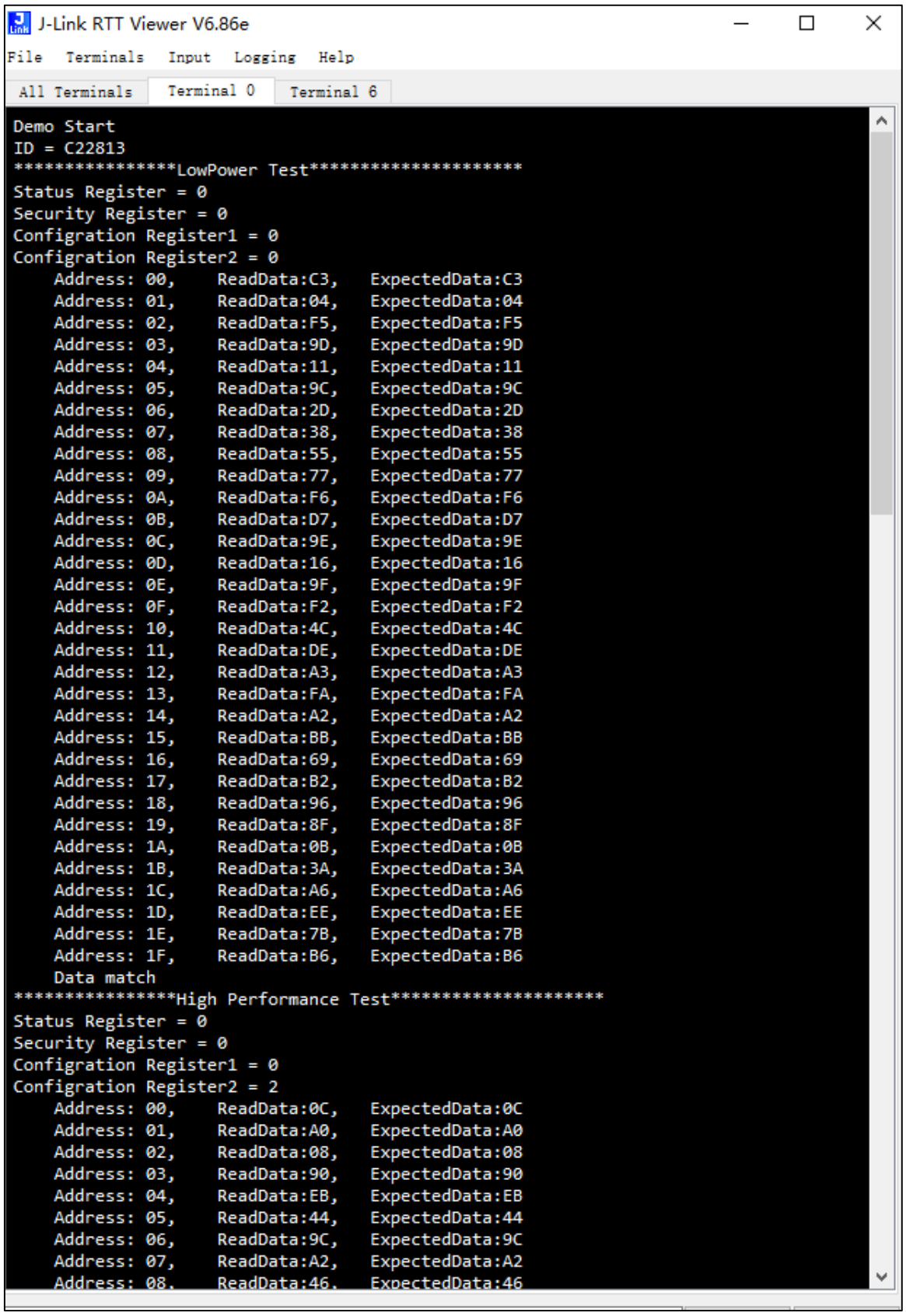
3.4 Add Testbench

You can copy **SEGGER_RTT** folder and **hal_entry.c** from **PowerManage_Sample_Project** and paste to **src** folder. Then, you should click the hammer button to build the project.



3 Run Demo

Download the code to develop board, and then connect to J-Link RTT Viewer.


J-Link RTT Viewer V6.86e
File Terminals Input Logging Help
All Terminals
Terminal 0
Terminal 6
Demo Start
ID = C22813
**********LowPower Test**********
Status Register = 0
Security Register = 0
Configration Register1 = 0
Configration Register2 = 0
Address: 00, ReadData:C3, ExpectedData:C3
Address: 01, ReadData:04, ExpectedData:04
Address: 02, ReadData:F5, ExpectedData:F5
Address: 03, ReadData:9D, ExpectedData:9D
Address: 04, ReadData:11, ExpectedData:11
Address: 05, ReadData:9C, ExpectedData:9C
Address: 06, ReadData:2D, ExpectedData:2D
Address: 07, ReadData:38, ExpectedData:38
Address: 08, ReadData:55, ExpectedData:55
Address: 09, ReadData:77, ExpectedData:77
Address: 0A, ReadData:F6, ExpectedData:F6
Address: 0B, ReadData:D7, ExpectedData:D7
Address: 0C, ReadData:9E, ExpectedData:9E
Address: 0D, ReadData:16, ExpectedData:16
Address: 0E, ReadData:9F, ExpectedData:9F
Address: 0F, ReadData:F2, ExpectedData:F2
Address: 10, ReadData:4C, ExpectedData:4C
Address: 11, ReadData:DE, ExpectedData:DE
Address: 12, ReadData:A3, ExpectedData:A3
Address: 13, ReadData:FA, ExpectedData:FA
Address: 14, ReadData:A2, ExpectedData:A2
Address: 15, ReadData:BB, ExpectedData:BB
Address: 16, ReadData:69, ExpectedData:69
Address: 17, ReadData:B2, ExpectedData:B2
Address: 18, ReadData:96, ExpectedData:96
Address: 19, ReadData:8F, ExpectedData:8F
Address: 1A, ReadData:0B, ExpectedData:0B
Address: 1B, ReadData:3A, ExpectedData:3A
Address: 1C, ReadData:A6, ExpectedData:A6
Address: 1D, ReadData:EE, ExpectedData:EE
Address: 1E, ReadData:7B, ExpectedData:7B
Address: 1F, ReadData:B6, ExpectedData:B6
Data match
**********High Performance Test**********
Status Register = 0
Security Register = 0
Configration Register1 = 0
Configration Register2 = 2
Address: 00, ReadData:0C, ExpectedData:0C
Address: 01, ReadData:A0, ExpectedData:A0
Address: 02, ReadData:08, ExpectedData:08
Address: 03, ReadData:90, ExpectedData:90
Address: 04, ReadData:EB, ExpectedData:EB
Address: 05, ReadData:44, ExpectedData:44
Address: 06, ReadData:9C, ExpectedData:9C
Address: 07, ReadData:A2, ExpectedData:A2
Address: 08, ReadData:46, ExpectedData:46

4 Revision History

Table 8-1: Revision History

Revision No.	Description	Page	Date
Rev. 1.00	Initial Release	ALL	April 14, 2021
Rev. 1.1.0	Update	4	April 24, 2023
Rev. 1.2.0	Update	4	December 1, 2023

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