Angle Sensors

GMR-Based Angle Sensors

TLE5012B Register Setting

TLE5012B

Application Note

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ATV SC

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V1.5, 2012-11-15	
All	Changed reset values of fuse-calibrated registers to “device-specific”
8	Added description for CRC check, derivate-specific reset values, device-specific reset values and multi-purpose registers.
All	Added extensive description to all registers

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1 Introduction

This document is the second part of the electrical specification. Generally the latest data sheet of TLE5012B is valid.

The main interface of the TLE5012B is Synchronous Serial Communication (SSC) and the following section describes the configuration bits.

2 SSC Registers

Table 1 lists the various bit types used in the SSC registers.

Table 1 Bit Types

Abbreviation	Function	Description
r	Read	Read-only registers
w	Write	Read and write registers
u	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

2.1 Registers Chapter

This section describes the registers of the TLE5012B. It also defines the read/write access rights of the specific registers. Table 2 identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 2 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers Chapter, Register Descriptions			
STAT	STATus register	00_H	9
ACSTAT	ACtivation STATus register	01_H	12
AVAL	Angle VALue register	02_H	14
ASPD	Angle SPeeD register	03_H	15
AREV	Angle REVolution register	04_H	16
FSYNC	Frame SYNChronization register	05_H	17
MOD_1	Interface MODe1 register	06_H	17
SIL	SIL register	07_H	18
MOD_2	Interface MODe2 register	08_H	20
MOD_3	Interface MODe3 register	09_H	21
OFFX	OFFset X	$0A_H$	22
OFFY	OFFset Y	$0B_H$	22
SYNCH	SYNCHronicity	$0C_H$	23
IFAB	IFAB register	$0D_H$	23
MOD_4	Interface MODe4 register	$0E_H$	24

Table 2 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TCO_Y	Temperature COefficient register	$0F_H$	27
ADC_X	ADC X-raw value	10_H	28
ADC_Y	ADC Y-raw value	11_H	28
IIF_CNT	IIF CouNTer value	20_H	29

The register is addressed wordwise.

Configuration Register Checksum

To monitor the integrity of the sensor configuration, the TLE5012B performs a cyclic redundancy check of the configuration registers in address range 08_H to $0F_H$. The 8bit CRC is stored in register CRC_PAR (address $0F_H$). When changing one or more of these registers, a new checksum has to be calculated from registers 08_H to $0F_H$ using the generator polynomial described in the **TLE5012B Data Sheet**, and written to the CRC_PAR register. Otherwise, a CRC fail error (status bit S_FUSE = 1) will occur. The CRC check can be disabled by setting register AS_FUSE to 0. It is automatically deactivated if auto calibration is active, as auto calibration performs periodical adjustments of several configuration registers.

Derivate-Specific Reset Values:

The reset values of certain registers (for example interface settings) are set by laser fuses which are specific for the employed derivate (Exxxx number) of the TLE5012B. In this case, the reset values in the register table are marked as "derivate-specific". A list of specific reset values for all derivates is given in **Chapter 3**.

Factory-Calibrated Reset Values:

The reset values of calibration registers (for example offset calibration) are set by laser fuses which are written during the factory calibration of the sensor. These values are specific for each individual device. In this case, the reset values in the register table are marked as "device-specific". When modifying parts of these registers, the register content should be read first, then only the relevant bits should be changed and the content should be written back into the register in order to avoid unintended over-writing of the calibration values.

Multi-Purpose Registers:

Some configuration registers have more than one assignment and change different settings depending on the selected interface for the IFA, IFB, IFC pins (selectable via the IF_MD register, address $0E_H$). These registers are marked as "multi-purpose", and their assignments are described separately for each relevant interface.

2.1.1 Register Descriptions

Status Register

STAT	Offset	Reset Value
Status Register	**00_H**	**8001_H**

15	14	13	12	11	10	9	8
RD_ST	**S_NR**		**NO_GMR_A**	**NO_GMR_XY**	**S_ROM**	**S_ADCT**	Res
r	w		ru	ru	r	ru	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
S_MAGOL	**S_XYOL**	**S_OV**	**S_DSPU**	**S_FUSE**	**S_VR**	**S_WD**	**S_RST**
ru	ru	ru	ru	ru	ru	ru	ru

Field	Bits	Type	Description
RD_ST	15	r	**Read Status** 0_B status values not changed since last readout 1_B status values changed Reset: 1_B
S_NR	14:13	w	**Slave Number** Used to identify up to four sensors in a bus configuration. The levels on pin SCK and pin IFC can be used to change the default slave number for SPC interface. Pin SCK represents S_NR[13] and pin IFC the S_NR[14]. Reset: 00_B
NO_GMR_A	12	ru	**No valid GMR Angle Value** Cyclic check of DSPU output. 0_B valid GMR angle value on the interface 1_B no valid GMR angle value on the interface (e.g test vectors) Reset: 0_B
NO_GMR_XY	11	ru	**No valid GMR XY Values** Cyclic check of ADC input. 0_B valid GMR_XY values on the ADC input 1_B no valid GMR_XY values on the ADC input (e.g. test vectors) Reset: 0_B

Field	Bits	Type	Description
S_ROM	10	r	**Status ROM**[1)] Check of ROM-CRC at startup. After fail, DSPU does not start. SPI access possible. 0_B CRC ok 1_B CRC fail or running Reset: 0_B
S_ADCT	9	ru	**Status ADC-Test**[1)] Check of signal path with test vectors. All test vectors at startup tested. Activation in operation via AS_ADCT possible. 0_B Test vectors ok 1_B Test vectors out of limit Reset: 0_B
S_MAGOL	7	ru	**Status Magnitude Out of Limit**[1)] Cyclic check of available magnetic field strength (magnet loss check). Deactivation via AS_VEC_MAG. 0_B GMR-magnitude ok 1_B GMR-magnitude out of limit Reset: 0_B
S_XYOL	6	ru	**Status X,Y Data Out of Limit**[1)] Cyclic check of X and Y raw values. Deactivation via AS_VEC_XY 0_B X,Y data ok 1_B X,Y data out of limit (>23230 digits, <-23230 digits) Reset: 0_B
S_OV	5	ru	**Status Overflow**[1)] Cyclic check of DSPU overflow. Deactivation via AS_OV. 0_B No DSPU overflow occurred 1_B DSPU overflow occurred Reset: 0_B
S_DSPU	4	ru	**Status Digital Signal Processing Unit** Check of DSPU, CORDIC and CAPCOM at startup. Activation in operation via AS_DSPU possible. 0_B DSPU self-test ok 1_B DSPU self-test not ok, or self test is running Reset: 0_B

Field	Bits	Type	Description
S_FUSE	3	ru	**Status Fuse CRC**[1)] CRC check configuration registers 08_H to $0F_H$ (CRC_PAR register $0F_H$). Deactivation via AS_FUSE. CRC check is automatically disabled if auto calibration is active. *Note: When changing the content of one or more configuration registers in address range 08_H to $0F_H$, a new CRC has to be calculated and stored in register CRC_PAR (address $0F_H$), otherwise CRC fail will occur.* 0_B CRC ok 1_B CRC fail Reset: 0_B
S_VR	2	ru	**Status Voltage Regulator**[1)] Permanent check of internal and external supply voltages. Deactivation via AS_VR 0_B Voltages ok 1_B V_{DD} over voltage; V_{DD}-off; GND-off; or V_{OVG}; V_{OVA}; V_{OVD} too high Reset: 0_B
S_WD	1	ru	**Status Watchdog** Permanent check of watchdog. After watchdog-counter overflow, the DSPU stops. Deactivation via AS_WD 0_B normal operation 1_B watchdog counter expired (DSPU stop), AS_RST must be activated. Outputs deactivated, Pull Up/Down active. Reset: 0_B
S_RST	0	ru	**Status Reset**[1)2)] Permanent check of any reset. Deactivation via AS_RST. 0_B no reset since last readout 1_B indication of power-up, short power-break, firmware or active reset Reset: 1_B

1) reset to “0” after readout

2) bit remains “1” after reset occurred until status register is read.

Note: When an error occurs, the corresponding bit in the safety word remains “0” until the status register is read.

Activation Status Register

ACSTAT	Offset	Reset Value
Activation Status Register	01_H	$5AFE_H$

15				11	10	9	8
Res					AS_FRST	AS_ADCT	Res
		w			w	w	

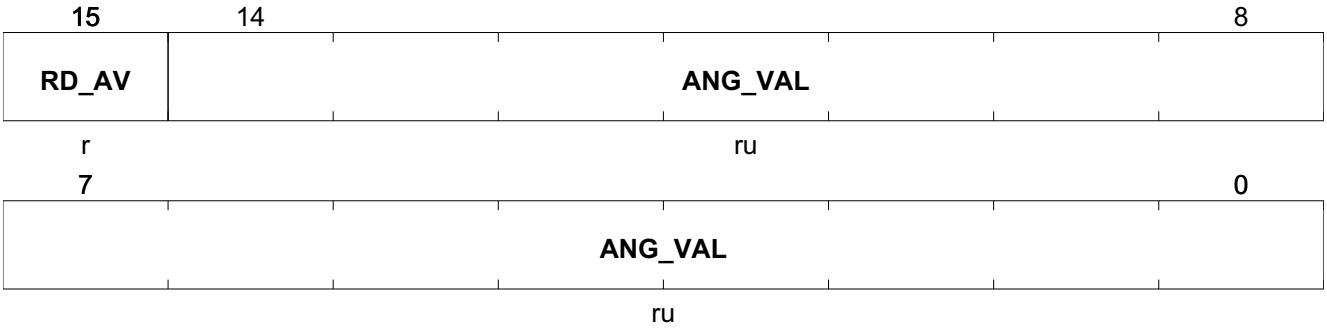
7	6	5	4	3	2	1	0
AS_VEC_MAG	AS_VEC_XY	AS_OV	AS_DSPU	AS_FUSE	AS_VR	AS_WD	AS_RST
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
Res	15:11	w	**Reserved** Reset: 01011_B
AS_FRST	10	w	**Activation of Firmware Reset** All configuration registers retain their contents. 0_B after execution 1_B activation of firmware reset (S_RST is set) Reset: 0_B
AS_ADCT	9	w	**Enable ADC Test vector Check** Activation of this test is only allowed by deactivated AUTOCAL. 0_B after execution 1_B activation of ADC Test vector Check Reset: 1_B
AS_VEC_MAG	7	w	**Activation of Magnitude Check** 0_B monitoring of magnitude disabled 1_B monitoring of magnitude enabled Reset: 1_B
AS_VEC_XY	6	w	**Activation of X,Y Out of Limit-Check** 0_B monitoring of X,Y Out of Limit disabled 1_B monitoring of X,Y Out of Limit enabled Reset: 1_B
AS_OV	5	w	**Enable of DSPU Overflow Check** 0_B monitoring of DSPU Overflow disabled 1_B monitoring of DSPU Overflow enabled Reset: 1_B
AS_DSPU	4	w	**Activation DSPU BIST** 0_B after execution 1_B activation of DSPU BIST or BIST running Reset: 1_B

Field	Bits	Type	Description
AS_FUSE	3	w	**Activation Fuse CRC** Automatically enabled by deactivation of AUTOCAL. 0_B monitoring of CRC disabled 1_B monitoring of CRC enabled Reset: 1_B
AS_VR	2	w	**Enable Voltage Regulator Check** 0_B check of regulator voltages disabled 1_B check of regulator voltages enabled Reset: 1_B
AS_WD	1	w	**Enable DSPU Watchdog-HW-Reset** 0_B DSPU watchdog monitoring disabled 1_B DSPU Watchdog monitoring enabled Reset: 1_B
AS_RST	0	w	**Activation of Hardware Reset** Activation occurs after CSQ switches from ’0’ to ’1’ after SSC transfer. 0_B after execution 1_B activation of HW Reset (S_RST is set) Reset: 0_B

Angle Value Register

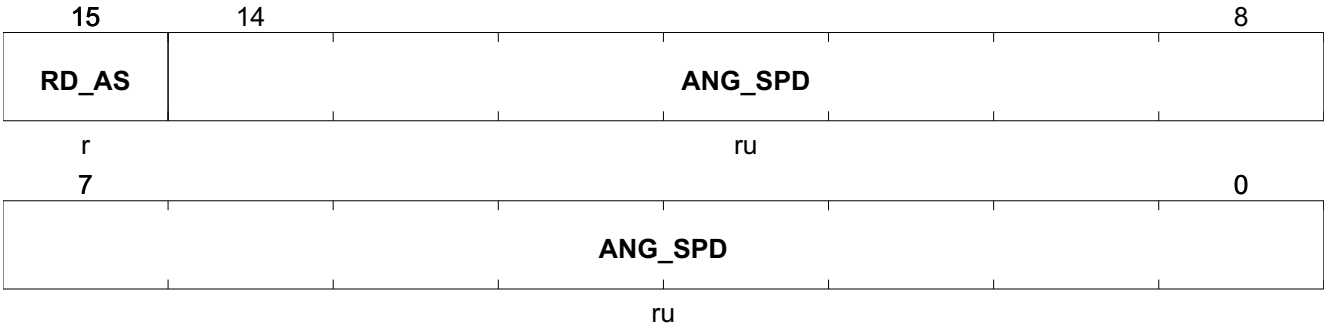
AVAL	Offset	Reset Value
Angle Value Register	**02_H**	**8000_H**



Field	Bits	Type	Description
RD_AV	15	r	**Read Status, Angle Value** 0_B no new angle value since last readout 1_B new angle value (ANG_VAL) present Reset: 1_B
ANG_VAL	14:0	ru	**Calculated Angle Value (signed 15-bit)** $Angle[°] = \frac{360°}{2^{15}} ANG\_VAL[digits]$ (1) 4000_H -180° 0000_H 0° $3FFF_H$ +179.99° (valid for ANG_RANGE = 0x080) Reset: 0_H

Angle Speed Register

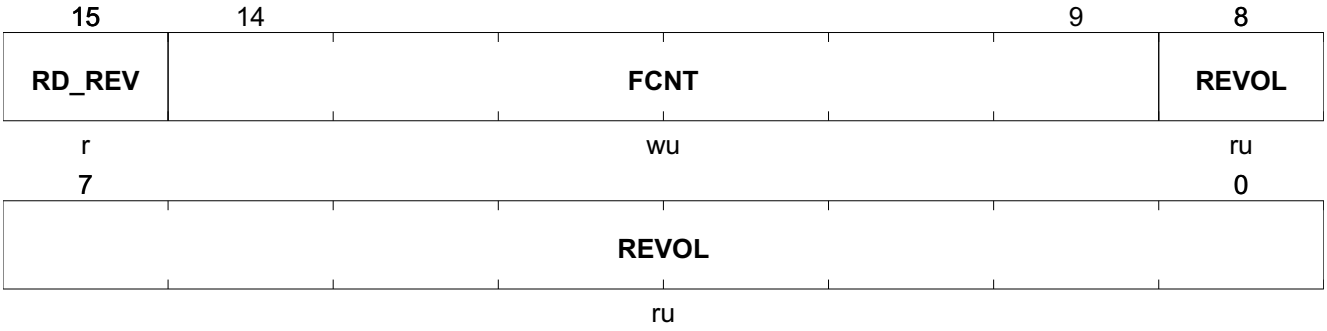
ASPD	Offset	Reset Value
Angle Speed Register	03_H	8000_H



Field	Bits	Type	Description
RD_AS	15	r	**Read Status, Angle Speed** 0_B no new angle speed value since last readout 1_B new angle speed value (ANG_SPD) present Reset: 1_B
ANG_SPD	14:0	ru	**Calculated Angle Speed** Without prediction difference between three consecutive angle values. $Speed\ [°/s] = \frac{\frac{AngleRange\ [°]}{2^{15}} ANG\_SPD\ [digits]}{2t_{upd}\ [s]}$ (2) With prediction, difference between predicted value and next-to-last measured angle value. $Speed\ [°/s] = \frac{\frac{AngleRange\ [°]}{2^{15}} ANG\_SPD\ [digits]}{3t_{upd}\ [s]}$ (3) Reset: 0_H

Angle Revolution Register

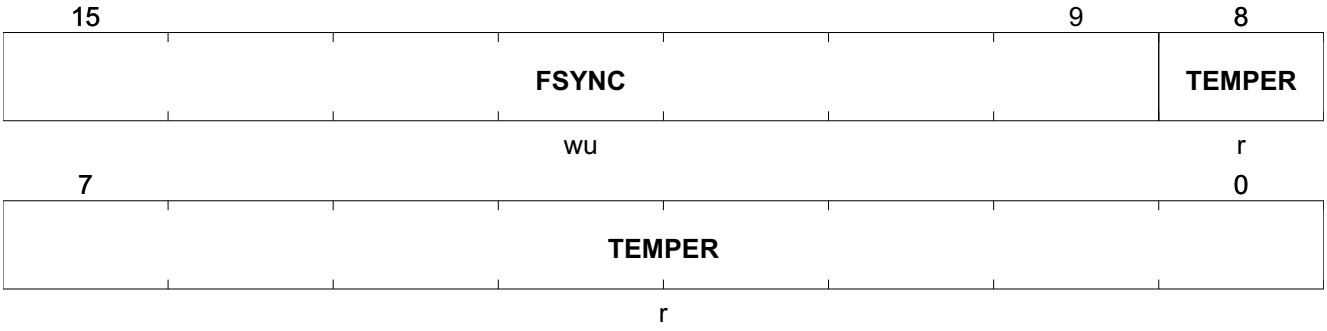
AREV	Offset	Reset Value
Angle Revolution Register	**04_H**	**8000_H**



Field	Bits	Type	Description
RD_REV	15	r	**Read Status, Revolution** 0_B no new values since last readout 1_B new value (REVOL) present Reset: 1_B
FCNT	14:9	wu	**Frame Counter (unsigned 6-bit value)** Internal frame counter. Increments every update period (FIR_MD setting). Reset: 0_H
REVOL	8:0	ru	**Number of Revolutions (signed 9-bit value)** Revolution counter. Increments for every full rotation in counter-clockwise direction (at angle discontinuity from 0° to 360°) and decrements for every full rotation in clockwise direction (at angle discontinuity from 360° to 0°) Reset: 0_H

Frame Synchronization Register

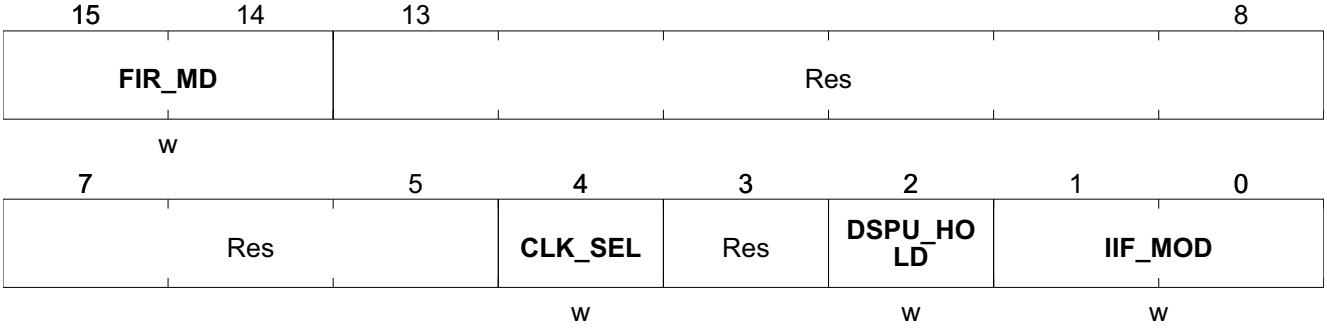
FSYNC	Offset	Reset Value
Frame Synchronization Register	05_H	0000_H



Field	Bits	Type	Description
FSYNC	15:9	wu	**Frame Synchronization Counter Value** Subcounter within one frame. Increments every internal clock cycle. Maximum counter value depends on FIR_MD setting. 16 @ FIR_MD=00; 32 @ FIR_MD=01; 64 @ FIR_MD=10; 128 @ FIR_MD=11. Reset: 0_H
TEMPER	8:0	r	**Temperature Value** Signed integer temperature value. T[°C] = (TEMPER+152) / 2.776 Reset: 0_H

Interface Mode1 Register

MOD_1	Offset	Reset Value
Interface Mode1 Register	06_H	derivate-specific



Field	Bits	Type	Description
FIR_MD	15:14	w	**Update Rate Setting (Filter Decimation)** 00_B 21.3 µs 01_B 42.7 µs 10_B 85.3 µs 11_B 170.6 µs Reset: derivate-specific
CLK_SEL	4	w	**Clock Source Select** Switch to external clock. If there is no clock signal on the IFC pin or PLL out of lock, the sensor automatically switches to internal oscillator. 0_B internal oscillator 1_B external 4-MHz clock (IFC pin switched to input) Reset: 0_B
DSPU_HOLD	2	w	**Hold DSPU Operation** If DSPU is on hold, no watchdog reset is performed by DSPU. Deactivate watchdog with AS_WD before setting DSPU on hold. 0_B DSPU in normal schedule operation 1_B DSPU is on hold Reset: 0_B
IIF_MOD	1:0	w	**Incremental Interface Mode** 00_B IIF disabled 01_B A/B operation with Index on CLK/HS3 10_B Step/Direction operation with Index on CLK/HS3 11_B not allowed Reset: derivate-specific

SIL Register

SIL	Offset	Reset Value
SIL Register	07_H	0000_H

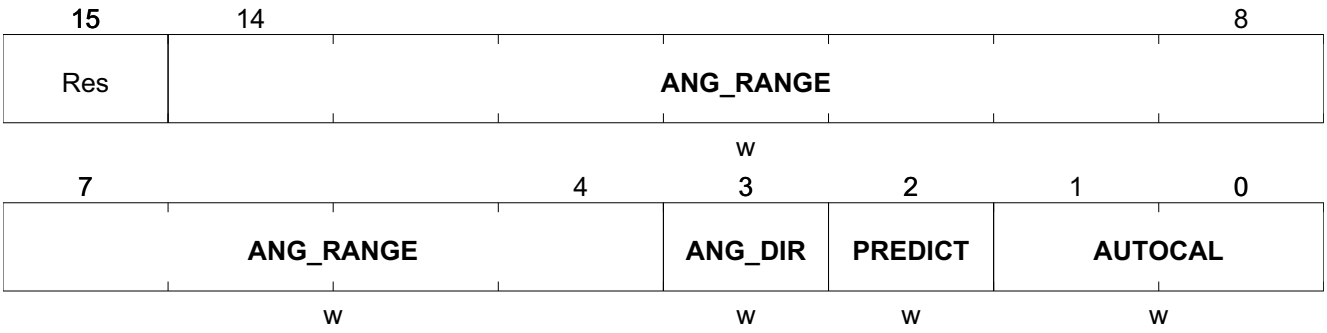
15	14	13	11	10	9	8
FILT_PAR	**FILT_INV**	Res		**FUSE_REL**	Res	
w	w			w		

7	6	5	3	2	0
Res	**ADCTV_EN**	**ADCTV_Y**		**ADCTV_X**	
	w	w		w	

Field	Bits	Type	Description
FILT_PAR	15	w	**Filter Parallel** Diagnostic function to test ADCs. If enabled, the raw X-signal is routed also to the Y-ADC so SIN and COS signal should be identical. 0_B filter parallel disabled 1_B filter parallel enabled (source: X-value) Reset: 0_B
FILT_INV	14	w	**Filter Inverted** Diagnostic function to test ADCs. If enabled, the X- and Y-signals are inverted. The angle output is then shifted by 180°. 0_B filter inverted disabled 1_B filter inverted enabled Reset: 0_B
FUSE_REL	10	w	**Fuse Reload** 0_B normal operation 1_B fuse parameters reloaded to DSPU at next cycle start Reset: 0_B
ADCTV_EN	6	w	**ADC-Test Vectors** Diagnostic function to test ADCs. If enabled, sensor elements are internally disconnected and test voltages are connected to ADCs. Test vectors can be selected via the register ADCTV_Y and ADCTV_X. 0_B ADC-Test Vectors disabled 1_B ADC-Test Vectors enabled Reset: 0_B
ADCTV_Y	5:3	w	**Test vector Y** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 0_H
ADCTV_X	2:0	w	**Test vector X** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 0_H

Interface Mode2 Register

MOD_2	Offset	Reset Value
Interface Mode2 Register	08_H	derivate-specific

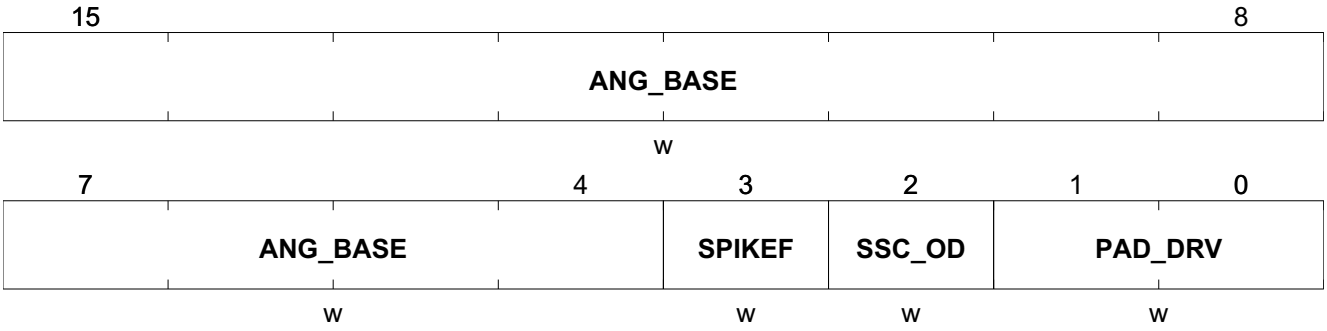


Field	Bits	Type	Description
ANG_RANGE	14:4	w	**Angle Range**[1)] Changes the representation of ANG_VAL. ANG_VAL = ANG_VAL_INT*ANG_RANGE/128 (ANG_VAL_INT is always -180°..180° -> -16384..16383) Angle Range [°] = 360° * (2^7 / ANG_RANGE[digits]) 200_H represents 90° (-45°..45° -> -16384..16383) 080_H represents 360° (-180°..180° -> -16384..16383) Reset: 080_H
ANG_DIR	3	w	**Angle Direction** 0_B counterclockwise rotation of magnet 1_B clockwise rotation of magnet Reset: 0_B
PREDICT	2	w	**Prediction** 0_B prediction disabled 1_B prediction enabled Reset: derivate-specific
AUTOCAL	1:0	w	**Auto-calibration Mode** Automatic calibration of offset and amplitude synchronicity for applications with full-turn capability. CRC check of calibration registers is automatically disabled if auto-calibration is activated. A detailed description of auto-calibration is given in the data sheet. 00_B no auto-calibration 01_B auto-cal. mode 1: update every angle update cycle (FIR_MD setting) 10_B auto-cal. mode 2: update every 1.5 revolutions 11_B auto-cal. mode 3: update every 11.25° Reset: derivate-specific

1)Auto-calibration works only for ANG_RANGE = 080_H.

Interface Mode3 Register

MOD_3	Offset	Reset Value
Interface Mode3 Register	09_H	device-specific



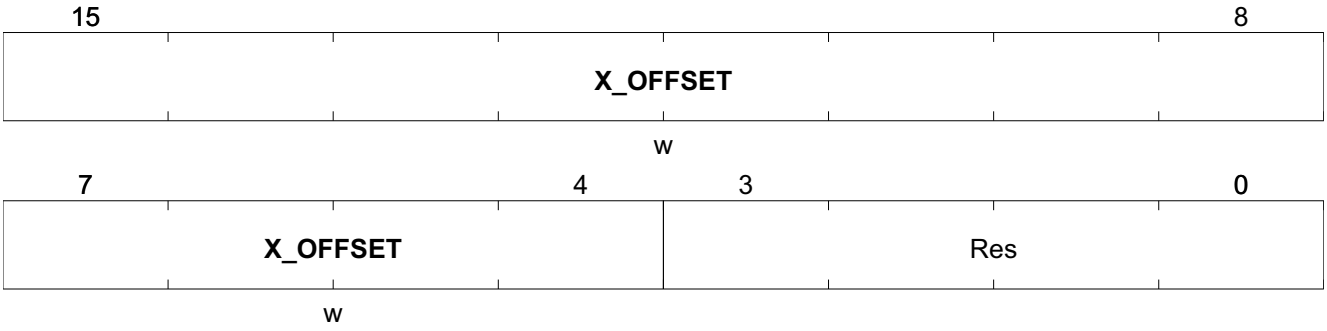
Field	Bits	Type	Description
ANG_BASE	15:4	w	**Angle Base**[1)2)] Sets the 0° angle position (12 bit value). 800_H -180° 000_H 0° $7FF_H$ +179.912° Reset: device-specific
SPIKEF	3	w	**Analog Spike Filter of Input Pads** Filters voltage spikes on input pads. Additional delay of 10 µs for data input. 0_B spike filter disabled 1_B spike filter enabled Reset: derivate-specific
SSC_OD	2	w	**SSC-Interface Data Pin Output Mode** 0_B Push-Pull 1_B Open Drain Reset: 0_B
PAD_DRV	1:0	w	**Configuration of Pad-Driver** 00_B IFA/IFB/IFC: strong driver, DATA: strong driver, fast edge 01_B IFA/IFB/IFC: strong driver, DATA: strong driver, slow edge 10_B IFA/IFB/IFC: weak driver, DATA: medium driver, fast edge 11_B IFA/IFB/IFC: weak driver, DATA: weak driver, slow edge Reset: derivate-specific

1) factory-calibrated to make the 0° direction parallel to the edge of the chip.

2) to manually set the 0° position, rotate the magnet into the desired position, then read the AVAL register and drop the 3 LSBs to obtain a 12bit angle value; then subtract this value from the ANG_BASE register.

Offset X Register

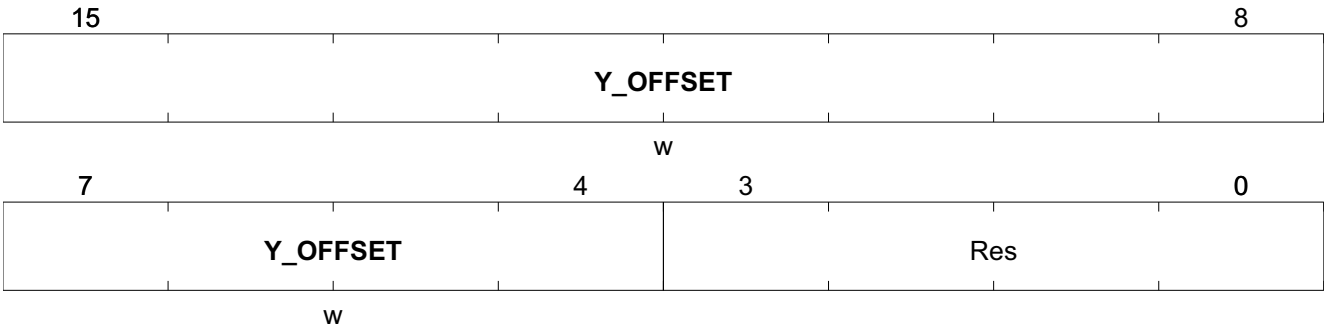
OFFX	Offset	Reset Value
Offset X	$0A_H$	device-specific



Field	Bits	Type	Description
X_OFFSET	15:4	w	**Offset Correction of X-value in digits** Raw X-value offset correction at 25°C. Reset: device-specific

Offset Y Register

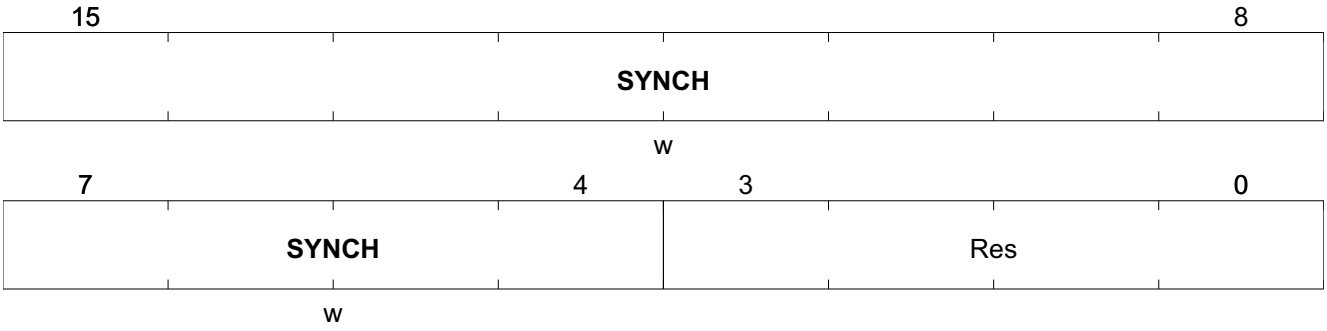
OFFY	Offset	Reset Value
Offset Y	$0B_H$	device-specific



Field	Bits	Type	Description
Y_OFFSET	15:4	w	**Offset Correction of Y-value in digits** Raw Y-value offset correction at 25°C. Reset: device-specific

Synchronicity Register

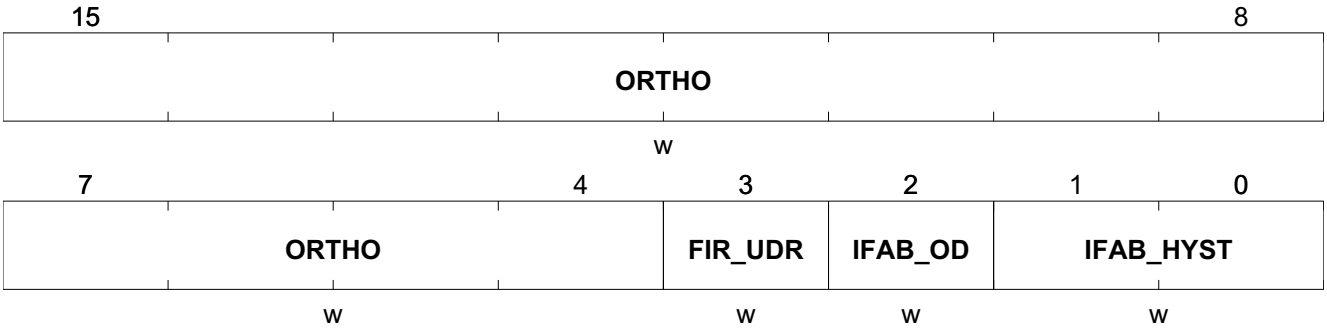
SYNCH	Offset	Reset Value
Synchronicity	$0C_H$	device-specific



Field	Bits	Type	Description
SYNCH	15:4	w	**Amplitude Synchronicity** Raw value amplitude synchronicity correction. $+2047_D$ 112.494% 0_D 100% -2048_D 87.500% Reset: device-specific

IFAB Register (multi-purpose)

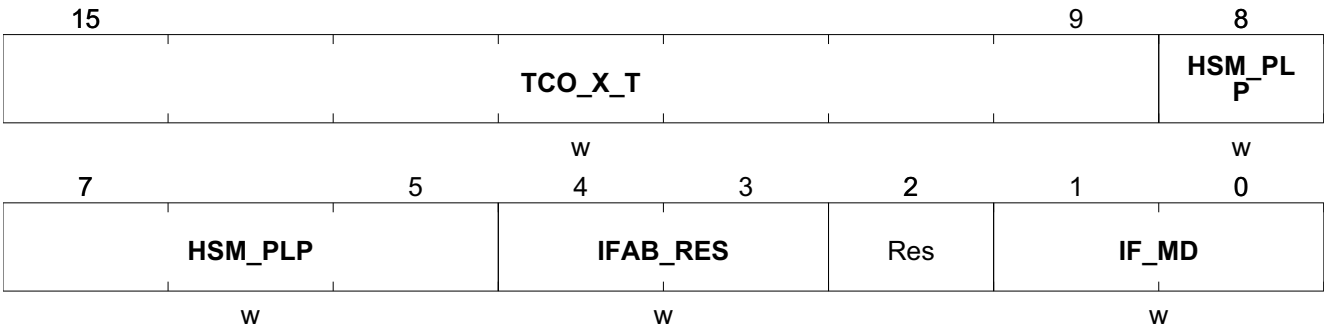
IFAB	Offset	Reset Value
IFAB Register	$0D_H$	device-specific



Field	Bits	Type	Description
ORTHO	15:4	w	**Orthogonality Correction of X and Y Components** GMR element orthogonality correction. $+2047_D$ 11.2445° 0_D 0° -2048_D -11.2500° Reset: device-specific
FIR_UDR	3	w	**FIR Update Rate** Initial filter update rate (FIR) setting to be loaded into FIR_MD on startup. Changes of FIR setting can be done after power-on via SPI within FIR_MD. 0_B FIR_MD = '10' (85.3 µs) 1_B FIR_MD = '01' (42.7 µs) Reset: derivate-specific
IFAB_OD	2	w	**IFA,IFB,IFC Output Mode** 0_B Push-Pull 1_B Open Drain Reset: derivate-specific
IFAB_HYST (multi-purpose)	1:0	w	**HSM and IIF Mode: Hysteresis** Electrical switching hysteresis for HSM and IIF interface. 00_B 0° 01_B 0.09° 10_B 0.27° 11_B 0.625° **SPC Mode: Unit Time** 00_B 3.0 µs 01_B 2.5 µs 10_B 2.0 µs 11_B 1.5 µs Reset: derivate-specific

Interface Mode4 Register (multi-purpose)

MOD_4	Offset	Reset Value
Interface Mode4 Register	$0E_H$	device-specific



Field	Bits	Type	Description
TCO_X_T	15:9	w	**Offset Temperature Coefficient for X-Component**[1)] Reset: device-specific
HSM_PLP (multi-purpose)	8:5	w	**Hall Switch Mode: Pole-Pair Configuration** 0000_B 1 pole pairs 0001_B 2 pole pairs 0010_B 3 pole pairs 0011_B 4 pole pairs 0100_B 5 pole pairs 0101_B 6 pole pairs 0110_B 7 pole pairs 0111_B 8 pole pairs 1000_B 9 pole pairs 1001_B 10 pole pairs 1010_B 11 pole pairs 1011_B 12 pole pairs 1100_B 13 pole pairs 1101_B 14 pole pairs 1110_B 15 pole pairs 1111_B 16 pole pairs **Pulse-Width-Modulation Mode: Error Indication** 0000_B error indication enabled 0010_B error indication disabled **Incremental Interface Mode: Absolute Count** Interface counts to absolute value at startup 0000_B absolute count enabled 0100_B absolute count disabled **SPC Mode: Total Trigger Time** Duration of the master pulse to trigger SPC output 0000_B 90*UT 1000_B t_{mlow} + 12 UT Reset: derivate-specific

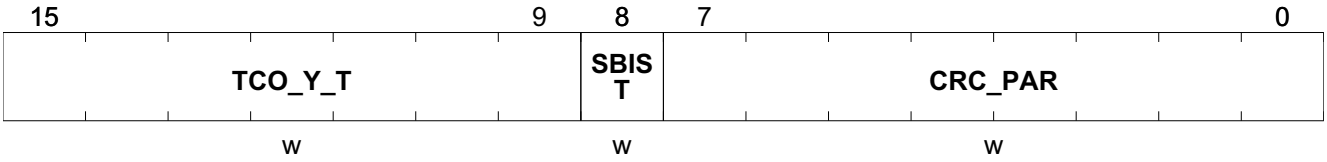
Field	Bits	Type	Description
IFAB_RES (multi-purpose)	4:3	w	**Pulse-Width-Modulation Mode: Frequency** Selection of PWM frequency. 00_B 244 Hz 01_B 488 Hz 10_B 977 Hz 11_B 1953 Hz **Incremental Interface Mode: IIF resolution** 00_B 12bit, 0.088° step 01_B 11bit, 0.176° step 10_B 10bit, 0.352° step 11_B 9bit, 0.703° step **SPC Mode: SPC Frame Configuration** 00_B 12bit angle 01_B 16bit angle 10_B 12bit angle + 8bit temperature 11_B 16bit angle + 8bit temperature Reset: derivate-specific
IF_MD	1:0	w	**Interface Mode on IFA,IFB,IFC** Selected by external circuit of CLK pin at Power On Time. pull-up on IFC (CLK) pin --> Incremental Interface is selected; pull-down on IFC (CLK) pin --> IF_MD stored Interface is used. Switching to another interface during operation needs to stop the DSPU (DSPU_HOLD). SSC interface is always active in parallel on pins SCK, CSQ and DATA. 00_B IIF 01_B PWM 10_B HSM 11_B SPC[2)] Reset: derivate-specific

1) If auto-calibration is enabled, TCO_X_T is automatically set to 0. Once auto-calibration is deactivated, laser-fused calibration values are loaded into TCO_X_T.

2) In SPC interface configuration, the sensor updates the AVAL register only when receiving an SPC trigger pulse on the IFA pin.

Temperature Coefficient Register

TCO_Y	Offset	Reset Value
Temperature Coefficient Register	$0F_H$	device-specific

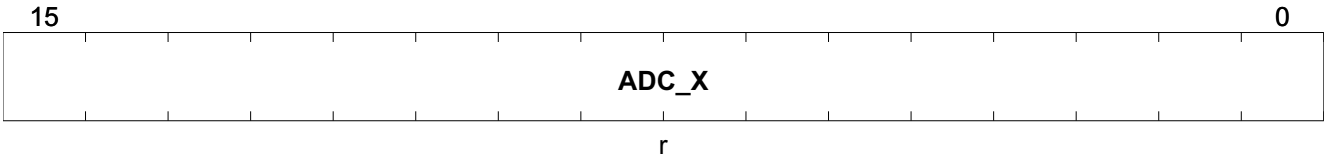


Field	Bits	Type	Description
TCO_Y_T	15:9	w	**Offset Temperature Coefficient for Y-Component**[1)] Reset: device-specific
SBIST	8	w	**Startup-BIST** 0_B Startup-BIST disabled 1_B Startup-BIST enabled Reset: 1_B
CRC_PAR	7:0	w	**CRC of Parameters** CRC of parameters from address 08_H to $0F_H$. If any settings within these registers are changed, this CRC has to be changed accordingly. Reset: device-specific

1) If auto-calibration is enabled, TCO_Y_T is automatically set to 0. Once auto-calibration is deactivated, laser-fused calibration values are loaded into TCO_Y_T.

X-raw Value Register

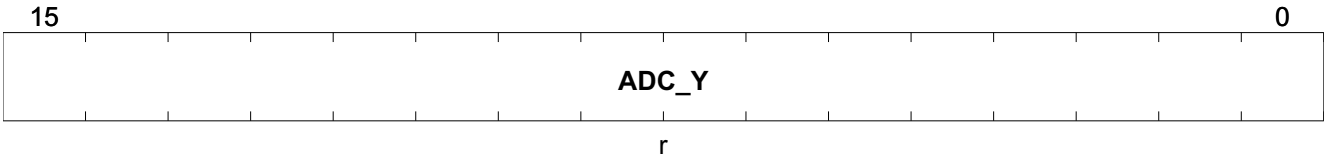
ADC_X	Offset	Reset Value
X-raw value	10_H	0000_H



Field	Bits	Type	Description
ADC_X	15:0	r	**ADC value of X-GMR** Read-out of this register will update ADC_Y Reset: 0_H

Y-raw Value Register

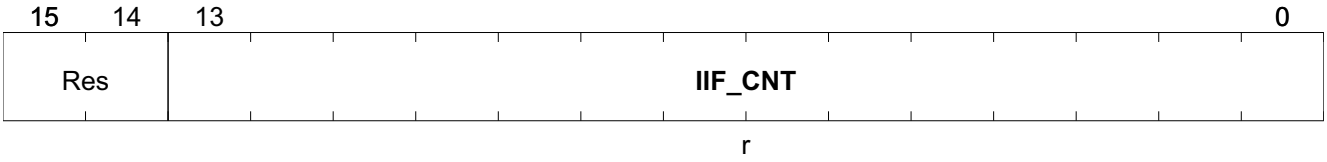
ADC_Y	Offset	Reset Value
Y-raw value	11_H	0000_H



Field	Bits	Type	Description
ADC_Y	15:0	r	**ADC value of Y-GMR** Updated when ADC_X or ADC_Y is read. Reset: 0_H

Increment Counter Register

IIF_CNT	Offset	Reset Value
IIF Counter value	20_H	0000_H



Field	Bits	Type	Description
IIF_CNT	13:0	r	**Counter value of increments** This counter increments or decrements for every pulse on the incremental interface, depending on the rotation direction. It can be used for synchronization purposes between sensor and counter value on microcontroller side. Reset: 0_H

2.2 Communication Examples

This chapter gives some short SPI communication examples. The sensor has to be selected first via CSQ, and SCK must be available for the communication.

Table 3 SSC Command to read the angle value

SSC Word No.	Description	Master transmitting	TLE5012B transmitting	Note
1	Command	1_0000_0_000010_0001		R/W_Lock_UPD_ADD_ND
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle value
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

Table 4 SSC Command to read angle speed and angle revolution

SSC Word No.	Description	Master transmitting	TLE5012B transmitting	Note
1	Command	1_0000_0_000011_0010		R/W_Lock_UPD_ADD_ND
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle speed
3	Read Data		1_xxxxxx_xxxxxxxxx	Read angle revolution
4	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

Table 5 SSC Command to change Interface Mode2 register

SSC Word No.	Description	Master transmitting	TLE5012B transmitting	Note
1	Command	0_1010_0_001000_0001		R/W_Lock_UPD_ADD_ND
2	Write Data	0_00010000000_1_0_01		ANG_Range: 080_H; ANG_DIR: 1_B; PREDICT: 0_B; AUTOCAL: 01_B
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

3 Fuse Values

The derivate specific reset values for the configuration registers, which are stored in laser fuses on the sensor are shown in **Figure 1**.

Interface Mode2 Register / Interface Mode3 Register

	ang_range										ang_dir	predict	autocal		spikef	ssc_od	pad_drv	
TLE5012B - E1000 (IIF)	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
TLE5012B - E3005 (HSM)	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0
TLE5012B - E5000 (PWM)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
TLE5012B - E5020 (PWM)	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0
TLE5012B - E9000 (SPC)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
TLE5012B - E9010 (SPC)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
	msb								*lsb*				*msb*	*lsb*			*msb*	*lsb*

Temp. Coeff. Reg.

IFAB Register / Interface Mode4 Register

	sbist	fir_udr	ifab_od	ifab_hyst		hsm_plp				ifab_res		if_mod	
TLE5012B - E1000 (IIF)	1	1	0	1	1	0	0	0	1	0	0	0	0
TLE5012B - E3005 (HSM)	1	1	0	1	1	0	1	0	0	0	0	1	0
TLE5012B - E5000 (PWM)	1	0	0	0	0	0	0	0	0	0	0	0	1
TLE5012B - E5020 (PWM)	1	1	1	0	0	0	0	0	0	1	1	0	1
TLE5012B - E9000 (SPC)	1	0	1	0	0	0	0	0	0	0	0	1	1
TLE5012B - E9010 (SPC)	1	0	1	1	1	0	0	0	0	0	0	1	1
				msb	*lsb*	*msb*			*lsb*	*msb*	*lsb*	*msb*	*lsb*

Interface Mode1 Register

	FIR_MD		CLK_SEL	DSPU_HOLD	IIF_MOD	
TLE5012B - E1000 (IIF)	0	1	0	0	0	1
TLE5012B - E3005 (HSM)	0	1	0	0	0	0
TLE5012B - E5000 (PWM)	1	0	0	0	0	0
TLE5012B - E5020 (PWM)	0	1	0	0	0	0
TLE5012B - E9000 (SPC)	1	0	0	0	0	0
TLE5012B - E9010 (SPC)	1	0	0	0	0	0
	msb					*lsb*

Figure 1 Derivate-specific fuse settings

w w w . i n f i n e o n . c o m

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