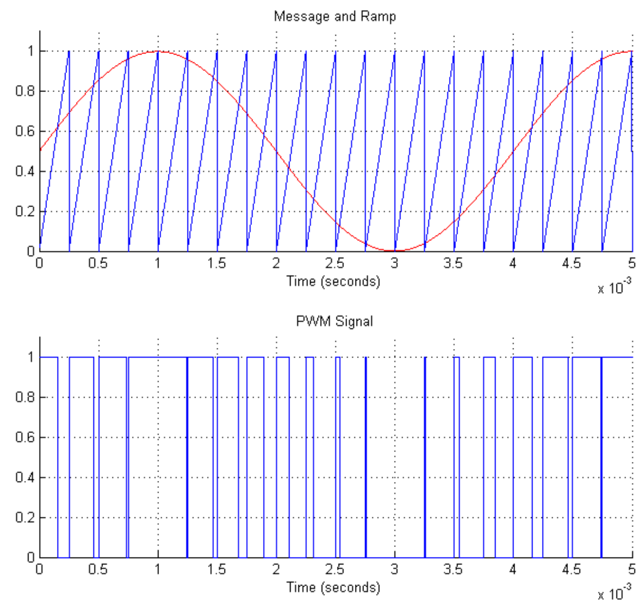
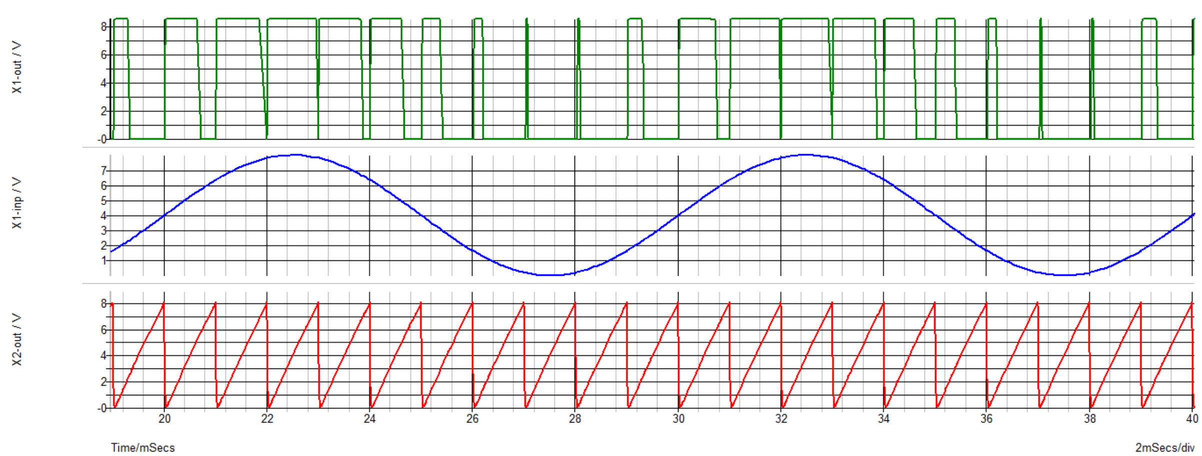
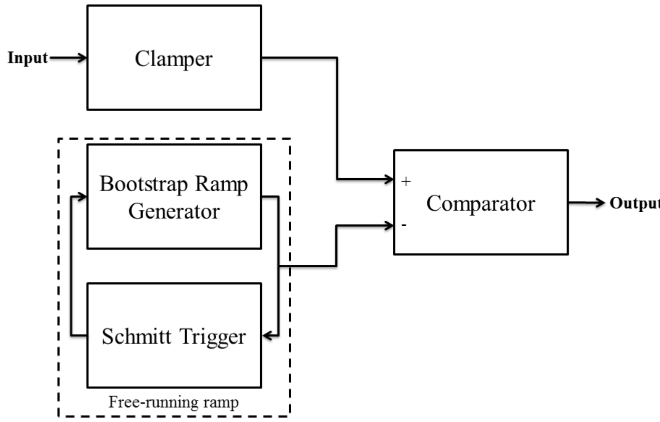
EEE 54 Design Problem 2
Pulse Width Modulator

Pulse Width Modulation (PWM) is a technique that encodes messages into pulses by modulating the duration or width of the pulse. It is also known as Pulse Duration Modulation (PDM). Although it is a technique for encoding and transmission, it is widely used for motor control and many other industrial applications. Below is a sample PWM signal compared to the message and ramp plotted in MATLAB and Simulated in SIMetrix.





You are to design a PWM modulator with varying sampling frequency. Notice how the samples are defined by the time when the ramp resets to zero. Below is the complete block diagram of a Pulse Width Modulator Circuit. It consists of a ramp generator, clamper, and comparator.



The clamper levels the input signal to a DC level that the most negative component of the signal is at zero. It also acts as a high-pass filter. The output of the ramp generator is a ramp waveform, which in turn, is the input of the Schmitt Trigger. The ramp generator output is also the output of the free-running ramp. The comparator is simply an operational amplifier that should have a fast switching time.

The source DC voltage is from -12 V to 12 V. The output of the comparator should be from 0 V to approximately 10 V to 12 V. The specifications of your circuit depend on your student number. If your student number is 20XX–ABCDE, digits CDE determine the specifications of your ramp generator.

Third digit, C (Peak to peak voltage):

C	V_{MIN}	V_{MAX}
0	-10	-5
1	-10	-2
2	-10	0
3	-5	0
4	-5	5
5	0	4
6	0	8
7	0	10
8	1	5
9	5	10

Fourth and Fifth digits:

D	f_{MIN} (kHz)	E	f_{MAX} (kHz)
0	1.00	0	6.00
1	1.00	1	6.25
2	1.50	2	6.50
3	1.50	3	6.75
4	2.00	4	7.00
5	2.00	5	7.25
6	2.50	6	7.50
7	2.50	7	7.75
8	3.00	8	8.00
9	3.00	9	8.25

For example, if the student number is xx-07580, the sawtooth waveform should be from 0 to 4 V (C = 5), and the frequency should be from 3 kHz (D = 8) to 6 kHz (E = 0)

Requirements:

1. Implement a pulse width modulator. Refer to the specs above.
2. You can implement the operational amplifiers with ICs or any transistors.
3. Soldered boards are recommended but not required. You can use pin headers to easily change resistors and transistors.

Checking:
Each component of the block diagram will be checked with a total of 100 points and a corresponding weight is given to them for the final score. Refer to the table below:

Component	Specifications	Guidelines	Points Given
Clamper (10%)	Input: $V_{in}(t) = V_{pp}\sin(2\pi f t) \quad f_{min} \leq f \leq f_{max}$ $V_{pp} = V_{max} - V_{min}$ The DC level of the output must correspond to: $V_{DC} = \frac{V_{max} + V_{min}}{2} \pm 5\%$	Within 5% of spec	**100**
		Greater than 5% but less than 10% of spec	-70 points
		Greater than 10% of spec	-100 points
Bootstrap Ramp Generator (35%)	Using a step input: The time difference between V_{max} and V_{min} is measured and it should correspond to: $\Delta t = \frac{V_{max} - V_{min}}{f} \pm 5\% \quad f_{min} \leq f \leq f_{max}$	Within 5% of spec	**100**
		For every 1% excess	-10 points
		For significant jitters and spikes (around 3%)	-1 point
		Minimum score	10
Schmitt Trigger (25%)	Input: $V_{in}(t) = \left(V_{pp} - 1\right)\sin(2\pi f t) + \frac{V_{max} + V_{min}}{2}$ $f_{min} \leq f \leq f_{max}$ Output: 50% duty cycle square wave.	Within 5% of spec	**100**
		Greater than 5% but less than 10%	-70 points
		Greater than 10% of spec	-90 points
Comparator (10%)	Positive Input: $\sin(2\pi f t) + V_{DC}, f_{min} \leq f \leq f_{max}$ Negative Input: $V_{DC} = \frac{V_{max}+V_{min}}{2}$ Expected output: Square wave from $0 \pm 0.1\, V$ to approx. 10 to 12 V	ALL OR NOTHING	**100**
Final Working Circuit (10%)	$V_{pp} = V_{max} - V_{min}$. Test inputs and expected outputs: In1: $V_{in}(t) = V_{max} - 0.1V_{pp}$ Out1: rectangular wave with duty cycle equal to 90% (**40 points**) In2: $V_{in}(t) = V_{min} + 0.1V_{pp}$ Out2: rectangular wave with duty cycle equal to 10% (**40 points**) In3: $V_{in}(t) = V_{pp}\sin(200\pi t)$ Out3: $V_{out}(t) = PWM\ signal$ (**20 points**)	For DC inputs, Duty cycle is not within 89% to 91% Duty cycle is not within 9% to 11% For sine input, Significant jitters and spikes Minimum	**100** -25 points -25 points -5 point 0
Docu (10%)		Maximum	**100**
		Minimum	50
		Early Submission	+10%

Each category has a total of 100 points.

TOTAL	100
Maximum	110
Minimum	14