Enhancing general performance of folded cascode amplifier by recycling current

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A modification to the conventional folded cascode transconductance amplifier is proposed. The proposed amplifier has the benefit of achieving a given set of design specifications while consuming a fraction of the power compared to the conventional folded cascode. Moreover, the proposed modification is robust even for low voltage applications.

Introduction: A major building block of analogue integrated circuits is the operational transconductance amplifier (OTA), which for many applications is the most power consuming block. Recently, the folded cascode (FC) amplifier has gained preference over the telescopic owing to the low voltage nature of present and future CMOS technologies, despite the higher power budget. In addition, the PMOS driven FC has become the optimal choice for its lower flicker noise, higher non-dominant poles and low input common/mode level, which makes input switching using a single NMOS transistor possible [1, 2]. However, the choice comes at the expense of increased input capacitance and power. In this Letter, a modification to the FC aims to resolve its power limitation by recycling the bias current of idle transistors. This is done at virtually no expense in performance.

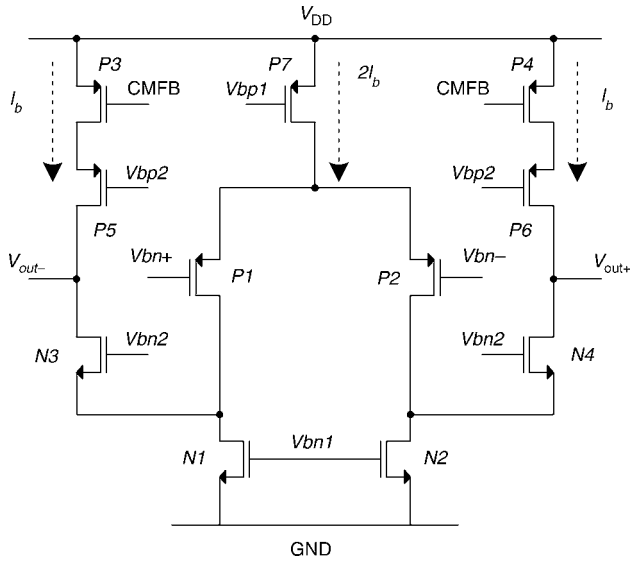

Fig. 1 *Conventional folded cascode*

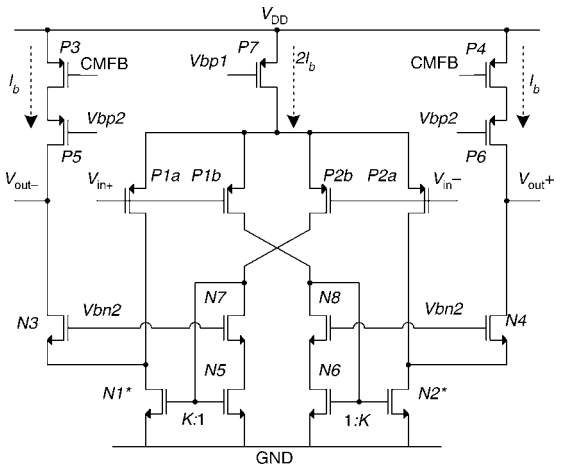

Fig. 2 *Recycling folded cascode*

Recycling folded cascode (RFC): The conventional FC is shown in Fig. 1. Note that transistors *N1* and *N2* conduct the most current and thus have the largest transconductance, yet act as current sinks only. Previous work to enhance the performance of the FC exploited multipath schemes [3]. However, *N1* and *N2* were left unexplored. Another multipath scheme was applied to the three-current-mirror OTA [4] to specifically enhance the output impedance and slew rate, but was not suitable for high-speed applications as the open loop transfer function of the OTA had numerous pole-zero pairs. Nonetheless, [3] and [4] form the basis of the proposed RFC amplifier, which is shown in Fig. 2.

The modifications present in Fig. 2 are intended to use *N1* and *N2* as driving transistors. First, the original drivers, *P1* and *P2* in (Fig. 1), are split in half to produce transistors *P1a(b)* and *P2a(b)* in Fig. 2. Each pair of *P1a(b)* and *P2a(b)* is driven by the same input and thus the input capacitance remains the same as in Fig. 1. Next, the diode connected pair *N5* and *N6* (Fig. 2) is used to make a cross-over and drive *N1** and *N2**, such that the small signal currents added at the sources of *N3* and *N4* are in phase. The ratio of *N1* to *N1** and *N2* to *N2** as shown in Figs. 1 and 2 is 4:3 to maintain the correct summation of DC currents. Therefore the current mirror factor K in Fig. 2 is 3. Now it can be shown that the low frequency transconductance of the RFC is expressed as in (1), which for $K=3$ and $gm_{P1}=2gm_{P1a}$, makes the transconductance of the RFC twice that of the FC for the same current consumption:

$$Gm_{RFC} = gm_{P1a}(1+K) \tag{1}$$

Given the proposed modifications, the slew rate is also improved. Let us first consider the FC. Assuming a load CL, the slew rate of the FC can be derived from Fig. 1 as I_b/CL. Now consider the RFC when a large signal is applied as an input. As Vin+ approaches V_{DD}, transistors *P1a* and *P1b* shut off, which forces transistors *N6*, *N2** and *N4* to shut off. Hence the total current available to charge the capacitance at Vout+ is I_b and is provided by *P4*. On the other hand, with *N2** and *N4* off, *P2a* also shuts off and all the tail current, $2I_b$, is forced to flow through *P2b*. This current is in turn mirrored from *N5* to *N1** by a factor of 3. Hence, *P3* is sourcing I_b while *N1** is sinking $6I_b$, resulting in the capacitance at Vout− being discharged by $5I_b$. This differential imbalance in the charging and discharging of Vout+ and Vout− is quickly converted to a common-mode error and fixed by the common-mode feedback (CMFB), and the result is a maximum symmetrical slew rate of $3I_b/CL$, triple that of the FC. In design, however, the slew rate will be restricted by the size and biasing conditions of *N3* and *N4*, which will limit the slew rate to a smaller value, especially for low voltage implementations (1.2 V or less). The last remaining additions in the RFC are the transistors *N7* and *N8*. Their inclusion is necessary to ensure accurate mirroring in *N5*, *N1** and *N6*, *N2**.

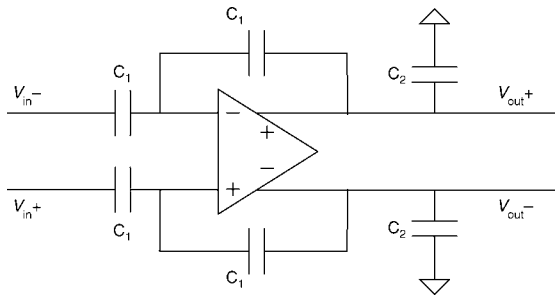

Fig. 3 *Unity gain capacitive buffer*

Implementation and results: The improvements seen in the RFC are critical when power is of concern. Since the RFC is capable of delivering twice the transconductance and better slew rate compared to the FC for equal power budgets, then it is capable of delivering a similar performance to the FC for less power. Two amplifiers, an FC and an RFC, were designed for the same gain bandwidth product (GBW) specification in a standard 0.18 µm CMOS technology using minimum channel length for speed, and using a single supply of 1.2 V (low voltage). The amplifiers were biased with the same circuitry and had the same CMFB implementation. Both the FC and RFC were used as a unity gain capacitive amplifier, as seen in Fig. 3, driving a total capacitive load of 1 pF ($C_1=1$ pF, $C_2=0.5$ pF). The AC and transient responses are shown in Figs. 4 and 5, respectively, and a list of various key parameters is found in Table 1. Note how both the FC and the RFC have almost the same GBW, but the RFC consumes half the power of the FC. Despite this power reduction both the FC and RFC experience practically the same slew rate as seen in Fig. 5. Also, since the RFC uses less overall current, the output conductance of the

transistors is smaller, and that is reflected in an increased DC gain and reduced static error. As for the phase margin, the slight degradation is due to the pole-zero pair of the NMOS current mirror. Finally, the settling time improvement in the RFC is due to the slightly higher GBW.

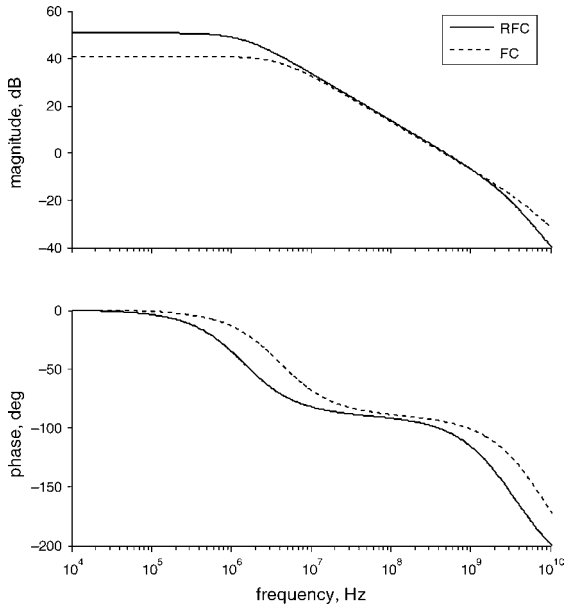

Fig. 4 *AC response of conventional folded cascode and recycling folded cascode*

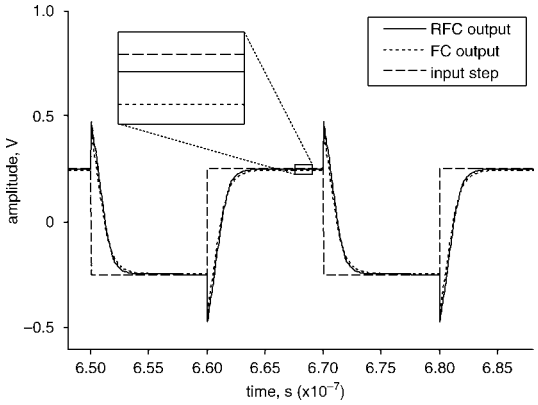

Fig. 5 *Transient response of conventional folded cascode and recycling folded cascode to differential 50 MHz, 500 mVpp step*

Table 1: Performance summary of conventional folded cascode and recycling folded cascode

Parameter	Folded cascode	Recycling folded cascode
C_L (pF)	1	1
GBW (MHz)	467.7	**489.8**
Power (μA)	1185	**551**
Gain (dB)	41.1	**50.9**
Phase margin (deg)	**85.1**	77.2
0.1% setting time (ns)	5.7	**5.1**
Static error (%)	2.04	**0.61**

Conclusion: A modified folded cascode was proposed to improve general performance without sacrificing power. Using a capacitive unity gain amplifier as an example, simulation results show that the newly proposed RFC can achieve the same specifications, with fewer static errors, but for half the power.

30 September 2007
Electronics Letters online no: 20072031
doi: 10.1049/el:20072031

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