An Improved Recycling Folded Cascode Amplifier with Gain Boosting and Phase Margin Enhancement

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***Abstract*—An improved recycling folded cascode operational transconductance amplifier with gain boosting and enhanced phase-margin is proposed. Among four variants of folded cascode amplifiers that have been implemented in TSMC 0.18μm CMOS process under same power and area constraints, the proposed amplifier achieves the lowest settling error of less than 0.5% compared to 1.1% settling error by Improved Recycling Folded Cascode (IRFC), 1.4% settling error by Recycling Folded Cascode (RFC) and 30% settling error by conventional Folded Cascode (FC) amplifier. This performance enhancement is attributed to 30dB increment in low-frequency gain and 7° improvement in the phase margin when compared with the second best performing Improved Recycling Folded Cascode amplifier.**

***Keywords* - Improved recycling folded cascode amplifier, Gain boosting, phase margin enhancement.**

I. Introduction

Folded Cascode amplifier is one of the most commonly used OTA architecture for switched-capacitor (SC) applications in modern CMOS processes. In high speed ADC applications, telescopic and folded-cascode amplifiers are the preferred design choice for their large DC gain, high unity-gain frequency (GBW) and low noise characteristics. Telescopic OTA is more power efficient than folded cascode but offers less output voltage swing since it incurs one extra overdrive voltage. Folded cascode, on the other hand, achieves higher output swing but consumes more power because of an added input branch. For higher output swing reason alone folded cascode OTA has become optimal design choice in current and future CMOS processes where supply voltage is being consistently scaled to lower values.

To address the issue of power efficiency, [2] proposed Recycling Folded Cascode amplifier which recycles the tail current back into the input differential pair and boost the input transconductance to achieve large increase in unity gain frequency and moderate improvements in DC gain, slew rate and input referred noise [1]. The conventional folded cascode amplifier is shown in Fig. 1. The tail transistors $M3$ and $M4$ carry large current which is recycled by first splitting the input pair $M1$,$M2$ into equal halves $M1a$, $M1b$ and $M2a$, $M2b$ and the tail transistors $M3$ and $M4$ to form current mirrors $M3a$:$M3b$ and $M4a$:$M4b$ with a ratio K:1 as shown in Fig. 2. By choosing the value of $K = 3$, 200% improvement in UGBW and approximately $10dB$ increment in DC gain could be achieved. The only drawback is reduced phase margin by introducing extra pole-zero pairs at the gate terminals of the current mirror.

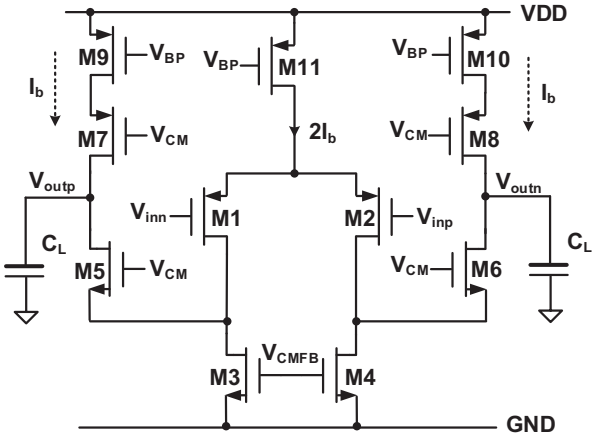

Fig. 1. Conventional Folded Cascode (FC) Amplifier.

Y. L. Li et al. [3] proposed further improvements in the recycling folded cascode structure by separating the AC path from DC path. As shown in Fig. 3 transistors $M3b$ and $M4b$ are further split into $M3b$,$M3c$ and $M4b$, $M4c$. Their cascodes $M12$ and $M13$ are also split into $M12a$, $M12b$ and $M13a$, $M13b$ to maintain equal drain potentials for improved matching. These modifications allow higher value of K without adversely affecting the phase margin by enabling lower current and thereby reduced sizing and MOS capacitance of transistors $M3b$ and $M4b$. Thus an enhanced input transconductance and output impedance is achieved within same area and power budget. However, phase margin of this amplifier is exacerbated by the addition of extra high impedance nodes.

In switched capacitor applications, settling speed is determined by the unity-gain frequency and phase margin while settling accuracy depends upon DC gain of the OTA. The recycling and improved recycling techniques boost the transconductance of OTAs by multiple times and achieve very high GBW values in power efficient way. However, the DC gain is not enhanced by similar amount on dB scale. Recently, many authors have tried to address this issue.

Zhao et al. [4] proposed to boost the output impedance by employing positive feedback in the output stage of RFC but in doing so the output swing is reduced by an overdrive voltage which may become unacceptable in low-voltage processes.

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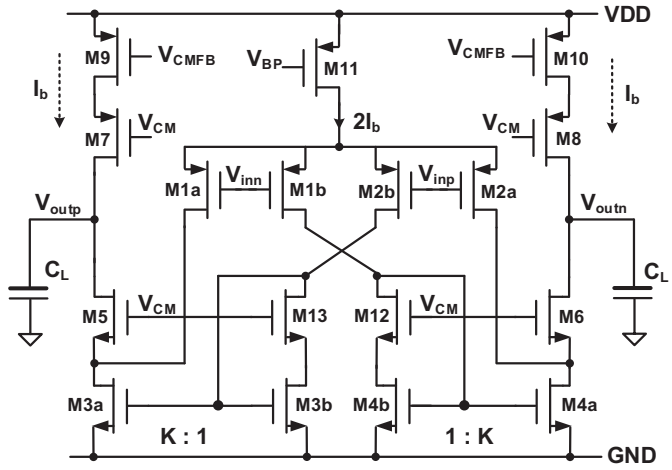

Fig. 2. Recycling Folded Cascode (RFC) Amplifier [2]

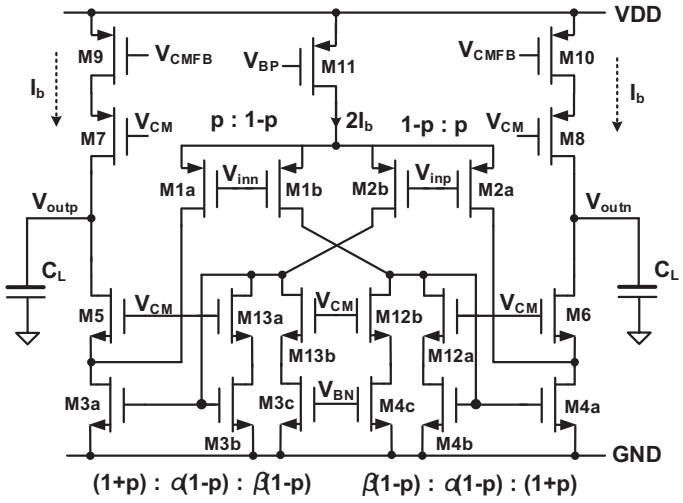

Fig. 3. Improved Recycling Folded Cascode (IRFC) Amplifier [3]

Farahmand et al. [6] increase the gain without sacrificing output voltage swings but her method based on exploiting positive feedback introduce several poles and requires careful circuit design to avoid instability. Besides them, several authors have presented gain enhancement techniques based mostly on positive feedback which require judicious circuit design as the OTA could easily become unstable due to PVT variations, predominantly so in scaled CMOS processes.

We propose a robust gain-boosting technique by adding single-stage amplifiers with the cascode pairs of the Improved Recycling Folded Cascode (IRFC) OTA and achieve more than 30dB increment in gain without introducing positive feedback or compromising stability. The paper is organized as follows: In section II, the proposed gain-boosted improved recycling folded cascode OTA is briefly explained. Section III covers the simulation results and comparison summary of the four implemented OTA topologies. Section IV concludes the paper.

II. Proposed Gain Boosted IRFC

The proposed OTA architecture based on Improved Recycling Folded Cascode structure with gain-boosting and phase margin enhancement is shown in Fig. 4. We propose to enhance the gain of IRFC using gain-boosting technique first demonstrated by [7]. Furthermore, we improve the phase margin by introducing transistors Mx, Mz that operate in triode region and cancel the non-dominant poles at current mirror nodes A and B; thus bringing the first non-dominant poles to the folding nodes C and D as in the case of conventional folded cascode amplifier [5].

The gain-boosting principle works by increasing the output resistance of the casocode pairs $M5$, $M6$ and $M7$, $M8$ as shown in Fig. 4. The boosted resistance as seen from the drain of cascode $M6$, while ignoring the resistance of input branch at this moment, is given by:

$$R_{D6} = (g_{m6} r_{ds6}(1 + A_{M20}) + 1) r_{ds4a} \tag{1}$$

where A_{M20} is the gain of transistor $M20$ which is connected in common-source configuration and serves as an auxiliary amplifier. Similar analysis applies to the other three cascodes too. The auxiliary amplifiers are implemented using low threshold transistors $M14$, $M15$, $M20$ and $M21$, while transistors $M16$, $M17$, $M18$ and $M19$ serve as their current load. The total output resistance of the proposed architecture is:

$$\begin{aligned} R_{out} =& \gamma (g_{m6} r_{ds6}(1 + A_{M20}) + 1) r_{ds4a} || \\ & (g_{m8} r_{ds8}(1 + A_{M14}) + 1) r_{ds10} \end{aligned} \tag{2}$$

where A_{M14} is the gain of the auxiliary common-source amplifier M_{14}. Following the treatment in [8] γ can be shown as:

$$\begin{aligned} \gamma =& \left[\frac{(\alpha + \beta)(1 - p) + (1 + p)}{-(\alpha + \beta)(1 - p) + (1 + p)} \right] r_{ds2a} || \\ & \left[\frac{(\alpha + \beta)(1 - p) + (1 + p)}{(1 + p)} \right] r_{ds4a} \end{aligned} \tag{3}$$

We assume that net transconductance of the IRFC remains unchanged by adding gain-boosting devices (an assumption validated by simulation results as both amplifiers achieve similar GBW values). Hence, total gain of the proposed amplifier becomes:

$$A_{IRFC_{GB}} = G_{mIRFC} \times R_{out} \tag{4}$$

where R_{out} is given by Eq. 2 and G_{mIRFC} is expressed by [3] as:

$$G_{mIRFC} = [p + \frac{(1 + p)}{\alpha}] G_m \tag{5}$$

G_m here represents the transconductance of conventional folded cascode amplifier.

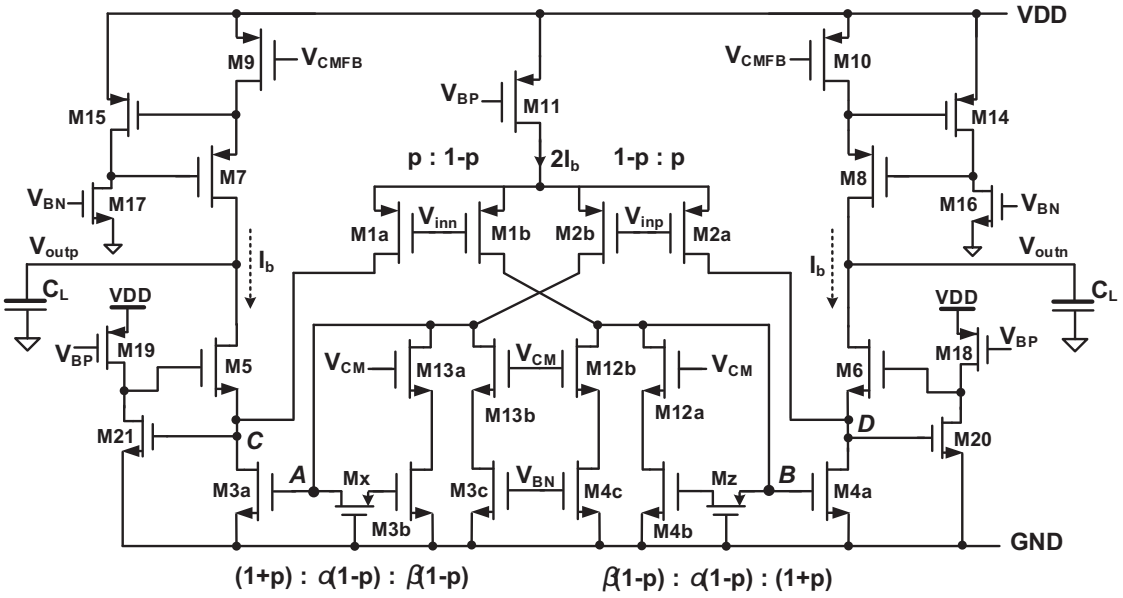

Fig. 4. Proposed Gain-Boosted Improved Recycling Folded Cascode (IRFC GB) Amplifier.

III. Simulation results

All four variants of folded cascode amplifier discussed thus far, have been realized in TSMC $0.18\mu m$ CMOS process under same power and area constraints. For implementing the RFC OTA, K is set to be 3 while in IRFC and proposed architecture, $\alpha = \beta =$ p$= \frac{1}{2}$. Post-layout simulations were carried out across process corners to ascertain fair comparison among four topologies. As shown in Fig. 5 the conventional folded cascode OTA exhibits the lowest DC gain, as expected, followed by recycling folded cascode (RFC) and improved recycling folded cascode (IRFC) amplifiers. The proposed architecture achieves the highest DC gain thanks to gain-boosting principle. Fig. 6 shows the phase margin response which illustrates that simple folded cascode amplifier exhibits excellent phase margin due to lower number of circuit nodes while other architectures suffer due to increased pole-zero pairs introduced by additional circuit nodes. However, the phase margin of proposed amplifier has been improved by adding the triode operated pair Mx, Mz which cancels the pole at current mirror nodes A and B.

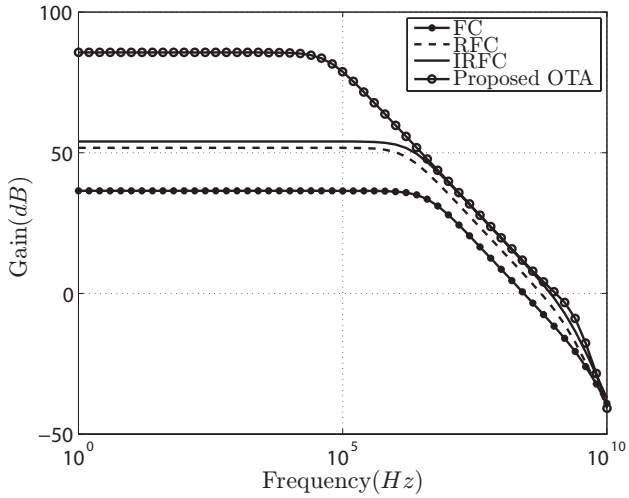

Fig. 5. Simulated DC Gain of the proposed OTA along with IRFC, RFC and conventional FC OTA.

To validate the settling performance for $10bit$, $50MS/s$ pipeline ADC, the closed-loop test is carried out with $2.5bit/stage$ MDAC architecture where the input stimulus is set to be $200mV$ and expected output is $800mV$ because of closed-loop gain of 4. The sampling capacitors ($200fF$ each) and output capacitance representing the next stage load ($840fF$) are so chosen that each OTA sees a net capacitive load of $1pF$. As shown in Fig. 7, the folded cascode amplifier performs worst among all due to extremely low-gain and unity gain frequency while other three topologies exhibit better settling behavior. The proposed amplifier architecture outperforms all by settling to within 0.5% error due to its large DC gain and improved phase margin as shown in Fig. 8.

Table I presents the performance comparison of the proposed OTA against previously reported amplifier architectures. As a downside, the proposed amplifier exhibit higher noise and offset voltage. When integrated from $1Hz$ to $100MHz$, the input referred noise of the gain-boosted IRFC increased by 18 % compared to IRFC. This noise increment is attributed to lower device sizing of the input differential pair and tail current-mirrors in order to create space for the gain-boosting auxiliary amplifiers so that fix power and area constraints remain satisfied. Similarly, the minor increase in offset voltage is caused by the splitting of input pair and current mirror into smaller transistors but offset voltage do not matter as we employ an autozero MDAC stage which cancels the offset voltage to insignificant level. For higher resolution ADC and precision instrumentation amplifiers, techniques such as correlated double sampling and chopping are preferably used to alleviate noise and offset issues.

TABLE I. PERFORMANCE COMPARISON OF THE FOUR OTAS IMPLEMENTED IN TSMC $0.18\mu m$ CMOS PROCESS.

Parameters	Proposed OTA	IRFC [3]	RFC [2]	Conventional FC
Supply voltage (V)	1.8	1.8	1.8	1.8
Bias current (mA)	1	1	1	1
Layout Area (μm^2)	27 x 50	27 x 50	27 x 50	27 x 50
Capacitive load (pF)	1	1	1	1
DC Gain (dB)	85.6	54	51.7	43.7
GBW (MHz)	987	965	593.8	284.3
Phase margin $(degree)$	66.7	62	71.8	88
Input referred noise $(1Hz - 100MHz)$ (μV_{rms})	118	100.7	91.74	95
Settling error (%)	0.46	1.1	1.4	30

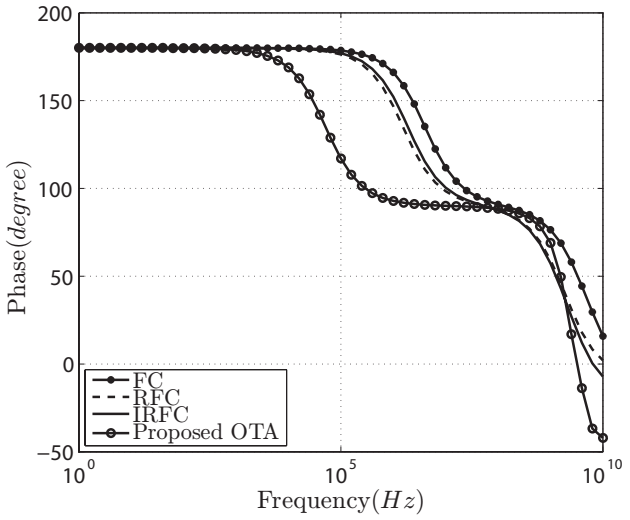

Fig. 6. Simulated phase plot of the proposed OTA along with IRFC, RFC and conventional FC OTA.

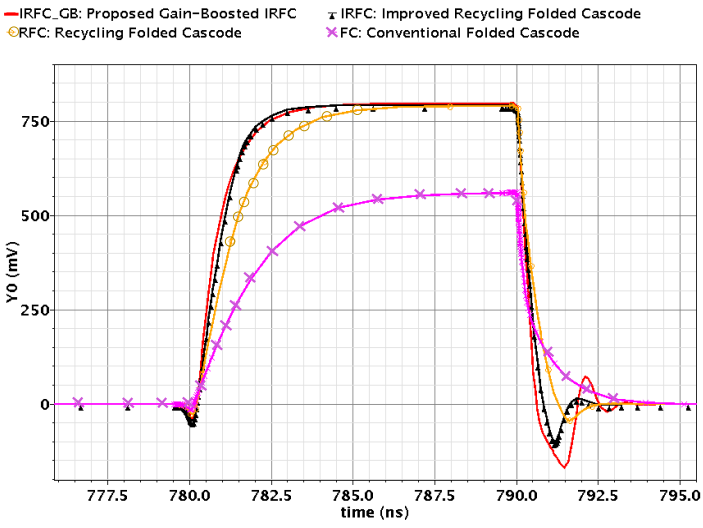

Fig. 7. Simulated settling behavior of the proposed IRFC GB OTA along with IRFC, RFC and conventional FC OTAs.

IV. CONCLUSION

We present a robust, gain-boosted recycling folded cascode amplifier that achieves superior AC and transient performance when compared to three other topologies namely Folded Cascode (FC), Recycling Folded Cascode (RFC) and Improved Recycling Folded Cascode (IRFC) OTAs. For fair comparison, the four amplifiers have been realized in TSMC $0.18\mu m$ CMOS process using the same power and area budget. When simulated in $2.5bit$ MDAC stage for $10bit$, $50MS/s$ pipeline ADC prototype, the proposed amplifier settles with less than 0.5% error as compared to IRFC which settles with 1.1% error, RFC that settles with 1.4% error and conventional FC amplifier which settles with 30% settling error exhibiting the worst performance among all.

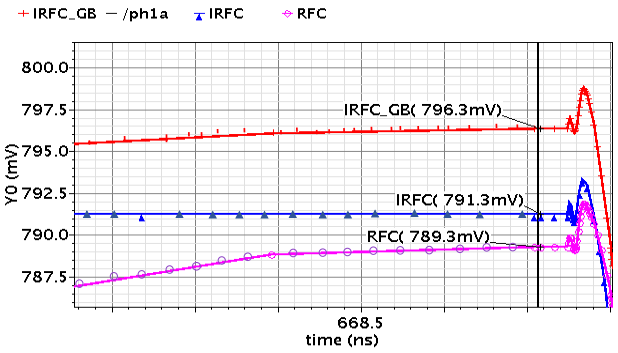

Fig. 8. Zoomed settling behavior of the three better performing OTAs. Note that IRFC GB here represents the proposed amplifier.

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