1 V rail-to-rail constant-g_m CMOS op amp

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A 1 V rail-to-rail constant-g_m CMOS operational amplifier is proposed. This study shows that keeping the sum of currents in the complementary differential pairs constant rather than controlling the tail currents produces a constant-g_m input stage operating in the weak inversion. The currents in the n-channel differential pair are regulated to keep the sum of currents in the complementary differential pairs constant using a negative feedback loop. This study also provides experimental results obtained from a 0.35 μm CMOS prototype chip.

Introduction: Designing ultra-low supply voltage analogue circuits for portable electronic products has several challenges. This is particularly true for designing a low-supply rail-to-rail CMOS operational amplifier (op amp) [1–3]. A well-known method for producing a rail-to-rail input stage is to connect a p-channel and an n-channel differential pair in parallel. At least one of the two differential pairs is thus active for any input common-mode level. However, this input stage produces twice the normal transconductance (g_m) when both differential pairs are active. The large g_m variation prevents optimal frequency compensation and introduces severe signal distortions [1–3]. Researchers have proposed several methods to achieve a rail-to-rail constant-g_m input stage. These methods are based on controlling the tail currents of the differential pairs. Since the transconductance of an MOS device operating in the weak inversion is proportional to the drain current, a constant g_m can be obtained by keeping the sum of the tail currents of the complementary differential pairs constant. In this study, a constant g_m is achieved by keeping the sum of currents in the complementary differential pairs constant rather than controlling the tail currents.

Proposed circuit: Fig. 1 shows a schematic diagram of the proposed rail-to-rail constant-g_m op amp, which consists of an input stage (M1-M14), an output stage (M15-M16) and a g_m-control circuit (M17-M31). The tail current of the p-channel differential pair is designed to equal that of the n-channel differential pair, i.e. $I_p = I_T$. M11-M12 and M13-M14 are the resistance loads for the n-channel and p-channel differential pairs, respectively. The common-gate amplifiers, M8 and M10, combine and amplify the signals of the complementary differential pairs to the output stage [4]. The output stage is a complementary common-source amplifier.

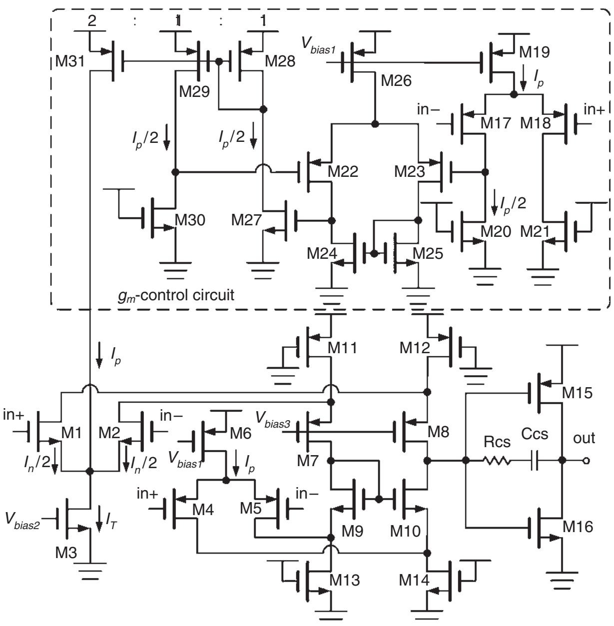

Fig. 1 *Schematic diagram of proposed rail-to-rail constant-g_m CMOS op amp*

The constant g_m is obtained by keeping the sum of currents in the complementary differential pairs constant rather than controlling the tail currents. The differential amplifier, constituted by M17-M21, is a replica of the p-channel differential amplifier, M4-M6 and M13-M14. Hence, the current flowing in the devices of these two amplifiers is equal. A negative feedback loop copies the currents in the replicate differential pair, M17-M18, to the devices, M27-M30. This negative feedback loop consists of a one-stage amplifier, M22-M26, and the current mirrors, M27-M30. By setting the sizes of M31 and M28 at a ratio of 2:1, a same value of the tail current, I_p, of the p-channel differential pair flows into the tail current source, M3, of the n-channel differential pair. The value of I_p depends on the input common-mode voltage (V_{icom}). The currents flowing in the n-channel differential pair can be expressed as:

$$I_n(V_{icm}) = I_T - I_p(V_{icm}) \tag{1}$$

When V_{icom} is in the low-level region, the current flowing in the p-channel differential pair, M4-M5, equals I_p. The same current value of I_p is also flowing in M3. This increases the voltage at the M1-M2 source node, and no current flows in M1-M2. The total current in the complementary differential is then I_T. If V_{icom} increases to the middle range, the currents in M4-M5 and M31 begin to reduce along with the M1-M2 source voltage. The currents in M1-M2 are then increased. However, the sum of currents in the complementary differential pairs is maintained at a constant value of I_T. When V_{icom} further increases to a higher level, no current flows in M4-M5, i.e. the value of I_p becomes zero. The total current in M1 and M2 then increases to the value of I_T. In summary, the currents in the n-channel differential pair are regulated to keep the sum of currents in the complementary differential pairs constant. Since the transconductance is proportional to the device current in the weak inversion, the total g_m of the first stage is constant over the input range.

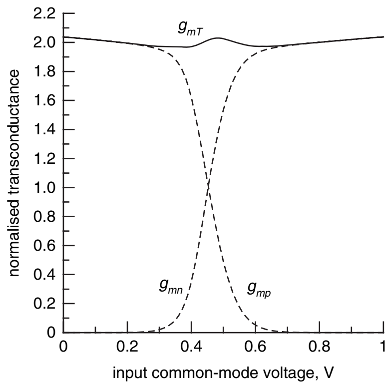

Fig. 2 *Simulated normalised amplifier transconductances against input common-mode voltage*

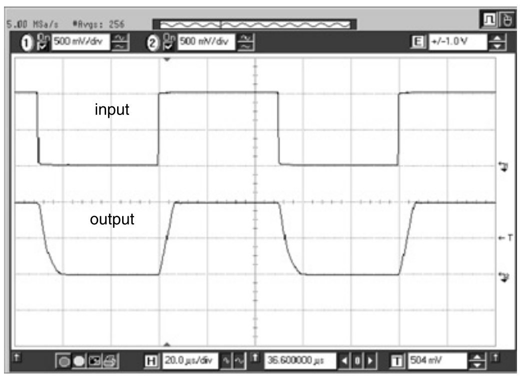

Fig. 3 *Measured step response with input of 1 V amplitude and 10 kHz square wave*

Simulation and experimental results: The proposed amplifier was simulated and fabricated using 0.35 μm CMOS technology. Fig. 2 shows the simulated normalised amplifier transconductances against V_{icom}. Variations in g_m lie within an error interval of $\pm 1.8\%$. The prototype test chip was connected as a unit-gain amplifier with a 1 V single power supply. The test chip was also loaded with a 55 pF capacitor. Fig. 3 shows the measured step response with the input of a 1 V amplitude and 10 kHz square wave. The slew rates are 0.17 and 0.13 V/μs for the rising and falling edges, respectively. Fig. 4 shows the measured magnitude spectrum with the input of a 0.9 V and 10 kHz sinusoidal input waveform. The total harmonic distortion (THD) is −58 dB. Table 1 summarises the performance of the op amp. The figure-of-merit (FOM) of the proposed op amp is much larger than that for previous circuits.

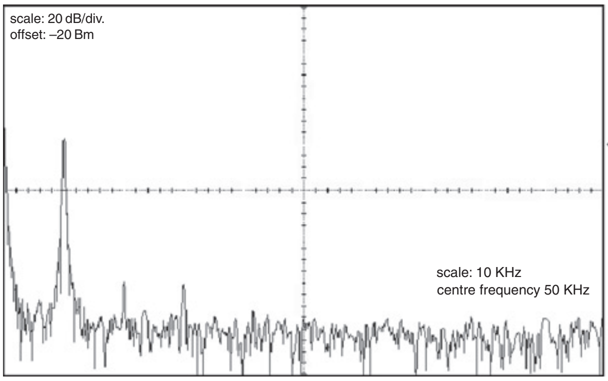

Fig. 4 *Measured magnitude spectrum with input of 0.9 V and 10 kHz sinusoidal input waveform*

Table 1: Performance summary

Authors	[1]	[2]	[3]	This work
Tech. (μm)	2.5	1.2	0.18	0.35
V_{DD} (V)	0.9	1	1	1
Load	12 pF ∥ 1 MΩ	15 pF	5 pF ∥ 10 kΩ	55 pF ∥ 1 MΩ
DC gain (dB)	79	87	53	90
GBW (MHz)	0.0056	1.9	1.3	0.278
Input $V_{p\text{-}p}$ (V)	0.89	0.9	0.6	1
THD (dB)	NA	−54 (0.5 V, 1 kHz)	NA	−58 (0.9 V, 10 kHz)
I_{supply} (μA)	0.5	410	40	15.6
Area (mm^2)	0.5	0.8	NA	0.1
FOM	13	7	16	98

FOM = $(100 \times \mathrm{GBW} \times C_L/I_{supply})$

Conclusion: A 1 V rail-to-rail constant-g_m operational amplifier is presented. The complementary differential pairs of this amplifier have a constant transconductance that varies by ±1.8% for rail-to-rail input common-mode levels. The experimental prototype op amp demonstrates that the circuit draws only 15.6 μA of static current, and exhibits the slew rates of 0.17 and 0.13 V/μs for the rising and falling edges, respectively, under a 55 pF capacitance load. The total harmonic distortion (THD) is −58 dB.

18 March 2009
doi: 10.1049/el.2009.0763

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