Design of 12bit 100MHz Sample and Hold Circuit for Pipeline ADC

Zheng Hao, Fan Xiangning, *Member IEEE,* Sun Yutao,
Institute of RF- & OE-ICs, School of Information Science and Engineering
Southeast University
Nanjing 210096, China

***Abstract*—In this paper, design methods of Sample and Hold (S/H) circuit are discussed and g_m/i_d method in OTA (Operational Transconductance Amplifiers) design is applied. Based upon the discussion, circuit design develops from the signal modeling, which would make circuit design concisely and easily. This work is elaborated in details by TSMC 0.18μm CMOS process. Folding telescope structure is applied for main OTA design, with two gain-boost OPAMPs, in order to achieve high gain and high GBW. In this paper, both main OTA and gain-boost OPAMP are design in g_m/i_d method, and obtain circuit parameters from interpolated data simulated by H-Spice and MATLAB. Post-simulation and chip measurement results show that the S/H circuit performs well.**

Keywords—g_m/i_d method; Gain-boost folding telescope OTA; Slew rate; Flip-around S/H

I. INTRODUCTION

Confronted with the high-speed promotion of ADC technology, wireless transceiver technology, sharing features of flexibility and configurability, which requires transceivers to support a variety of models and communication standards, is becoming the focus within the industry. Moreover, high-speed and high-precision Analog-to-Digital converter (ADC) technology is the key to the wireless transceiver technology [1-3]. Also, as the leading part of pipeline ADC, the performance of Sample and Hold (S/H) circuit has direct impacts on the precision and speed of the whole ADC. In that case, precision and speed are both critical issues should be focused on during circuit design. As the S/H circuit works, with the OTA connected as a negative feedback loop, precision and speed of S/H are close related to open loop gain, slew rate and gain-bandwidth product (GBW) of the OTA. When OTA connected as a negative feedback loop, the static error ε_s (also called absolute error) of S/H is related to $1/A_0$ (A_0 is open loop low-frequency gain of OTA). Thus, static error of S/H will be smaller, if A_0 become larger. For S/H circuit work in sampling cycle, when S/H circuit samples the input signal, the settling time of the sampling is limited, which is determined by sample capacitance C_S and the resistance of switch. However, considering the typical signal behavior of OTA in S/H which works in holding mode, the settling time in holding cycle is determined by slew rate and GBW [4]. As we know, slew rate evaluates the large signal behavior of OTA, and GBW is involved with linear signal settling [5, 6]. If we want to model the signal settling behavior of the S/H in the holding mode, which stands for setting time of the S/H, the slew and linear settling should be joined together consistently. If the holding cycle signal modeling is more precise, the performance and the scale of circuit would be more reasonable.

This paper is organized as follows. Section II describes the basic theory of S/H circuit and g_m/i_d method in general. Section III emphasizes circuit design applying g_m/i_d method, with a simple model describing the signal settling. In section IV, S/H circuit is proposed and it is designed based on TSMC 0.18μm CMOS process, and both simulation and measurement results of the S/H circuit are presented. Section V is the conclusion of this paper.

II. THEORY OF S/H CIRCUIT AND BASIC g_m/i_d METHOD

Fig.1 shows the typical structure of S/H applied in this paper—Flip-Around S/H.

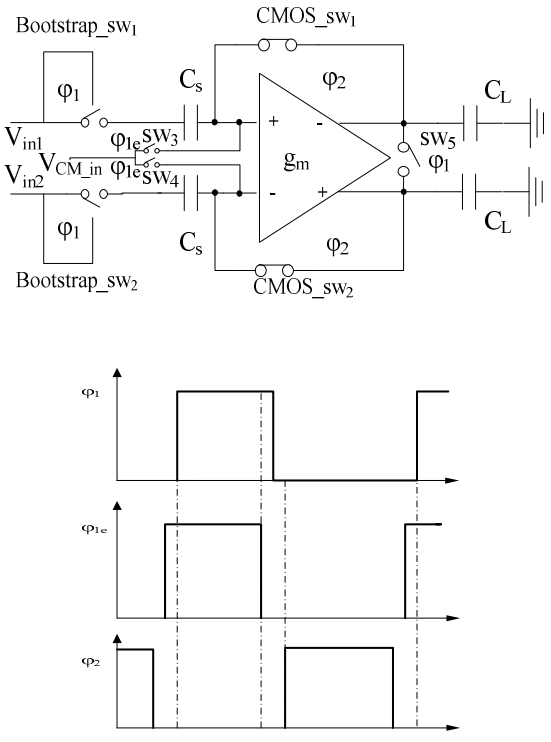


Figure 1. Flip-Around S/H

As Fig.1 shows, if clock φ_{1e} is on with clock φ_2 off, the Bootstrap_sw$_1$, Bootstrap_sw$_2$ turn on. The clock φ_1 is as same as φ_{1e}, but a little bit later than φ_{1e}. After Bootstrap_sw$_1$ sw$_2$

Sponsored by the National Science and Technology Major Project of China (No. 2009ZX03002-004).

978-1-4577-1010-0/11/$26.00 ©2011 IEEE

turning on, the sw_3 and sw_4 turn on. Thus, S/H circuit works in sampling mode. The input signal is reserved in the sample capacitance C_S. This sampling methodology is called Bottom Plate Sampling, in order to reduce the impacts of charge injection and feed through effects of switch transistor.

In the holding mode, $Bootstrap\_sw_1$, $Bootstrap\_sw_2$, together with sw_3, sw_4 are all off, when φ_2 turns on, $CMOS\_sw_1$, $CMOS\_sw_2$ both turn on. OTA is connected as a negative feedback loop, with capacitance C_L served as output loading of the OTA.

The function of S/H in sampling mode is not complicate. THus, the complex trade off design work is concentrated in OTA design, when S/H shift into holding mode. As the section I referred, slew rate, GBW, open loop low-frequency gain of OTA, as well as phase margin are essential design specifications. There should be some trade-off between these features.

g_m/i_d is new design method which is popular recently [7]. It is a methodology which obtains series of specifications of transistor under specific process, using the transistor model document offered by the foundries. Sometimes, these specifications are simulated by H-Spice, and transformed into curves by MATLAB, such as g_m/i_d curve, i_d/w curve, $g_m r_o$ curve, and ft curve. Depending on these curves simulated from the parameters of model, circuit design work will be reasonable.

III. Circuit Design Method

Generally, OTA design takes great importance in the S/H design. Considering large capacitance loading effect and the limit conversion time, the performance of the S/H should be optimized. The main OTA chooses typical folding-telescope structure, with two gain-boost OPAMPs showed in Fig.2.

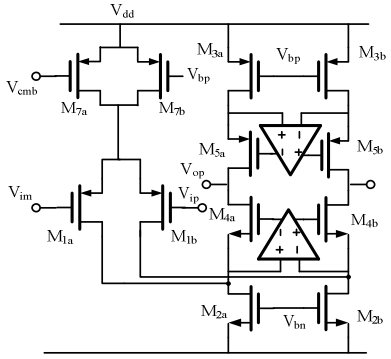


Figure 2. OTA for S/H circuit with two gain-boost OPAMPs

As Fig.2 shows, based on the analyses of section I, the OTA design for S/H should obsess the merits of large GBW with necessary phase margin, high open loop low frequency gain, and ample slew rate. The two gain-boost OPAMPs are used to expand the open loop low frequency gain of OTA, and also expand the GBW. As the structure of OTA is selected, the expression of GBW for the OTA is already fixed [8, 9].

$$GBW=g_m/C_{Ltot} \quad (1)$$

For output load is not concerned with gain-boost OPAMPs, as Fig.3 shows, C_{Ltot} is consisted of output load C_L, parasitic capacitance of C_{db4}, C_{db5} (C_L is consisted of the sample capacitance of next stage and the capacitance of comparator).

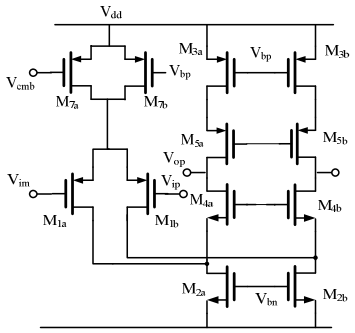


Figure 3. Fold-telescope OTA

The loading capacitance C_L is 2.4pF, and the sample capacitance C_S is 4pF, differential input range $2V_{od}$ is 1200mV with dc 900mV.

A. Gain

According to the structure of the folding-telescope OTA with two gain-boost OPAMPs in Fig.2, the open loop low-frequency gain of the OTA with gain-boost OPAMP is expressed as:

$$A_0 = g_m \cdot \left[(g_m r_o)^3 \cdot \frac{1}{2} r_o \parallel (g_m r_o)^3 \cdot r_o \right] \cong \frac{1}{3}(g_m r_o)^4 \quad (2)$$

If the settling time in infinite, the output of S/H circuit would be expressed as:

$$V_o = V_{in} \frac{1}{1+\frac{1}{A_0\beta}} \approx V_{in}(1-\frac{1}{A_0\beta}) \quad (3)$$

β is the feedback index, which equals C_s/C_s+C_{in}. C_{in} is the parasitic capacitance at the input node.

For obtaining the design value of low-frequency gain, we make static error ε_s equal to dynamic error ε_d, as:

$$\varepsilon_s=\varepsilon_d=\varepsilon/2 \quad (4)$$

And,

$$\varepsilon < \frac{1LSB}{FSR} = \frac{1}{2^{12}} \quad (5)$$

Pick ε_s as:

$$\varepsilon_s = \frac{1}{A_0\beta} \quad (6)$$

Thus,

$$A_0 = \frac{1}{\varepsilon_s \beta} \tag{7}$$

As mentioned in (2):

$$g_m r_o = (4 \bullet \frac{1}{\varepsilon_s \beta})^{\frac{1}{4}} \tag{8}$$

From the Fig.4, which is the curves simulated by H-Spice and MATLAB, $g_m r_o$ should equals or be larger than 14.95, then we choose L=0.24μm as the design Minimum gate length.

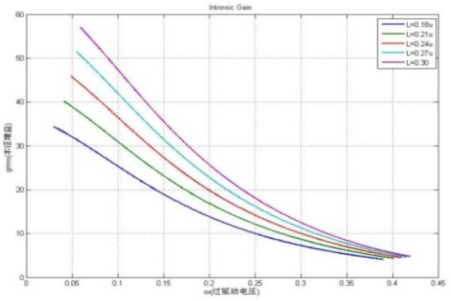


Figure 4. Intrinsic gain for various L

B. Operating Currents

As mentioned in section I, settling time is determined by slew rate and GBW.

If the behavior of signal settling of the OTA could be modeling, the whole process can be described as slewing and linear settling. At the breaking point, where exponential function (linear settling) joins together with linear function (slewing), the two functions should follow one order continuous differentiable [5].

$$V_o(t) = \begin{cases} \frac{2 \bullet I_{d1}}{C_{Ltot}} \cdot t & t < t_{slew} \\ V_{slew} + (V_{final} - V_{slew})(1 - e^{-\frac{t - t_{slew}}{\tau}}) & t > t_{slew} \end{cases} \tag{9}$$

$2I_{d1}/C_{Ltot}$ is the slew rate of the OTA, and I_{d1} is the operating current through the input transistor M_1.V_{slew} is the voltage that slewing reaches till linearity settling begins.

For the whole signal settling should be one order continuous differentiable, the left and right derivative of the breaking point should be equal.

$$\frac{2 \bullet I_{d1}}{C_{Ltot}} = \frac{V_{final} - V_{slew}}{\tau} \tag{10}$$

$$V_{slew} = SR \bullet t_{slew} \tag{11}$$

From (10), (11), the slewing time can be expressed as follows:

$$t_{slew} = \frac{V_{final}}{SR} - \tau \tag{12}$$

The linear settling time can be expressed as:

$$\varepsilon_d = \left| \frac{V_o - V_i}{V_i} \right| = e^{-\frac{t - t_{slew}}{\tau}} \tag{13}$$

$$t_{lin} = t - t_{slew} = -\tau In(\varepsilon_d) \tag{14}$$

As mentioned in section II, settling time can be as follows:

$$\begin{aligned} t_{tot} &= t_{slew} + t_{lin} \\ &= \frac{V_{final}}{SR} - \tau - \tau In(\varepsilon_d) \end{aligned} \tag{15}$$

Considering sampling rate is 100MHz, holding cycle is 5ns, input range $2V_{od}$, the Id1 can be expressed as:

$$I_{d1} = \frac{V_{od} \bullet C_{Ltot}}{\left(\frac{1 + In(\varepsilon_d)}{w_c} + t_s \right)} \tag{16}$$

C. Simulation Curves

According to the (16), the I_{d1} - g_m/i_d, β - g_m/i_d can be draw from simulation data, as showed in Fig.5, Fig.6:

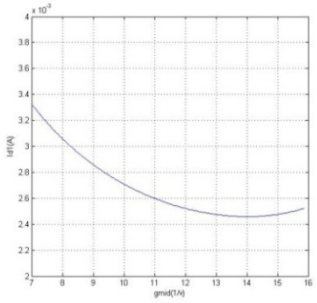


Figure 5. I_{d1} - g_m/i_d curve

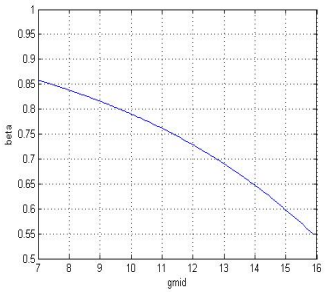


Figure 6. β - g_m/i_d curve

As showed in Fig.5, the operating current of M_1 picks the

minimum value at the point where g_m/i_d equals nearly 14. However, if g_m/i_d equals to 14, the input transistor will be working in weak inversion region, with over drive voltage below 50mV. So, actually in view of the working condition of transistor, we often make g_m/i_d range from 9 to 10, within which the over drive voltage of transistor would be from 100mV to 200mV. In this paper, we make g_m/i_d equal to 9. Thus, from the MATLAB interpolation, the I_{d1} equals to 2.85mA. The feedback index is 0.826.

$$g_{m1} = g_m id_1 \bullet I_{d1} \tag{15}$$

From (15), g_{m1} equals to 25.65ms.

$$C_{gg1} = \frac{g_{m1}}{2\pi f_{T1}} \tag{16}$$

From (16), C_{gg1} equals to 844.258fF.

Thus the GBW and the close loop dominant pole can be expressed as:

$$f_u = \frac{g_{m1}}{2\pi C_{Ltot}} \tag{17}$$

$$f_c = \beta \frac{g_{m1}}{2\pi C_{Ltot}} \tag{18}$$

From (17), (18), f_c=421.857MHz, f_u=510.291MHz

Slew rate is expressed as follow:

$$SR = \frac{2 \bullet I_{d1}}{C_{Ltot}} \tag{19}$$

From (19), SR=712.5v/μs, $\tau=1/2\pi f_c$, put them into formula (15), thus:

t_{slew}=0.67536ns, t_{lin}=3.29748ns, t_{tot}=4.072ns

The total settling time meets the design requirement.

The second pole of OTA which is connected as negative feedback close loop can be expressed as follow:

$$f_{p2} = \frac{g_{m4}}{2\pi C_n} \tag{20}$$

$$C_n = C_{db1} + C_{db2} + C_{db4} \tag{21}$$

Through simulation in H-Spice, C_n evaluates to 701fF, f_{p2}=7.377GHz. Thus the phase margin can be expressed as:

$$PM = \arctan\left(\frac{f_{p2}}{f_{p1}}\right) \bullet \frac{180}{\pi} \tag{22}$$

PM=86.7°, the phase margin meets the design requirement.

D. Design for Two Gain-boost OPAMPs

Referred to [10, 11], unity gain bandwidth of gain-boost OPAMP do relate to the dominant pole of main OTA. The relationship can be expressed as:

$$\beta w_u < w_{au} < w_{o2} \tag{23}$$

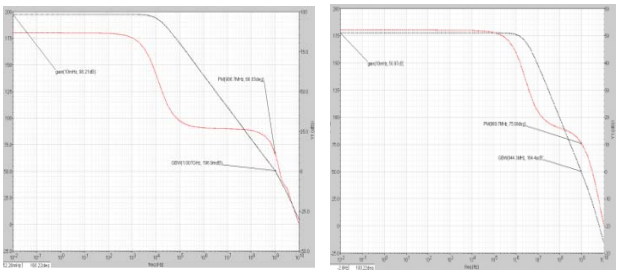
W_u is the GBW of the OTA, W_{o2} is the second pole of OTA, W_{au} is the unity gain bandwidth of gain-boost OPAMP.

The gain-boost OPAMP can also be designed according to the process mentioned in the A, B.

The simulation and the test results will be given in the section IV.

IV. SIMULATION AND TEST RESULTS

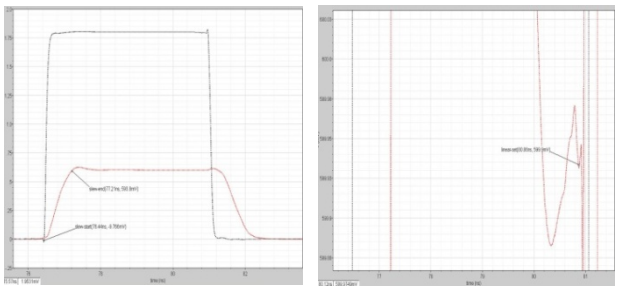
According to the design method mentioned in the section III, the S/H circuit was fabricated in TSMC 0.18μm process.



(a).OTA without gain-boost (b).OTA with gain-boost

Figure 7. The Amplitude-frequency characteristics of OTA.

From Fig.7, the gain of OTA without gain-boost OPAMP is 50.97dB, GBW is 944MHz, PM is 75.9°. Adding gain-boost OPAMP, the gain of the whole OTA is 98.21dB, and GBW is nearly 1GHz, PM is 66.83°.



(a).Slewing time of output (b).Settling precision

Figure 8. The output wave, when input differential voltage 600mV

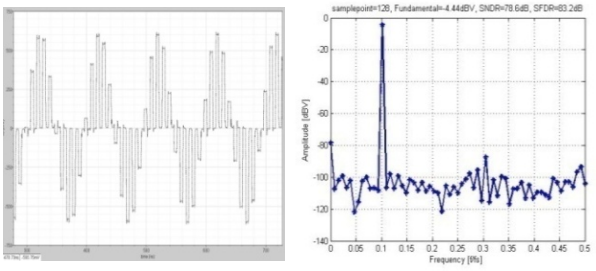
As the Fig.8 shows, slewing time is 0.77ns, the design slewing time is 0.675ns. The output of OTA in holding mode is 599.93mV, ε= (600-599.9)/600=0.012%. The slewing time and settling precision both meet the design requirements.

As Fig.9 shows, input signal is 10.15625MHz peak-peak 1200mV Sinusoidal signal, the output wave is showed in Fig.9

(a).

And from FFT results showed in Fig.9 (b), we can find out that:

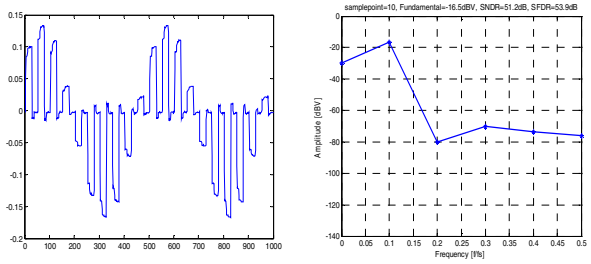
SNDR=78.6dB SFDR=83.2dB ENOB=12.77



(a).100MHz S/H output wave (b).FFT results of output wave.

Figure 9. Wave and FFT results of 10MHz 600mV sinusoidal input signal through 12bit 100MHz S/H.

Considering the S/H designed for the 2.4pF capacitance load, but the capacitance of test instruments is nearly 17pF. Slew rate and GBW will suffer some attenuation from the load capacitance enlargement. In that case, the testing clock is changed from 100MHz to 10MHz, regarding the enlargement of load capacitance. From Fig.10, measured results show that OTA works properly, but the performance is not that good.



(a).Output wave of 1MHz input (b).FFT result of output wave

Figure 10. Measured form and FFT results of 1MHz 200mV sinusoidal input signal through 12bit 100MHz S/H at 10MHz clock.

From Fig.10 (b), we could find out that SNDR=51.2dB SFDR=53.9dB ENOB=8.2. The large capacitance load does affect the linearity and the precision of the whole S/H.

V. CONCLUSTION

In this paper, a novel design method for S/H circuit is introduced. The g_m/i_d design method bases on data simulated by H-Spice and MATLAB, with model parameters offered by foundries. This method can also be applied in design other OPAMP, for it is more reasonable design process using original data. However, there are still many improvements should be made. For example, the signal linear settling after slewing is not as simple as the one-order linear response as we mentioned in section III, because the OTA is a multiple poles system with several zeros. If the model could join the slewing and high-order linear response together, the simulation would be more approximate to the real wave. And the testing program can be also improved by adding low-pass filter to the source of clock generator, and enhancing the driving capacity of S/H to cover the large loading capacitance problem.

ACKNOWLEDGEMENT

This paper is supported by the National Science and Technology Major Project of China (No. 2009ZX03002-004).

REFERENCE

[1] T. N. Anderson et al., “A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-um Digital CMOS,” IEEE JSSC, pp. 1506-1513, Jul 2005.

[2] A. Loloee, et al, “A 12b 80-MSs Pipelined ADC Core with 190mW Consumption from 3 V in 0.18-um, Digital CMOS”, Proc. ESSCIRC, pp. 467-469, 2002

[3] P. Bogner et al., “A 14b 100MS/s digitally self-calibrated pipelined ADC in 0.13um CMOS,” ISSCC Dig. Techn. Papers, pp. 832-833, Feb. 2006.

[4] B. Murmann, “EE315 Course Reader,” Stanford University, Fall 2007.

[5] P.R. Gray, P.J. Hust, S.H. Lewis and R.G. Meyer, “Analysis and Design of Analog Integrated Circuits”, 4th edition, John Wiley, 2001.

[6] P. E. Allen and D. R. Holberg, “CMOS Analog Circuit Design”, 2nd edition, Oxford University Press, 2002.

[7] Paul G.A. Jesper., “The g_m/i_d methodology a sizing tool for low-voltage analog cmos circuits”, Springer Press, 2009

[8] B. Razavi. “Design of sample-and-hold amplifiers for high-speed low-voltage A/D converters”. In: Proceedings of the IEEE 1997 Custom Integrated Circuits Conference. Santa Clara, CA, USA: IEEE, 1997. 59-66.

[9] Kamath, B.Y.T. Meyer, R.G. Gray, P.R. “Relationship Between Frequency Response and Settling Time of Operational Amplifiers”. IEEE Journal of Solid-State Circuits, 1974. 9 (6): 347- 352.

[10] Chuang, C.T. “Analysis of the settling behavior of an operational amplifier”. IEEE Journal of Solid-State Circuits, 1982. 17 (1): 74- 80.

[11] K. Bult, J.G.M. Geelen. “A fast-settling CMOS opamp for SC circuits with 90-dB DC gain”, IEEE Journal of Solid-State Circuits, 1990, 25(6). 1379-1384.