Design and Implementation of Sample and Hold Circuit in 180nm CMOS Technology

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***Abstract*—This project presents the implementation of error reduction techniques in sample and hold circuit(S/H).S/H suffers from multiple errors such as droop, acquisition error, aperture jitter,etc.Mainly two hold mode errors that is charge injection and clock feedthrough.We are trying to mitigate these errors by using different design techniques. When a switch in the S/H turns on, the capacitor starts charging and discharges when it turns off. Due to this action the sampled output signal may suffers from attenuation that is called charge injection. Due to the some overlap capacitance of gate and drain clock feed through error may also occur. This paper presents designing different S/H architectures to reduce these errors and also gives high gain, more stable, increased acquisition range, low power consumption. The proposed architectures are designed in 180nm CMOS Technology with input sinuesoidal frequency 10MHz and 1V P-P.Sampling rate is 500MHz.The design is target to gain of 65dB.**

***Index Terms*—**Sample and hold circuits, Operational amplifiers,ADC,unity gain buffer, voltage follower.

I.INTRODUCTION

In most of the analog to digital converters (ADC), sample and hold circuitry is the front end device. Sample and Hold circuits are used for performing the sampling operation on the analog input signal at a sample moment in an analog to digital converter. The sample and hold circuit can keep the signal at that level for the time period thus allowing repeated use of the signal during the analog to digital conversion. Sample and Hold circuits are important building blocks in data converter system. Traditional switched capacitor techniques take a advantage of the excellent properties of on chip capacitors and MOS switches and permit the realization of numerous analog sampled data circuits. It is an analog device that samples the voltage of continuously varying analog signal and holds it value at a constant level for a specified minimum period of time.S/H samples the continuous varying signal and holds it for particular time duration.In S&H the channel charge injection and clock feedthrough are the major source of errors when the switch is turned off. The fact that the output value is internally used at slightly delayed time moments will not create any effect in signal transfer characteristics, because in the end the resulting value will be assigned to the original sampling moment. As the output value of the S/H circuit is used only at specific time moments, some compromises may be acceptable in obtaining a high quality output signal. e.g. slewing during the initial phase of the settling will not affect the overall performance as long as a stable value is reached at the required time moment. A MOS transistor holds mobile charge in its channel when it is on. When the transistor is turned off, a certain portion of this charge is released from the channel to the hold capacitor and the rest is transferred back to the voltage source. The charge transferred onto the hold capacitor while the transistor is turned off determined the total error as a result of charge injection. Clock feedthrough is the errors that set the maximum usable resolution of an S/H.

II.BASIC STRUCTURE OF S/H

S/H creates the stable signal for a sample period of ADC and converts analog signal into digital. Basic S/H consists of a switch and a capacitor is shown in Fig.1.S/H circuit works mainly in two modes that is sampling mode and hold mode. M1 and Ch are the sampling switch and hold capacitor[1]. Whenever CLK goes high,M1 switch will turn on which intern allows Vout to track the continuous analog input signal. In hold mode the signal value remain fixed at its value at the moment of opening the switch. When CLK goes low,M1 switch turns off and Ch will keep Vout equal to the value of Vin.Sampling can be of two methods which are series sampling and parallel sampling.Here we refer parallel sampling because the hold capacitor is in parallel with the signal. In series sampling hold capacitor will be connected in series

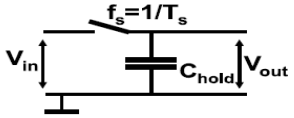

Fig.1 Basic sample and hold

There are many errors which degrades the fruitfulness of S/H[2]. Mainly the hold mode errors cause difficulties in the operation than in sample mode. Clock feed through and charge injection are the two main errors realy need to consider in S/H.

A.Charge injection

When sampling switch is on. its drain to source voltage become zero because it is operating in triode region. It contains mobile charge carriers that should flow out from the channel and into the drain and source. When the CLK signal goes low,the

charge is distributed equally between the drain and the source of M1.but in reality a fraction of charge goes back.

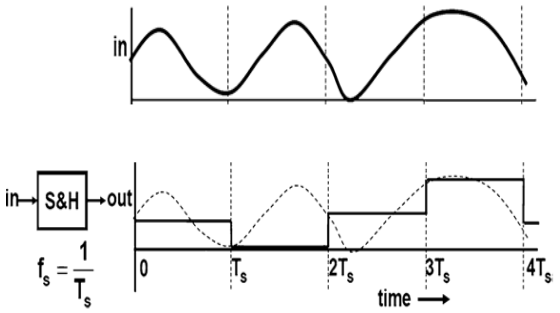

FIG.2.ERRORS ASSOCIATED WITH S/H

B.Clock feed through

This is due to some overlap capacitance. Gate to source overlap capacitance causes this clock feedthrough error. This error is very small when compared to charge injection. So this is less considerable

C Pedestal step

This occurs when S/H goes from sample mode to hold mode so there will be a small error in the voltage being held that makes it different from the given analog input voltage at the time of sampling. These error should be small and even more importantly be signal independent to avoid nonlinear distortion.

D Droop

Droop characterize a slow charge in output voltage in hold mode. During the hold phase of the sample and hold, charge can leak from the hold capacitor, the signal will show"droop'.In a bipolar design this leakage is caused by the base current. This effect results in a minimum sample rate of e.g.A few hundred samples/s.In deep-submicron processes gates may become so leaky that again droop will become a relevant parameter.

E.Aperture jitter

This is because of effective sampling time changing from cycle to cycle. When high speed input signal are sampled, it causes the held voltage to be significantly different from the ideal held voltage. The aperture time is the relatively small time period in which the sample pulse makes the transition to switch off. During this clock edge still some tracking of the signal may continue. A content aperture time is therefore mostly just a small additional fixed delay of the sampling respect to the start of the switch off process. More devastating are changes in aperture time. Deviations of the aperture time can also arise from changed related to the signal amplitude causing distortion. Aperture delay time can be measured by applying a bipolar sine wave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero crossing the input sine wave is the aperture delay time

III.DESIGN OF PROPOSED S/H ARCHITECTURE

The proposed S/H architecture consists of an operational amplifier (op-amp) at the input stage and a unity gain buffer at the output stage is shown in the Fig.3. A sampling switches and hold capacitor is connected in between buffers. Design procedure includes first designing of an operational amplifier. Here a two stage op-amp is designed for high gain with more stability. Although a single stage op-amp can also do the same job in S/H,Two stage is preferred here because multistage op-amp consumes less power and gives high gain. Two stage op-amp is as shown in the Fig.4.The design procedure follows as

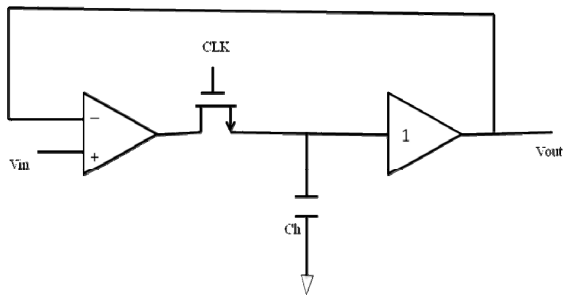

Fig.3. Proposed S/H architecture

A. AN OP-AMP DESIGN

Two stage opamp is used in proposed S/H architecture[3].opamps gives very high input impedance and low output impedanceThe design procedure for two stage opamp is as follows.

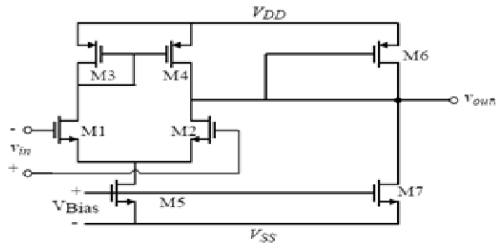

Fig.4. Two stage operational amplifier

The above opamp consists of two differential inputs and a output.M1 and M2 serves as input differential pairs.M3 and M4 will act as current mirror.M6 and M7 acts as common source gain stage.M1 and M2 is biased by the current provided by M5.Current mirror used here is to replicate and distribute the DC bias current

- The two stage opamp is designed with 100MHz frequency and 75mv P-P for positive input,50mv for negative input
- The circuit is first checked for saturation condition
- Value of current is determined by

$$I=SR.C$$

Where SR is the slew rate and C is the load capacitance of two stage opamp

- W/L ratio of each transistor is calculated then by using current equation

$$I_{D=}1/2u_{n,p}C_{ox}(W/L)_{n,p}[V_{gs}-V_t]^2$$

- Positive power supply=1.8v and negative power supply=-1.8v
- For 0.18µm technology, threshold voltage for CMOS Vthn=0.48V , Vthp=0.43V
- Value of Transconductance in saturation Kn=289uA/V^2 ,Kp=77uA/V^2

Calculated W/L ratios for transistors are shown below

M1	4	M5	7
M2	4	M6	8
M3	8	M7	5
M4	8		

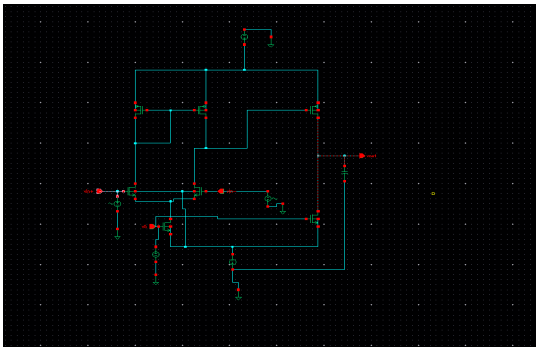

Fig.5. Schematic of Two stage opamp

B. Design of Sample and Hold

Proposed S/H architecture consists of a sampling switch, hold capacitor, a voltage follower at the input stage and a unity gain buffer at the output stage. The sampling switch is controlled by positive CLK .Input is sampled with sampling frequency 10MHz and 1V P-P.The S/H actives when it comes to the saturation region, pinchoff situation will occur and disconnected from drain. If drain of the sampling switch is connected to the hold capacitor, drain will not get affected except source junction. because it will suffers from charge injection. During sampling mode, the output value will just follows the input value. During hold mode, the transistors which are connected to the output of opamp are turned off even though they are still operating in saturation. this will prevent the charge injection in channel from flowing into the output of the opamp.The opamp will turn off and its output is held at high impedence,allowing the charge on hold capacitor to be saved during the hold mode[1]. Unity gain buffer which is connected at the output stage of the S/H circuit is always operational during both sample and hold mode and provides the voltage on hold capacitor to output of S/H circuit.

IV.SIMULATION RESULTS

The simulation of proposed S/H architecture is done in 180nm CMOS Technology.Sampling frequency is 100MHz and powerm supply is 1.8V.Input continous wave is 10MHz with 1V.

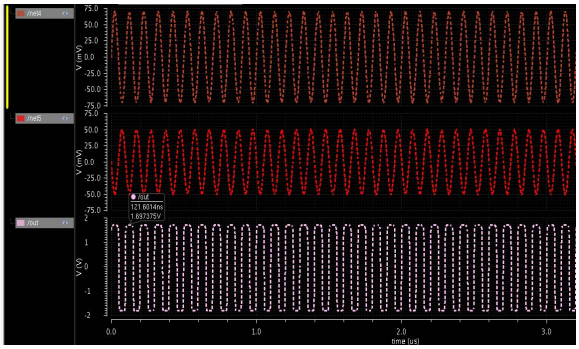

Fig.6. Transient response of Two stage opamp

The measured aperture jitter is about 617.352psec.Acquisition time is nearly 1.68679nsec.Hold step mode is 6.7878mV/nsec.Settling time is 1.00737nsec.

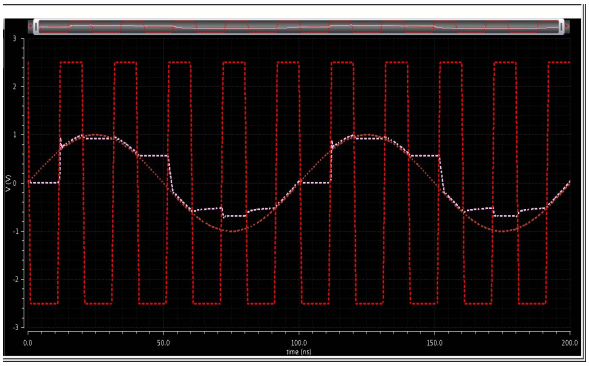

Fig.7.Result of proposed S/H

IV.CONCLUSION

The proposed opamp based S/H architecture is processed in 0.18µm CMOS technology with the sampling frequency 10MHz with p-p 1V.Using opamp as voltage follower at the input stage, output is made less dependent on input .Charge injection error in hold mode is considerably reduced here. The acquisition time is increased. The gain of the S/H is 64dB and phase margin is 237.512 deg.A future improvement in proposed architecture can be made as differential circuit for faster ADC applications. Also the buffers can be replaced with the foaldedcascode for still less power consumption.

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