The Enhancement of Recycling Folded Cascode Amplifier

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***Abstract*–The enhancement of recycling folded cascode (RFC) operational transconductance amplifier (OTA) is described in this paper. The proposed enhanced recycling folded cascode (ERFC) structure improves dc gain and unity-gain frequency of RFC amplifier. The ERFC OTA has been implemented using TSMC 0.18μm CMOS process and simulated with a 1.8V power supply and a 5.6pF capacitor load. Simulation results show that the proposed ERFC OTA achieves 27dB increment in dc gain (72.2dB versus 45.2dB) and about 11 times better in unity-gain frequency (66.5MHz versus 746MHz) compared with the RFC OTA.**

I. INTRODUCTION

The operational transconductance amplifier (OTA) is an important building block in most analog circuits [1]–[3]. Recently, the folded cascode (FC) amplifier is commonly used in the single-stage or multi-stage amplifiers due to its high gain and large signal swing. Therefore, many circuit topologies has been proposed to improve the traditional FC amplifier in the past decades [4]-[5]. The recycling folded cascode (RFC) structure have been proposed to enhance the performance of traditional FC amplifier for its higher non-dominant poles, slew rate, unity-gain frequency, and dc gain [5].

In this paper, an enhanced RFC (ERFC) amplifier is proposed by adding an output-stage to improve the dc gain and unity-gain frequency. With the extra output-stage, the output impedance is increased so that the dc gain is enhanced [6]. Moreover, the proposed amplifier also improves the unity-gain frequency of the RFC amplifier.

II. PROPOSED ENHANCED RFC AMPLIFIER

The proposed enhanced recycling folded cascode (ERFC) amplifier is shown in Fig.1. The transistor M7, M8, M9, M10 conduct the most currents in amplifier. The transistor M1, M2, M3, M4 limits the currents flowing through whole amplifier from power supply V_{DD}. The current flowing through M14 and M15 is identical and equal to $I_b/2$ [5]. The cross-over connections of current mirrors M7, M8 and M9, M10 ensure the small signal currents injecting into the sources of M11 and M12. Thus, the current can be utilized by devices efficiently and perform additional task. Moreover, the proposed amplifier modify the RFC amplifier by adding the transistor M17 and M18 as enhanced device transistors. Since the dc gain of amplifier is dominated by common source stage, the dc gain can be improved with the enhanced device transistors.

In the following of this paper, we will compare the proposed amplifier with FC and RFC amplifier. Although

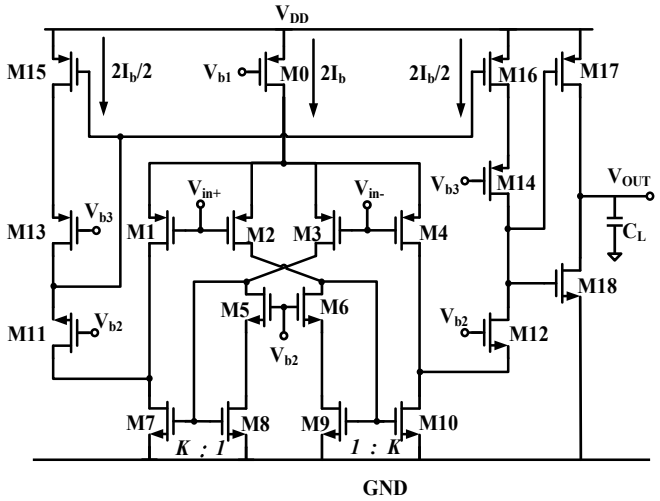

Figure 1. Proposed enhanced RFC amplifier.

some topologies have been proposed to improve RFC amplifier, the circuit complexity increases significantly [6]-[7]. However, the proposed ERFC amplifier only adds two transistors M17 and M18 over RFC amplifier as shown in Fig. 1. It not only reduces the complexity of the circuits but also improves the general performance compared with other counterparts.

III. SIMULATION RESULTS

The proposed ERFC amplifier is implemented using TSMC 0.18μm CMOS process and simulated with a 1.8V power supply and a 5.6pF load. The simulated frequency response of the proposed enhanced RFC amplifier is shown in Fig. 2. From the simulation results, the dc gain of the FC, RFC and ERFC is 34.3dB, 45.2dB and 72.2dB. The phase margin of the FC, RFC and ERFC is 87.3°, 80° and 105.2°, respectively. The proposed ERFC structure achieves the highest DC gain and phase margin comparing to the FC and RFC amplifiers. Moreover, the unity-gain frequency of ERFC amplifier achieves 746MHz, which is about 11 times better than that of RFC amplifier (66.5MHz versus 746MHz). The simulated transient response of the proposed amplifier is shown in Fig. 3. From the simulation results, the average slew rate of the proposed amplifier is 4.02 V/μs.

Table I shows the performance comparison of the proposed enhanced recycling folded cascode (ERFC) amplifier against previously reported amplifier architectures. From the summary table, the proposed amplifier achieves 27dB enhancement of dc gain over the RFC OTA for the same output load. The unity-gain frequency of ERFC amplifier also achieves 746MHz, which is about 11 times better than that of RFC

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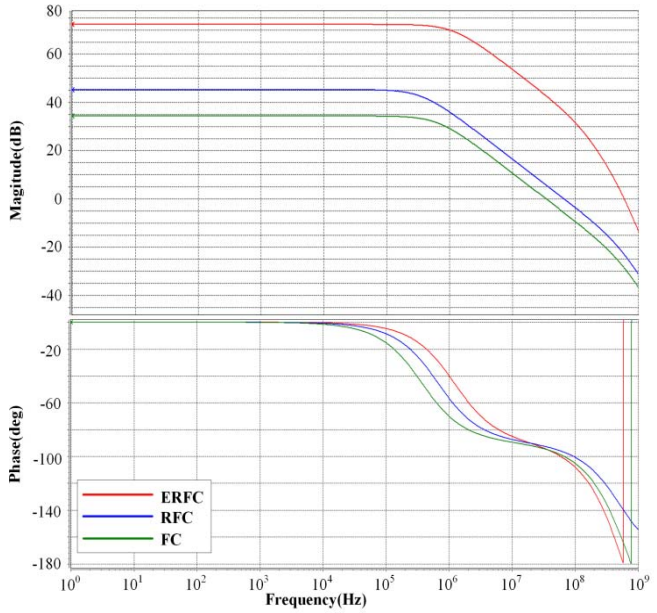

Figure 2. Simulated frequency response of designed amplifiers.

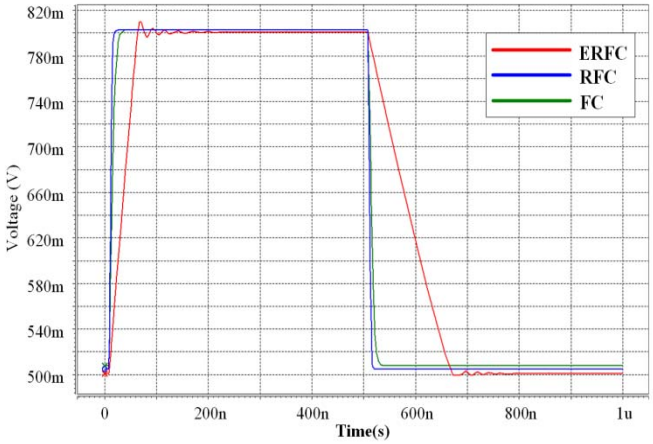

Figure 3. Simulated transient response of designed amplifiers.

amplifier. Hence, the proposed ERFC amplifier obtain highest performance such as dc gain, phase margin and unity-gain frequency, comparing with the previously reported amplifier architectures.

IV. CONCLUSIONS

In this paper, an enhanced RFC amplifier is proposed and implemented. The proposed amplifier modifies the RFC amplifier by adding a common source stage. It not only reduces the complexity of the circuits but also improves the general performance compared with other counterparts. From the simulation results, the enhanced RFC amplifier improves the dc gain by 27dB over the RFC amplifier for the same power supply. Moreover, it also achieves high unity-gain frequency and phase margin which is 746MHz and 105°, respectively.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED AMPLIFIER AND PREVIOUSLY REPORTED AMPLIFIER ARCHITECTURES

Parameter	RFC [5]	2V-RFC [6]	IRFC [7]	**This work (FC)**	**This work (RFC)**	**This work ERFC**
Technology	0.18 μm	65 nm	0.13 μm	**0.18** μm	**0.18** μm	**0.18** μm
Supply Voltage [V]	1.8	2	1.2	**1.8**	**1.8**	**1.8**
C_L [pF]	5.6	1	7	**5.6**	**5.6**	**5.6**
DC Gain [dB]	53.6	63.4	70.2	**34.3**	**45.2**	**72.2**
PM [deg]	70.6	63.6	70	**87.3**	**80**	**105.2**
UGF [MHz]	134.2	236	83	**34**	**66.5**	**746**
SR (Average) [V/μs]	94.1	19	29.8	**20.5**	**41.4**	**4.02**

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