Physical Design of Two Stage Ultra Low Power, High Gain Cmos OP-AMP for Portable Device Applications

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Abstract. A Two-Stage CMOS Op-Amp using P-Channel input differential stage suitable for portable device applications with ultra-low power, high swing, high gain is proposed. DC gain is increased by using Cascode Technique. A gain-stage implemented in Miller capacitor feedback path enhances the Unity-Gain Bandwidth. Topology selection, practical issues in designing micro-power Op-Amps and theoretical analysis of the design are discussed. The circuit is designed and simulated using TSMC 180nm technology. The circuit is simulated with 1.5V DC supply voltage. The proposed Op-amp provides 228MHz unity-gain bandwidth, 61.3 degree phase margin and a peak to peak output swing 1.15v. The circuit has 95.6dB gain. The maximum power dissipation of the designed Op-Amp is only 72µW. Suitable response in different temperature range is demonstrated by the designed system. Layouts of the proposed Op-Amp have been done in Cadence® Virtuoso Layout XL Design Environment.

Keywords: Two stage Op-Amp, Low voltage, Ultra low power, Cascode technique, Unity-Gain Bandwidth.

1 Introduction

Research in analog-circuit design is focused on low-voltage low-power battery operated equipment to be used as an example in portable equipment, wireless communication products and consumer electronics. A reduced supply voltage is necessary to decrease power consumption to ensure a reasonable battery lifetime in portable electronics. For the same reason, low-power circuits are also expected to reduce thermal dissipation, of increasing importance with general trend in miniaturization [1].

Advancements required by International Technology Roadmap for Semiconductors (ITRS), means that with current CMOS standard fabrication processes, circuits must work at supply voltages as low as 1.5V. Industry and academia are researching new circuits techniques that will make them operate at this voltage. For this fact, the

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industry and the academia are doing research in new circuit's techniques that will make them able to operate at this voltage [1].

Also other point, as for various recently developed high-performance integrated electronic systems or subsystems, e.g. A/D converter, switched-capacitor filter, RF modulator and audio system, CMOS operational amplifier with high unity-gain bandwidth and large dynamic range are required [2].

Another important consideration from bio-medical applications typically requires high gain, high swing and ultra low power amplifiers that typically occupy the minimal chip real estate [10].

So, it can be deducted that designing of Op-Amp puts new challenges in low power applications with reduced channel length devices.

2 Circuit Topology Selection

The comparison of performance of various Op-Amp topologies is presented in Table 1. Each topology exposes its uniqueness of performance. Considering the design requirements the two-stage amplifier seems most suitable one. In a two-stage Op-Amp, the first stage provides high gain and the second provide high output swing.

Table 1. Topology Selection for CMOS Op-Amp[4]

Topology	*Gain*	*Output Swing*	*Speed*	*Power Dissipation*	*Noise*
Telescopic	Medium	Medium	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two Stage	High	Highest	Low	Medium	Low
Gain Boosted	High	Medium	Medium	High	Medium

3 Conventional RHP Zero Controlling and Improved Compensation Techniques

The RHP zero creates the un-stability problem as it boosts the magnitude but lags the phase which can be solved by eliminating one of the paths to the output. The effect of RHP zero on the stability or phase margin of Op-Amp is shown in Fig. 1 [4].

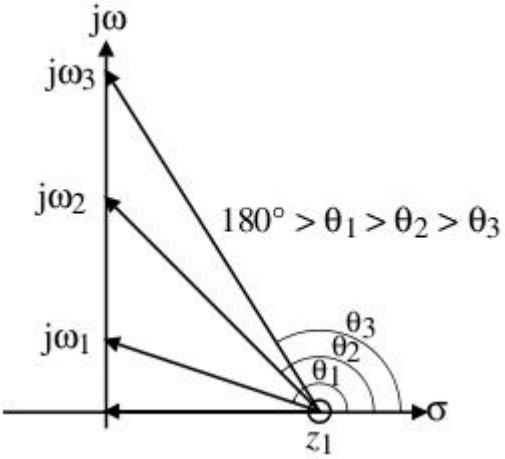

Fig. 1. RHP-Zero effect on stability

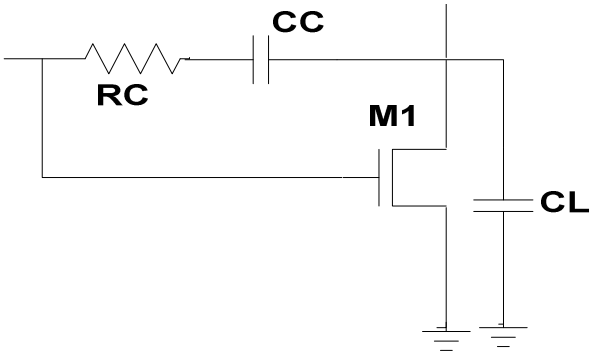

Fig. 2. RHP Zero control by nulling resistor approach

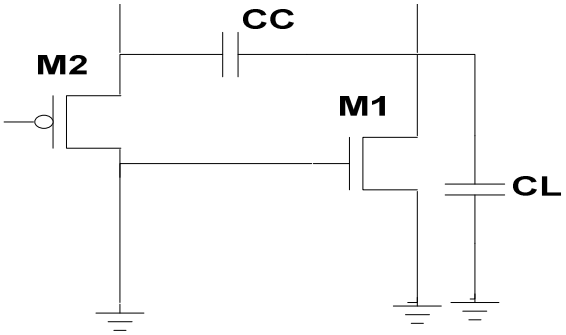

Fig. 3. RHP Zero control by gain stage approach

RHP zero control using nulling resistor and gain stage approach is illustrated in Fig.2. and Fig.3. respectively. RHP zero displacement form the basis of nulling resistor approach. On the other hand, as shown in Fig.4 ., the employed gain-stage M2 prevent the input current from going directly through the Miller capacitor, thus, the RHP zero will eliminate [7]. As observed in Fig. 2. , the compensation capacitor Cc

can be ignored at frequencies near unity gain frequency. Therefore, the output resistance seen by C_L can be derived as given by

$$R_{out} = 1 / g_{m1} \tag{1}$$

while from Fig. 2. , the output resistance seen by C_L can be expressed as [5]

$$R_{out} = 1 / (g_{m1}\, g_{m2}\, r_{ds2}) \tag{2}$$

Also the output pole can be written as,

$$P_o = 1 / R_{out}\, C_{out} \tag{3}$$

Obviously, it can be deduced from (1) and (2) that noticeable reduction of R_{out} by a factor of gm2 r ds2 is the basis of improvement in "pole-splitting" effect which is valid only for Fig. 2. and not for Fig. 3. Unity-Gain Bandwidth is enhanced by increasing the magnitude of the non-dominant output pole by employed gain-stage M2.

As observed in Fig. 3. , the compensation result is to keep the dominant pole roughly the same as normal Miller compensation and to increase the output pole by approximately the gain of a single stage M6 the magnitude of the output pole can be given by

$$P_o = (g_{m12}\, g_{m6}\, r_{ds6}) / C_{out} \tag{4}$$

Consequently, the output pole Po has split from the dominant pole by a factor of gm6rds6 which leads to an enhancement in unity gain bandwidth, when compared to the nulling resistor approach.

4 Circuit Design and Implementation

The proposed schematic of a Two-Stage CMOS Op-Amp with p-channel input pair, with un-buffered output for Unity-Gain Bandwidth enhancement is shown in Fig. 4.

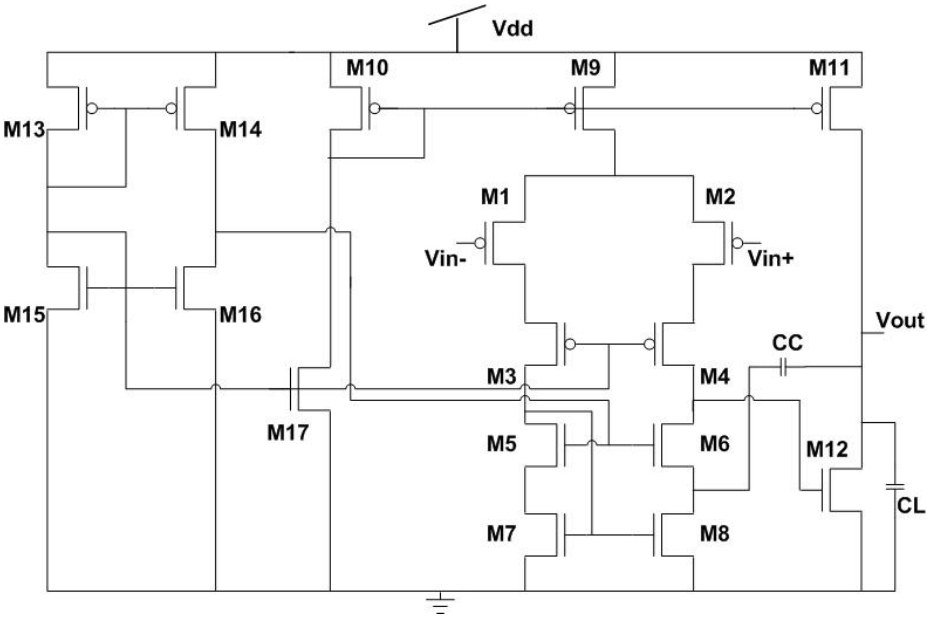

Fig. 4. Schematic proposed Two-Stage Op-Amp

In this work the various transconductance parameters are related as:

$$g_{m1} = g_{mI}\ ,\ g_{m2} = g_{mII}\ ,\ g_{ds2} + g_{ds4} = G_I \tag{5}$$

Also

$$g_{ds6} + g_{ds7} = G_{II} \tag{6}$$

$$g_m = \sqrt{2\mu_{n,p}\, C_{ox}\, \frac{W}{L}\, I_D} \tag{7}$$

$$g_m = 2\ \frac{I_D}{V_{eff}} \tag{8}$$

While the I_d current is given as

$$I_D = \frac{\mu_{n,p}\, C_{ox} \frac{W}{L} V_{eff}}{2} \tag{9}$$

from the expressions in relation with the compensation capacitor Cc, the slew rate is given by

$$SR = dv_o/dt \tag{10}$$

Therefore,

$$SR = I_{9(max)} / Cc \tag{11}$$

Requirements for the transconductance input transistors can be determined from Knowledge of Cc and GBW the transconductance g_{ml} can be calculated by the following equation

$$GBW = g_{m1} / Cc \tag{12}$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{ml} as shown below.

$$(W/L)_1 = g^2_{m1}/2\beta I_1 \tag{13}$$

5 Simulation Results

The circuit is simulated with BSIM3v3.1 model based on a standard 0.18 µm CMOS process. The OP AMP operates with the 1.5V power supply and consumes maximum 72µW power at maximum amplitude. Simulations resulted on considerable increase of unity-gain bandwidth to the value of 228 MHz, the improved DC gain of 95.6 dB, phase margin of 61.3 degree and output swing of 1.15V. Layout of the proposed Op-Amp has been done in Cadence® Virtuoso Layout XL Design Environment. LVS and DRC has been checked and compared with the corresponding circuits using Mentor Caliber, Synopsys Hercules and STAR RCXT respectively. The simulated results have been developed for the various performance characteristics and the superior features of the proposed Op-Amp are established.

Fig. 5. presents the simulated DC gain and Fig. 6. shows the phase margin of the OPAMP. Swing voltage is 1.15 v presented by Fig. 7. Additionally, with the load capacitor CL of 1 pF and with a compensation capacitor Cc of 208 fF. Fig. 8. demonstrates the performance metrics at different temperature range. The layout is depicted in Fig. 9. Simulation Results represent that the designed OP AMP has high voltage gain, low supply voltage, high swing voltage, high unity-gain bandwidth and ultra-low power dissipation.

Table 2. Aspect Ratios of proposed Op-Amp design

Transistor	***W***	***Transistor***	***W***
M1	15	M10	2.8
M2	15	M11	11
M3	10	M12	8
M4	10	M13	0.38
M5	2	M14	0.31
M6	2	M15	0.21
M7	3	M16	0.21
M8	3	M17	0.21
M9	6.8	***L***	***0.36***

* All the above measurements are in micro-meters.
**L is length of all the transistors

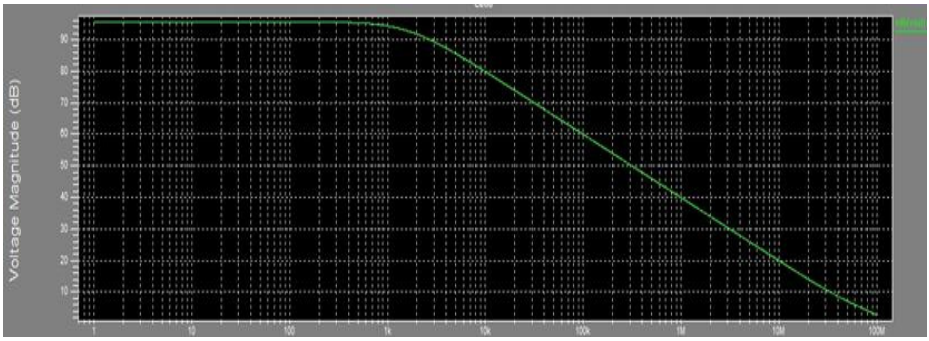

Fig. 5. Simulated DC Gain

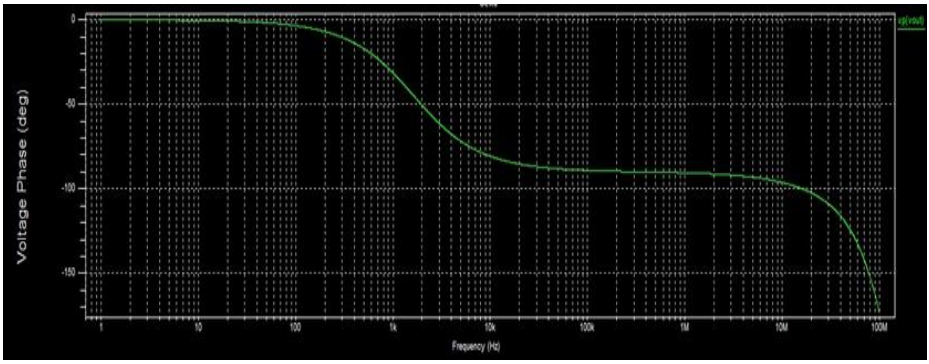

Fig. 6. Simulated Phase Margin

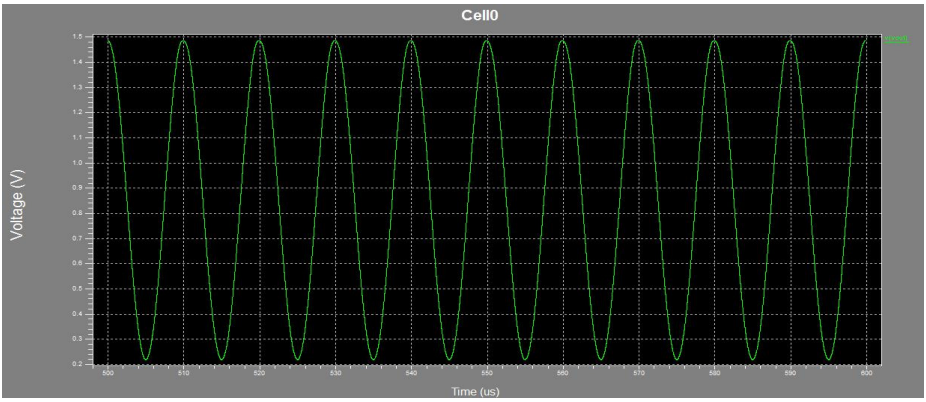

Fig. 7. Simulated Output-Swing

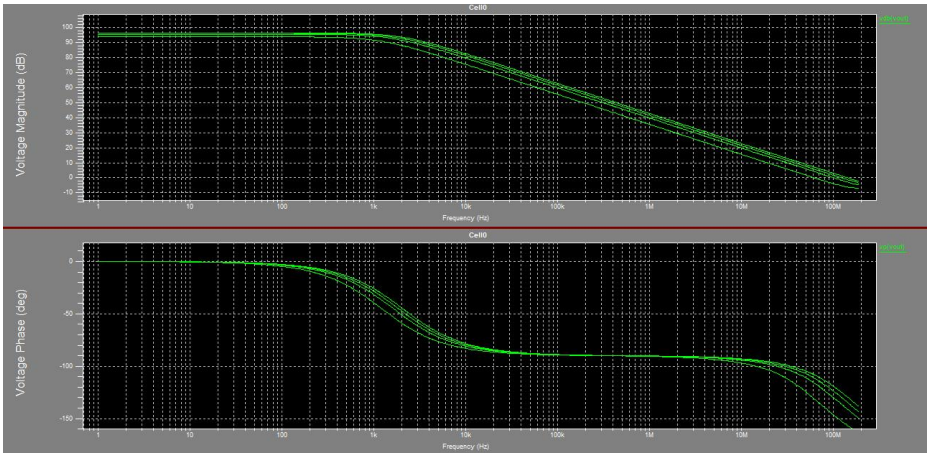

Fig. 8. Performance analysis at different temperature range of proposed Op-Amp

Table 3. The designed system demonstration in different temperature

Temp. (deg)	-20	0	27	100
Gain (db)	94	95.6	96.2	96.6
Phase Margin (deg)	12	61.3	63	66
UGB (MHz)	220	228	238	102

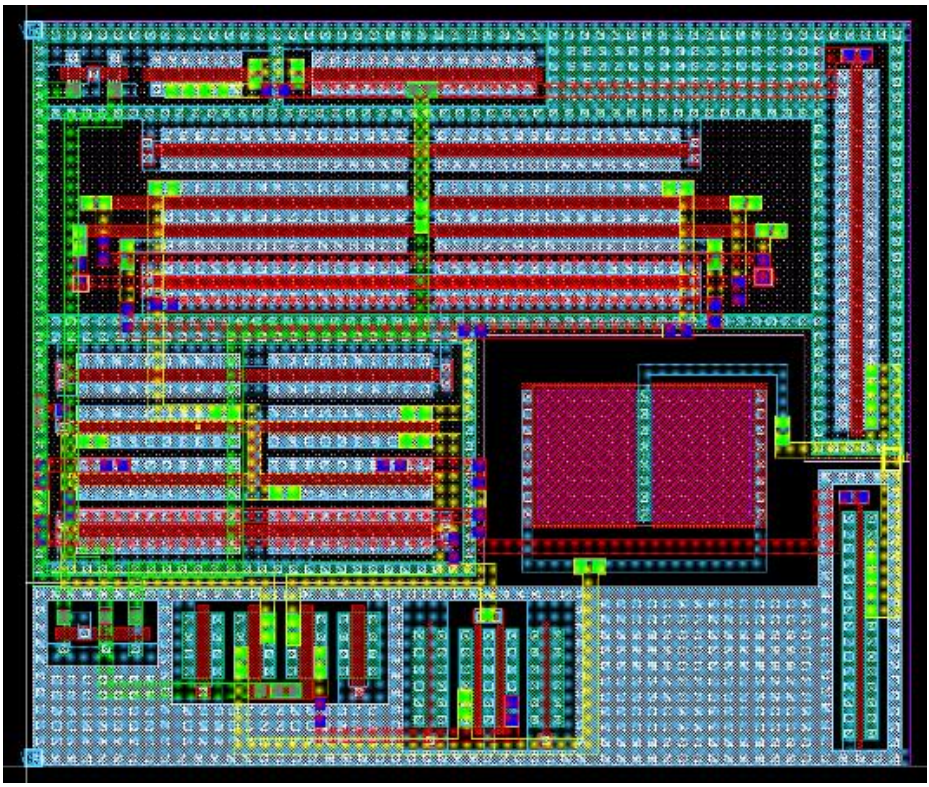

Fig. 9. Layout view of the proposed Op-Amp

Table 4. Performance summary of the proposed Op-Amp

Reference	Performance Metrics					
	DC Gain (db)	UGB (MHz)	PM (degrees)	Power Supply (V)	Power Diss. (µW)	Output Swing (V)
This Work	95.6	228	61.3	1.5	72	1.15

The OP AMP performance at different temperature is illustrated in Table 3. The performance summary of this proposed CMOS OPAMP is listed in Table 4.

6 Applications

Recent advances in IC technology as well as innovation in circuit design techniques, have led to system with processing capabilities that can supplement or even entirely replace complex circuits in the mixed signal system.

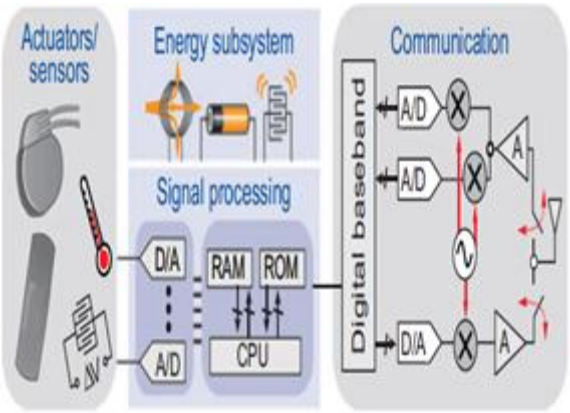

Fig. 10. Electronic Bio-Medical system

The electronic bio-medical system can be observed from Fig. 10. Due to the small voltage drops, the ultra-low power consumptions the system is very amenable too implantable, bio-medical and portable device applications, where battery size and capacity are limited.

7 Conclusion

The design procedure of low voltage, high gain, ultra-low power two stage CMOS Op-Amp is discussed in this paper. The unity-gain bandwidth enhancement using a gain-stage in the Miller capacitor feedback path is presented and verified by simulation achieving the UGB of 228MHz with peak to peak output swing of 1.15V. The concept of stability is presented and implemented with the phase margin of 61.3°. The technique implemented in the circuit with 0.18µm CMOS technology and supply voltage of 1.5v. The circuit is power efficient with consumption of 72µW and DC gain of 95.6dB. A relatively suitable response in different temperature range is demonstrated by this system. Layout of the proposed Op-Amp have been done in Cadence® Virtuoso Layout XL Design Environment. LVS and DRC has been checked and compared with the corresponding circuits using Mentor Caliber, Synopsys Hercules and STAR RCXT respectively. Continued device scaling, reduction in power-supply voltage and integration of technology makes this design amenable to implantable, bio-medical and portable device applications, where battery size and capacity are limited.

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