Comparative Study on Multistage Amplifier and Folded Cascode Amplifier Design in Sample and Hold Circuit using 0.18µm CMOS Technology

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***Abstract*—This paper presents the comparison between multistage amplifier and folded cascode amplifier design using 0.18µm CMOS technology. The objective of this project is to compare gain and power dissipation between these two design models. Sample and hold circuit (SHC) is the main component in pipelined ADC. Designing a low power, high gain SHC is crucial, that is the main reason why multistage amplifier is applied in this project. Implementation has been done in 0.18µm technology, for a 5MHz sampling frequency, considering 1.2 Vpp voltage and 1.8V voltage supply using SILVACO EDA tools. From the simulation, the multistage amplifier consumes 0.139mW power and has gain of 94.64dB. The folded cascode amplifier has 6.5mW power dissipation and 70dB gain. From the simulation results, the multistage amplifier is better in term of gain and power dissipation than the folded cascode design.**

Keywords-component—Multistage amplifier; folded cascode amplifier; ADC; sample and hold circuit; low power consumption.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are important building blocks in modern signal processing and communication systems. There are many types of ADC such as flash ADC, folding and interpolating ADC, pipeline ADC, delta-sigma ADC and integrating ADC [3]. The pipelined ADC is one of the types of ADC which is having a lot of advantages. One of the benefits, it is being an alternative solution for wireless communication system. Pipelined ADC consists of several components which are the coarse and fine ADCs, sample-and-hold circuit, digital-to-analog converter (DAC) and the interstate amplifier [1]. Sample-and-hold circuit is an important part in the pipeline ADC architecture and other data-converter systems. The conversion process of pipelined ADC begins with sample-and-hold circuit.

The sample-and-hold circuit can give some isolation between the pipelined ADC and its driving circuit. So, the driver faces less back noise from the comparators in pipelined ADC [3].There is many different structures for sample-and-hold circuits. For example, flip around sample-and-hold circuit, circuit of unity gain of sample-and-hold circuits and switch-capacitor based sample-and hold circuit. This paper focus on design and implementation of modified switch-capacitor based sample-and-hold circuit architecture with modified clock sequence. The operation of sample-and-hold circuit is divided into two phase which is the sampling phase and hold phase. The design of sample-and-hold circuit in pipelined ADC is challenging especially in a low power consumption application. Instead of using the folded-cascode amplifier, the multi-stage amplifier is applied in order to achieve high gain. To ensure this circuit operates efficiently in a closed loop feedback system, the high gain is required [4]. In this paper, the main application of this sample-and-hold circuit is in the low power consumption pipelined ADCs.

This paper is divided into seven main parts. Section 2 is the design of sample-and-hold circuit and overview of the clock scheme. In section 3, op-amp architecture design. Section 4, compile the simulation results. In section 5 is the layout of sample-and-hold circuit. Finally, section 6 concludes the work of low power sample-and-hold circuit for pipelined ADC.

II. DESIGN OF THE SAMPLE-AND-HOLD ARCHITECTURE

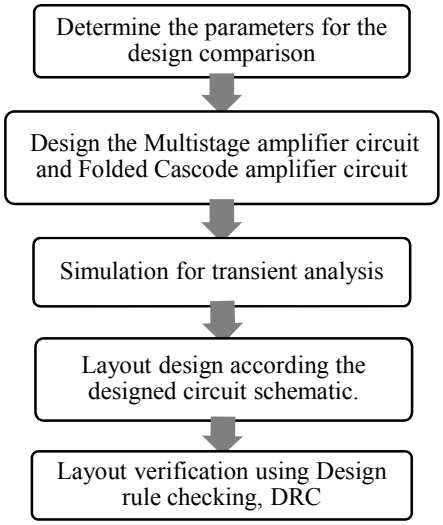

Figure 1: Flow chart of the project

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The flow chart on Figure 1 shows the step to complete designing a low power CMOS multistage amplifier and folded cascode amplifier in SHC using 0.18µm technology.

A switch-capacitor sample-and-hold architecture with modified clock sequence is shown in Figure 2. The four clock scheme for switch-capacitor sample-and-hold circuit is employed. The clock waveforms are shown in Figure 3.Four capacitors with same size are used in this structure. During the sampling phase, □1 switches "on" and the differential input signal is sampled into two input sampling capacitor. The voltage reference, V_{ref} is referred to the output voltage, V_{out}. Next, during the holding phase, the bottom plates of input capacitor are connected to the □2 switches which are the input capacitors connecting their bottom plate to the output amplifier. Therefore, both common mode and differential mode charge is transferred [3]. The output capacitors are disconnected before putting the circuit into sample mode by ensuring □4 switches is open.

The op-amp remains in open-loop configuration during the sampling phase when using this architecture. Therefore, op-amp doesn't have to settle down when switching from hold phase to sampling phase.

The input differential voltage of sample-and-hold circuit can be described as [7]:

$$V_{in} = V_{in+} - V_{in-} \qquad (1)$$

Whereas, the output differential voltage of sample-and-hold circuit can be described as:

$$V_{out} = V_{out+} - V_{out-} \qquad (2)$$

The switch in sample-and hold circuit can be realized as simple MOS transistor, transmission gate or bootstrapped type. For low power consumption requirement, the switches of simple MOS transistor are used in this circuit due the lowest number of transistor. The minimum value of sampling capacitor, Cs is approximately 1pf and the maximum value of load capacitance, $C_L$is assumed as 1pf.

III. OP-AMP DESIGN

Op-amp is the main part of sample and hold circuit. There are several types of fully differential op-amps which are telescopic, folded-cascode, multi-stage and gain boosted op-amps [5]. In designing an op-amp, several electrical characteristics, for example gain-band width, slew rate, common-mode range and output swing have to be taken into consideration. Table I shows the comparison of performance of various amplifiers topologies [5].

TABLE I. COMPARISON OF PERFORMANCES OF VARIOUS OP-AMP TOPOLOGIES

	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic	3	5	2	2	2
Folded-cascode	3	4	3	3	3
Multi-stage	5	2	5	2	3
Gain-Boosted	4	3	3	3	5

1=LOWEST 2=LOW3=MEDIUM 4=HIGH 5=HIGHEST

As seen from Table I, the multi-stage topologies would results in higher gain and medium power consumption. The folded-cascode amplifier also results in medium power consumption but it give a medium gain. Therefore, for this paper the two-stage (multistage) amplifier is chosen to be compared with the folded cascode amplifier. The design of multistage amplifier can be used where low power consumption and high gain are the main requirements.

The topology of two-stage op amp is shown in Figure 4. For the design of input amplifier, a fully differential (in and out) pair with current mirror biasing is employed. For output stage a common source amplifiers is been used to provide a large gain in output stage [4].

IV. SIMULATION RESULTS

There are three parts of simulation result discussed in this section which is the simulation output of sample-and-hold circuit and in the second part the result of power consumption of sample-and-hold circuit and the last part is the DC gain.

A. Simulation of sample-and-hold-circuit

Sample and hold circuits (SHC) are important in converting analog signals to digital signals. The main function of SHC is to copy of the analog signal and hold its value until the ADC can process the information [7].

Figure 5 shows the simulation output of switch capacitor sample-and-hold circuit. The simulations are done in 0.18µm CMOS technology considering 1.2 Vpp voltage and 1.8V voltage supply. The output of the sample-and-hold seen does not exactly match the input signal. From the output, it showed that the output is referred to voltage reference, Vref which is equal to 0.3V.

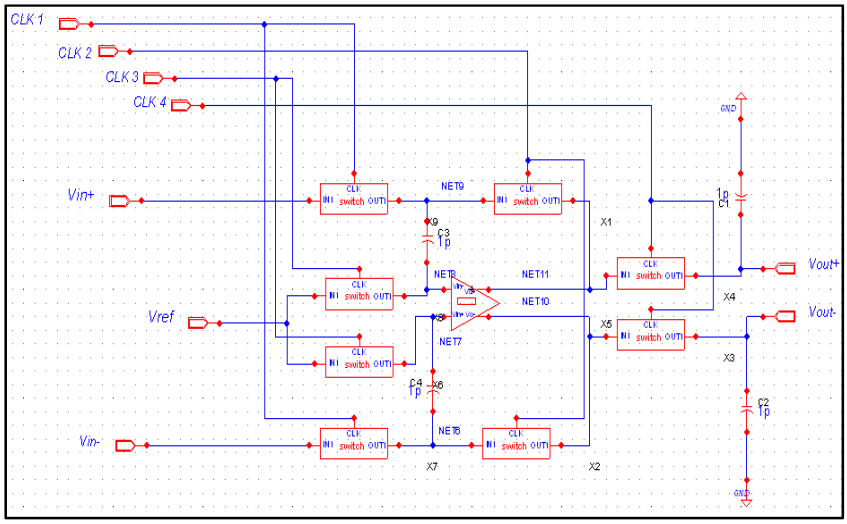

Figure 2: Switch-capacitor sample and hold circuit

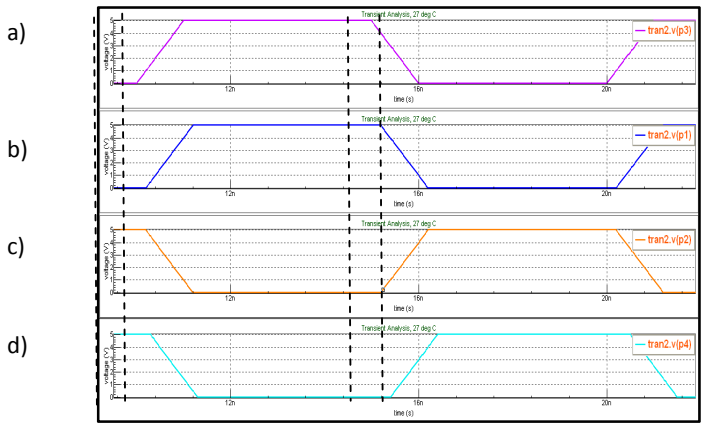

Figure 3: Clock scheme: a) Clock 3 (ϕ3), b) Clock 1 (ϕ1), c) Clock 2 (ϕ2), and d) Clock 4 (ϕ4)

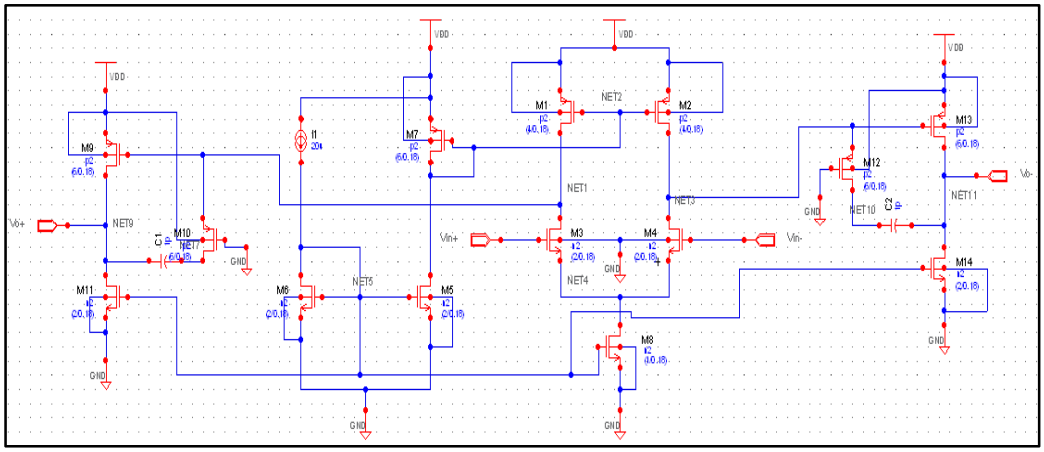

Figure 4: Circuit of two-stage op-amp

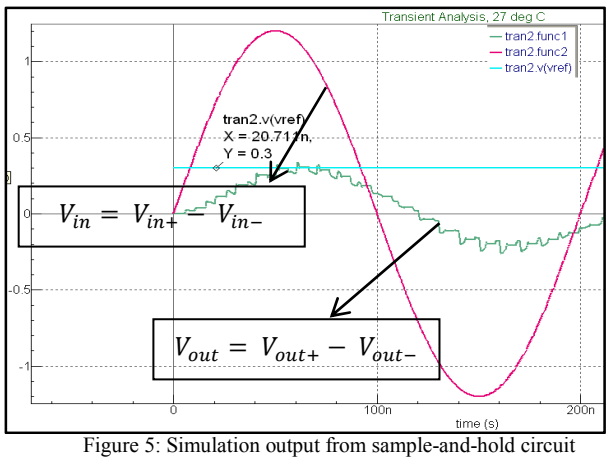

Figure 5: Simulation output from sample-and-hold circuit

B. *Power consumption*

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Nowadays, minimum power consumption in integrated circuit is necessary in reducing cost and noise. Significant power is only drawn when the transistors in the CMOS device switch between on and off state. Power dissipation is the wastes power in form of heat and voltage drop. For this paper, power consumption for sample-and hold circuit are measured by editing SEdit as in Figure 6.

The comparison with the previous work is summarized in Table II. From Table II, the power consumption in present work has reduced 97%compared to the previous work [2].

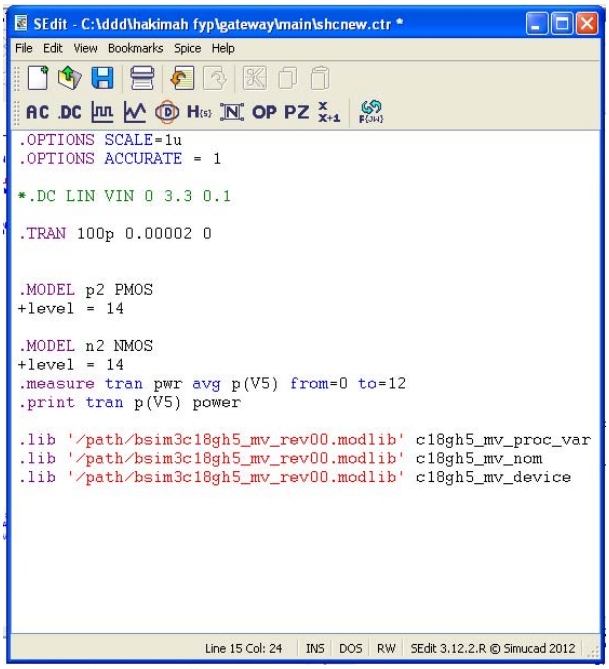

Figure 6: SEdit for power consumption measurement

C. Gain

There are different types of frequency compensation techniques. These include pole splitting miller compensation, self-compensating capacitor, additional amplifier and negative miller compensation. In resolve the stability problem, the proper compensation techniques employed. A RC miller compensation technique is employed in this study.

For two-stage op-amp, the DC gain can be express as:

$$A_v = A_{v1} \times A_{v2} \qquad (3)$$

A_{v1} or A_{v2} are gain of two different stages for a two-stage op-amp. For the first stage, a fully differential amplifier has been employed. Figure 7 is the fully differential amplifier circuit.

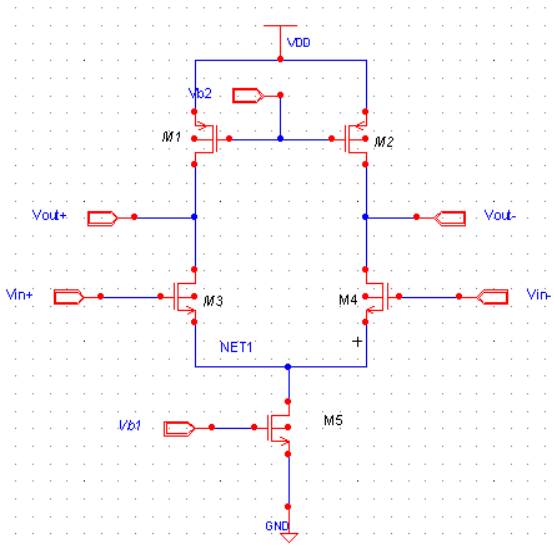

Figure 7 : Fully differential amplifier

The DC gain also can be represented in following form:

$$A_{vi} = G_{mi} \times R_{out\,i} \qquad (4)$$

Here A_{vi} is DC gain of i_{th} stage of amplifier system independent from the frequency, G_{mi} is transconductance of input network and R_{outi} is the effective output resistance of output network. The equation (4) is derived from AC equivalent circuit analysis for the load circuit of differential amplifier. For this circuit all DC supplies must be assumed grounded (0V) and replace the transistor with hybrid-π equivalent circuit as in Figure 8.

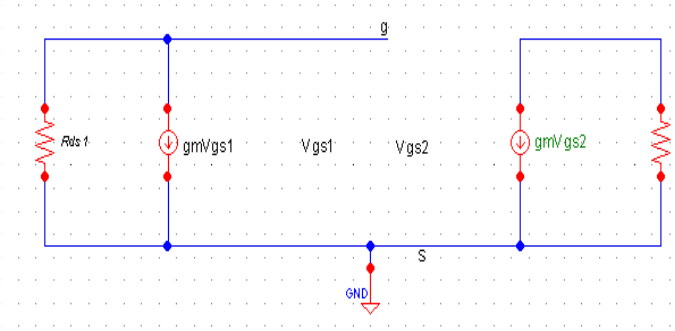

Figure 8 : hybrid-π equivalent circuit for transistor

Current source is remove by using equivalent transistor technique.

$$R_{eq} = \frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m} \quad (5)$$

$$A_v = \frac{V_o}{V_{in}} = \frac{-g_m v_{gs} R_{ds}}{V_{gs}} \quad (6)$$

$$A_v = -g_m R_{ds} \quad (7)$$

$$R_{ds} \approx R_L = R_{out} \quad (8)$$

Lastly, the differential amplifier can be simplified as shown in Figure 9. From the complete circuit analysis,

$$G_{m1} = g_{m1,2} \quad (9)$$

Here the $g_{m1,2}$is the transconductance of NMOS input transistor M1 or M2.

For the second stage, the common source amplifier is employed. Like the first stage, AC equivalent circuit analysis for the common source amplifier is employed.

From the complete circuit analysis,

$$G_{m2} = g_{m9,11} \quad (10)$$

Here the $g_{m9,11}$ is the transconductance of PMOS transistor M9 or M11. g_m is a function of device dimension (W/L), bias current (I_D) and overdrive voltage (Vov).

$$g_m = f\left(\frac{W}{L}, I_D, V_{ov}\right) \quad (11)$$

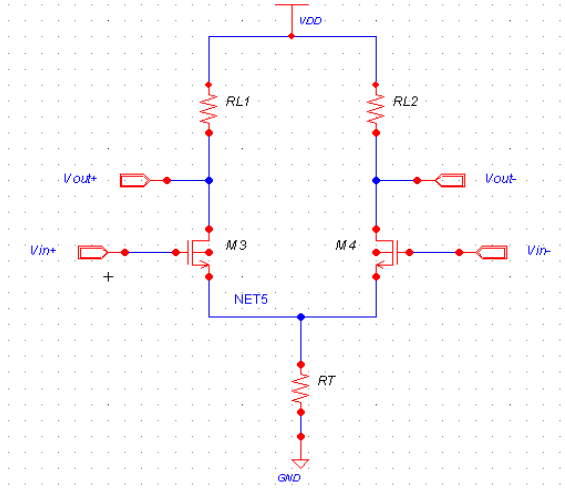

Figure 9: Differential amplifier with load resistor, R_L

The circuit is analyzed using AC analysis. The RC circuit with 1µF capacitor and 1kΩ resistor is applied to the op amp. Finally, simulation results of the two-stage amplifier are shown in Fig. 9. This simulation result is compared to the previous work which is the folded-cascode amplifier was used. Table II shows the comparison of present design results with previous work [2] and there is improvement in the present results compared to the previous design.

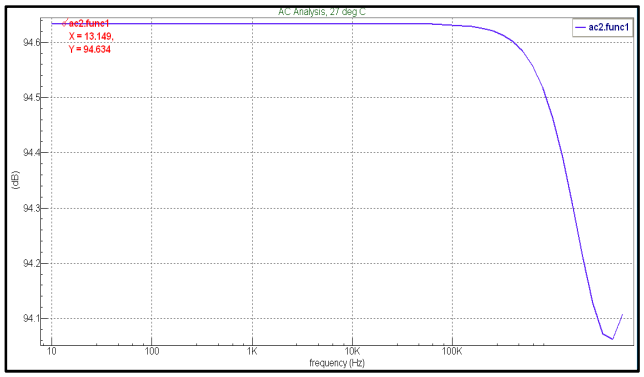

Figure 10: Simulation result of AC analysis of op-amp

TABLE II. COMPARISON BETWEEN PREVIOUS AND PRESENT WORK

	Previous work	**Present work**
Type of op-amp	Folded-cascode	Two-stage
CMOS technology	0.18µm	0.18µm
Power consumption	6.5mW	0.139mW
DC gain	70dB	94.64dB

V. LAYOUT OF SHC

The layout of the low power consumption sample-and-hold circuit for pipelined ADC using 0.18µm is shown in Fig. 10. The design rule check (DRC) with no error is shown in Fig. 11.The area of the layout is 77.83µm x 49.91µm.

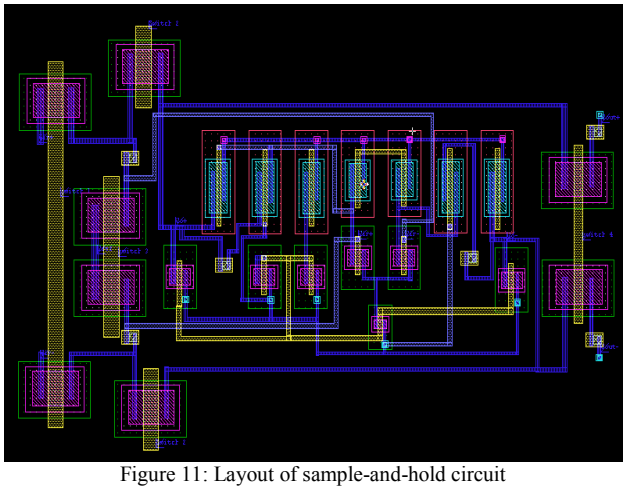

Figure 11: Layout of sample-and-hold circuit

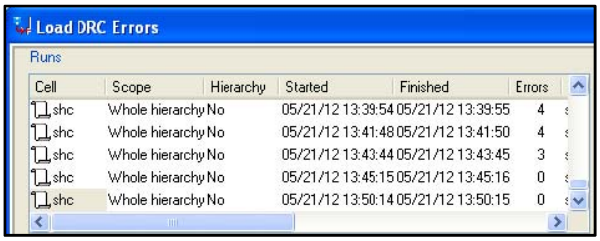

Figure 12: Design rule check (DRC) of layout sample-and-hold circuit

VI. CONCLUSIONS

In this paper, low power sample-and-hold architecture use two-stage op-amp to achieve low power operation and high gain. The design is simulated using 0.18µm technology and can operate in low power which is 1.8V of power supply. The switch-capacitor sample-and-hold circuit is compared with previous sample-and-hold circuit using a folded-cascode amplifier. The simulation results indicate that the sample-and-hold circuit with two-stage op-amp reduced 97% low power consumption compared to the previous work and increased the gain approximately 35%. The specification for the low power sample-and-hold circuit is 5GHz of sampling frequency and 0.139mW of power consumption based to Gateway EDA tools simulation result. For future development, 90nm technology can be applied to this sample and hold circuit to obtain higher gain and lower power.

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