Low-Voltage CMOS Analog Bootstrapped Switch For Sample-and-Hold Circuit: Design and Chip Characterization

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Abstract - **This paper presents the design and characterization of a sample-and-hold circuit based on a novel implementation of the bootstrapped low-voltage analog CMOS switch. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage doubler. Through the use of a dummy switch, the charge injection induced by the bootstrapped switch is greatly reduced, resulting in improved sample-and-hold accuracy. Experimental results in a 0.18 μm digital CMOS process show that a resolution greater than 10 bits can be obtained with a 1.0 V supply voltage. Circuit operation is also possible for supply voltages close to transistor threshold (e.g., 0.65 V)**.

1. INTRODUCTION

Most analog-to-digital converters (ADC) typically employ a sample-and-hold circuit at the front end that must achieve high speed, high linearity and high precision with low-power dissipation. In low-voltage systems, analog sampling becomes particularly difficult because the limited headroom severely degrades the tradeoffs among dynamic range, linearity, speed and power dissipation.

Among the most serious factors affecting the performance of a high-precision CMOS sample-and-hold circuit are charge injection and clock feedthrough [1]. Several methods have been proposed to overcome these problems, such as charge cancellation by a dummy MOS transistor and an offset cancellation by adding a compensation network [2]. Although charge cancellation methods that make use of a dummy transistor produce good simulation results, great care must be exercised when laying out the clock tree controlling the complementary switches. Other methods have either limited input bandwidth or introduced high design complexity.

Although the above techniques are useful and commercially utilized, it should be understood that they represent a tradeoff with respect to speed, power consumption and design flexibility. Alternatively, bootstrapped analog switches have been extensively used for rail-to-rail switching functions in low-voltage SC circuits [3]. They show a constant charge injection through the whole range of operating supply voltage at the expense of an input-dependent clock feedthrough. This technique, however, introduces reliability problems, in particular for devices with reduced oxide thickness, t_{ox}. The Semiconductor International Association (SIA) roadmap [4] shows the forecasted gate-oxide thickness as a function of time. It also indicates the maximum electrical field across the oxide. The electrical field becomes increasingly high as t_{ox} shrinks below 2 nm. It is known that oxide breakdown is one of the limiting factors for circuit reliability. Therefore, utilization of the bootstrapped low-voltage analog switch for advanced VLSI processes will be limited in the next few years by the need for a low-stress clock voltage doubler circuit. To overcome these limitations, we propose a novel low-voltage, low-stress and reliable clock signal doubler. This clock doubler has been used in the implementation of a dummy compensated bootstrapped switch.

We will start with a brief review of the basic principle of the analog low-voltage bootstrapped switch in Section 2, followed by the development of our main proposal. Section 3 will focus on the experimental test chip results and we will conclude in Section 4.

2. DEEP SUBMICRON LOW-VOLTAGE CMOS ANALOG SWITCH

The main characteristic of the MOS transistor is that by itself it is an analog switch. It is extensively used in switched capacitor circuit gain stages, capacitors and resistors, D/A and so on. Drain and source terminals are the two switch terminals and the gate (and sometimes the bulk) terminals are used to control conductivity. Ideally, the switch in the on state acts as a fixed linear conductance g_{ds}. In practice, the conductance is strongly signal-dependent. Equation (1) gives the conductivity of the transistors as a function of the power supply voltage V_{DD} and the input signal.

$$g_{ds} = \begin{cases} kp_n \cdot \frac{W}{L} \cdot \left[V_{DD} - V_{in} - V_{tn} - \gamma_n \left(\sqrt{2\phi_f + V_{in}} - \sqrt{2\phi_f} \right) \right] \text{ nMOS} \\ kp_p \cdot \frac{W}{L} \cdot \left[V_{in} - \left| V_{tp} \right| - \gamma_p \left(\sqrt{2\phi_f + V_{DD} - V_{in}} - \sqrt{2\phi_f} \right) \right] \text{ pMOS} \end{cases} \quad (1)$$

The bulk of the nMOS and pMOS transistors are respectively connected to V_{SS} and V_{DD} unless otherwise stated.

Plots in Fig. 1, show the switch conductance versus input signal V_{in}.

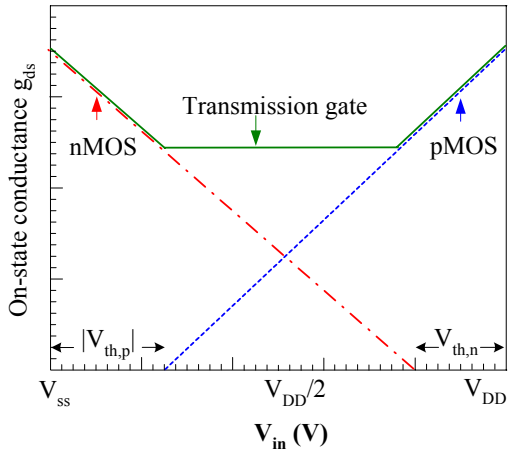

Figure 1: On-state conductance of MOSFET switch versus the potential of the switched input signal.

As shown in equation (1) and corresponding Fig. 1, the switch conductivity depends not on the absolute potential of the control terminals, but on their potential relative to the others. The conductance through the whole range of input is also not constant, and depends on the supply voltage, which becomes extremely low. To ensure rail-to-rail switching operations control, signals exceeding the supply voltage range are required. This is known as the bootstrapped switching technique [3].

A general block diagram of the bootstrapped switch is shown in Fig. 2a. It consists of three main elements: the pass-transistor (nMOS, pMOS or both types), a control signal generator and, finally, a clock booster. The control circuit generates a signal linearly related to the input signal. The purpose of the clock booster is to generate a clock signal over and above the supply voltage. In the classical case of a transmission gate, the clock booster and the control circuit are absent.

A functional diagram of a clock booster is shown in Fig. 2b and the new low-voltage low-stress clock booster circuit is depicted in Fig. 2c. Feedback transistor P_{b4} keeps the gate-drain voltage of transistor P_{b3} to a reasonably low level and is subjected to a maximum source-gate voltage of $V_{DD}+|V_{tp}|$, which is acceptable in most processes.

The bootstrapped switch compensation scheme is depicted in Fig. 3a while the control circuit (with pMOS–type pass devices) is shown in Fig. 3b. Several issues have been considered in the type of transistor for the pass device (i.e., nMOS or pMOS). The most important from a dynamic linearity viewpoint are the ON-resistance R_{ON} and the channel charge Q_{CH}. All of these parameters scale with switch size; in the n-well process used where $kp_n \approx 4 \times kp_p$ and $kp_p = \mu C_{ox}$, a pMOS device will consume 4 times the area of an nMOS device. However, a pMOS device exhibits a relatively constant conductance and channel charge, independent of the input signal, and can therefore be more easily compensated. Hence, we use a pMOS device as the pass device. The dummy analog bootstrapped switch is shown in Fig. 3c.

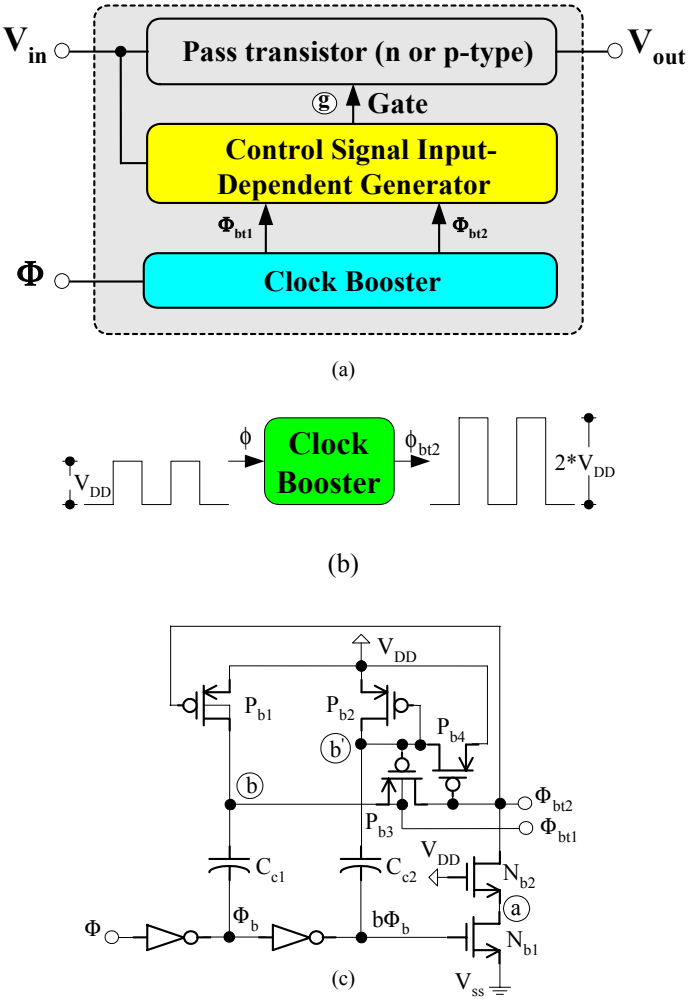

Figure 2: (a) Block diagram of a bootstrapped switch (b) Functional diagram of a clock booster (c) pMOS-type clock booster circuit.

The reliability of the circuit can be further improved by carefully laying out some of the critical devices. Although the relative voltages between gate, source, and drain do not exceed V_{DD}, the drain-to-substrate and source-to-substrate voltages of some devices exceed V_{DD} (assuming an n-well process). Devices N_{b2} (Fig 2c) and N_2 with P_{5b} (Fig. 3b) are subject to this large voltage. Thus, for improved reliability, the drain of devices N_{b2} (Fig. 2c) and N_2 with P_{5b} (Fig 3b) should be laid out circularly. The "doughnut" transistor structure also has the advantage of being area-efficient with less parasitic capacitance at the drain, making this structure attractive for high-speed applications. The lateral spacing of the metal layers shrinks with scaling while the thickness of the metal layers and the vertical spacing of the metal layers stay relatively constant. This effect has been used in the capacitor implementation [5].

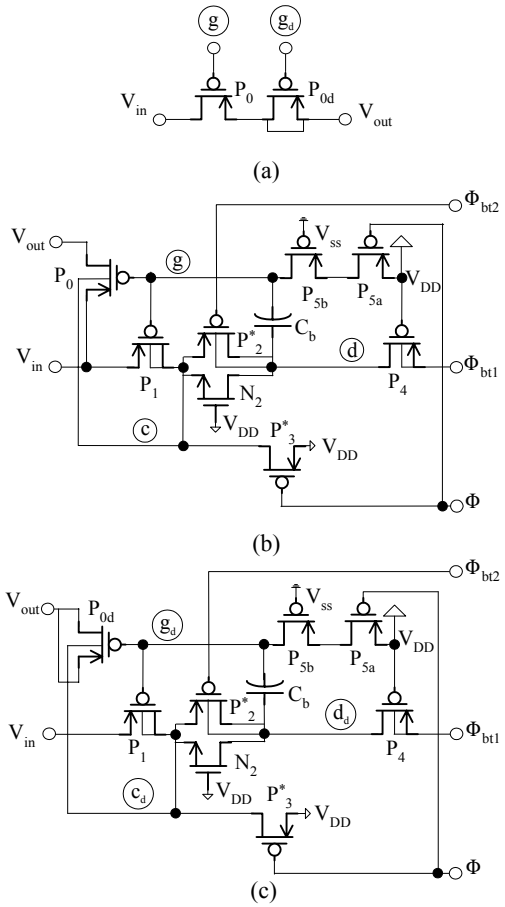

Figure 3: (a) Bootstrapped switch compensation scheme; (b) Proposed pMOS-type pass transistor implementation; (c) Dummy bootstrapped switch.

3. EXPERIMENTAL RESULTS

A test chip was designed and fabricated with a TSMC 0.18 µm CMOS process (single poly, n-well) to confirm the operation of circuit topology, and Fig. 4 shows the die photography of the clock booster with the bootstrapped switch.

Clocks and single frequency sinusoidal input signals were generated using Hewlett Packard HP81130A pulse and HP33120A arbitrary waveform generators, respectively. Chip output signals were observed using Tektronix analog and digital oscilloscopes TDS320 and TDS7154.

The design procedure and characterization method of a low-voltage CMOS analog switch without the need for clock boosting are presented in [6] with application to the design of a CMOS transmission gate operating at a 10 MHz clock signal under a 1.8 V supply voltage in a 0.18 µm digital CMOS process. This characterization method is extended here to the bootstrapped analog switch and results will be reported. The load resistance, R_L, and capacitance, C_L, are respectively chosen to be 1 kΩ and 5 pF.

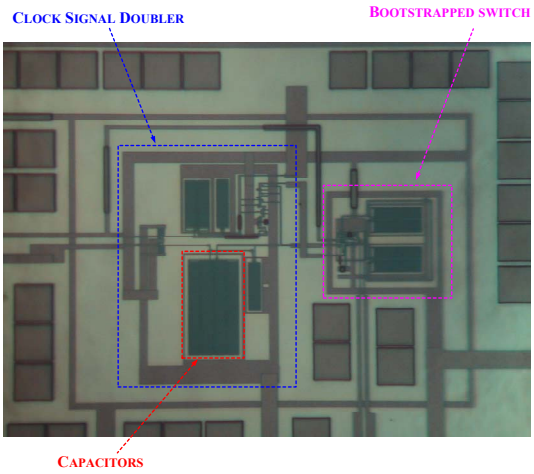

Figure 4: Photography of the test chip.

The off-chip input clock signal falling and rising times are equal to 2ns. It should be noted that this signal is reshaped by the on-chip pad buffer. Fig. 5 presents the results of a comparison between the simulated ON-resistance and the measurement results under a 1.0 V operating supply voltage respectively.

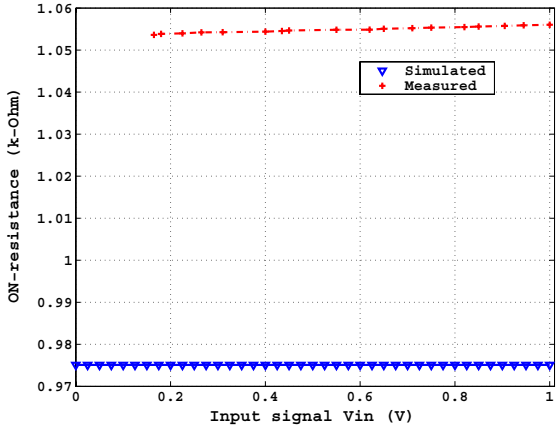

Figure 5: Comparison between simulated and measured switch ON-resistance variations at 1.0 V supply voltage.

Fig. 6 presents the dependence of the feedthrough error voltage with respect to the analog input. An almost linear variation is observed. The dummy compensation mechanism removes the charge injection contribution from the observed voltage error to a very low level. It should be noted that charge injection is a function of many factors, and the effects of load capacitor size, clock edge speeds, impedance loads, etc. on the injection mechanism are well described in [1].

Measured waveforms in Figure 7 show the circuit performing a sample-and-hold operation with an input signal amplitude of 1 V_{pp} under a supply voltage of V_{DD} = 1 V. Figs 8 and 9 show the spectrum of the sample-and-hold waveform under a sampling frequency of 0.25 MHz based on a coherency sampling method [5]. The measured SINAD obtained for a

supply voltage of about 1.0 and 0.65 V is 71.0527 dB and 45.775 dB, respectively in the Nyquist bandwidth. This corresponds to an effective resolution of 11.5 bits and 7.3 bits, respectively.

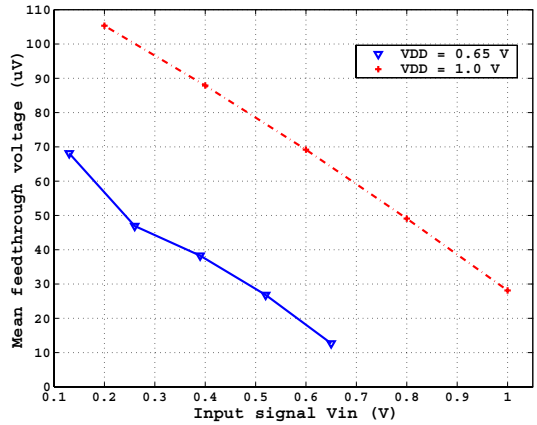

Figure 6: Measured dependence of the feedthrough voltage on the analog input.

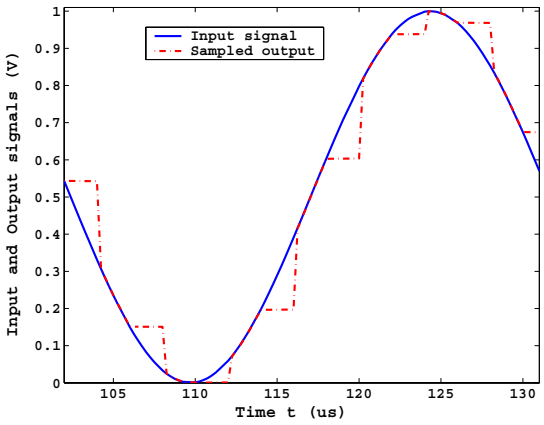

Figure 7: Measured input/output of the bootstrapped switch circuit test chip under a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 1 V_{PP} under V_{DD} = 1 V.

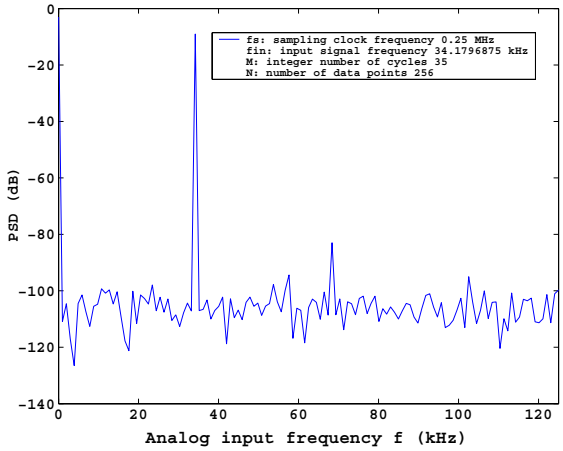

Figure 8: Measured spectrum of the bootstrapped switch-based sample-and-hold circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 1 V_{PP} under a supply voltage of V_{DD} = 1 V.

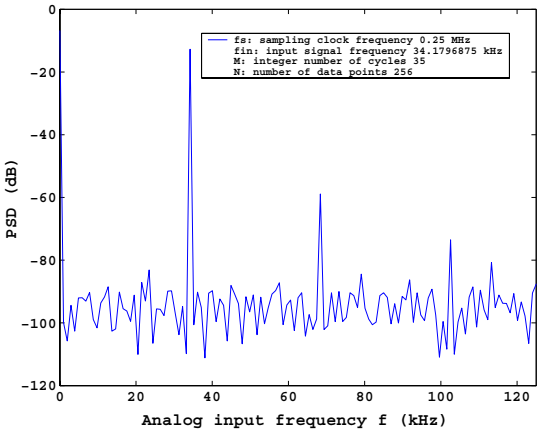

Figure 9: Measured spectrum of the bootstrapped switch-based sample-and-hold circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 0.65 V_{PP} under a supply voltage of V_{DD} = 0.65 V.

4. CONCLUSION

In this paper the design and characterization of a low-voltage, CMOS analog bootstrapped switch suitable for a high-precision sample-and-hold circuit has been presented. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage double. An important attribute of the design is that the ON-resistance is nearly constant. Test chip experimental results using a 0.18 µm digital CMOS process show that a resolution greater than 10 bits can be obtained with a 1.0 V supply voltage. The rail-to-rail input range capability enables the circuit to be used in high-resolution applications such as successive approximation and pipelined ADCs, to name just a few examples.

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