The testing of this circuit required the use of active probes and "bias-tee" networks. In this way superpositions of dc and high-frequency ac signals were delivered to the circuits and the on-chip signals were measured reasonably uncorrupted by reflections. The experimental results are shown in Fig. 4 and Table I. The ratio of the differential response to the common-mode response at dc, as illustrated in Fig. 4(b), is only 32 dB. This considerably smaller number than in the "two-stage" case is mainly due to the lower common-mode-signal open-loop gain. However, the differential offset voltage is also smaller. The noisy appearance at high frequencies in the phase curves in Fig. 4(c) is due to measurement inaccuracies. The output swing is limited by the value of the balancing voltage V_{bal}, which for the application intended was 3.5 V.

V. Conclusions

Differential amplifiers with accurately balanced outputs can be easily realized if the differential-mode circuitry and the common-mode circuitry are treated equally in the design process. A convenient way of accomplishing this is to use a topology that combines the two parts as close as possible to the front end of the amplifier. In this way most of the design issues such as gain, compensation, etc. are addressed at the same time for both the differential- and common-mode signal paths. The design strategy discussed in this paper has been verified with two CMOS balanced amplifiers.

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A Rail-to-Rail CMOS Op Amp

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***Abstract*—A CMOS op amp is reported which has a rail-to-rail voltage range at its input as well as its output. A new area-efficient output stage has been used. While the entire op amp occupies only 600 mil^2, when used as a unity-gain buffer, and with ±5-V supplies, the op amp can drive a 9-V_{pp}/1-kHz sine wave across a 300-Ω load with −64 dB of harmonic distortion.**

I. Introduction

The first generation of CMOS op amps was limited to transconductance amplifiers. They had modest performance and were able to drive only capacitive loads. The second generation of these op amps, in addition to high-performance transconductance amplifiers, includes general-purpose op amps. These op amps can drive resistive as well as capacitive loads with a level of performance which is comparable to that of their bipolar counterparts [1]. For these op amps folded-cascode amplifiers are commonly used as the input stage. For the output stage, on the other hand, a variety of different circuits have been used [2]–[4]. In this paper a new output stage is presented which, although compared to the previous works uses smaller size output transistors, nevertheless has a very good current driving capability. It is described in Section II, while the overall op amp is covered in Section III. Finally, the measurement results obtained from an integrated test circuit are given in Section IV.

II. The Output Stage

The important criteria for designing an output stage are as follows:

1) low standby power dissipation which is controlled by a, preferably supply-independent, current source;
2) good current driving capability;
3) large small-signal transconductance in order to provide some voltage gain when driving heavy resistive loads and also to move the capacitive load-dependent pole to higher frequencies; and
4) simple circuit configuration so as to avoid additional parasitic poles.

Most of the output stages reported in the literature [2]–[4] have limited driving capability mainly because of the limited V_{GS} of the output devices. Consider now the new output stage which along with its biasing section and the block diagram representation of the input stage is shown in Fig. 1. Here, a differential-output, input stage is employed where an additional common-mode feedback (CMF) circuit sets the dc voltage values of the two differential outputs, i.e., $V_{o1} = V_{o2} = V_n = V_b$. Therefore, assuming that $(W/L)_1/(W/L)_3 = (W/L)_2/(W/L)_4$, the current I_o in the output devices becomes

$$I_o = \left[\frac{(W/L)_2}{(W/L)_5}\right] I_Q \tag{1}$$

which can be made supply independent.

For this circuit, assuming that the input stage does not impose any limit, when the output stage needs to draw its maximum

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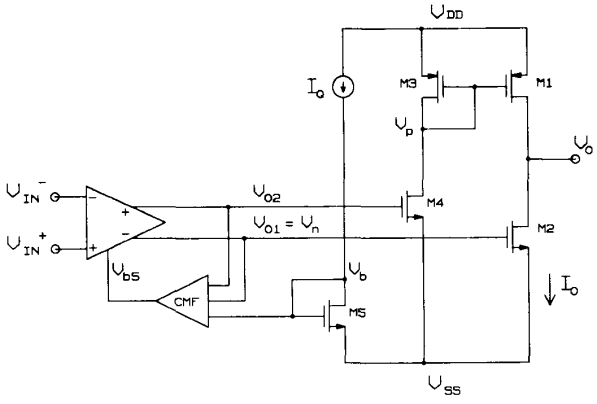


Fig. 1. The new output stage along with a block diagram of the input stage and the biasing section.

sinking current, $V_{o1} = V_n$ can swing all the way up to V_{DD} resulting in a rail-to-rail gate-to-source voltage for M_2. For the sourcing condition, V_{o2} swings to V_{DD} forcing M_4 into the linear region. This in turn causes V_p to move close to V_{SS} resulting in a large V_{GS} for M_1. In fact, using simplified $I-V$ equations for the saturation and linear regions and applying them to transistors M_3 and M_4, respectively, it can be shown that

$$(V_{GS})_{\max} = \frac{\alpha(V_{DD} - V_{SS}) + V_T}{\alpha + 1} \tag{2}$$

where $\alpha = 2(k_4/k_3)$ and k_3 and k_4 are the transconductance parameters while V_T is the threshold voltage for both n- and p-channel transistors. Notice that by choosing large values for α, i.e., by increasing $(W/L)_4$ with respect to $(W/L)_3$, $(V_{GS1})_{\max}$ approaches the rail-to-rail voltage. Even when M_3 and M_4 have equal sizes, due to the higher mobility of the carriers in n-channel devices versus those in p-channel devices $(V_{GS1})_{\max} \simeq 0.86(V_{DD} - V_{SS})$. Because of the complementary nature of the differential outputs of the input stage, when one of the outputs is close to V_{DD}, the other one is close to V_{SS}. As a result, when one of the output transistors is heavily conducting, the other transistor is OFF. In this output stage, unlike the ones mentioned before, since the output transistors can have rail-to-rail V_{GS} voltages, for a given amount of output current they can have smaller sizes.

The small-signal transconductance of the output stage is $g_{mtot} = g_{m2}$ which is determined only by the n-channel output transistor M_2. There is only one parasitic node in addition to the two input nodes and one output node. This makes the circuit suitable even for high-frequency applications where excess phase shift must be avoided.

III. The Complete Op Amp

A circuit diagram of the complete op amp is shown in Fig. 2. Transistors $M_{40} - M_{47}$ along with resistor R_B constitute the biasing section. Here a resistor is used to set the biasing current. This reduces its sensitivity to supply and process.

A. Input Stage

The output stage which was discussed in the previous section must have a balanced-differential input which can swing rail to rail and with such a common-mode voltage so as to generate a given quiescent current in the output transistors. Moreover, when driving heavy resistive loads, the output stage has a low gain, therefore the input stage must provide a large voltage gain. Finally, for a unity-gain buffer, wide common-mode input range is required. Based on these requirements, a folded-cascode differential-input, differential-output circuit was chosen. Transistors $M_6 - M_{17}$ and $M_{26} - M_{29}$ realize the main differential-output input stage which has a rail-to-rail input range. $M_{18} - M_{23}$ comprise the CMF circuit while M_5 along with its cascode current-source devices M_{24} and M_{25} make up the output stage biasing section.

B. Power Regulation

The input stage includes transistors $M_{30} - M_{37}$. These transistors are used to regulate the variations in the op-amp power dissipation with respect to the input common-mode range. The same circuit also reduces the changes in open-loop gain and phase margin with respect to the common-mode input. Here, the current in transistors M_{10} and M_{11} as well as M_{16} and M_{17} has been divided into two components: one which is constant and the other which is input dependent; i.e., when their corresponding input pair devices turn off that current component becomes zero [8]. Now the sum of the currents through the pairs $M_{10A} - M_{10B}$, $M_{11A} - M_{11B}$, $M_{16A} - M_{16B}$, and $M_{17A} - M_{17B}$ are normally equal to $2I$ while the currents in $M_{12} - M_{15}$ are equal to I. When the input common-mode voltage increases to V_{DD} or decreases to V_{SS}, devices M_8, M_9, M_{32} or M_{26}, M_{27}, and M_{36} cut off, respectively. For the first case, the current through devices M_{16A} and M_{17A} drops to zero while for the second case that of M_{10A} and M_{11A} reduces to zero. As a result, the voltages V_{o1} and V_{o2} and hence the bias current in the output devices M_1 and M_2 become insensitive to the input common-mode voltage.

C. Frequency Compensation

The op amp has been compensated using two Miller capacitors along with their corresponding zero-nulling MOS resistors. The open-loop gain is calculated to be $A = (g_{m8} + g_{m26}) r_o g_{m2} R_L$ where r_o is the output impedance of the input stage. Assuming widely spaced poles and zeros, the dominant pole is calculated as

$$p_D = -\frac{1}{r_o(C_{M1} + C_{M2})}. \tag{3}$$

The first term $C_{M1} = (1 + g_{m4}/g_{m3})(C_1/2)$ is the one-half of the Miller capacitance which is due to the compensation capacitance C_1 and the gain stage made out of transistors M_3 and M_4. The second term $C_{M2} = g_{m2} R_L C_2$ is the Miller capacitance due to the compensation capacitance C_2 and the gain stage made out of transistors M_1 and M_2. While C_L along with other parasitic capacitances generate poles and zeros which are above the unity-gain frequency, the CMF circuit creates a pole–zero doublet which is an order of magnitude below the unity-gain frequency. These are given by

$$p_1 = -\frac{g_{m20}}{\left(\dfrac{C_{M1}C_{M2}}{C_{M1} + C_{M2}}\right)}$$

$$z_1 = -\frac{2g_{m20}}{C_{M1} + C_{M3}} \tag{4}$$

where $C_{M3} = (1 + 2g_{m20}R_2)C_2$ and p_1 and z_1 are close to each other. In fact, for actual values in our case they are off by only 20 percent. As a result this pole–zero doublet does not cause any instability in the frequency response or long tail in transient response [9].

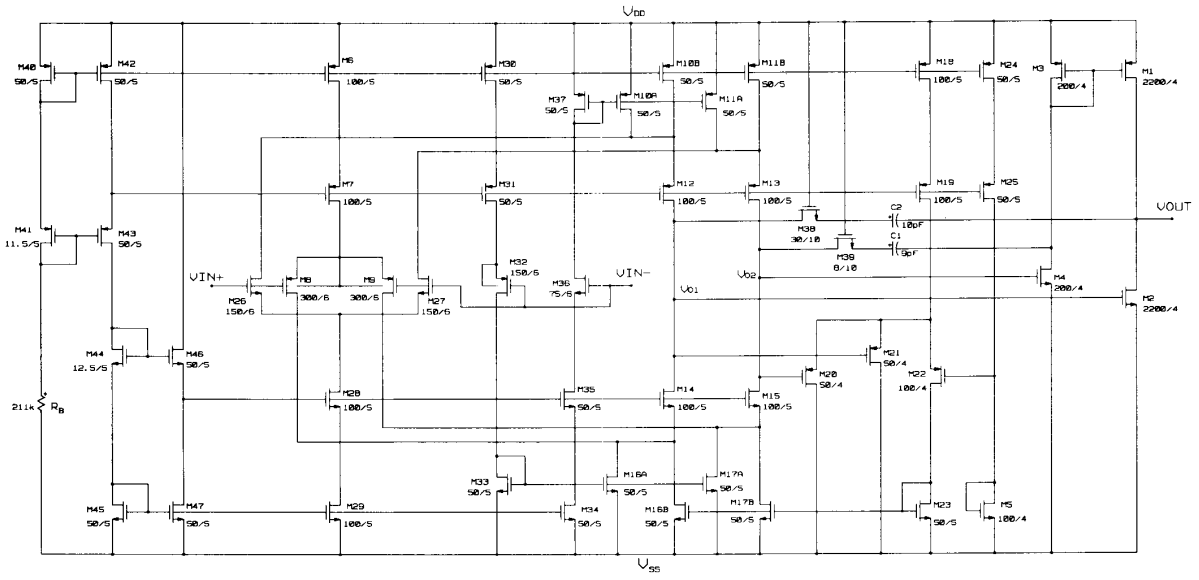


Fig. 2. The complete op amp.

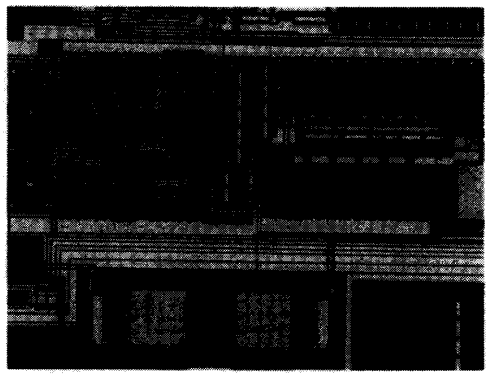


Fig. 3. Die photo of the rail-to-rail op amp.

IV. Measurement Results

The circuit of Fig. 2 was integrated as an uncommitted op amp in a PCM codec chip using a 3-μm, double-polysilicon, single-metal, 10-V process. A photomicrograph of the chip is shown in Fig. 3. In order to reduce the input referred offset voltage, all the critically matched devices of the input stage, i.e., M_8-M_9, $M_{10}-M_{11}$, $M_{16}-M_{17}$, and $M_{26}-M_{27}$, were laid out using the common-centroid technique. Fig. 4 is a histogram of the measured offset voltage of 108 devices. The mean and standard deviation are calculated to be 0.74 and 1.57 mV, respectively. The offset changes by only 1 mV when the input is changed from rail to rail. In order to measure the input voltage range, the op amp was connected in the unity-gain feedback configuration and for ± 5-V supplies a 10-V_{pp} triangular waveform was applied to the input and the unloaded output was measured. The output waveform along with the inverted version of the input waveform and the difference between input and output are shown in Fig. 5(a). Notice that the input range is rail to rail. Fig. 5(b) shows the waveforms when the output is driving a 300-Ω load. The swing loss from the positive side is 400 mV while from the negative side

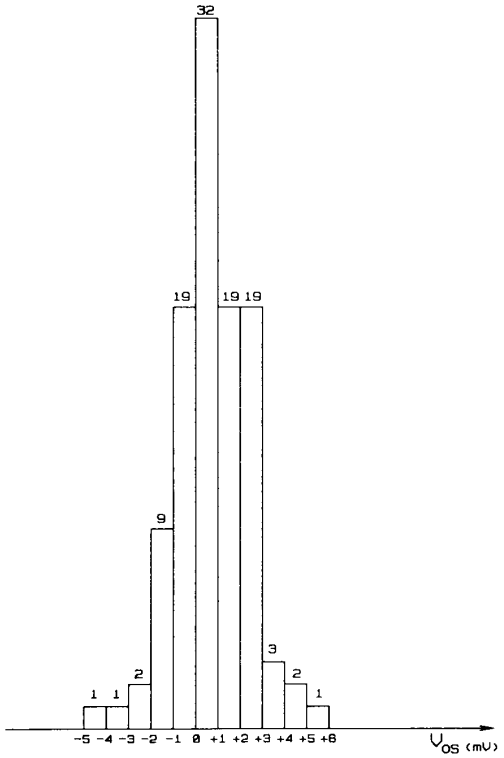


Fig. 4. The distribution of V_{os} for 108 packaged parts. The mean is 0.74 mV and the standard deviation is 1.57 mV.

it is 200 mV. Other measured characteristics of the op amp are tabulated in Table I. Among them notice the high values of open-loop gain, CMRR, total harmonic distortion (THD), and the short-circuit sink and source currents. The latter is an indication of the op amp's driving capability when driving heavy

TABLE I
MEASURED CHARACTERISTICS OF THE OP AMP

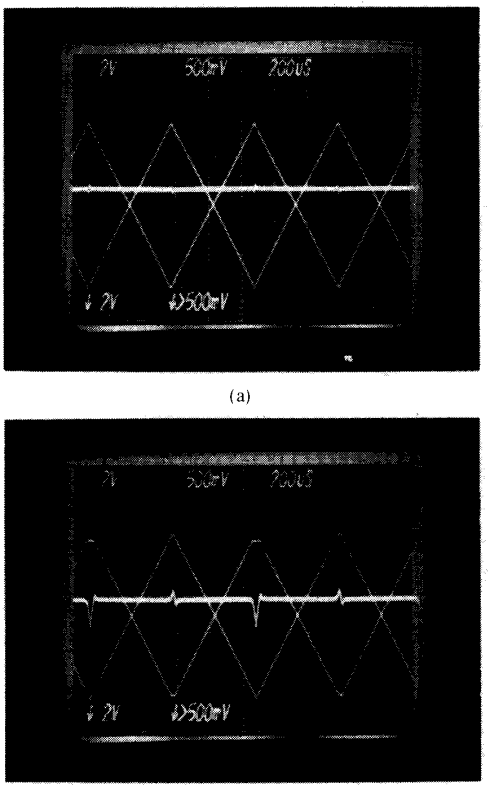
PARAMETER	VALUE
Power Supply Voltage	± 5V
Power Dissipation at zero input	12mW
Variation in Power Dissipation with input common_mode voltage	2mW
Offset voltage Mean Standard Deviation	 0.74mV 1.57mV
PSRR (V_{DD}) @DC @100kHz	 87dB 35dB
PSRR (V_{SS}) @DC @100kHz	 85dB 45dB
Open Loop Gain @DC with 300ohm load without load	 88dB 110dB
CMRR	100dB
Unity Gain Bandwidth with 300ohm || 100pF load with 100pF load	 2.6MHz 3.7MHz
Phase Margin with 300ohm || 100pF load with 100pF load	 81° 47°
Slew Rate Up Down	 3.3V/μsec 2.5V/μsec
Voltage swing no load 300ohm load	 -5V/+5V -4.8V/+4.6V
THD @1kHz 10Vpp no load 9Vpp 300ohm load 7.5Vpp 300ohm load	 -61dB -64dB -79dB
Short circuit current Source Sink	 114mA 290mA
Input noise Spectral density @1kHz	140nV/$\sqrt{Hz}$
Area	600 sq.mils

resistive load. For example, the op amp can drive a 1.5-V_{pp} audio signal across an 8-Ω speaker with −60 dB of harmonic distortion.

V. CONCLUSION

A new op amp has been discussed which has a rail-to-rail voltage range for its input and output. The employed output stage achieves an excellent load driving capability.

Although the proposed op amp was originally designed for ±5-V supplies and a 300-Ω load, it has been used as a unity-gain buffer driving a 100-Ω load while using a single 5-V supply; the signal swing was 3.85 V_{pp}. While this swing is slightly less than the swing of the 5-V buffer op amp which was reported in [2] (4 V_{pp}), the latter occupies three times as much area as the present op amp. The smaller size of the new op amp is mostly due to the smaller size of its output stage.



(a)

(b)

Fig. 5. (a) Output waveform, inverted input waveform, and their difference for no load. (b) Output waveform, inverted input waveform, and their difference for a 300-Ω load.

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