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Methodology for designing and verifying switched-capacitor sample and hold circuits used in data converters

Mahmood Mohammed, Sanad Kawar, Khaldoon Abugharbieh

Department of Electrical Engineering, Princess Sumaya University for Technology, Amman 11941, Jordan
E-mail: m.mohammed@psut.edu.jo

Abstract: This study presents a full methodological approach to designing and verifying differential sample and hold switched-capacitor circuits generally used in analogue-to-digital converters (ADCs). It provides a step-by-step process for translating system requirements such as signal-to-noise ratio and sampling frequency into ADC requirements and subsequently into operational amplifier topology and specifications. It also includes the design process of a switched-capacitor common mode feedback circuit to control the common mode output voltage. Furthermore, this study discusses the noise aspects of the switched-capacitor circuits. It also provides practical methods for verifying the stability of the system by using step voltage and step current techniques. A design and simulation example for a differential sample and hold switched-capacitor circuit operating in a system requiring a 5 MHz sampling frequency and a 6-bit ADC is provided. Mentor Graphics CAD tools were used in the design and the simulations process by using 180 nm complementary metal oxide semiconductors (CMOS) device models. This study can be used as a resource for the design engineers in the industry as well as the universities teaching graduate level advanced electronics and data converter courses.

1 Introduction

Sample and hold circuits (S/H) are used in many applications including biomedical [1, 2] and energy harvesting applications [3], in addition to analogue-to-digital converters (ADCs) [4]. Owing to their ability of tracking an analogue input and storing its value according to the sampling frequency for a specific time length [5], the S/H circuits are considered the core components of the ADCs [6]. Therefore care must be taken in the design of each of their components in order to guarantee a proper and a stable data conversion [7]. Many topologies of the S/H circuits for the ADCs have been proposed such as a bipolar circuit and a current mode circuit in [8, 9], respectively. However, the option of preference is the switched-capacitor circuits as in [10]. These circuits have compatibility with the CMOS processes, good accuracy of time constants, good voltage linearity and good temperature characteristics [11].

The essential components of the S/H circuits for the ADCs, using switched-capacitor circuits, are the operational amplifier (op-amp) and the common mode feedback circuit (CMFB). The CMFB circuit and the S/H circuit are switched-capacitor circuits, whereas the op-amps are designed by using different topologies. However, these topologies must be stable and have the capability of operating within the system requirements. Hence, because of the non-linear nature of the S/H circuits, special attention is required in the design process and the stability verification methods.

It should be noted that the switched-capacitor circuits have some disadvantages. They are subjected to clock feed-through errors and require non-overlapping clocks. In addition, the sampling frequency must be at least twice the bandwidth of the signal [11].

This work presents a full design and verification methodology for the differential S/H switched-capacitor circuits used in the ADCs. It provides a clear step-by-step guidance on how to translate the system requirements into choosing and designing all the components of the S/H circuits. It also provides two unique, yet simple, methods for checking the stability of the system in transient simulations instead of the ordinary AC methods as in [12]. To illustrate the design process, an example S/H circuit is designed to operate in a 6-bit pipeline ADC. The ADC will be used in a system requiring a 36 dB signal-to-noise ratio (SNR) and a 5 MHz sampling frequency, whereas it has a maximum differential input of 1 V peak to peak. Each section contains the corresponding design example and simulation results. Hence, this paper offers a detailed resource for the design engineers and the universities teaching graduate level advanced electronics courses.

The general concept of the S/H circuits is presented in Section 2. It is followed by the design procedure in Section 3, which contains a design flowchart that explains how to translate the system requirements into the ADC specifications. Section 4 introduces the op-amp design with a detailed comparison between different op-amp topologies,

the biasing technique, in addition to the AC and the DC design parameters along with their simulation results. The common mode feedback design, the noise analysis and the overall S/H circuit are presented in Sections 5–7, respectively. Section 8 introduces two unique methods to check the system's stability. Finally, Section 9 concludes the work presented in this paper.

2 S/H circuits

For an ADC system to work properly, a S/H circuit is probably used as the first stage. Fig. 1*a* shows a block diagram of a switched-capacitor S/H circuit including a common mode feedback circuitry. During the sample stage shown in Fig. 1*b* (ϕ1 high), the capacitor C_{IN} will hold a charge equal to the product of its value and the input voltage as shown in (1). During the hold stage shown in Fig. 1*c* (ϕ2 high), both the input capacitors C_{IN} will appear connected in series between the two inputs of the op-amp. Therefore, there will be no voltage difference across these capacitors, and consequently they will no longer have the ability to hold any charge. As demonstrated in Fig. 1*c*, the charge stored on C_{IN} will be completely transferred to the feedback capacitor C_F because of charge conservation. As a result, the output of this circuit tracks its input with a closed-loop gain as shown in (2). The bias block provides the bias currents and the voltages for the op-amp, whereas the CMFB controls the common mode output voltage.

$$Q_{IN} = C_{IN} V_{IN} \tag{1}$$

$$v_{o,differential} = \frac{C_{IN}}{C_F} v_{in,differential} \tag{2}$$

3 Design procedure

Design engineers are usually given system specifications in terms of the SNR, the sampling frequency and the input voltage range. It is vital to know how to translate these requirements into a specific ADC topology and resolution. Subsequently, op-amp specifications like open-loop gain and unity-gain frequency are determined. Fig. 2 is a full design flowchart showing a step-by-step guide of the design process.

The first step is determining the number of the ADC bits, which is determined by the minimum SNR requirement of the system. Equation (3), relates the system SNR requirement directly to the number of the bits N [5], where it has been derived based on the quantisation noise of the ADC.

$$\text{SNR(dB)} = 6.02N + 1.76 \text{ dB} \tag{3}$$

Following that, an ADC topology is selected based on the required resolution and the sampling frequency as shown in Fig. 3 [13]. For the example in this paper, a 6-bit pipeline ADC is used because of its ability to satisfy the system requirements.

Also, the pipeline ADC has the advantages of high speed, high precision and low-power consumption. As a result, the pipeline ADC has become an important topology in the high-speed and the low-power applications [10].

In addition to the speed–resolution trade-off shown in Fig. 3, there is a strong relation between the speed of the S/H circuit and the metal-oxide semiconductor field-effect transistor (MOSFET) devices channel length. This can be clearly seen in the sampling mode where the bandwidth, BW, depends on the time constant, τ, according to (4) [14]. However, τ depends on the capacitor C_{IN} and the

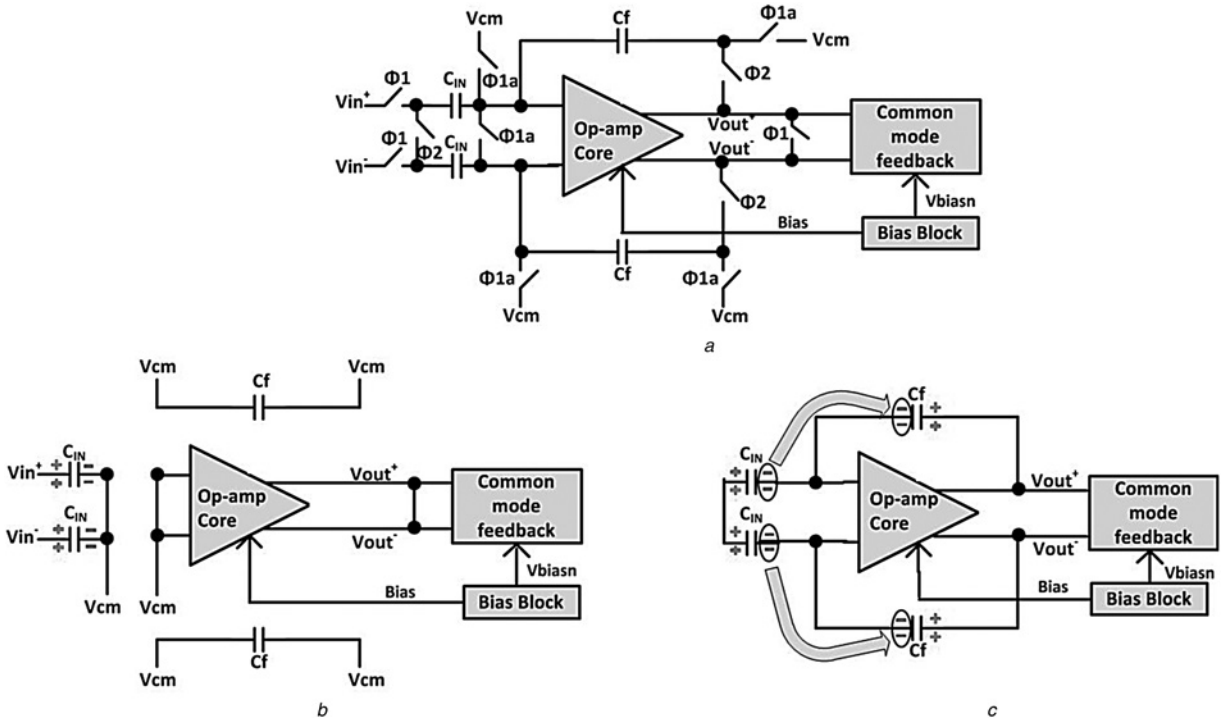

Fig. 1 *Overall sample and hold circuit diagrams*

a S/H block diagram
b Sample stage
c Hold stage

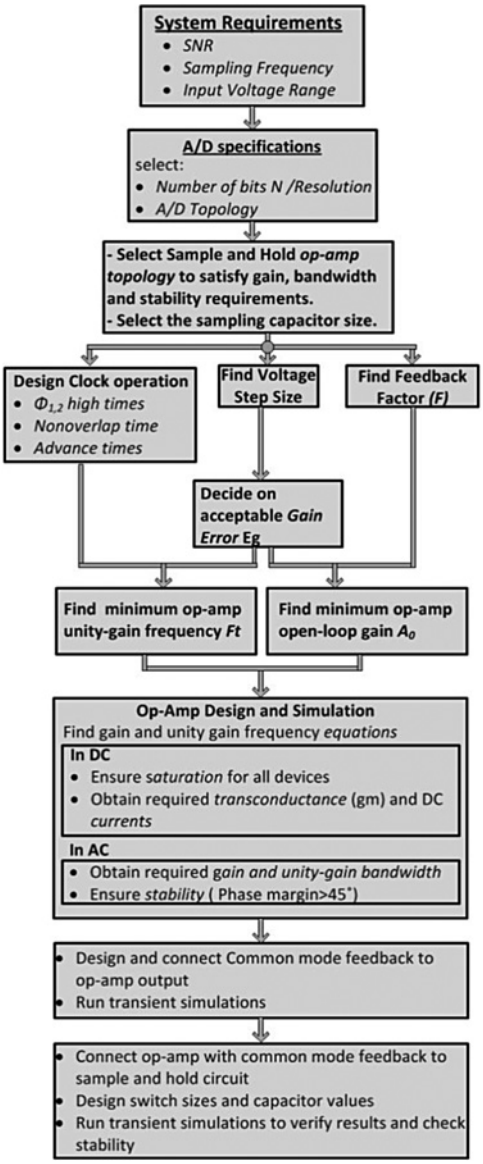

Fig. 2 *Design procedure flowchart*

equivalent resistance of the MOSFET switch R_{ON}, which is approximated by (5). The charge in the switch, Q_{ch}, is given by (6).

$$BW = \frac{1}{2\pi\,\tau} \tag{4}$$

$$R_{ON} \simeq \frac{1}{\mu_n\, C_{ox}\,(W/L)(V_{GS} - V_t)} \tag{5}$$

$$Q_{ch} = W\,L\,C_{OX}\,(V_{GS} - V_t) \tag{6}$$

Now, (7) represents R_{ON} after substituting (6) into (5), hence τ can be written in terms of the channel length and the input capacitance as in (8).

$$R_{ON} = \frac{L^2}{\mu_n\, Q_{ch}} \tag{7}$$

$$\tau = \frac{L^2\, C_{IN}}{\mu_n Q_{ch}} \tag{8}$$

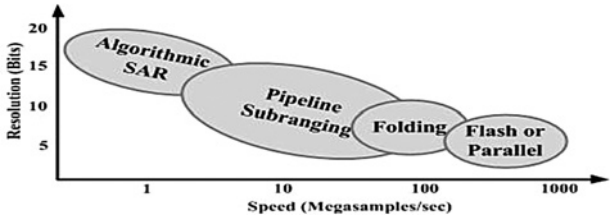

Fig. 3 *ADC topology selection*

Consequently, to improve the speed, the length of the switch (L) should be as small as possible. Moreover, the speed can be increased by reducing the value of the capacitor C_{IN}. However, there are some limitations on the minimum value of C_{IN}, which will be discussed while calculating the open-loop gain of the op-amp and the switch capacitor sampling noise. This will be detailed in Sections 4 and 6.

4 Op-amp design

After an ADC topology and resolution have been selected, the op-amp and the biasing techniques must be selected and designed.

4.1 Topologies

The first step in the op-amp design is to select a topology that is capable of satisfying the gain and the unity-gain frequency requirements. Four topologies are discussed and compared below.

(1) *Telescopic cascode op-amp:* Fig. 4*a* shows a schematic of the telescopic cascode. The gain this circuit can provide is shown in (9), while the unity-gain frequency, f_t, is provided by (10). r_o and g_m are the small signal output resistance and the transconductance of the field-effect transistor (FET) devices, respectively. One of the major drawbacks of this topology is the difficulty in maintaining saturation for all the devices when shorting its inputs and outputs. Since some switched-capacitor topologies require this at certain stages of their operation, using the telescopic cascode with switch-capacitor circuits is not recommended. [15]

$$A_{(Telescopic)} = -g_{m2}(g_{m6}r_{o6}r_{o8}//g_{m4}r_{o2}r_{o4}) \tag{9}$$

$$ft_{(Telescopic)} = \frac{g_{m1}}{2\pi\, c_L} \tag{10}$$

(2) *Folded cascode Op-amp:* Fig. 4*b* shows a schematic of the folded cascode op-amp topology. The gain and the unity-gain frequency provided by this op-amp are shown in (11) and (12), respectively. The folded cascode overcomes the drawback of the telescopic cascode shown earlier. The input and the output terminals can be shorted without any major limitation to the output voltage swing [15]. This makes the folded cascode a suitable topology for the switched-capacitor circuits. Another favourable characteristic is the ability to achieve stability without the use of any additional compensation circuitry. This not only reduces the circuit components, such as the capacitors and the resistors, but also considerably simplifies the design process. This is not true for some other topologies as will be seen in the two-stage

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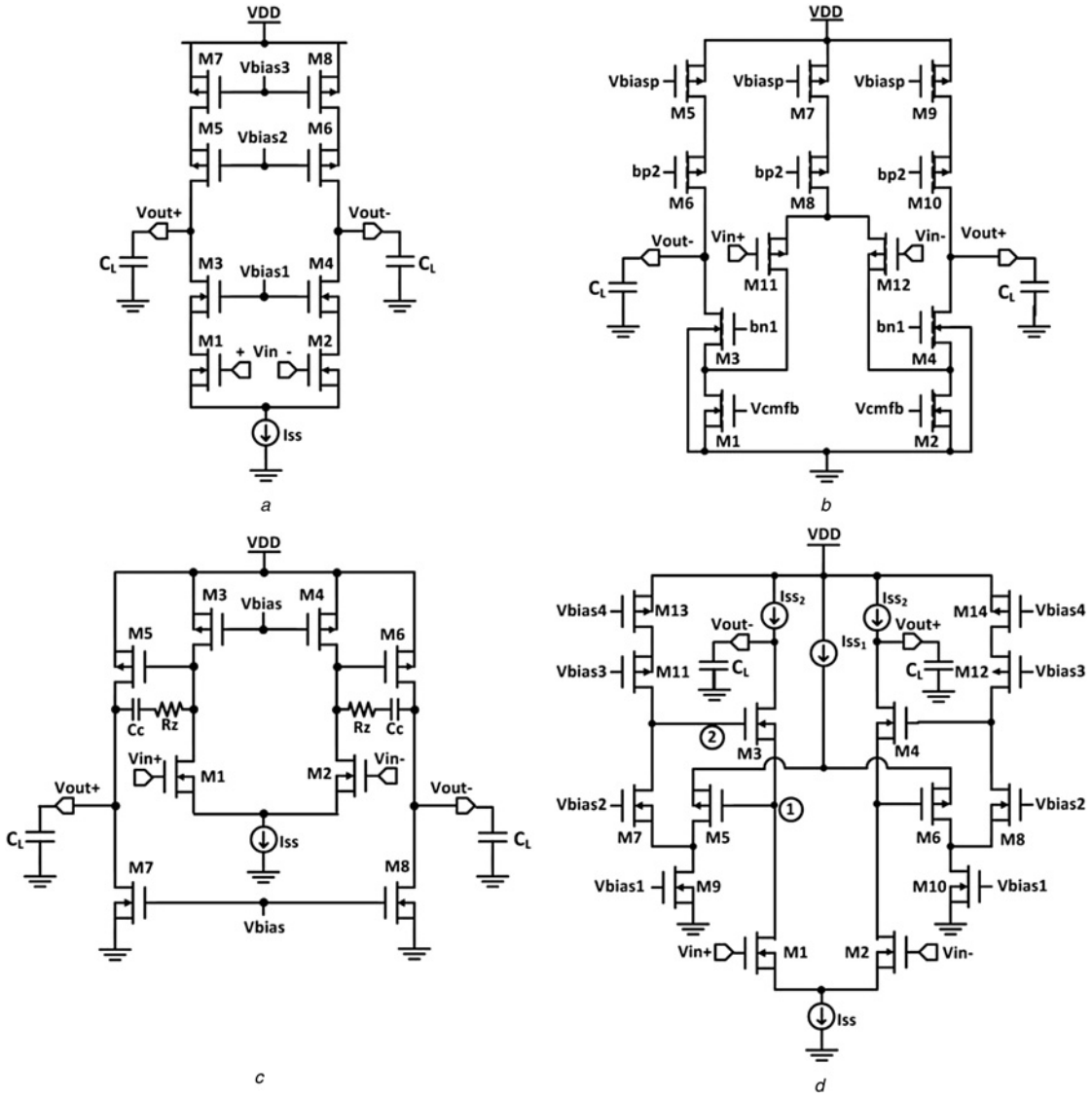

Fig. 4 *OP-amp topologies*

a Telescopic cascode
b Folded cascode
c Two-stage op-amp and
d Cascode gain-boosted by folded cascode

op-amp in the following subsection.

$$A_{(\text{Folded})} = g_{m12}[(g_{m10}r_{o9}r_{o10})//\,(g_{m4}r_{o2}r_{o4})] \quad (11)$$

$$ft_{(\text{Folded})} = \frac{g_{m11}}{2\pi\, c_L} \quad (12)$$

However, this topology requires higher power consumption since the input differential pairs (M11 and M12) require an additional bias current as compared with the telescopic cascode. Another major design challenge is to have all the transistors operating in the saturation region. This is due to the four devices in series in the output branches. The design becomes more cumbersome as the power supply voltages decrease and less headroom is available.

(3) *Two-stage Op-amp:* Fig. 4*c* shows a schematic of the two-stage op-amp topology. This op-amp is used when high gain and high output swing are required. The cascading of the stages provides a higher gain as seen in (13), where $A1$ is the gain of the first stage, $A2$ is the gain of the second stage and A is the total gain. The unity-gain frequency of this op-amp is given by (14). The second stage consists only of two transistors in series as opposed to four in the telescopic cascode. This allows these transistors to remain in saturation despite the large swing at the output. For this reason, the two-stage amplifier can be used in the switched-capacitor circuits with lower power supply voltages where the headroom issues are present [16]. This is especially true when large output voltage swings are required. For example in [17], a 1.26 V peak-to-peak output swing is achieved with a 1.5 V supply.

$$A_{(\text{Two-stage})} = A1^{*}A2 \;= [\,g_{m2}(r_{o2}//r_{o4})][g_{m6}(r_{o6}//r_{o8})] \quad (13)$$

$$ft_{(\text{Two-stage})} = \frac{g_{m1}}{2\pi\, c_c} \quad (14)$$

Table 1 Op-amp topologies comparison [15]

Topology	Gain	Output swing	Speed	Power dissipation	Noise
telescopic	medium	medium	highest	low	low
folded-cascode	medium	medium	high	medium	medium
two-stage	high	highest	low	low	low
gain-boosted	high	medium	medium	medium	medium

One of the major drawbacks of using the two-stage op-amp is the need for the compensation circuitry to achieve stability. Each stage produces one pole to the open-loop transfer function creating challenges to the stability of the amplifier [15]. Therefore a compensation capacitor C_c is connected as seen in Fig. 4*c* to perform a pole-splitting compensation scheme [12]. C_c creates a dominant low-frequency pole and the second pole is shifted beyond the unity-gain frequency (f_t) allowing the phase margin to remain within the stable boundaries. The addition of the compensation capacitor introduces a zero. However, the resistance R_z shifts this zero to the left-hand plane allowing it to be added to the phase margin.

The need for a compensation circuit results in limiting the speed of this amplifier. Since C_c creates a dominant pole, the speed of the amplifier strongly depends on the compensation scheme and the capacitor values [16]. Therefore the high gain and the high swing in this topology come at the expense of speed and difficulty in achieving stability.

(4) *Gain boosting Op-amp:* As shown in the previous amplifiers, such as the folded cascode, a large output impedance causes a large DC gain. Gain boosting is a technique that uses an additional auxiliary amplifier to increase the output impedance by the gain of the additional amplifier [18]. This results in increasing the overall gain without increasing the number of the cascaded devices [15]. Fig. 4*d* shows a differential cascode amplifier gain-boosted by an auxiliary folded cascode. The single-ended gain, $A_{(\text{single-ended})}$, provided by the auxiliary amplifier, from points 1 to 2 is equal to $(g_{m5}R_{\text{out1}})$, where R_{out1} is shown in (15). This results in the total gain shown in (16) and the unity-gain frequency shown in (17), where R_{cs} is the equivalent resistance of the current source I_{SS2} of Fig. 4*d*. This topology overcomes the low speed drawback of the two-stage op-amp while achieving high gain, but the output voltage swing will not be as high as the two stage. Therefore the two-stage op-amp remains favourable in the low headroom designs.

$$R_{\text{out1}} = [g_{m7}r_{\text{o7}}(r_{\text{o9}}//r_{\text{o5}})]//[g_{m11}r_{\text{o11}}r_{\text{o13}}] \tag{15}$$

$$A_{(\text{Gain-boosted})} = g_{m1}\left(g_{m3}r_{\text{o3}}r_{\text{o1}}\right)\left(g_{m5}R_{\text{out1}}\right) \tag{16}$$

$$ft_{(\text{Gain-boosted})} = \frac{A_{(\text{Gain-boosted})}}{2\pi\, C_L[(r_{\text{o1}}\, g_{m1}g_{m3}A_{(\text{single-ended})})//\, R_{\text{cs}}]} \tag{17}$$

(5) *Comparison:* When designing for the switched-capacitor circuits, the design requirements govern the choice of the op-amp topology. Table 1 below shows a qualitative comparison between the four op-amp topologies presented in this paper.

The contribution of the noise in these topologies will be fully discussed along with the noise equation of the op-amps in Section 6. For the design example given in this paper, the folded cascode shown in Fig. 5 is used. This is due to its ability to provide a high gain while easily maintaining stability without the use of any additional compensation circuitry. It is also necessary to select a current source to provide the bias currents and the voltages for both the op-amp and the CMFB. The wide-swing cascode current mirror shown in Fig. 5 is used in the example. It provides the bias voltages V_{biasp}, bp2 and bn1 to the op-amp. Therefore it determines the currents passing through its branches. It also provides bias voltage V_{biasn} to the CMFB circuit which will be discussed in Section 5.

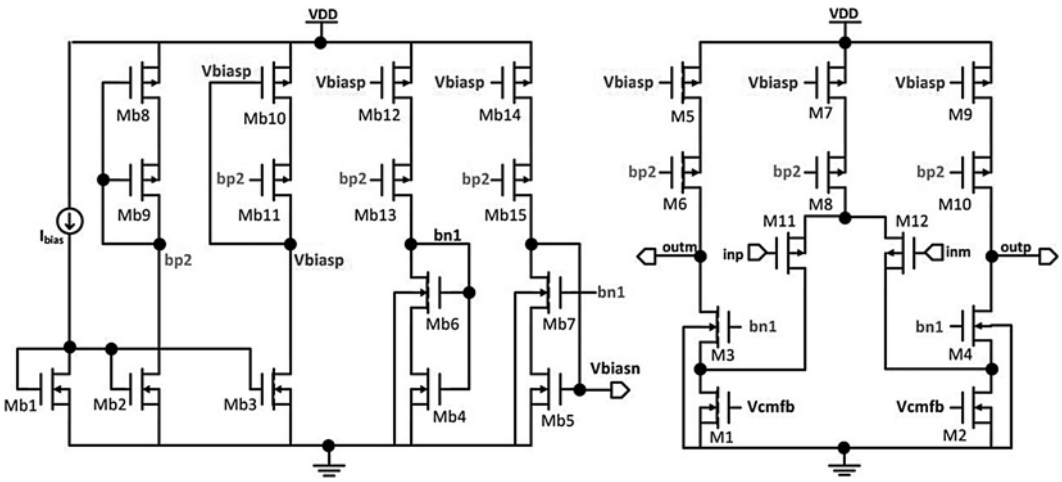

Fig. 5 *Folded cascode op-amp with biasing*

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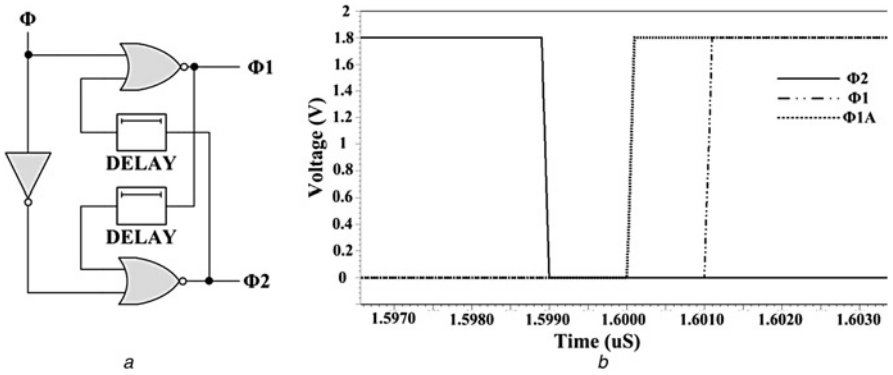

Fig. 6 *Clocks operation*

a Realising two non-overlapping clocks from a single source
b Close-up snapshot of the clocks

4.2 Clocks operation

As shown in Fig. 1*a*, there are three clocks that operate the S/H circuit: ϕ1, ϕ1A and ϕ2. During ϕ1's high time, the S/H circuit samples (tracks) the input. During ϕ2's high time, the circuit holds the output at the value it has sampled during ϕ1. The circuit operates in an entirely different way in these two stages. Therefore it is the designer's responsibility to make sure that ϕ1 and ϕ2 never overlap. Fig. 6*a* shows one way to realise two non-overlapping clocks from a single source to guarantee proper operation. ϕ1A is an advanced ϕ1 clock and is used to minimise the non-ideal charge sharing issues such as charge injection and clock feed-through. These errors occur because of the injection of the charge from the channel and the overlap capacitances into the circuit as the MOSFETs switch off. As seen in [5], operating certain clocks with slightly advanced time can minimise such errors. Fig. 6*b* is a close-up snapshot of the clocks as ϕ2 turns off and ϕ1A and ϕ1 turn on. At this stage, it is necessary to calculate ϕ1's high time according to (18). Suitable non-overlap and advanced times are selected.

$$t_{\Phi 1\text{-high}} = \frac{t_{\text{period}}}{2} - t_{\text{non-overlap}} - t_{\text{advanced time}} - t_{\text{rise and fall}} \tag{18}$$

4.3 Open-loop amplifier specifications

After determining the sampling time, the least significant bit (LSB), the gain error (Eg) and the feedback factor (F) must be calculated. The LSB is calculated according to (19), where N is the number of the bits and $V_{\text{pp-differential}}$ is the maximum differential input voltage. Following that, Eg must be defined as a fraction ($1/x$) of the LSB. The value selected for x depends on the speed and the accuracy requirements of the system. The next step is using (20) to calculate $\tau_{\max}$ as shown in (21). Then, the minimum unity-gain frequency ($ft_{\min}$) can be found by using (22). However, as mentioned previously in Section 3, the value of C_{IN} should be large enough to overcome the effect of the parasitic capacitance. It must be noted that the time (t) in (20) and (21) is the settling time of the sample stage only, and is considered to be 80% of $t_{\Phi 1\text{-high}}$ found in (18) (i.e. excluding 20% for the slew time). A_0 is the open-loop op-amp gain. Finally, by using the right side of (20), and substituting F from (23), the minimum op-amp open-loop gain A_{o} can be calculated. For the design example, where the required SNR is 36 dB and the sampling frequency is 5 MHz, a closed-loop gain of 2 is chosen, and x in (20) is selected to be equal to 2. $t_{\Phi 1\text{-high}} = 96.8$ nS, LSB = 15.625 mV and $F = 0.3125$, respectively. $A_{\text{o, min}}$ and $ft_{\min}$ were then calculated to be 46.2 dB and 19.94 MHz, respectively.

$$\text{LSB} = \frac{V_{\text{PP-differential}}}{2^N} \tag{19}$$

$$e^{-(0.8t_{\Phi 1-\text{high}}/\tau)} \leq \text{Eg} = \frac{1}{A_0 F} = \frac{1}{x}\text{LSB} \tag{20}$$

$$\tau_{\max} = \frac{-0.8\ t_{\Phi 1\text{-high}}}{\ln\left((1/x)\text{lsb}\right)} \tag{21}$$

$$ft_{\min} = \frac{1}{2\pi\tau_{\max}} \times \text{ Closed-loop gain} \tag{22}$$

$$F = \frac{C_f}{C_f + C_{\text{IN}} + C_{\text{parasitic}}} \tag{23}$$

4.4 Design and simulations

Now that the op-amp specifications are set, the design process must start at the DC. The FETs are sized to ensure that all the devices are operating in saturation, and obtain the required transconductances and DC currents. At first, devices M5–M10 in Fig. 5 are sized such that their ratios to the corresponding FETs in the current mirror can set the current passing through each branch. The rest of the FETs are sized afterwards. Following that, the AC simulations are performed, and the design is tweaked to obtain the required gain and bandwidth. It is important to verify that the open-loop system is stable by verifying that the phase margin is above 45° at the unity-gain frequency. To obtain a valid AC simulation, the CMFB must not be connected at this stage of the design process for the reasons explained in Section 8. To properly bias the op-amp without including the CMFB, the gates of M1 and M2 in Fig. 5 should be connected directly to the bias voltage V_{biasn}. This biases M1 and M2 with a voltage comparable with the output of the CMFB.

Fig. 7*a* shows the differential input connected directly to the op-amp as should be done for the open-loop simulations. Fig. 7*b* shows the AC simulations of the open-loop op-amp's output magnitude and phase. The gain

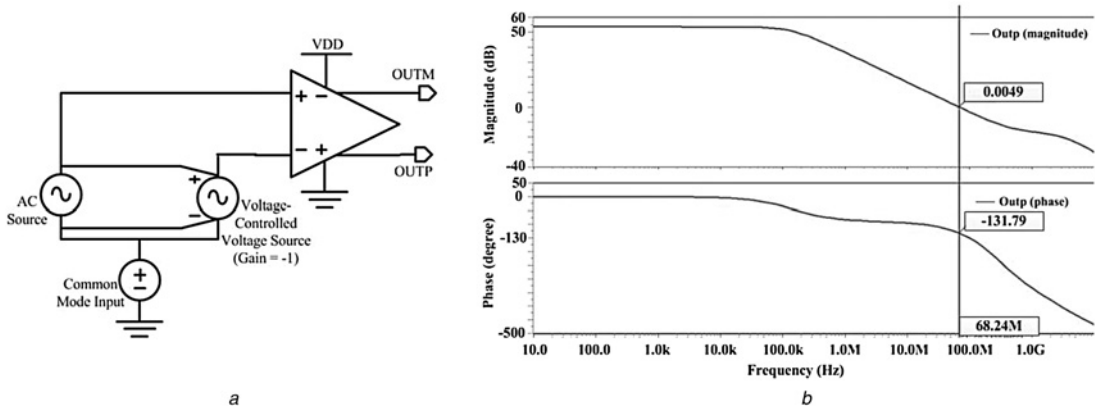

Fig. 7 *Open-loop design and simulation*

a Open-loop simulation schematic
b AC simulation of the open-loop op-amp output magnitude and phase

and the unity-gain frequency are 53 dB and 68.2 MHz, respectively. The phase margin is 48.21° indicating the stability of the open-loop op-amp. The closed-loop gain is presented in Section 6.

5 Common mode feedback design

The output common mode voltage of the op-amp tends to drift because of the process variations, the offsets and the sensitivity to the device's characteristics [19]. Therefore, it is necessary to add additional common mode feedback circuitry to control the common mode output voltage at a required value, which is usually halfway between the power supplies [5]. An example of a switched-capacitor CMFB circuit is shown in Fig. 8*a*. This circuit is normally used for the switched-capacitor applications rather than the continuous time applications because it consumes less power [20, 21].

The switched-capacitor C_s is switched between the fixed bias voltages V_{cmref} and V_{biasn} during $\phi 1$ and is in parallel with the non-switched capacitor C_c during $\phi 2$. This allows the C_s to determine the DC voltage across the C_c by altering the control voltage V_{cmfb} to keep the common mode output voltage constant [5]. The bias voltage V_{cmref} is a low impedance reference voltage that sets the value of the common mode output voltage. V_{biasn} is a fixed bias voltage supplied by the bias block. The switched capacitor along with the switches on its sides will operate as an equivalent resistance determined by (24), where f_s is the sampling frequency. As a result, the equivalent circuit shown in Fig. 8*b* will effectively act as an RC circuit. The common mode feedback may possibly control the dominant pole of the system. Therefore care must be taken when selecting the capacitor values.

$$R_{equivalent} = \frac{1}{f_s C_s} \tag{24}$$

According to (24), the 3 dB bandwidth of the common mode feedback can be written as in (25). It can be seen that this bandwidth is well controlled since f_s is fixed, and the capacitors C_s and C_c are exposed to the same process and temperature variations.

$$f_{3\,dB} = \frac{f_s\, C_s}{2\pi C_c} \tag{25}$$

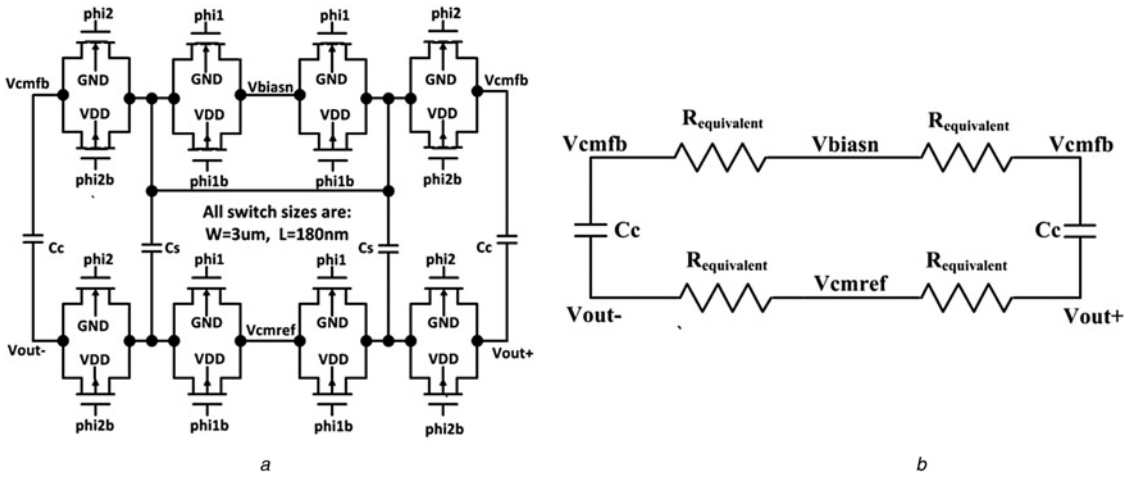

Fig. 8 *Common mode feedback circuit*

a Common mode feedback circuit
b Common mode feedback equivalent circuit

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6 Noise analysis of the switched-capacitor circuits

The random motion of the charge carriers is the source for the noise in the electronic circuits [22]. Hence, because of the random nature of the noise, its behaviour is predicted via statistical analysis. Noise is considered problematic in analogue circuit design, because it affects the other parameters such as speed, linearity and power dissipation [15].

Switched-capacitor circuits have four sources of noise: noise of the sampling phase, noise of the holding phase, the op-amps noise and the quantisation noise. The last source of the noise, quantisation, has been mentioned in Section 3.

6.1 Noise of the sampling phase

According to Fig. 1*b* of Section 2, during the sampling phase each capacitor and switch acts as a simple RC circuit where each switch is replaced by an equivalent resistance and noise voltage source. The thermal noise voltage in the RC circuits is given by (26) [23].

$$V_{\text{sampling noise-RMS}} = \sqrt{\frac{KT}{C_{\text{IN}}}} \tag{26}$$

where $V_{\text{sampling noise}}$ is the total noise voltage at the output, K is the Boltzmann constant and T is the absolute temperature in kelvin. It can be seen from (26) that the total noise power in the sampling phase is independent of the equivalent resistance of the switch [15].

6.2 Noise of the holding phase

Fig. 1*c* of Section 2 shows the circuit construction during the holding phase. Fig. 9 illustrates the noise contribution in the holding phase, where the switches $\phi 2$ are replaced by the equivalent resistance, R_{SW}, and the noise voltage source, $V_{\text{SW}\phi 2\text{-Noise}}$. From Fig. 9, the noise behaviour during the holding phase is no longer a simple RC circuit noise. It is a continuous time noise because of $V_{\text{SW}\phi 2\text{-Noise}}$. Equation (27) gives the total RMS voltage noise in the holding phase [23].

$$V_{\text{holding noise\_out-RMS}} = \sqrt{KT\left(\frac{C_{\text{IN}} + C_f}{C_f^2}\right) + V^2_{\text{SW}\phi 2\text{-Noise}}} \tag{27}$$

After the output is sampled, and the output voltage noise is referred back to the input of the op-amp, the equivalent input referred noise voltage is given by (28). It represents the mean square of the RMS value of the noise taking into account the sampling and the holding noises [23].

$$V_{\text{noise\_in-RMS}} = \left(\frac{C_f}{C_{\text{IN}} + C_f}\right)\sqrt{KT\left(\frac{C_{\text{IN}} + C_f}{C_f^2}\right) + V^2_{\text{SW}\phi 2\text{-Noise}}} \tag{28}$$

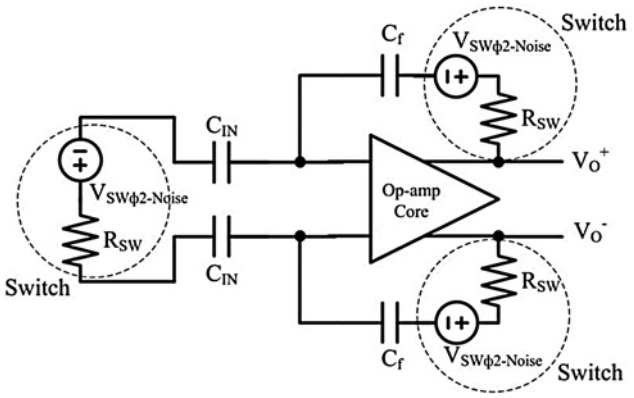


Fig. 9 *Noise contribution in the holding phase*

6.3 Op-amps noise

For a simple analysis of the noise amplification in the op-amps, it will be assumed that the only input source is the noise source as in Fig. 10. The transfer function of the circuit configuration in Fig. 10 is given by (29), where the gain of the op-amp, A, is considered finite. Hence, the mean square value of the output noise in the closed-loop op-amps is given by (30), where C_{O} depends on the topology of the op-amps. For illustration, in the two-stage op-amps, C_{O} is equal to the compensation capacitor C_{C}, while it is equal to the load capacitance of the output node for the folded and the telescopic cascode op-amps [24].

$$\frac{V_{\text{out}}}{V_{\text{noise}}} = \frac{A}{1 + A\left((C_f/C_{\text{IN}} + C_f)\right)} \tag{29}$$

$$\overline{V^2_{\text{out}}} = \left(\frac{4KT}{3C_{\text{O}}}\right)\left(\frac{C_{\text{IN}} + C_f}{C_f}\right) \tag{30}$$

For the design example in this paper, the sampling noise is 2.289×10^{-9} V, and the folded cascode op-amp noise is 1.1168×10^{-9} V according to (26) and (30), respectively. The quantisation noise is related to the feedback factor and the open-loop gain. Hence, it is calculated by using (20). For example, by substituting $x = 8$, the quantisation noise is 1.953×10^{-3} V.

In the properly designed systems, the quantisation noise – which is included in the SNR equation of Section 3 – should be the dominant noise as mentioned in the previous paragraph. Hence, the sampling noise should be reduced by increasing the value of C_{IN}. However, increasing the capacitor value will affect the bandwidth of the system. Hence, the designer has to be aware of the trade-off between the noise and the bandwidth. The noise of the holding phase affects systems with high resolution and high speed primarily. For example, in the 10 bits systems, the holding noise effects start at 100 MHz [23].

7 Final S/H circuit

The current mirror, the op-amp and the common mode feedback should now be inserted into the S/H configuration. Fig. 11*a* is the final S/H schematic used in the design example. The capacitors' values must be selected to satisfy (2). Regarding the closed-loop simulations, Fig. 11*b* shows

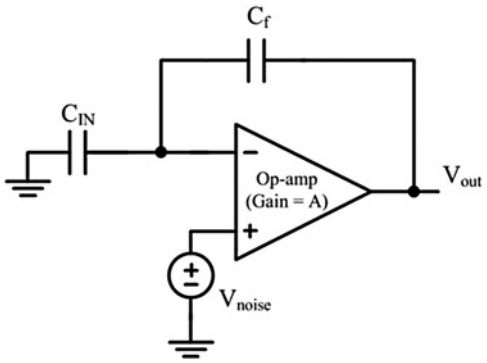


Fig. 10 *Op-amp configuration with noise source*

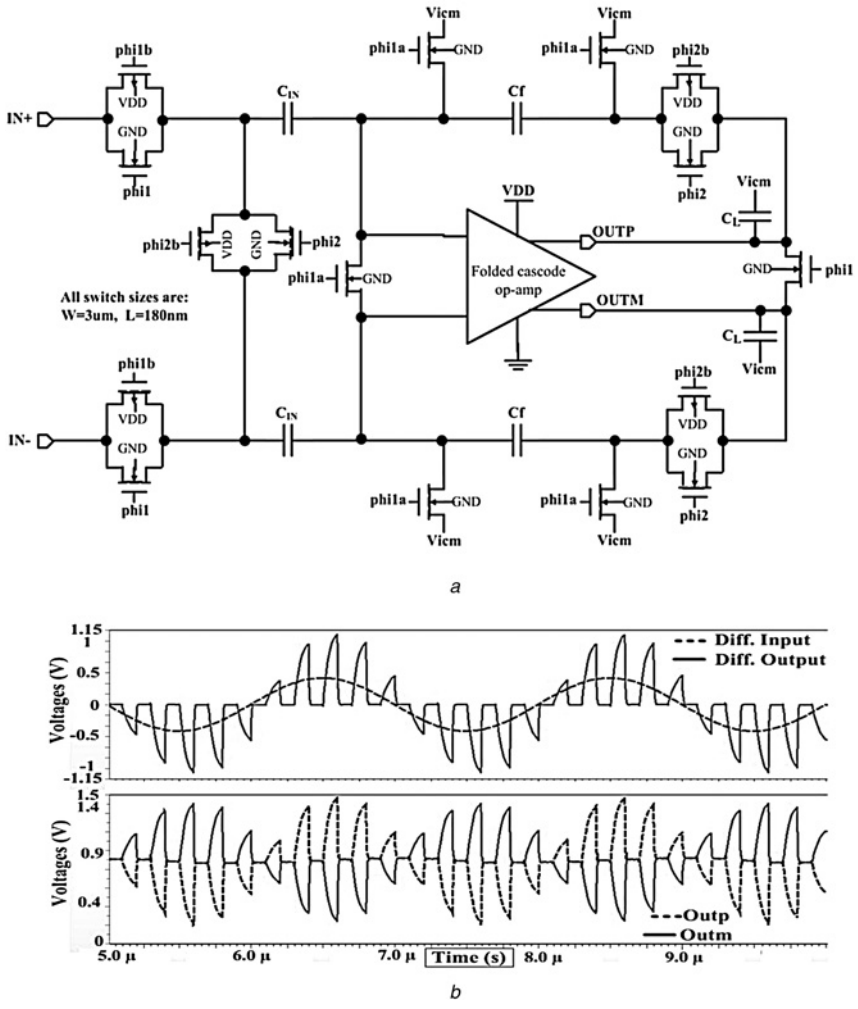
the transient simulations for the S/H differential and single-ended outputs. The circuit is operating at 5 MHz and provides a closed-loop gain of 2.

8 System stability and verification methods

Stability describes the ability of a system to withstand variation in the conditions under which the circuit is operating. New stability verification methods have been introduced in this paper based on the transient analysis and simulations since the typical AC simulations used in [12] do not account for the switching operation in the switched-capacitor circuit. Furthermore, the AC simulations will face a problem with the capacitors in the feedback loop, since these capacitors block the DC signal. Fig. 12*a* illustrates these two transient simulation methods on the S/H schematic circuit graphically. The first method is applying a step voltage to the power supply (V_{DD}), whereas the second method is applying a step current to the input of the op-amp. The use of a step is necessary to verify the stability at all the frequency components. To differentiate between the system response to the variation in the input signal and its response to the applied steps, the inputs are driven with the DC voltage sources.

As shown in Figs. 12*b* and *c*, which represent the simulations of the first and the second methods, respectively, the system is considered stable if the output responds smoothly without overshooting and ringing to the change in the operating conditions.

The step responses of the node Outp in Fig. 12*a* have been plotted to show the difference between the stable (Outp1: Figs. 12*b* and *c*) and the less stable (Outp2: Figs. 12*b* and *c*) systems. Also, in order to show the effect of the



a

b

Fig. 11 *Final sample and hold circuit and simulation*

a S/H schematic
b Differential input and output superimposed (top), single-ended outputs superimposed (bottom)

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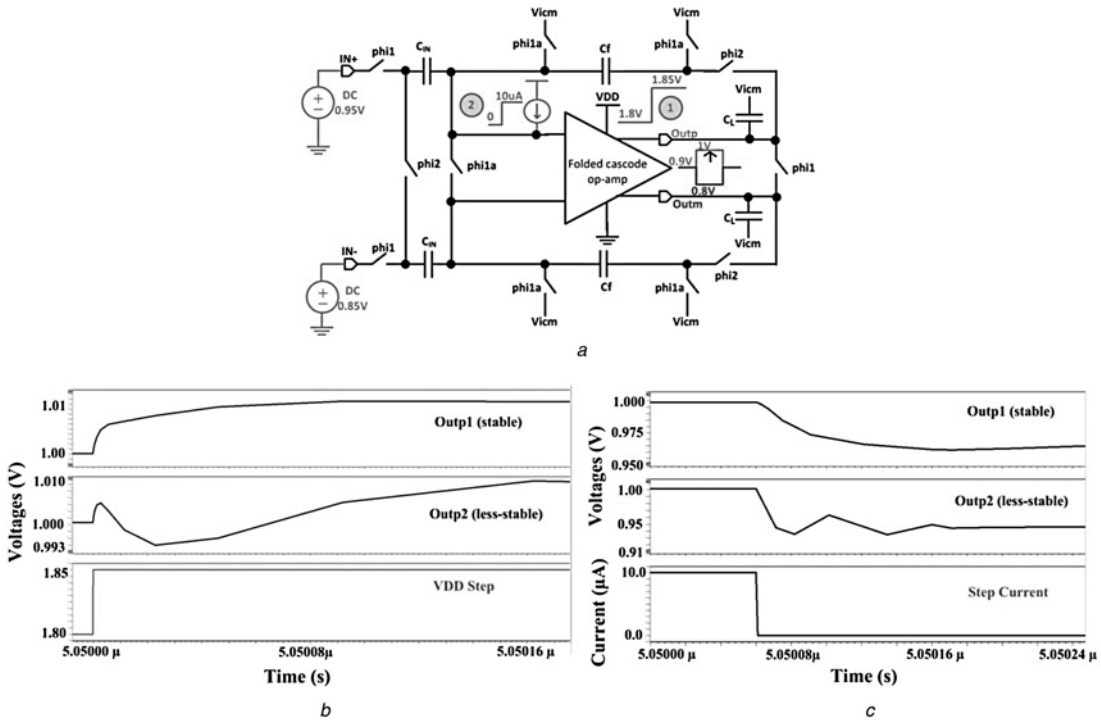

Fig. 12 *System stability and verification methods*

a Stability verification methods
b VDD step (bottom), stable (top) and less stable responses (middle)
c Step current (bottom), stable (top) and less stable responses (middle)

different step cases, a step-up voltage and a step-down current, as shown in the bottom waveforms of Figs. 12*b* and *c*, are simulated.

9 Conclusion

In this paper, the design process of a S/H circuit generally used for the ADCs was fully presented. The selection criteria of the ADC topologies were discussed along with the translation of the system requirements into the op-amp specifications. Based on this, different op-amp topologies are presented in order to select the appropriate topology that attains the system requirements. The S/H circuit including the common mode feedback design and the noise impact was detailed. Furthermore, two transient simulation methods for checking the stability of the closed-loop system have been implemented thus solving the difficulty of using the ordinary AC simulation methods. A design example including the simulations has been provided throughout the sections to illustrate the design procedure. This paper offers a guide for the design engineers and the graduate students on how to approach the non-linear switched-capacitor circuit design.

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