A new technique for designing high performance front-end Sample and Hold circuits

Y. Chouia, K. El-Sankary, A. Saleh, M. Sawan and F. Ghannouchi

PolySTIM Neurotechnology Laboratory
Ecole Polytechnique de Montréal, Department of Electrical Engineering,
P.O.Box 6079, Station Centre-ville, Montreal, QC, H3C3A7, Canada

***Abstract*– Based on the behavioral modelisation of each element in a sample and hold (S/H) circuit, and using the Verilog-A language, such approach effectively allow us to get the best performances that the circuit can give. Using switched capacitor differential topology, double bootstrapped switches and several native transistors, we optimized with Verilog-A models the amplifier and the switches to end up with the optimized high performance circuit. Post layout simulation of the optimized circuit using CMOS 0.18µm technology with a V_{DD} of 1.8V allowed to reach an SFDR of 88.6dB for 20MHz input signal. The circuit was integrated to other building blocks to construct a pipelined ADC which is now under fabrication.**

***Index Terms*– Sample and Hold, ADC, bootstrapped switch, Verilog-A modelling.**

I. INTRODUCTION

The wave of digitalization which nowadays strikes almost all the fields of electronics starting from most complex telecommunication systems to simple appliances, at the same time, the borders between the treatment of analog and digital signals are moving more and more towards the antenna in order to have a software based radio, which require high rate analog to digital converters (ADC), operating at high performances and with a very low consumption in power. Those ADCs have an important building block called the front-end sample-and-hold (S/H) which reduces their most dynamic errors. We present in this paper a new technique for designing a high performance front-end S/H, the designed circuit will be dedicated to a 10 bit 50MS/s pipelined ADC using 0.18µm CMOS process. The pipelined ADC is a first step in the realization of a time interleaved one that will operate at 200MS/s and intended for wireless communication devices. This ADC has another important requirement which is low power consumption that has been taken into consideration in this design. Many S/H circuits have been designed either by using complex compensations of errors as in [1], or simple architecture to minimize power consumption, as in [2], we introduced Verilog-A modeling in order to optimize the circuit so it can give its best performances, we used bootstrapping switches for achieving high performance operation and by using simple architecture for minimum power consumption. This approach allowed us to reach a resolution of 14 bits with very low power consumption.

This paper is organized as follows; S/H circuit architecture is described in section 2. In section 3, we will discuss design procedure and methodology, with the different blocks specifications. Simulation results are shown in section 4. Conclusions are given at last.

II. CIRCUIT ARCHITECTURE

The architecture of the proposed S/H is shown in Fig.1. Its closed loop configuration makes it suitable for high resolution S/H circuits. A differential topology was used to eliminate the common mode offset voltage, and the bottom-plate technique to cancel charge injection dependence on the input signal.

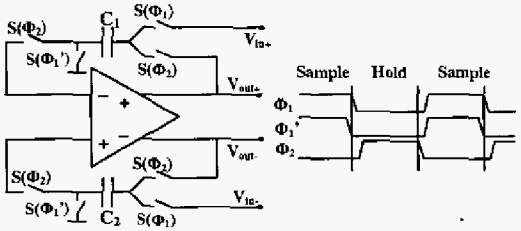

Figure 1. Architecture of the differential S/H.

As we notice in the clock diagram of Fig. 1, there are two phases, the sample phase and the hold one, in the sample phase, input voltages are sampled into C_1 and C_2 through $S(\Phi_1)$ and $S(\Phi_1)$ switches, notice that $S(\Phi_1')$ closes slightly before $S(\Phi_1)$, so the charge in the sampling capacitor cannot change because there is no other DC path, this is called bottom-plate technique which makes the charge injection signal independent. When switching to hold phase the sampling capacitor is connected in feedback loop around the amplifier.

The next important components are the switches which are the main source of distortion in S/H circuits that can be minimized by making them more linear. A commonly used basic switch, the transmission gate, can itself be considered as a linearized circuit. In fact, as the signal voltage rises the increase in the on-resistance (R_{ON}) of the NMOS transistor is compensated by the decrease in PMOS R_{ON} and vice versa. However in low voltage applications this technique gives more distortion with higher input range. This gives rise to gate boosting or charge pumping technique, where we apply $2V_{DD}$ on the gate instead of V_{DD}, but this technique reduces the reliability of the switch. Moreover, the bootstrapping technique is used to overcome the problem of reliability and to have more linearized switch. This technique will be explained in the next section. For the switches $S(\Phi_2)$ that are connected to the output of the amplifier we used

0-7803-8656-6/04/$20.00 ©2004 IEEE

native transistors that have small threshold voltages and gave much less hold step than if we used a simple NMOS switch.

III. CIRCUIT DESIGN

A Verilog-A model of the switches and the amplifier was used to optimize the circuit. Shown on Fig.2 is the switch's model used which is simply a resistor that has a low value R_{LOW} if its controlling signal exceeded a given threshold voltage V_T and a very high value R_{HIGH} if the same signal was lower than V_T.

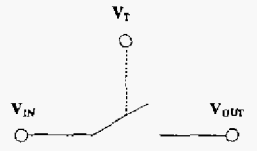

Figure 2. Switch's model.

The model that has been used for the amplifier is shown on Fig.3, many parameters was included in the model like the unity gain frequency, DC gain and slew rate.

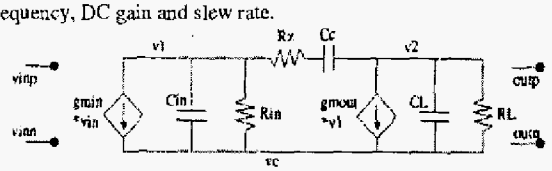

Figure 3. Amplifier's model.

The realized SH circuit using Verilog-A models gave a perfect result i.e. the output signal followed exactly the sampled signal during the sampling phase, and held the exact value during the hold mode without any loss. There were no distortion since no clock feedthrough nor charge injection can be induced with ideal switches. Here comes the advantage of Verilog-A in the optimization process. Each switch model replaced by a CMOS transistor brings some imperfections to the circuit. The dimensions of CMOS transistors are optimized one by one till a complete CMOS circuit is reached instead of Verilog-A models. The objective of this optimization was to get a CMOS circuit with the minimum distortion possible. Another advantage of Verilog-A models is that they can be analyzed using Analog Design as any Cadence CMOS component.

A telescopic OTA was used because of its high operation speed, low power consumption and low noise level. Fig. 4 shows the differential amplifier that has been implemented for the proposed S/H circuit.

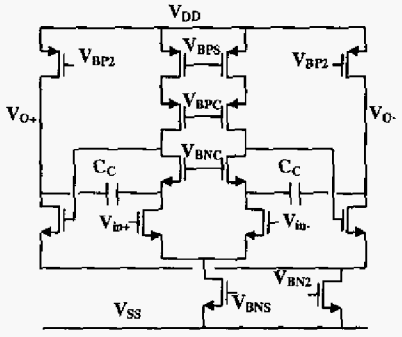

Figure 4. Fully-differential 2-stage OTA.

Cascode compensation has been used with its pole-splitting effect which moves one pole to a lower frequency and another to a higher frequency [3]. As seen in Fig. 5 we obtained a good phase margin of 71° at 931MHz bandwidth with a DC gain of 106.1dB, which maintains the output voltage to be more stable.

Switches in S/H circuit are of essential importance for avoiding distortion and especially the charge injection dependence on the input signal. In fact, accuracy and signal bandwidth are limited by distortion, which are originated from the fact that switch R_{ON} varies as a function of drain and source voltages. In sampling mode, a simple S/H circuit forms a low pass filter; consequently, the maximum frequency that the circuit can track is limited and the 3dB frequency of the circuit is

$$f_{3dB} = \frac{1}{2\pi R_{ON}(C_S + C_{P1} + C_{P2})} \tag{1}$$

Where C_S, C_{P1}, C_{P2} are the sampling, drain and source junction capacitances respectively.

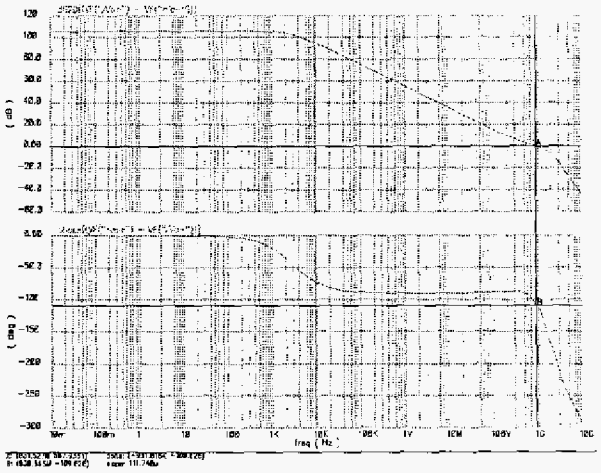

Figure 5. Bode diagrams of the amplifier: upside is the magnitude variation and bottom side is the phase.

If absolute accuracy is required then the minimum 3dB frequency is given by

$$f_{3dB} > 2^{(N-1)/2} f \tag{2}$$

Where f is the frequency of the input signal and N the resolution in bits. Using equations (1) and (2) the maximum switch R_{ON} can be calculated.

Unlike attenuation, harmonic distortion is intolerable in ADC application. When the signal amplitudes are large, accuracy and signal bandwidth are limited by distortion, which originates from the fact that switch R_{ON} and stray capacitances are not constant but vary as functions of drain and source voltages. For a short channel device the R_{ON} is given in equation (3)

$$R_{ON} = \frac{1 + \frac{V_D - V_S}{E_C L}}{C_{OX}\mu_{eff}\frac{W}{L}\left[V_G - \frac{V_S}{2} - \frac{V_D}{2} - V_{TO} - \gamma\left(\sqrt{V_S - V_B - 2\Phi_F} - \sqrt{2\Phi_F}\right)\right]} \tag{3}$$

Where V_G, V_S, V_D, and V_B are the voltages on the transistor's gate, source, drain, and bulk terminals. From equation (3), the dominant signal-dependent term can be identified as the gate-channel voltage $V_G-(V_S+V_D)/2$ in the denominator.

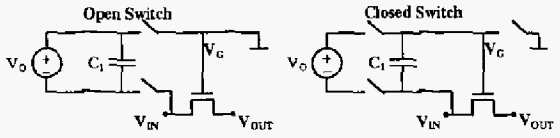

Figure 6. Bootstrapped switch (a) open (b) closed.

Few solutions were proposed to achieve more switch linearization, like the transmission-gates that need optimum sizing; however process parameters make this solution rather moderate. Also gate voltage boosting technique has a reliability drawback. We end up with the bootstrapped switches which are shown in Fig. 6, and we used this architecture on both sides, gate to source and gate to drain terminals to ensure more linearization which is called "double-bootstrapped switch" [4] that is shown in Fig.7.

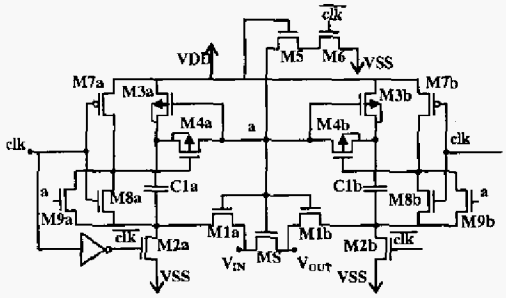

Figure 7. Double-Bootstrapped switch.

During OFF mode the main switch's (MS) gate is connected to V_{SS} through M_5 and M_6, while the capacitors C_{1a} and C_{1b} are being charged through $M_{2(a,b)}$ and $M_{3(a,b)}$, then for the ON mode, the V_{DD} charged capacitors will be connected simultaneously between the gate/drain and gate/source of the main switch MS through $M_{1(a,b)}$ and $M_{4(a,b)}$. This technique discussed thus far was used only for the most critical switch which is the sampling one at the input level, we used also in the feedback switch a native transistor that is characterized by low threshold voltage to allow a better linearization without using more space and complex circuit as with the double-bootstrapped switch. We used VerilogA models for the amplifier and with the same parameters as real ones to see easily the effect of each switch separately and optimize the S/H circuit to have the best performance we can get.

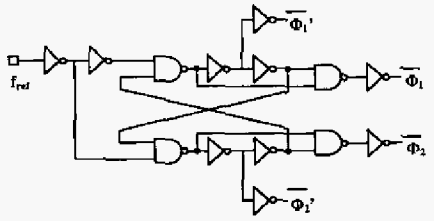

Figure 8. Non-overlapping clock generator.

We used the diagram shown in Fig. 8 for a non overlapping clock generation, which is essential in the S/H design first for realizing the bottom-plate technique, second for having two independent phases, sampling and holding, since we use the same capacitor for both operations.

IV. SIMULATIONS RESULTS

Fig. 9 is the FFT of 2^{15} samples with a rate of 50MS/s of the output signal from the S/H circuit, for an input frequency of 20 MHz and 100 KHz respectively with a differential peak-to-peak voltage of 1.2V.

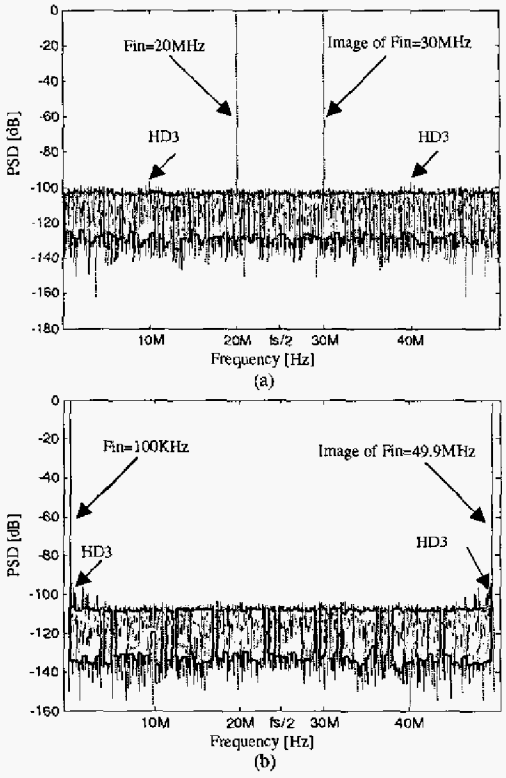

Figure 9. FFT of the output of the S/H with an input frequency (a) 20MHz, (b) 100KHz.

Table 1 shows a summary of the front-end S/H performances. The main purpose during the design of this circuit was to have a maximum possible SFDR (Spurious Free Dynamic Range) and SNDR (Signal to Noise and Distortion Ratio), with minimum power which was 7mw for all configurations.

Table 1. S/H Evaluation Results for an equal power consumption of 7mW

Parameter	Simple transistor 20MHz	Transmission gate 20MHz	Single booster 20MHz	Double booster 20MHz	Double booster 100KHz
SFDR[dB]	44.9	61.6	82.1	88.6	90.1
SNDR[dB]	40.2	57.4	78	84.1	86.7
SNR[dB]	49.3	65.2	85.2	91.2	93.4
ENOB[bits]	6.4	9.2	12.6	13.7	14.1

Note that the effective number of bits (ENOB) was above 13bits and this will give a good margin for the ADC and help in achieving good results with the pipelined ADC and in future works with the time interleaved ADC, also this circuit doesn't consume much power and this will be useful especially in wireless communication applications where low power is a main concern. Concerning the Native CMOS transistors used in the feedback path of the S/H circuit, Fig. 10 shows clearly the high linearization effect of this kind of switches, in addition to the hold step of each circuit, where using simple transistor it was around 35mV when holding a sample of 588mV while it was reduced to only 440µV using Native CMOS switch by holding the same voltage.

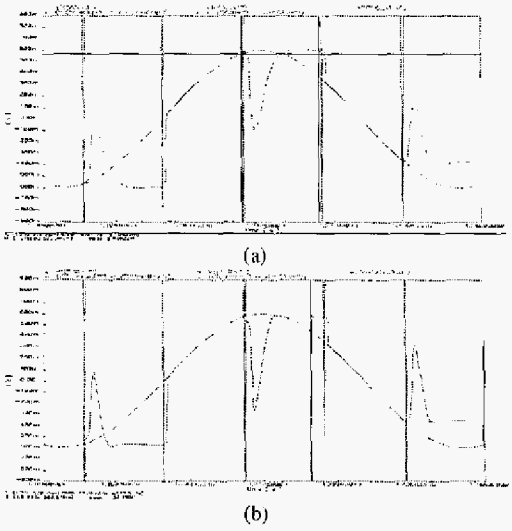

Figure 10. The output of the S/H using (a) Simple, (b) Native CMOS transistor.

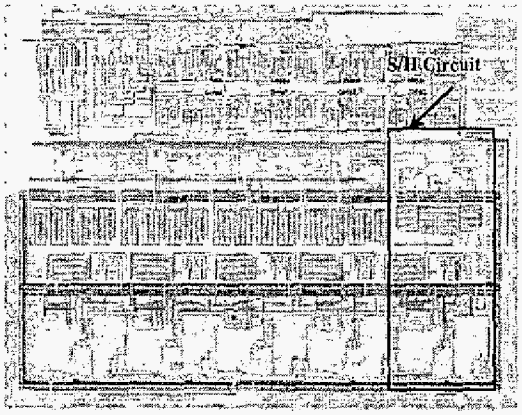

Figure 11. The Chip of Pipelined ADC with the front-end S/H.

Figure 11 illustrates the chip of the pipelined ADC (50Ms/s, 10 bits) with the front end sample and hold circuit that has been implemented and sent for fabrication. Post-layout simulations show an SFDR of 80dB (12 bits) using double boosting switches instead of 88.6dB that was in the schematic circuit as shown on Fig.12.

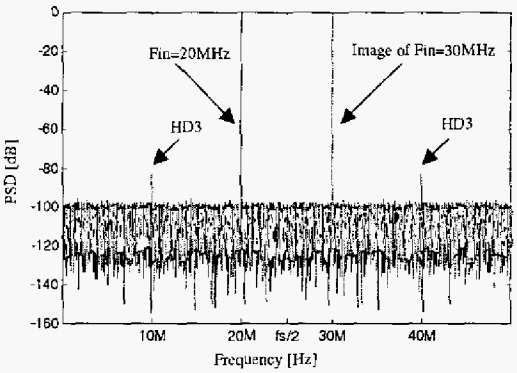

Figure 12. Post-Layout result of the S/H Circuit.

V. CONCLUSIONS

Verilog-A models of switches and amplifiers with programmable specifications were used at the beginning to optimize the front-end S/H circuit, and then those models were replaced by corresponding circuits in order to get the best circuit performances and maximize its SFDR and SNDR with low power consumption. The S/H has been designed and implemented using 0.18µm CMOS technology.The simulation of the proposed S/H indicated satisfactory results. Further works will be to test the performance of the chip of the pipelined ADC (50MS/s, 10 bits) including the proposed S/H.

ACKNOWLEDGMENTS

The authors would like to acknowledge the financial support from NSERC and design facilities from CMC.

REFERENCES

[1] Y. Huang; G. C. Temes; P. F. Ferguson, "Offset and Gain Compensated Track and Hold stages". IEEE –Int . Conf. on Electronics, Circuits and Systems, Vol2, pp. 13–16, 1998.

[2] E. Sall, "A 1.8 V 10-bit 80 MS/s low power track-and-hold Circuit in a 0.18µm CMOS process", Proceedings of the 2003 IEEE International Symposium on Circuits and Systems, Vol.1, 25-28 May 2003, P. 1-53 –1-56.

[3] A. Feldman, "High-Speed, Low-Power Sigma-Delta Modulators for RF Baseband Applications". Ph.D. Dissertation, University of California at Berkeley (ERL Memo # UCB/ERL M97/62), 1997.

[4] M. Waltari; L. Sumanen; T. Korhonen;K. Halonen, "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend". Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International,Vol.: 2, Feb 3-7, 2002 Pages: 250 – 493.