A 1-V 100-MS/s 8-bit CMOS Switched-Opamp Pipelined ADC Using Loading-Free Architecture

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***Abstract*—A 1-V, 8-bit pipelined ADC is realized using multi-phase switched-opamp (SO) technique. A novel loading-free architecture is proposed to reduce the capacitive loading and to improve the speed in low-voltage SO circuits. Employing the proposed loading-free pipelined ADC architecture together with double-sampling technique and a fast-wake-up dual-input–dual-output switchable opamp, the ADC achieves 100-MS/s conversion rate, which to our knowledge is the fastest ADC ever reported at 1-V supply using SO technique, with performance comparable to that of many high-voltage switched-capacitor (SC) ADCs. Implemented in a 0.18-μm CMOS process, the ADC obtains a peak SNR of 45.2 dB, SNDR of 41.5 dB, and SFDR of 52.6 dB. Measured DNL and INL are 0.5 LSB and 1.1 LSB, respectively. The chip dissipates only 30 mW from a 1-V supply.**

***Index Terms*—ADC, double-sampling, high speed, low voltage, pipelined, switched capacitor, switched opamp.**

I. Introduction

HIGH-SPEED, medium-resolution Nyquist-rate analog-to-digital converters (ADCs) find wide application in many different areas, such as high-speed wireline and wireless communications [1]–[3]. Relevant specifications usually require conversion rates higher than 80 MSample/s and resolution in the range of 7–9 bits [1]. For applications requiring the integration of multiple on-chip ADCs in the analog front-end with digital signal processors, low-power ADCs are highly preferred. In portable systems, low power consumption is even more important for extending the battery life. Among many ADC architectures, pipelined ADCs have proven to be very efficient for meeting the above requirements of high speed, medium resolution, and low power consumption [4]–[9]. The reason for their efficiency is mainly the concurrent operation of the pipelined stages. Each stage processes a new sample as soon as its residue is sampled by the following stage, which leads to a high throughput of one sample per clock cycle. By resolving a certain number of bits per stage, the operation speed and resolution are decoupled from each other for optimum power allocation [10], [11]. Moreover, the use of redundant-signed-digit (RSD) correction allows a large offset error in the comparator [4]. Hence, fairly simple dynamic latch-type comparators can be employed to further reduce power consumption.

Meanwhile, technology scaling commands the reduction of supply voltage for device reliability [12]. With the migration towards system-on-a-chip (SoC), it is becoming more popular for ADCs to be integrated with the digital backend processors. Since most pipelined ADCs are constructed by switched-capacitor (SC) circuits, they are known to exhibit the problem of insufficient switch overdrive under low supply voltage. This scenario deteriorates to a floating switch (a switch that passes varying voltage rather than constant voltage) with zero conductance when the supply voltage is lower than the sum of pMOS and nMOS threshold voltages. Several approaches have been proposed to address this issue. First, the use of low-threshold transistors as switches [13] involves special and expensive technology. Incomplete switching off due to leakage current is also an issue. Second, the clock voltage multiplier [4] may not be compatible with the maximum gate-source voltage rating in deep-submicron CMOS process. Third, the bootstrapped clock [12] linearizes the floating switch but it adds substantial capacitance to the opamp driving it. There may also be potential lifetime issues especially when a bootstrap circuit is used extensively with every floating switch in an ADC. Fourth, switched-opamp (SO) [14] is an analog circuit technique fully compatible with deep-submicron CMOS process. It has been considered a relatively speed-limited technique [14]–[17] except in a recent work [18].

This paper describes a switched-opamp pipelined ADC [19] which addresses the issue of limited speed in conventional SO pipelined ADC. Combining the proposed loading-free architecture with double-sampling technique together with a fast-wake-up dual-input–dual-output switchable opamp, the present work achieves a 100 MS/s under 1-V supply voltage. By either joining or separating the inputs, it can be configured as a single high-speed double-sampling ADC or a quadrature ADC. The former configuration is good for attaining high oversampling ratio for general purpose signal processing applications, while the latter can digitize signals from I/Q-channels for wireless receiver as reported in [3] at 40 MS/s per channel.

This paper is organized as follows. Section II reviews the pipelined ADC architecture and the limitation of conventional SO multiplying digital-to-analog converter (MDAC). Section III reviews the limitations of the switched-opamp technique with long wake-up time and opamp sharing and discusses their solutions. The overall ADC architecture consideration is discussed in Section IV with the proposed loading-free architecture. Proposed low-voltage building blocks are presented in Section V

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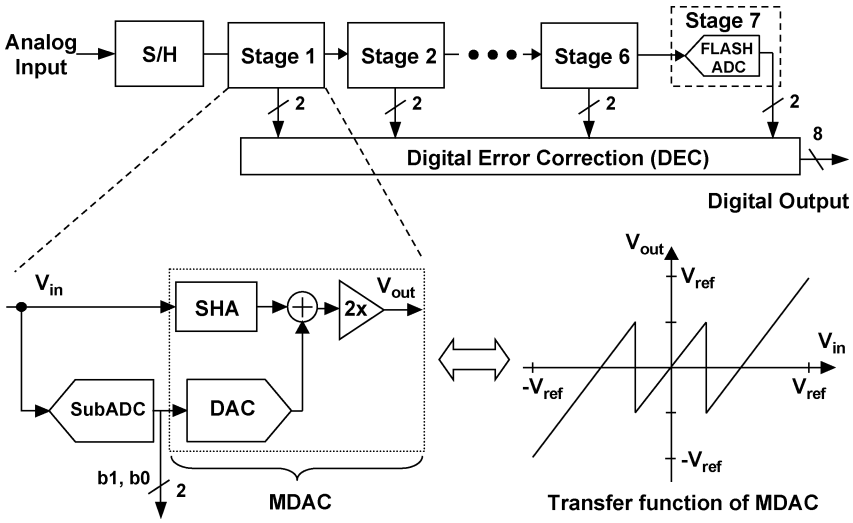

Fig. 1. Block diagram of 1.5-bit/stage pipelined ADC.

with emphasis on a fast-wake-up dual-input–dual-output switchable opamp. Section VI presents the measurement results and compares with state-of-the-art converters.

II. Review of Switched-Opamp Pipelined ADC

Pipelined architecture with 1.5-bit/stage structure is used in the proposed SO ADC as shown in Fig. 1. A dedicated sample-and-hold (S/H) is used at the front-end accepting the analog input signal. It is followed by six pipeline stages and the last stage is a 2-bit flash ADC. Each pipeline stage resolves 2 bits with a sub-ADC, and forms residue $V_{\rm out}$ for the next stage by doubling the difference between input $V_{\rm in}$ and the reconstructed quantization result. With 0.5-bit redundancy, offset error of the sub-ADC as large as $\pm V_{\rm ref}/4$ can be corrected by digital error correction (DEC). Thus, accuracy is mainly determined by the sample-and-hold amplifier (SHA), DAC, subtractor, and $2\times$ gain block, which are usually implemented in an SC circuit, called MDAC.

A common implementation of SC MDAC is shown in Fig. 2(a). C_s and C_f sample the input at ϕ_1 and then at ϕ_2 flip to appropriate reference voltage and output respectively to perform DAC and subtraction function. The stage gain of two is set by equating C_s and C_f. This is a highly efficient SC structure since both capacitors have explicit functions in both clock phases (sampling at ϕ_1, and reference subtracting or feedback at ϕ_2). Hence, a minimal number of capacitors with the simplest structure are achieved. It also gives a relatively large feedback factor β of 1/2, which favors MDAC speed and noise. Closed-loop bandwidth ω_u and sampling noise at MDAC output $\overline{v_o^2}$ are approximately given by [20]

$$\omega_u = \beta \frac{gm}{C_L} \tag{1}$$

$$\overline{v_o^2} = \frac{kT}{\beta C_f} \tag{2}$$

where gm is the transconductance of opamp's input differential pair, C_L is the loading of the opamp (assuming a single-stage opamp), and kT is the thermal energy. However, this SC MDAC commands the use of many floating switches as shown in the figure, which may lead to insufficient switch overdrive at low voltage.

Fig. 2(b) shows the previously reported SO MDAC [17]. It is noted that floating switches are removed and replaced by a switched-opamp. Its output shunts to ground in half clock cycle ϕ_1 for next stage's amplification (i.e., active at ϕ_2 only). Without floating switches, C_s and C_f are forced to permanently connect to the previous stage's output and around the opamp, respectively. They are used for sampling or feedback only in half clock cycle, hence they are sized in the ratio of 2:1 for setting a $2\times$ gain. Additional capacitors, C_{ls}, are required for reference subtraction and correct common mode (CM) setting. They are half the size of C_f. With the above setting, feedback factor of SO MDAC is only 1/4, and additional capacitors (C_{ls}) are added to the opamp's loading. The sizing of capacitors depends on many factors like stage scaling, matching and noise requirements. The matching requirement does not differ between the cases of SC and SO circuits. Stage scaling is the optimization of all stages and will be discussed in Section IV. Here, for fair comparison of SC and SO MDACs (i.e., single stage only), loading from the next stage in both cases is taken to be the same and only the noise given by (2) is considered. It can be seen that C_f in the SO MDAC needs to be twice as large as C_f in the SC MDAC for equal noise contribution. Worse yet, the allowable signal swing at the opamp output of the low-voltage SO circuit is considerably smaller than that of the high-voltage SC circuit. This may further require the use of larger capacitors to maintain the same dynamic range by reducing kT/C noise. Thus, the SO MDAC is inherently slower than its SC counterpart due to smaller feedback factor and larger capacitive load.

III. Wake-Up and Sharing of Switched Opamp

The previous section shows that the switched-opamp turns on and off alternatively between half clock cycles. Early SO works [14]–[17] generally suffer from slow transient for the switched-opamp to wake up from its off-state. Another limitation is the lack of ability of double-sampling since the opamp is off during half clock cycle. A recent work [18] proposed

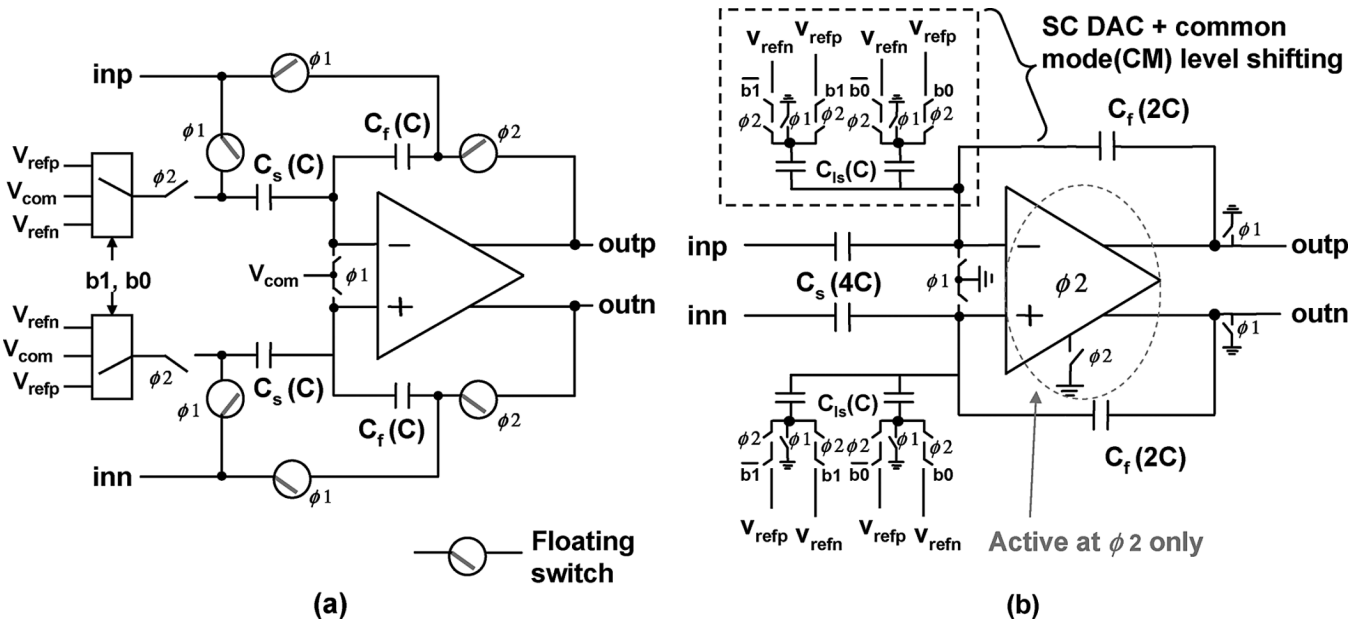

Fig. 2. Implementation of 1.5-bit/stage MDAC in (a) switched-capacitor (SC) and (b) switched-opamp (SO).

an advanced multiphase SO technique by adding a time-multiplexed output stage to the switched-opamp. As such, the opamp is available in both clock phases and double-sampling becomes possible for SO circuits. Hence, speed is essentially doubled without significant increase in power consumption.

Multiphase SO technique also allows the design of a fast-wake-up switched-opamp by time-sharing the current bias. This will be further explained in Section V. Fig. 3 shows the proposed SO MDAC using the multiphase SO technique. Besides the output pairs, two input pairs of opamps are also time-multiplexed between two paths (also termed I- and Q-channels in the context of quadrature transceivers). The SC network for MDAC function is duplicated for another channel, i.e., I-channel in the figure, while the switched-opamp is shared between two channels to achieve the maximum efficiency in terms of area, power, and speed.

In a previous work [21], two potential issues of opamp-sharing may arise. The first is the series input switch, which together with the opamp's input capacitance, may affect the settling performance. The second is the memory effect (due to the finite opamp gain) at the opamp input as there is no time to reset the opamp. These problems also exist when the opamp is shared across channels [25] (i.e., double-sampling) rather than between stages [21]. In the proposed SO MDAC, a series input switch is not required as a dedicated input pair is used for each channel. Moreover, each input pair and output stage are reset every half clock cycle. Therefore, the proposed multiphase SO MDAC helps to minimize the issue of opamp sharing. This results in better isolation of the coupling between two channels.

Nonidealities like offset, gain error, and timing skew exist in double-sampling ADCs [22]. They induce spurious tones and unwanted sidebands in frequency spectrum. In this work, except for careful layout and the described time-shared opamp, no other special circuit-level calibration is used to correct these nonidealities. For targeted application requiring signal bandwidth less than a quarter of sampling frequency [3], this will not cause any problem.

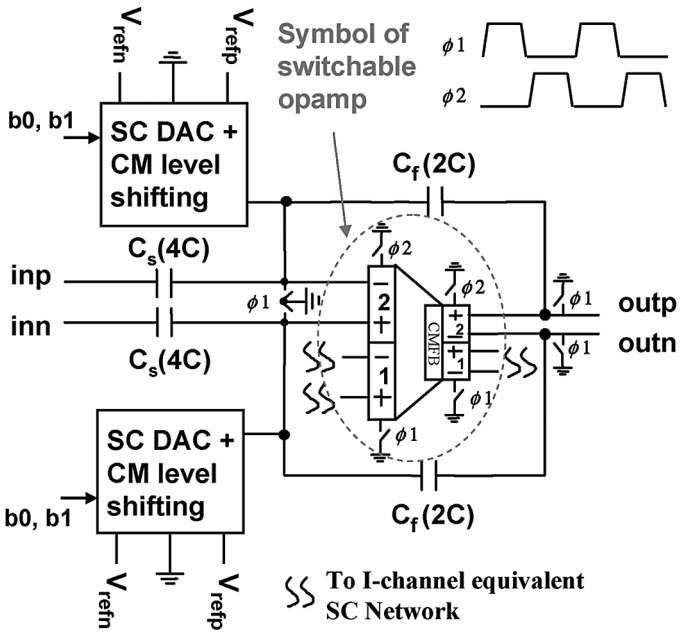

Fig. 3. 1.5-bit/stage SO MDAC using multiphase SO technique.

IV. Architectural Considerations

A. Stage Scaling

With interstage gain aggregating along the pipeline, the later stages contribute less noise than the front stages. Hence, capacitors can be scaled down towards the later stages for power saving. The optimum downscaling factor approximately equals the reciprocal of interstage gain, G, which is 2 in 1.5-bit/stage

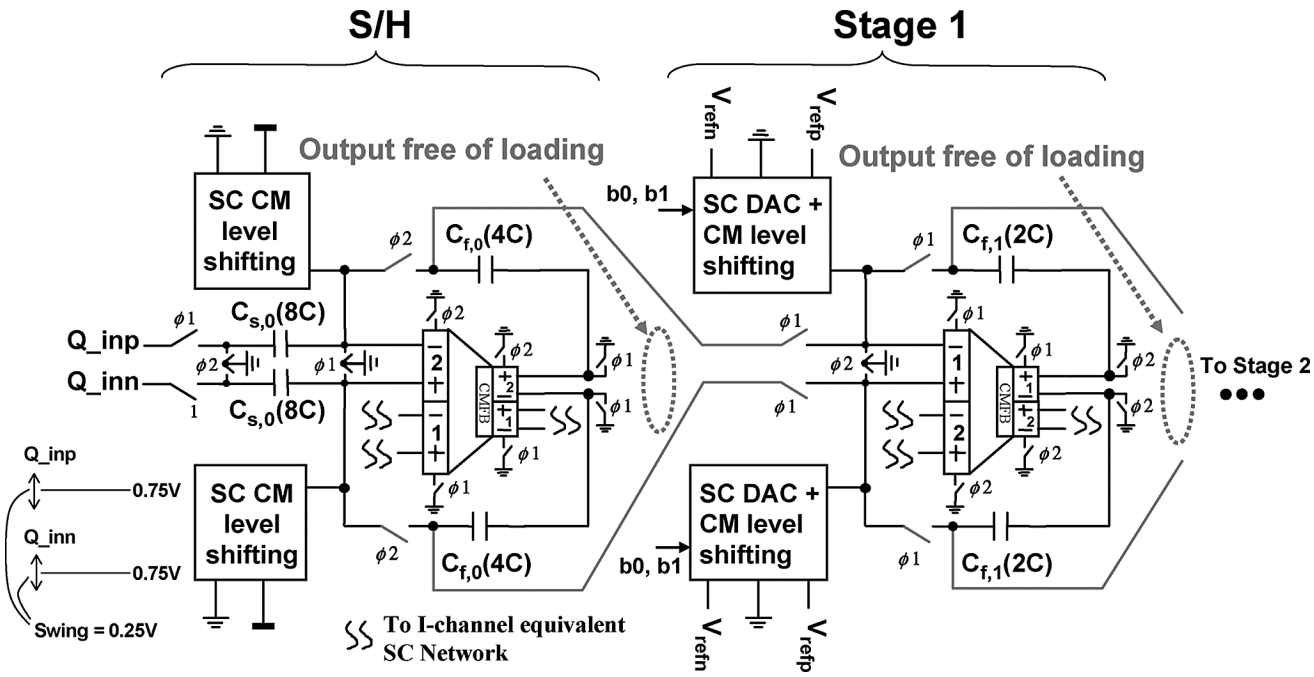

Fig. 4. Proposed loading-free architecture.

architecture [10]. In this design, a downscaling factor of 1/2 is used from S/H to stage 1, and from stage 1 to stage 2. The following stages are not further scaled down for modularity and ease of design. It is worth notice that choosing downscaling factor $= 1/G$ allows the straightforward implementation of the proposed loading-free architecture (to be discussed next).

B. Proposed Loading-Free Architecture

Fig. 4 shows the proposed loading-free architecture. Its working principle is described as follows: in ϕ_1, the sampling capacitor in the S/H (C_{sa} in Fig. 4) samples input voltage, while in ϕ_2, the feedback capacitor in the S/H (C_{fa} in Fig. 4) receives the charge transferred from C_{sa} with the aid of the opamp's virtual ground. This is the same as conventional SO MDAC operation. The difference is that the charge stored in C_{fa} is not reset in ϕ_1; instead, it is transferred to C_{fb} of the next stage when the next stage is in the amplification phase. The idea comes from the insight that when C_{fa} acts as feedback capacitor in ϕ_2, it is also storing the output voltage information. Hence, it is possible to remove the dedicated sampling capacitor from the next stage, and make use of C_{fa} to mimic the sampling capacitor of the next stage in ϕ_1. In other words, the opamp output is free from loading of the next stage's sampling capacitor. To achieve a stage gain of 2 for the next stage, C_{fb} has to be half of C_{fa}. Hence, the choice of downscaling factor of 1/2 is perfectly suitable for the proposed load-free architecture. Yet, other downscaling factors can also be employed for the architecture with some minor modification of the capacitor ratios.

By using feedback capacitors in both phases for different functions, the dedicated large sampling capacitor from next stage is removed and the capacitive loading of the opamp is reduced. As an illustration, the capacitive load of conventional SO MDAC stage i is given by

$$C_{L,i} = [(C_{s,i} + 2C_{ls,i}) \| C_{f,i}] + C_{\text{other}} + C_{s,i+1} \qquad (3)$$

where C_{other} is the sum of capacitance from opamp's common-mode feedback (CMFB), sub-ADC, etc. Using the previous sizing criteria $C_{s,i} : C_{f,i} : C_{ls,i} : C_{s,i+1} = 4C : 2C : C : 2C$, and assuming $C_{\text{other}} = 0.5C$ gives $C_{L,i} = 4C$. Loading-free architecture eliminates the last term, $C_{s,i+1}$ in (3) and reduce $C_{L,i}$ to 2C. Hence, the loading-free architecture significantly reduces the capacitive loading of the opamp and thus increases the operation speed.

A potential issue with loading-free architecture is that there is a small amount of charge remaining in the feedback capacitor due to the finite opamp gain in the next stage. This is similar to the memory effect. However, simulations show that high opamp gain (e.g., 70 dB) is enough to make this effect negligible for 8-bit resolution.

C. Input S/H Stage and Whole ADC Architecture

The SO technique helps to eliminate the problematic floating switches in the MDAC, but the input series switch in the S/H cannot be avoided. Bootstrapped input switch [12] and passive input stage [17] were proposed to solve this problem. Another simpler solution is using a reduced input signal swing [16]. In this design, the previous stage driving the ADC has a single-ended swing of 0.25 V centered at 0.75 V [3]. Hence, an S/H with $2\times$ gain is used in our design to get a reasonable output swing of 0.5 V (single-ended). An SC common-mode level shifter [15] is used to set a correct common-mode level of 0 V at opamp input. With the input signal near supply voltage, a pMOS input switch is used. The advantage is that its body can be tied to the source (in our N-well process) to reduce body-induced threshold voltage variation along the input range,

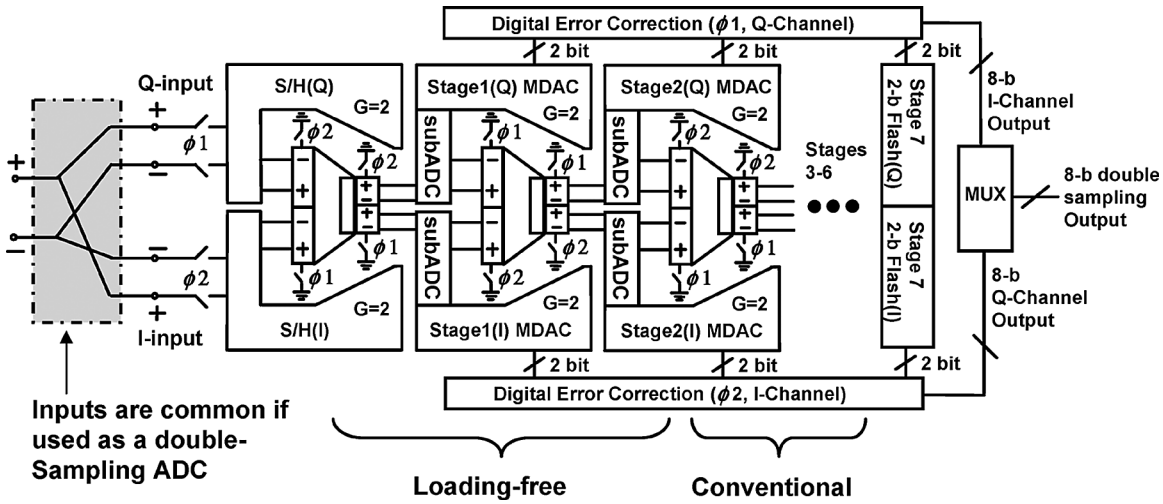

Fig. 5. Block diagram of proposed ADC in double-sampling mode.

thus reducing distortion to a certain extent. Yet, the overdrive of the input switch remains relatively small compared to the case using a sophisticated bootstrapped switch. The resulting larger switch on-resistance, and also the larger nonlinear junction capacitance (due to larger pMOS switch), is likely to dominate the high-frequency distortion performance. For applications requiring good high-frequency distortion performance, a bootstrapped input switch should be used.

The overall ADC architecture in double-sampling mode is shown in Fig. 5. Loading-free architecture is used in the front stages only; starting from stage 3, the conventional SO MDAC is used for modularity. When used as a quadrature ADC, I- and Q-inputs are separated. The input sampling capacitor is chosen to be 1.6 pF, taking into account the sampling noise scaling described previously and the opamp noise.

V. Proposed Low-Voltage Building Blocks

A. Switchable Opamp

Fig. 6 shows the proposed dual-input–dual-output (DIDO) switchable opamp, which features dual input $(\mathrm{M}_{1,2}/\mathrm{M}_{3,4})$ and output pairs $(\mathrm{M}_{5,6}/\mathrm{M}_{7,8})$ that turn on and off alternately. It is essentially a two-stage amplifier using Miller compensation. The first stage is a pMOS-input folded-cascode amplifier responsible for a large portion of amplifier's gain. Under low supply as 1 V, rail-to-rail output swing is critical for maximizing dynamic range. Thus, simple common-source amplifier is chosen to be the output stage. Earlier switched-opamps [14]–[17] either used a switch resetting the gate-source voltage of the tail current source, or a switch interrupting the current path between power supplies and current source. Hence, their current sources are switched on and off with the opamps, resulting in longer wake-up time. In this work, the current sources are always kept active [18]. The currents in tail current sources, M_{b1} to M_{b3}, are only steered from one branch to another through switches M_{s1} to M_{s7} when clock phase changes. When an output branch is inactive, its output voltage is also quickly shunted to zero by M_{s7}, M_{s8} (or M_{s9}, $\mathrm{M}_{\mathrm{s10}}$). The fastest possible switching is hence achieved. Also, it should be noted that the function of a switched-opamp to act as a switch replacing the floating switch for low-voltage SC circuits is still the same with the use of this switchable opamp. Another feature beneficial to the wake-up time is the complete symmetry in two time-multiplexed output stages, each with its own compensation capacitor. When a branch shuts off and its time-multiplexed branch wakes up, the charge stored in one compensation capacitor is passed to the other. This toggling see-saw action also speeds up the recovery of the opamp from the off-state. At 1-V supply, with 0.72-pF capacitive loading, the opamp achieves DC gain of 70 dB, 900-MHz unity gain frequency, 72 phase margin, and 1-V differential output swing while consuming 3.5 mW.

The CMFB consists of an SC level-shifter and an error amplifier. The SC level-shifter senses and level-shifts the CM output by 0.5 V for comparison with the ground reference. The error amplifier is a scaled-down version of the opamp's first stage for generating a stable CM control voltage, $\mathrm{v}_{\mathrm{cmfb}}$, to control the gate bias of tail current source and to set the CM output voltage to 0.5 V for maximum output swing.

B. Sub-ADC

Fig. 7 shows the sub-ADC, which includes a resistor string, an SC level-shifter and a latched-type comparator [17]. At ϕ_2, C_{ref} is precharged to V_{DD} and C_{smp} is reset; so that at ϕ_1, when C_{ref} samples the threshold voltages, and C_{smp} samples the opamp output, the comparator's input CM level is set to ground. The decision thresholds are set by the resistor string rather than by capacitor ratio. It has the advantage that minimum and equal capacitors can be used for reducing opamp's loading; otherwise, C_{smp} and C_{ref} would need to be sized in the ratio of 4:1 to set decision thresholds as $\pm V_{\mathrm{ref}}/4$, and an additional level-shifting switched-capacitor would need to be added for adjusting the CM input to comparator. The comparator uses a pMOS input

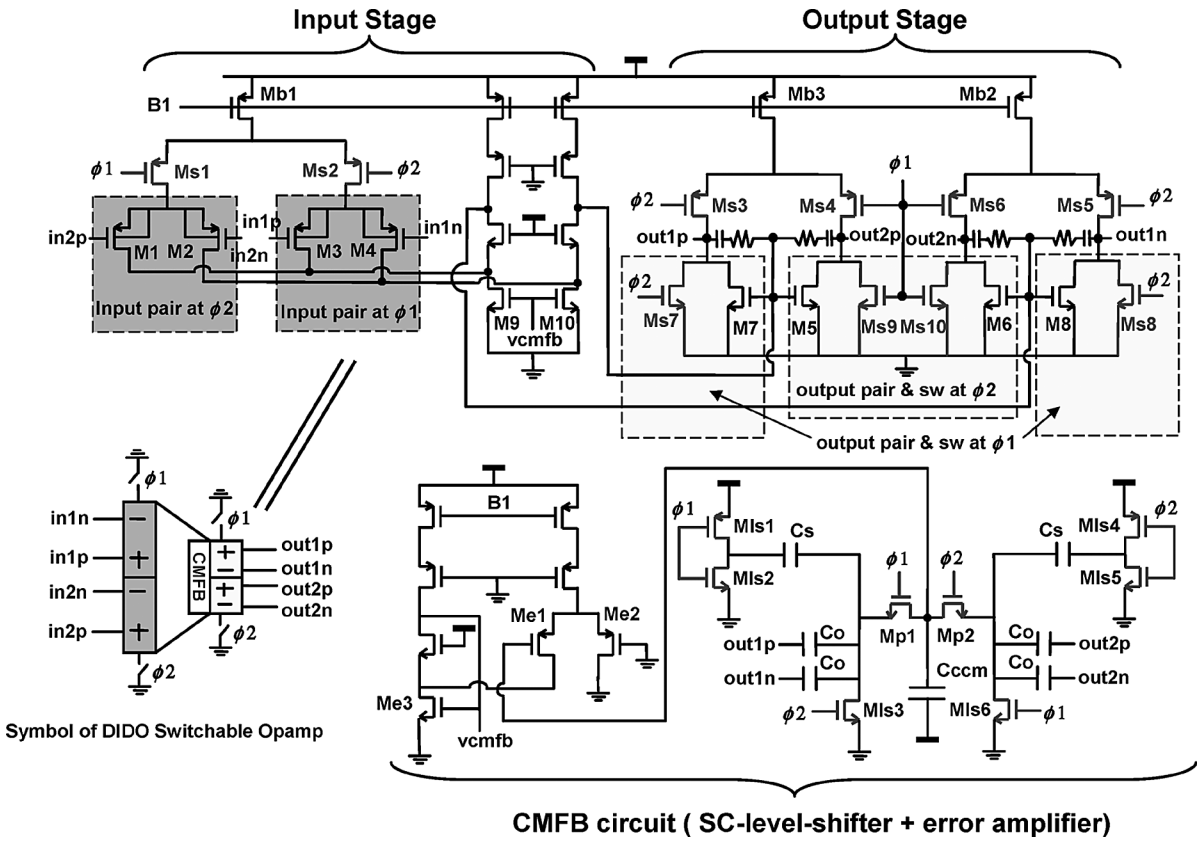

Fig. 6. Proposed dual-input–dual-output switchable opamp.

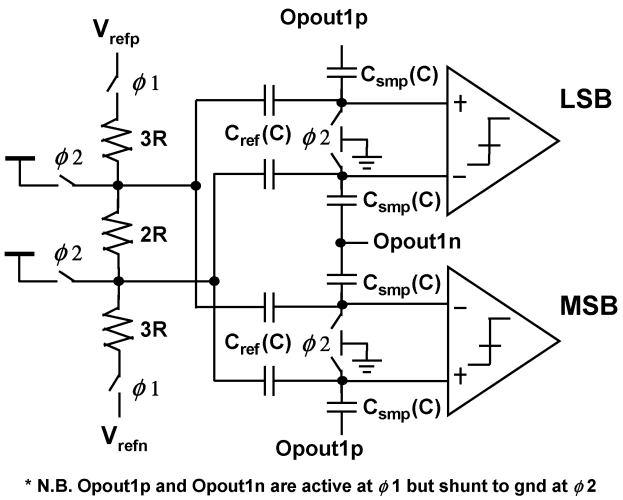

Fig. 7. Sub-ADC with thresholds $\pm V_{\rm ref}/4$ set by resistor string.

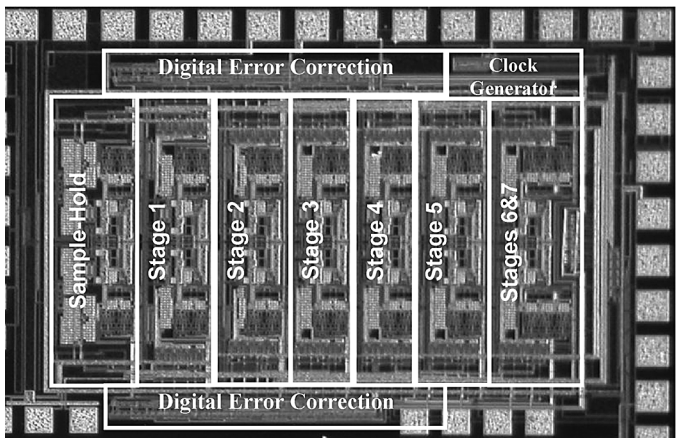

Fig. 8. Photomicrograph of prototype chip.

differential pair, an nMOS cross-coupled load, and a fixed tail current source consuming 350 μA.

VI. Measurement Results

The prototype chip has been fabricated in a 0.18-μm six-metal one-poly CMOS process. The capacitors are implemented using metal–insulator–metal (MIM) structures. The threshold voltages of the nMOS and pMOS transistors are 0.48 V and -0.47 V, respectively. Fig. 8 shows the die photo of the proposed ADC, which occupies an active area of 1.7×1.2 mm^2.

Static characteristics such as differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC were measured using a code-density test with a 1-MHz full-scale sine wave input. The measured DNL and INL profiles are shown in Fig. 9. The maximum DNL and INL are 0.5 LSB and 1.1 LSB, respectively.

Dynamic linearity is shown in the 16384-point Fast-Fourier-Transform (FFT) spectrum in Fig. 10. When the ADC is configured as a double-sampling ADC running at 100 MS/s, it achieves 52.6 dB spurious-free dynamic range (SFDR), 45.2 dB

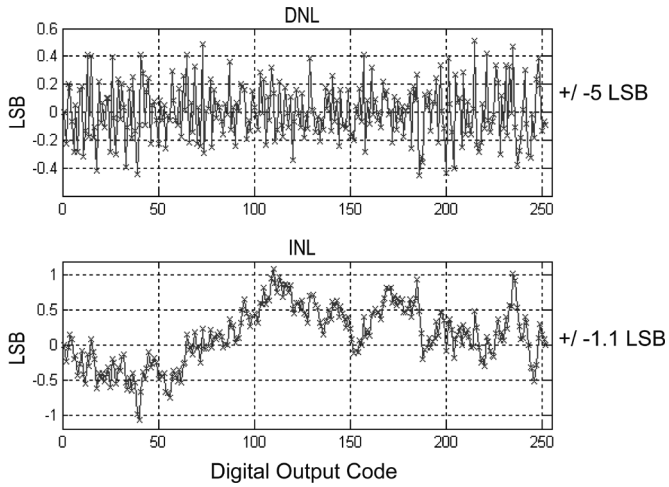

Fig. 9. Measured DNL and INL ($f_{\rm in} = 1$ MHz).

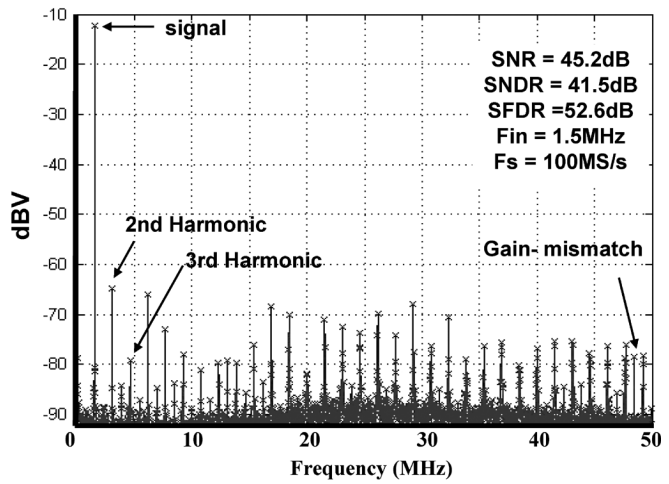

Fig. 10. Measured FFT spectrum (double-sampling).

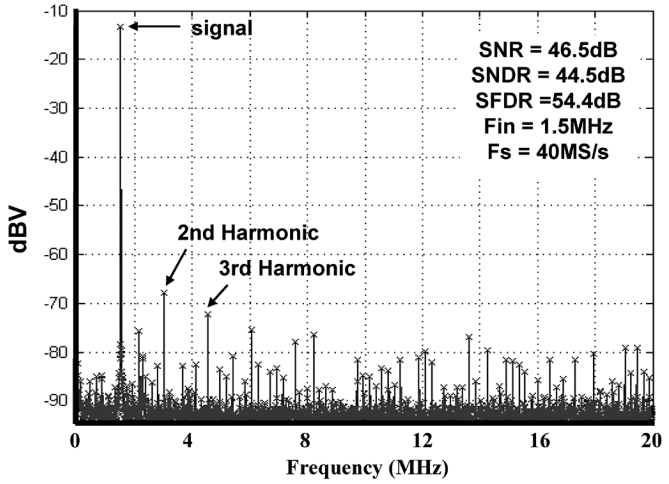

Fig. 11. Measured FFT spectrum (quadrature-sampling).

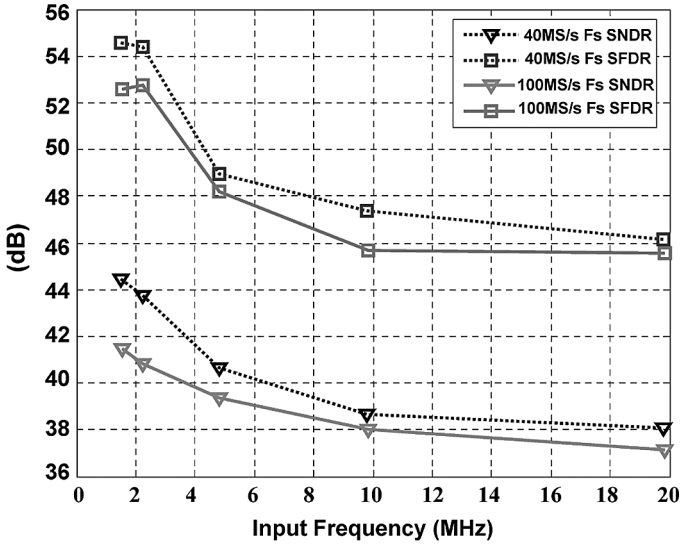

Fig. 12. SFDR and SNDR versus $F_{\rm in}$.

signal-to-noise ratio (SNR) and 41.5 dB signal-to-noise plus distortion ratio (SNDR) at input frequency of 1.5 MHz. The nonlinearity is dominated by the harmonics rather than the gain-mismatch between the channels. Offset mismatch tone at $f_s/2$ is not shown since it is filtered by the computer FFT program. The FFT spectrum of a single channel when the ADC is operating as a quadrature ADC at 40 MS/s with 1.5-MHz input frequency is shown in Fig. 11. Measured SFDR, SNR, and SNDR are 54.4 dB, 46.5 dB, and 44.5 dB, respectively.

Fig. 12 summarizes the measured dynamic performance with an input frequency span from 1.5 to 20 MHz. The linearity degrades in a relatively fast pace as input frequency increases. This is due to the distortion introduced by the simple input series switch.

The power consumption of the proposed ADC is only 30 mW including digital parts. Table I summarizes the measured performance. Table II summarizes the proposed design together with some state-of-the-art designs. Compared to the first SO pipelined ADC [17], the proposed ADC achieves more than 10 times improvement in speed and is the first 1-V SO pipelined ADC achieving conversion rate at 100 MS/s. This speed is comparable with many high-voltage SC pipelined ADC [8], [9]. A recent design [24] achieves the fastest operation at 200 MS/s by partially switching off the opamp. Yet, it operates at a high

TABLE I
MEASURED ADC PERFORMANCE SUMMARY

Operation Mode	Double-Sampling ADC	Quadrature ADC
Technology	0.18-μm, 1.8V, 6M1P CMOS	
Supply Voltage	1 V	
Resolution	8 bits	
Conversion Rate	100MS/s	40MS/s
DNL	+/-0.5LSB	+/-0.5LSB
INL	+/-1.1LSB	+/-1.1LSB
Peak SNR	45.2dB	46.5dB
Peak SNDR	41.5dB	44.5dB
Peak SFDR	52.6dB	54.4dB
Input Range	+/-250mV	
Power Consumption	30mW	
Active Area	1.7 x 1.2 mm^2	

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED ADC AND STATE-OF-THE-ART PIPELINE ADCS

Design	This Design	[17]	[23]	[24]	[9]	[8]
Technology (CMOS)	0.18-μm	0.5-μm	0.25-μm	0.18-μm	0.18-μm	0.18-μm
Supply Voltage	1 V	1 V	1.3 V	1.8 V	1.8 V	3 V
Technique	Multi-phase fast wake-up switchable opamp, double-sampling, loading-free architecture	Switched-opamp	SC with bootstrapped switches	Opamp partially shut down for power reduction Using bootstrapping technique	SC	SC with bootstrapped switches & opamp-sharing
Conversion rate	100MS/s	5MS/s	16.384MS/s	200MS/s	110MS/s	80MS/s
Resolution	8 bit	9 bit	13 bit	8 bit	12 bit	10-bit
SNDR	41.5dB	50dB	59.2dB	48dB	64.2dB	57.7dB
SFDR	52.6dB	59.5dB	62.5dB	57.5dB	69.4dB	72.8dB
DNL	+/-0.5LSB	0.6LSB	+/-0.5LSB	-0.44/+0.27LSB	+/-1.2LSB	+/-0.25LSB
INL	+/-1.1LSB	0.9LSB	+/-2.0LSB	-0.44/+0.34LSB	-1.5/+1LSB	+/-0.5LSB
Power Consumption	30mW	1.6mW	78mW	30mW	97mW	69mW

supply of 1.8 V under which the problematic floating switch issue does not exist.

VII. CONCLUSION

A 1-V SO pipelined ADC has been presented. Early SO works were mainly limited in speed by slow wake-up transient, large capacitive load, smaller feedback factor, and lack of ability of double-sampling. By using the proposed loading-free architecture, a fast-wake-up dual-input–dual-output switchable opamp, multiphase SO technique and double-sampling, the proposed ADC achieves 100-MS/s conversion rate, which is the fastest reported speed at 1-V supply voltage using the SO technique, and comparable to many high-voltage SC counterparts. With small power consumption of 30 mW, the proposed ADC is good for many portable applications.

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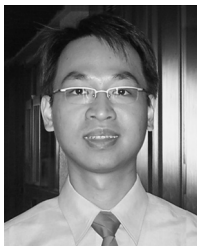

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