A 1.5 v High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18 µm Technology

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***Abstract*—A High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18 µm Technology with 1.5v supply, is presented.Topology selection and theoretical analysis of the design are discussed. Cascode technique has been used to increase the dc gain. The unity-gain bandwidth is also enhanced using a gain-stage in the Miller capacitor feedback path . The proposed opamp provides 236MHz unity-gain bandwidth, 81.3 degree phase margin and a peak to peak output swing 1.26v. The circuit has 92.5dB gain and slew rate is 16.75 v/µs . The power dissipation of the designed only is 50µw. The designed system demonstrates relatively suitable response in different temperature.**

Keywords- Two Stage CMOS OP-AMP , Cascode , High Swing ,Ultra-Low-Power , Low-Voltage

I. INTRODUCTION

Research in analog-circuit design is focused on low-voltage low-power battery operated equipment to be used as an example in portable equipment, wireless communication products, hearing aids, and consumer electronics. A reduced supply voltage is necessary to decrease power consumption to ensure a reasonable battery lifetime in portable electronics. For the same reason, low-power circuits are also expected to reduce thermal dissipation, of increasing importance with the general trend in minimization. Advancements required by International Technology Roadmap for Semiconductors (ITRS), means that with current CMOS standard fabrication processes, circuits must work at supply voltages as low as 1.5 V. Working at lower voltages poses new constraints, especially important for the specific case of analog design. However, a reduction in performance is not desirable. Nevertheless, going to lower voltages and higher efficiencies require innovative circuits to solve current design needs of faster circuits and better performance [1].

From the other point of view, as for various recently-developed high-performance integrated electronic systems or subsystems, e.g. A/D converter, switched-capacitor filter, RF modulator and audio system, CMOS operational amplifiers with high unity-gain bandwidth and large dynamic range are necessitated [2].

For high-accuracy circuits, op amps with very high open loop gain and high unity gain frequency are required in order to meet both accuracy and fast settling requirements. Satisfying both of these requirements is difficult with short-channel CMOS processes, since the intrinsic gain of the devices is limited [3]. Although long-channel transistors or subthreshold operations improve gain, the frequency response is sacrificed [4]. So from previous argument, it is deduced that the designing of op-amps puts new challenges in low power applications with reduced channel length devices.

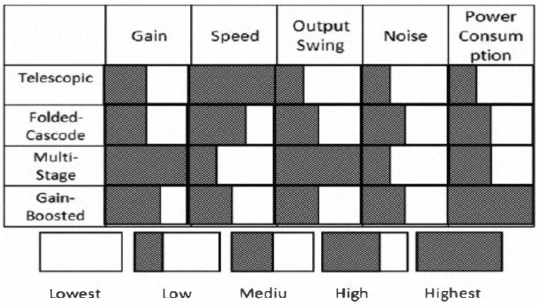
The organization of this paper is as follows. In section II, we will briefly review miscellaneous amplifier topologies. Following this, theoretical analysis of the design will be addressed in section III.Simulation results and conclusion will be studied in sections IV and V respectively.

II. SELECTING CIRCUIT TOPOLOGY

In TABLE I a comparison of performance of various op-amp topologies is represented. As seen from TABLE I, multi-stage op-amps are suitable for high gain, high swing and low noise applications. While as for the multistage topology, especially more than two stages, the stability problem will become severe for us. Large common mode input range is another benefit of two stage op-amps. Considering design specifications a two stage amplifier seems to be good. In a two stage op-amp, the first stage provides high gain and the second, arge swings. In contrast to cascode op-amps, a two stage configuration isolates the gain and swing requirements [5].

Since the operational amplifier developed here is unbuffered(output resistance will be high), might be better name it operational transconductance amplifier(OTA) [6].

TABLE I. COMPARISON OF PERFORMANCE OF VARIOUS OP-AMP TOPOLOGIES



III. CONVENTIONAL RHP ZERO CONTROLLING TECHNIQUES & CIRCUIT DESIGN

Clearly, a disadvantage of the Miller frequency compensation technique is the inconvenience of the right half

plane (RHP) zero. This RHP zero degrades the phase margin and leads to instability of operational amplifiers. Two different approaches of controlling the RHP zero are shown in Fig. 1 [5]. As observed in Fig. 1 (a), the nulling resistor controls the RHP zero by the basis of displacement. On the other hand, as shown in Fig. 1 (b), the employed gain-stage M2 prevent the input current from going directly through the Miller capacitor, thus, the RHP zero will eliminate [7]. As can be observed in Fig. 1 (a), at frequencies near unitygain frequency, the reactance of the compensation capacitor Cc can be ignored. Therefore, the output resistance seen by Cout can be derived as given by

$$R_{out} \approx 1 / g_{m1}. \quad (1)$$

while from Fig. 1 (b), the output resistance seen by Cout can be expressed as [5]

$$R_{out} \approx 1 / (g_{m1}\, g_{m2}\, r_{ds2}). \quad (2)$$

And also,

$$P_0 = 1 / R_{out} C_{out}. \quad (3)$$

Obviously, it can be deduced from (2) and (3) that noticeable reduction of R_{out} by a factor of $g_{m2}\, r_{ds2}$ is the basis of improvement in "pole-splitting" effect which is valid only for Fig. 1 (b) and not for Fig. 1 (a). Therefore, increasing the magnitude of the non-dominant output pole , mainly due to the employed gain-stage M2 , leads to a proportional enhancement in unity-gain bandwidth.

In this work, the output impedance of the first stage is increased, mainly thanks to the employed transistor M6, thus, the DC gain is improved. The unity-gain bandwidth is also enhanced using a gain-stage (common-gate) in the Miller capacitor feedback path as done by transistor M6. Consequently, the gain-bandwidth product (GBW) is considerably enhanced.

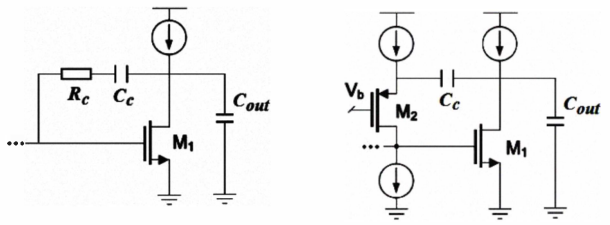


Figure 1. The RHP zero controlling structures: (a) nulling resistor approach, (b) gain-stage (common-gate) approach.

As observed in Fig. 2, the compensation result is to keep the dominant pole roughly the same as normal Miller compensation and to increase the output pole by approximately the gain of a single stage M6. the magnitude of the output pole can be given by

$$P_0 = (g_{m12} g_{m6} r_{ds6}) / C_{out}. \quad (4)$$

Consequently, the output pole P_0 has split from the dominant pole by a factor of $g_{m6} r_{ds6}$ which leads to an enhancement in unitygain bandwidth, when compared to the nulling resistor approach .

Consider schematic of an unbuffered, two stage CMOS op-amp with an p-channel input pair shown in Fig. 2.

In this work, from the expressions in relation with the compensation capacitor Cc, the slew rate is given by

$$SR = dv_o / dt = I_9 / C_C. \quad (5)$$

Requirements for the transconductance input transistors can be determined from Knowledge of Cc and GBW Using Equation (6) the transconductance gm1 can be calculated by the following equation

$$GBW = g_{m1} / C_C. \quad (6)$$

The aspect ratio $(W/L)_1$ is directly obtainable from gm1 as shown below.

$$(W/L)_1 = g^2_{m1} / 2\beta I_1. \quad (7)$$

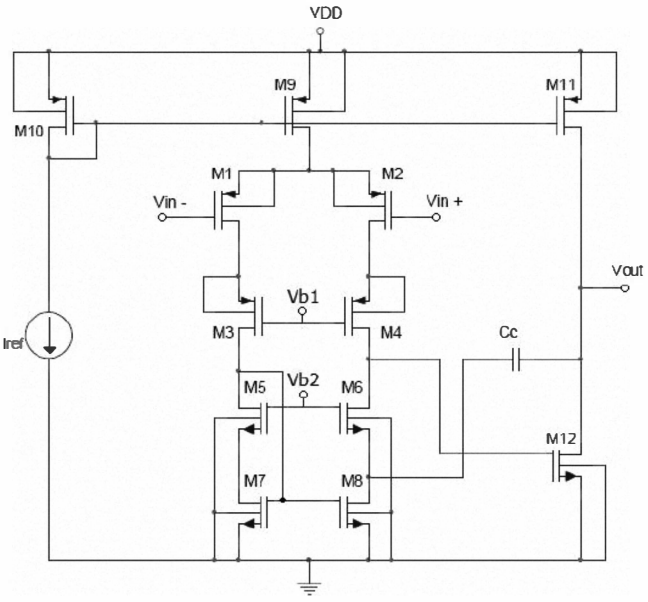


Figure 2. Schematic of an Unbuffered, Two Stage CMOS Op-Amp

The gain of the differential amplifier, is given by the product of g_{m1} and the load conductance

$$AV_1 \approx g_{m1}(R_{OP} \parallel R_{ON}). \quad (8)$$

And

$$R_o \approx g_m r_o^2. \quad (9)$$

The gain of the current source inverting amplifier, is given by the product of g_{m12} and the load conductance

$$AV_2 \approx g_{m12}(r_{o11} \parallel r_{o12}). \quad (10)$$

In order to avoid any systematic offset it is possible to derive an equation as follows.

$$V_{gs12} = V_{ds6} + V_{ds8}. \quad (11)$$

And

$$V_{gs7} = V_{ds5} + V_{ds7}. \quad (12)$$

So

$$V_{gs7} = V_{gs12}. \quad (13)$$

With respect to (11) and (12) we can write

$$I_{ds7} = (W/L)_7 / (W/L)_{12} \times I_{ds12}. \quad (14)$$

$$I_{ds7} = I_{ds9} / 2. \quad (15)$$

Table II exhibit the results of the calculation for the aspect ratios in the first and second stages.

IV. SIMULATION RESULT

The circuit was simulated in HSPICE with BSIM3v3.1 model based on a standard 0.18 µm CMOS process. The OPAMP operates with the 1.5V power supply and consumes only 50µW power. Simulations resulted on considerable increase of unity-gain bandwidth to the value of 236 MHz, the improved DC gain of 92.5 dB, and a phase margin of 81.3 degree.

TABLE II. ASPECT RATIOS OF OPAMP

Transistor	W	Transistor	W
M1	15 µm	*M7*	3 µm
M2	15 µm	*M8*	3 µm
M3	10 µm	*M9*	6.8 µm
M4	10 µm	*M10*	2.8 µm
M5	2 µm	*M11*	11 µm
M6	2 µm	*M12*	8 µm

For all Transistor L=0.36 µm

Fig. 3 presents the simulated DC gain and Fig. 4 shows the phase margin of the OPAMP. Swing voltage is 1.26 v. Additionally, with the load capacitor CL of 1 pF and with a compensation capacitor Cc of 208 fF, the Slew rate of 16.75 V/µs is resulted. The swing voltage and slew rate parametres are depicted in Fig.5 and Fig.6, respectively. Simulation Results represent that the designed OPAMP has high voltage gain, low supply voltage, high swing voltage, high unity-gain bandwidth and ultra low power dissipation and to evaluate this work using a figure of merit (FoM) defined as:

$$FOM = (Gain).(UGB) / (Vdd).(Power). \quad (16)$$

The OPAMP performance at different temperature is illustrated in Table III. The performance summary and comparison to other CMOS OPAMPs is listed in Table IV.

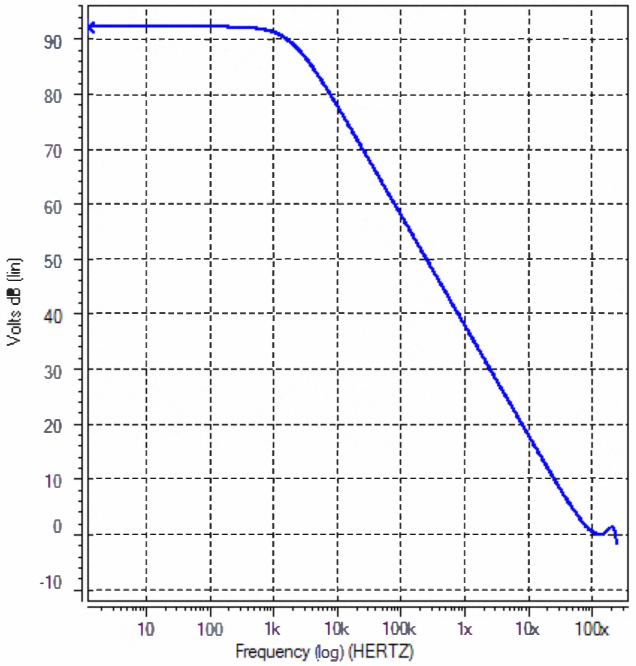


Figure 3. Simulated DC gain.

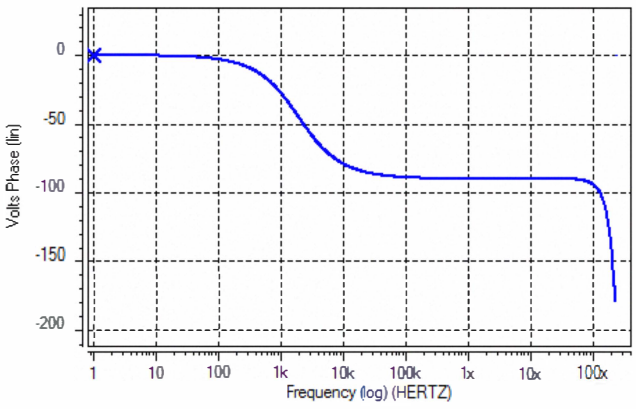


Figure 4. Simulated phase margin.

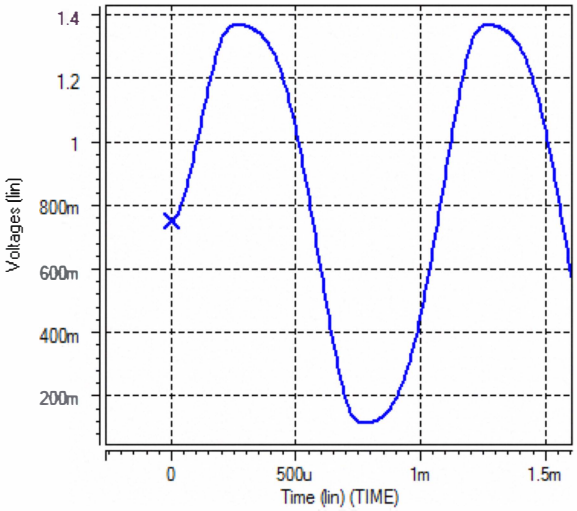


Figure 5. Simulated swing voltage

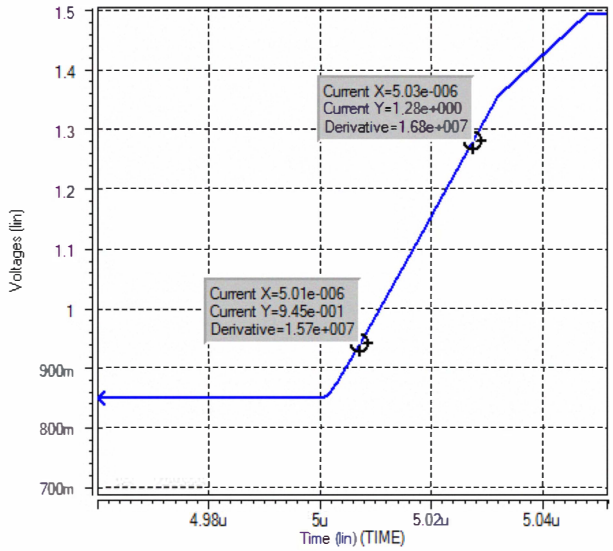


Figure 6. Simulated Slew rate

TABLE III. COMPARISON OF PERFORMANCE OP-AMP AT DIFFERENT TEMPERATURE

temp(degree)	-20	0	27	100
Gain(dB)	92.1	92.2	92.5	90.6
UGB(MHz)	229	230	236	108
PM(degree)	18	82	81.3	86.6

V. CONCLUSION

The design procedure of a low voltage, ultra low power two stage CMOS operational transconductance amplifier in 0.18µm technology has been discussed and verified by simulation. The unity-gain bandwidth is also enhanced using a gain-stage in the Miller capacitor feedback path. The design was performed in 1.5v power supply. Ultra Low power consumption, 81.3° phase margin, appropriate slew rate , high swing and unity gain frequency suitable are other from feature this OAMP. The designed system demonstrates relatively suitable response in different temperature.

TABLE IV. PERFORMANCE SUMMARY AND COMPARISON TO OTHER CMOS OPAMPS

Performance Summary	comparison				
	This work	[1]	[8]	[9]	[10]
DC Gain(dB)	92.5	100	80	44.7	81
UGB(MHz)	236	2.7	167	0.81	5
PM(degree)	81.3	N/A	73.5	52	65
Slew rate(V/µs)	16.75	1	N/A	1.25	6.5
Output swing(v)	1.26	N/A	1.13	N/A	2.3
Power supply(v)	1.5	0.75	1.5	1.9	2.5
Power diss(µW)	50	275	8900	62	378
FOM (dB.MHz/V.µW)	291	0.65	1	0.31	0.43

REFERENCES

[1] J. Ramos, M.S.J. Steyaert, "Positive Feedback Frequency Compensation for Low Voltage Low Power Three Stage Amplifier," in IEEE Transactions On Circuits and Systems, vol. 51,no. 10, , pp. 1967-1974, Oct,2004.

[2] Z. Liu, C. Bian,Z. Wang, C. Zhang, "Full custom design of a two-stage fully differential CMOS amplifier with high unity-gain bandwidth and large dynamic range at output", 48th IEEE International Midwest Symposium on Circuits and Systems, U.S.A., 2005.

[3] J. Liod, H. Lee, "A CMOS OP Amp with Fully- Differential gain-Enhancement," in IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 41, no. 3, March, 1994.

[4] W.W Sue, Z.M. Lin, C.H. Haung, "A High DCGain Folded-Cascode CMOS Operational Amplifier", IEEE Southeastcon Proceedings. , pp.176 – 177, Apr. 1998.

[5] P.E. Allen, D.R. Holberg, CMOS Analog Circuit Design, New York, Oxford University Press, 2002.

[6] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.

[7] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational Amplifiers," IEEE Journal of Solid-State Circuits, vol. SC-18, no. 6, pp. 629-633, Dec. 1983.

[8] M. Yavari, H. Zare-Hoseini,M . Farazian,a nd O. Shoaei," A new compensation technique for two-stage CMOS Operational Transconductanc Aemplifier" in Proc. IEEE Intl. Conf. Electronics, Circuits, Systems, ICECS , pp. 539-542,Dec. 2003.

[9] J.R. Angulo, A.J. Lopez-Martin, A. Garimella, L.M.K. Garimella, R.G. Carvajal, "Low voltage,Low Power Rail-to-Rail two stage OPamp with Dynamic Biasing and no Miller compensation", 50th Midwest Symposium on Circuits and Systems (MWSCAS), pp. 25-28, 2007.

[10] J. Mahattanakul, "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer" , IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 52, NO. 11, NOVEMBER 2005.