A GAIN-ENHANCED TWO-STAGE FULLY-DIFFERENTIAL CMOS OP AMP WITH HIGH UNITY-GAIN BANDWIDTH

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ABSTRACT

This paper presents a gain-enhanced two-stage fully differential CMOS op amp. A very high dc gain is achieved together along with a very high unity-gain bandwidth and low power dissipation. The pole-zero doublet arising from the gain-enhancement is analyzed in detail. The side effects of the gain-enhancement circuit are minimized. The frequency responses indicate that more than 120 dB open loop dc gain and 500 MHz unity-gain bandwidth are obtained. The simulated settling behavior shows that it only takes 13.5 ns to reach more than 120 dB settling accuracy. To date, this is one of the best high-performance op amps that have been reported.

1. INTRODUCTION

The op amps with both high dc gain and high unity-gain bandwidth are demanded in high performance A/D converters and switched-capacitor filters. Various CMOS op-amp designs [1][2][3][4] have been developed in an attempt to meet both requirements while minimizing performance trade-offs. In [1] the additional amplifiers provide local feedback to boost the dc gain of a differential folded-cascode op amp to 90 dB with high unity-gain bandwidth. To achieve fast settling and high gain, the power dissipation and area of additional op amp are relatively large [1]. As a result, the side effects that the gain-enhancement circuit may have on the main circuit are not minimized. A two-stage differential op amp using a telescopic as its first stage [3][4] is the other technique for optimizing both gain and bandwidth. However, only 90 dB of open-loop gain and 100 MHz unity-gain bandwidth are reported [3]. To support the fast development of increasingly higher performing circuits, the op amps with more than 120 dB dc gain and 500 MHz unity-gain bandwidth become necessary.

We will show here a two-stage op amp implemented with the gain-enhancement technique, which allows for a large output voltage swing, high unity-gain bandwidth and low power dissipation. The architecture of the high performance op amp and the pole-zero doublet due to the gain-enhancement are explained in section 2. Section 3 provides the simulation of frequency response and settling time. The conclusion will be given in section 4.

2. GAIN-ENHANCED TWO-STAGE OP AMP

Fig. 1(a) shows the proposed two-stage fully differential CMOS op amp. In the first stage, two small op amps, A_p with NMOS as the input-stage and A_n with PMOS as the input-stage which are shown in Fig. 1(b) and Fig. 1(c) respectively, are implemented in a telescopic op amp to realize very high open-loop dc gain.

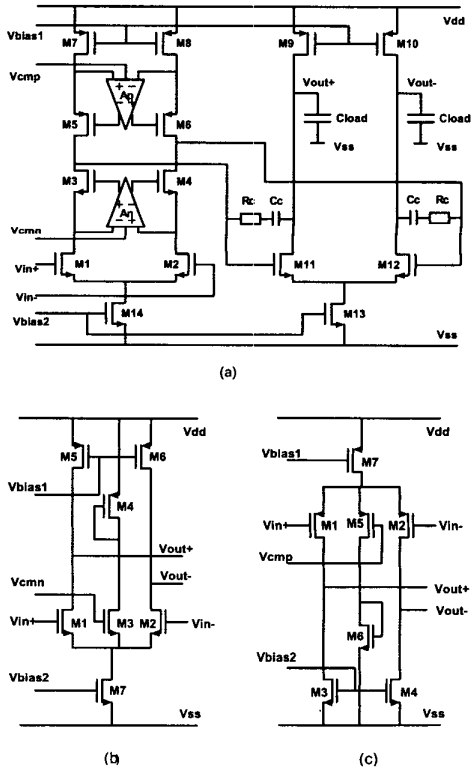

Fig. 1. (a) An gain-enhanced two-stage fully-differential CMOS operational amplifier. (b), (c) NMOS and PMOS input-stage gain-enhancement op amps.

The second stage of the amplifier consists of a differential source-coupled pair with tail current to attenuate substrate and common-mode noise, and to eliminate the need for a dc level shift between the output of the first stage and the input of the second stage. Two gain-enhancement op amps share the same biasing circuit with main op amp to achieve lower power consumption and small area. A dynamic switched-capacitor common-mode feedback, not shown here, is adopted for biasing the output common-mode levels of the first and second stage since it does not dissipate additional power.

This approach boosts the open-loop dc gain by a factor equal to the dc gain of the added amplifiers. The gain-enhancement will shift the dominant pole to a lower frequency, but will not affect the unity-gain bandwidth of the original op amp if the unity-gain bandwidth of the gain-enhancement op amps are designed such that their unity-gain bandwidth is larger than 3-dB of the original two-stage op amp. It's well known that such gain-enhancement method introduces a pole-zero doublet that may cause slow settling [1]. Hence a single-pole settling behavior demands a high unity-gain bandwidth of the gain-enhancement op amps.

For simplicity, the single-ended half circuit is used to explain the pole-zero doublet in the gain-enhanced two-stage op amp. Additionally, we assume tail current and active loads are all ideal current sources. The impedance plot is shown in Fig.2. Here, $\omega_{3dB,orig}$ and $\omega_{3dB,tot}$ are the dominant poles before and after applying gain-enhancement. $\omega_{3dB,enh}$ and $\omega_{u,enh}$ are the 3-dB frequency and the unity-gain bandwidth of the gain-enhancement op amp respectively. The unity-gain bandwidth of enhanced op amp is not degraded by gain-enhancement which is $\omega_{u,orig}$. In Fig. 1(a), the approximate dc gain of the first stage and entire op amp are

$$A_{o1,tot} = \frac{g_{m2}g_{m4}(1+A_{enh})}{g_{o2}g_{o4}}, \text{ and}$$

$$A_{o,tot} = \frac{g_{m2}g_{m4}(1+A_{enh})}{g_{o2}g_{o4}}\frac{g_{m12}}{g_{o12}} \quad (1)$$

where A_{enh} is the gain of gain-enhancement op amp. Hence the impedance R_{out1} is

$$R_{out1} = \frac{g_{m4}(1+A_{enh})}{g_{o2}g_{o4}}. \quad (2)$$

We define

$$R_{out} = R_{out1}\frac{g_{m12}}{g_{o12}} = \frac{g_{m4}(1+A_{enh})}{g_{o2}g_{o4}}\frac{g_{m12}}{g_{o12}}; \quad (3)$$

and also,

$$R_{orig} = R_{out1,orig}\frac{g_{m12}}{g_{o12}}, \text{ where } R_{out1,orig} = \frac{g_{m4}}{g_{o2}g_{o4}}. \quad (4)$$

As shown by dash line in Fig. 2, R_{out} starts to roll-off with slope of –20 dB per decade for frequencies above $\omega_{3dB,enh}$, and remains at R_{orig} after ω exceeds $\omega_{u,enh}$. Note that the dominant pole in this miller-compensated two-stage op amp is located at the first stage's output. If the total effective capacitance at the output of the first stage is C_{tot}, the impedance at the output of the first stage due to parallel connection between R_{out1} and C_{tot} is

$$Z_{tot1} = \frac{1}{\frac{1}{R_{out1}} + j\omega C_{tot}}. \quad (5)$$

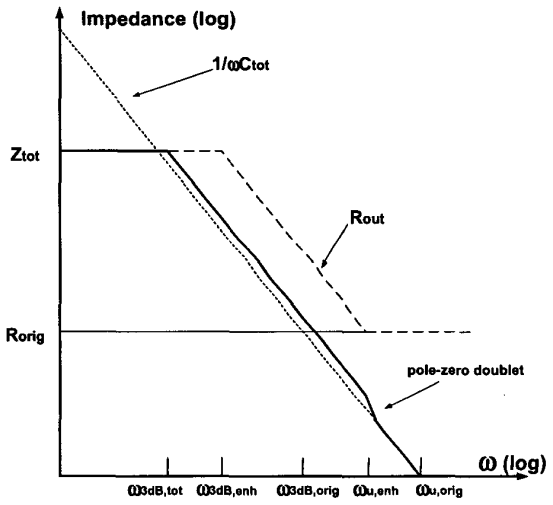

Fig. 2. Impedance plots illustrating the pole-zero doublet.

In Fig.2 ωC_{tot} is depicted by dotted line. Again we define

$$Z_{tot} = \frac{1}{\frac{1}{R_{out1}} + j\omega C_{tot}}\frac{g_{m12}}{g_{o12}} = \frac{1}{\frac{g_{o2}g_{o4}}{g_{m4}(1+A_{enh})} + j\omega C_{tot}}\frac{g_{m12}}{g_{o12}} \quad (6)$$

which is described by solid line in Fig. 2. Obviously, the susceptance ωC_{tot} results in the first order roll-off for frequencies above $\omega_{3dB,tot}$. The original total impedance Z_{orig} (without A_{enh}), should be

$$Z_{orig} = \frac{1}{\frac{1}{R_{out1,orig}} + j\omega C_{tot}} \frac{g_{m12}}{g_{o12}} = \frac{1}{\frac{g_{o2}g_{o4}}{g_{m4}} + j\omega C_{tot}} \frac{g_{m12}}{g_{o12}} \quad (7)$$

It is shown by (6) and (7) that Z_{tot} is slightly larger than Z_{orig} before A_{enh} decays to less than one (or for frequencies below $\omega_{u,enh}$). Z_{tot} and Z_{orig} are merged together for frequency above $\omega_{u,enh}$. Consequently, a pole-zero doublet is produced in which the pole is ahead of zero. It should be addressed that the pole-zero doublet corresponding to the gain-enhancement amplifier unity-gain bandwidth must be positioned out of the closed-loop band of the enhanced two-stage op amp to suppress the slow settling component arising from the doublet [1].

3. THE SIMULATION RESULTS

The gain-enhanced two-stage op amp as shown in Fig. 1 has been demonstrated using 0.5 um process and 5 V supply voltage. The designed op amp with 5pF load is compensated very well so that all non-dominant poles and zeros including the pole-zero doublet are adjusted to be much larger than the unity-gain bandwidth of the entire op amp for enough phase margin.

The simulated Bode plots of the frequency response are shown in Fig. 3. The solid curve represents the gain magnitude and phase characteriscs of the gain-enhanced op amp. The dashed line shows the gain magnitude and phase of the op amp without gain-enhancement. The significant increase in open-loop dc gain doesn't result in any decrease in unity-gain bandwidth. The logarithmic gain magnitude of the gain-enhancement op amp is also shown here by dotted curve. It is clear that the unity-gain bandwidth of the gain-enhancement op amps is slightly higher than the unity-gain bandwidth of the original op amp so that the pole-zero doublet will not cause the slow settling even if the op amp is used in a closed-loop with unity-gain feedback. Two gain-enhancement amplifiers which boost the overall dc gain by about 32x are designed with minimum channel length for high speed purpose. Each gain-enhancement amplifier only takes about 4% of the area and power dissipation of the entire op amp. Therefore, the side effects of the gain-enhancement circuit are minimized. As shown in Fig. 3, the total open-loop dc gain is 124 dB, and the unity-gain bandwidth is 512 MHz with 55 degree phase margin. The differential peak-to-peak output swing is designed to be 6V. The major characteristics of the op amp are summarized in Table 1.

The step response is simulated in a closed-loop configuration according to Fig. 4. Here, both input capacitor C_i and feedback capacitor C_f are 1 pF, while load capacitor C_L is 5 pF. The C_p represents parasitic capacitance which is 0.55pF.

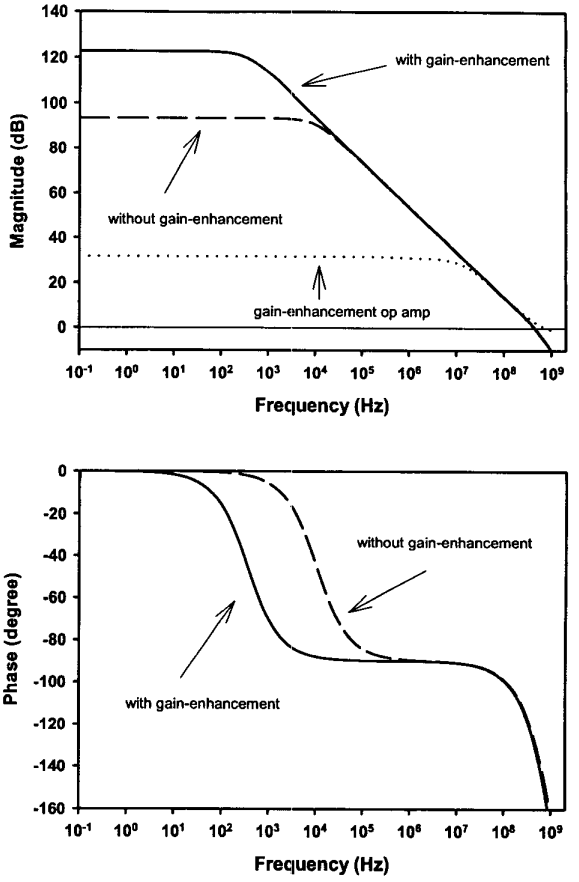

Fig. 3. Open-loop characteristic for op amps with and without gain-enhancement.

Table 1.
Summary of Op Amp Simulation Results

DC-gain	124 dB
Unity-gain bandwidth	512 MHz
Phase-margin	55 degree
Slew rate	0.32 V/ns
Load capacitor C_L	5 pF
Compensating capacitor C_c	1.75 pF
Differential output swing	+/- 3 V
Power supply	5 V
Power dissipation	46mW

A +/- 1.5 V large step-signal at the input is applied. The solid line in Fig. 5 shows the simulated settling accuracy of the op amp with gain-enhancement. The settling behavior without gain-enhancement is plotted by dash line here. Obviously, there is no slow settling component and the output quickly settles to its final state

without ringing. The gain-enhanced op amp takes 9.5ns to settle to 0.003% (90 dB), and 13.5 ns to reach its final accuracy (124 dB). To date, this is one of the best high-performance op amps that have been reported [1][3][4].

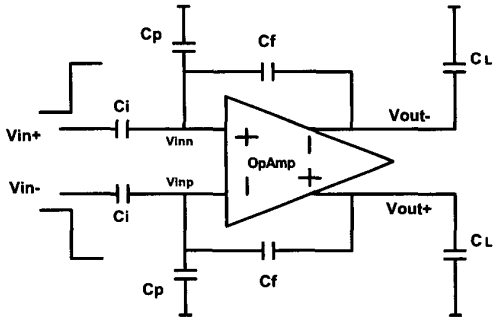

Fig. 4. The closed-loop configuration for simulating the settling-time.

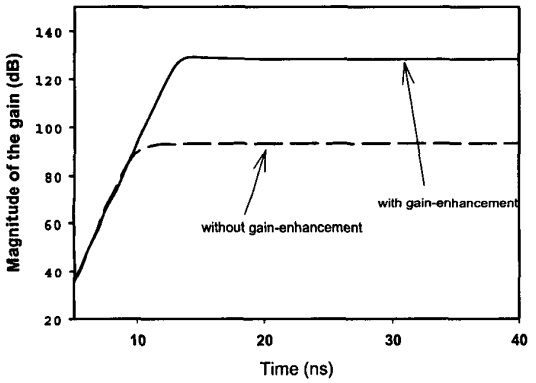

Fig. 5. The simulated settling accuracy as a function of time for with and without enhancement.

4. CONCLUSION

A gain-enhanced two-stage, fully differential CMOS op amp with high unity-gain bandwidth and low power dissipation is presented. The slow settling component arising from the pole-zero doublet due to the gain-enhancement is avoided. The designed op amp has 124 dB gain together along with a 512 MHz unity-gain bandwidth and 6V peak-to-peak output swing. This paper demonstrated that it is still possible to build a low power op amp having both high dc gain and high unity-gain bandwidth by using a modern short-channel CMOS process. The advantage of this architecture will become more evident if the cutting-edge sub-micro process with lower supply voltage is used.

5. REFERENCES

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