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Design Of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power and High CMRR

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Abstract—-- **In this paper a CMOS two stage operational amplifier has been presented which operates at 2.5 V power supply at 0.18 micron (i.e., 180 nm) technology and whose input is depended on Bias Current. The supply voltage has been scaled down to reduce overall power consumption of the system. The main aim of our work is to decrease power dissipation .At large supply voltages, there is a trade-off among speed, power and gain. Performance of any circuit depends upon speed, power and gain. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 36.747dB and a -3db bandwidth of 7.33 kHz and a unity gain bandwidth of 16.54 MHz for a load of 3 pF compensation capacitor & 10 pF load Capacitor. This op-amp has a PSRR (+) of 179.3dB , Common Mode gain of -102.4 dB, with a high CMRR of 133.69 dB and an output slew rate of 12.5 v/µs. The power consumption for the op-amp is .804mW.**

Keywords— CMOS, Two stage Opamp, CMRR, PSRR

I. INTRODUCTION

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits.

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device.

It consists mainly of an **Inverting input** denoted by a negative sign, **("-")** and the other a **Non-inverting input** denoted by a positive sign **("+")** in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.

An operational amplifier is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.

A basic op-amp consists of 4 main blocks:

a. Current Mirror

b. Differential Amplifier

c. Level shift, differential to single ended gain stage

d. Output buffer

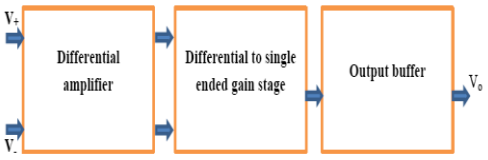

Fig.1 General Structure of op-amp

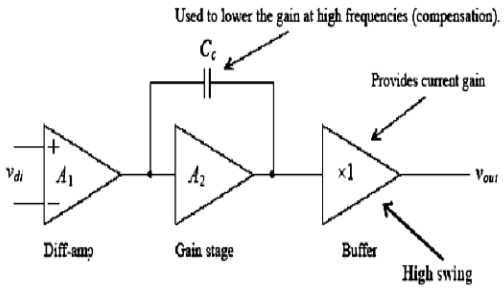

Fig. 2 Functional Block Diagram of two stage opamp

In above figures, The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single ended converter. The third block is the output buffer. The output buffer may sometimes be omitted to form a high output resistance un-buffered op-amp often referred to as Operational trans conductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).

CMOS Operational Amplifier is one of the most versatile and important building blocks in analog circuit design. Based upon the value of their output resistance they are being classified into two categories:

1.*Unbuffered Operational Amplifier***:** These are Operational Transconductance Amplifiers (OTA), which have high output resistance.

2. *Buffered Operational Amplifier*: These are Voltage Operational Amplifiers, which have low output resistance. Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer – function is practically independent of the gain of the opamp. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feedback concept.

CMOS op-amps are very similar in architecture to their bipolar counterparts.

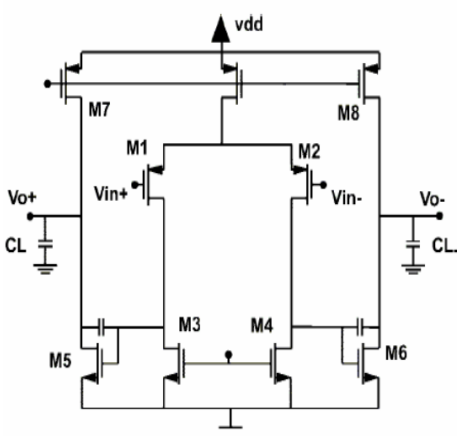

Fig. 3 A Typical Two Stage Amplifier

	Gain	Output Swing	Speed	Power dissipation	Noise
Telescopic	Medium	Low	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-boosted	High	Medium	Medium	High	Medium

Fig. 4 A Comparison of Multistage Architectures

The Two Stage op-amp shown in fig 3 is widely used because of its structure and robustness.

Our aim is to create the physical design and fabricate a low power Op-amp .An ideal op-amp having a single-ended out is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.

II. DESIGNING OF TWO STAGE CMOS OPAMP

The designed op-amp has been simulated to find the different characteristics of the designed op-amp. The total design performed in Cadence tool. Different test benches have been created and extracted design has been then simulated with the parasitic values and compared with the schematic. Later in the chapter we also have compared the obtained parameters of the device through simulation to the specifications for the device.

Design Issues

Typical specs	Design factors
! DC Gain (Av)	Frequency Response
! Unity Gain Bandwidth	Phase Margin
! Power Dissipation	Load Capacitance
! Slew Rate	Compensation
! Input Offset Voltage	Device Dimensions
! PSRR	
! Output Voltage Swing	
! ICMR	
! CMRR	

Steps in designing a CMOS OP AMP:

- Choosing or creating the basic structure of the op amp.
- Decide on a suitable configuration determination of the type of compensation needed for meeting the specification
- Selection of the dc currents and transistor sizes.
- Physical implementation of the design.
- Fabrication
- Measurement

The design process involves the two major steps, the first is the conception of design ,and second one is optimization of design . The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the

intuitive view point necessary for choices that must be made. Second step is to take the "first-cut" design and verify and optimize it. This is normally done by using Computer simulation and can include such influences as environmental or process variations.

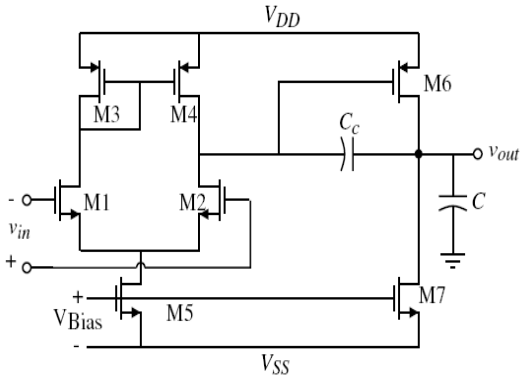

Fig.5 Unbuffered two stage CMOS OPAMP

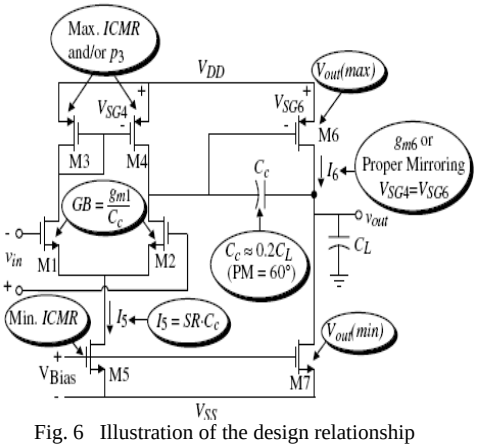

Fig. 6 Illustration of the design relationship and the ckt for a two stage OPAMP

This design procedure assumes that the gain at dc (Av), unity gain bandwidth (GB), input common mode range (Vin(min) and Vin(max)), load capacitance (CL), slew rate (SR), settling time (Ts), output voltage swing (Vout(max) and Vout(min)), and power dissipation (Pdiss) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, have to choose the minimum value for *Cc*, i.e. for a 60° phase margin we use the following relationship. This assumes that

z>=10*GB.*

$$Cc >= 0.22C_L \quad (1)$$

2. Determine the minimum value for the "tail current" (I_5) from

$$I_5 = SR \cdot Cc$$

Now , Tail Current (Iss/I5) can also be found by

$$2\Pi f_{T=} \; {}^{2I_{SS}}/_{(V_{GS}-V_{TH})} \; {}^{1}/_{C_L} \quad (2)$$

where Iss is the Tail Current

3. Design for S_5 from the minimum input voltage. First calculate *VDS*5 (sat) then find S_5.

$$V_{DS5(SAT)} = V_{IN(MIN)} - V_{SS} - \sqrt{{}^{I_5}/_{\beta 1}} - V_{T1\,(MAX)} \geq 100\text{mv}$$

$$S_5 = \frac{2I_5}{K'_5[V_{DS5\,(SAT)}]2} \quad (3)$$

4. Have to find S_6 by letting the second pole (*p*2) be equal to 2.2 times GB and assuming that

$$VSG_4 = VSG_6. \quad (4)$$

If VSG4 = VSG6, then then I6= $(S6|S4)I4$

For balance, I6 must equal I7 = $({}^{S6}/_{S7}) = ({}^{2S7}/_{S4})$, Called the "Balance Conditions"

First stage gain Av1= $g_{m1}/(g_{ds2} + g_{ds4}) = {}^{2g_{m1}}/_{I_5(\lambda 2 + \lambda 4))}$

Second Stage gain Av2 = $g_{m6}/(g_{ds6}+g_{ds7})$ = $g_{m6}/I_6(\lambda 6+\lambda 7)$

g_{m6} = 2.2 $g_{m2}\left(C_L/C_C\right)$ and S6 = S4$\left(g_{m6}/g_{m4}\right)$ (5)

5. I6 = $\frac{gm6^2}{2K'_6 S_6}$ (6)

and Power Dissipation

$$P_{diss} = (I_5 + I_6)(V_{DD} + V_{SS}) \quad (7)$$

There are three roots of importance:

Right Half Plane Zero (RHP zero) $z_1 = g_{m6}/C_c$

This root is very undesirable- it boosts the magnitude while decreasing the phase Dominant left-half plane pole (the Miller pole) $p_1 = -(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})/g_{m6}C_c$ This root accomplishes the desired compensation

Left-half plane output pole $p_{2=-}\, g_{m6}/C_L$ (8)

This pole must be ≥unity-gain bandwidth or the phase margin will not be satisfied

60 Degree phase Mergin Requires $g_{m6} = 2.2 g_{m2}\left(\frac{C_L}{C_0}\right)$

two stage OPAMP is designed for 180 nm technology for the following specifications :-

TABLE I DESIGN SPECIFICATION

Open loop Gain	100 V/V (40 dB)
Gain B/W at -3 db gain ,(f_{3db})	5 MHz
Load Capacitance (CL)	10 pf
Slew Rate	10 V/Us
Mirror Pole kept at	>=10*GB*.
Maximum Power Dissipation	≤ 2mw
Phase Margin Φ_m	$\geq 60°$
Channel Length	180 nm
CMRR	$\geq 60\ dB$
PSRR	$\geq 60\ dB$
Power Supply	2.5 Volt

Model or Device Parameters :

$K'_n = \left(\mu_n C_{OX}/2\right)$ = 177.2 μA/V^2

V_{tn} = 0.35 V

λ_n = 0.09 /V

$K'_P = \left(\mu_P\, C_{OX}/2\right)$ = - 35.6 μA/V^2

V_{tp} = - 0.39 V
λ_P = 0.1/V

III .EXPERIMENTAL RESULTS

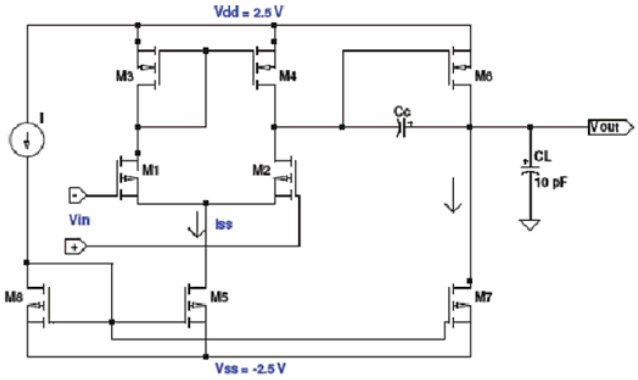

Fig. 7 Circuit Configuration for a two-stage op amp with an channel input pair

TABLE II CHANNEL WIDTH FOR MOS TRANSISTOR DESIGNED FOR 180 nm TECHNOLOGY OPAMP

MOS transistor	Aspect Ratio (W/L)	Channel width (µm)
M1	8	1.44
M2	8	1.44
M3	4	0.72
M4	4	0.72
M5	1	.4
M6	40	7.20
M7	8	1.44

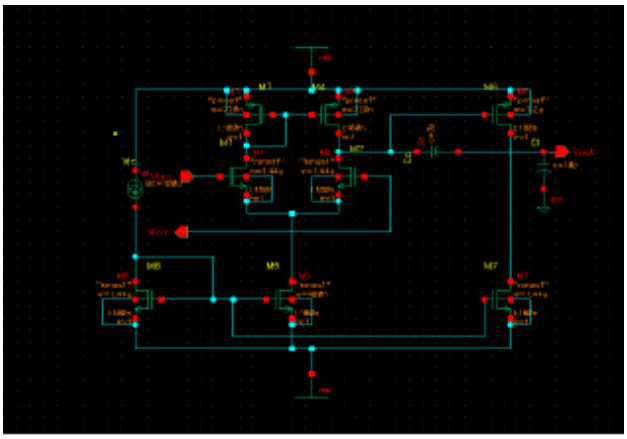

Fig. 8 Schematic configuration of two stage OPAMP

Frequency response

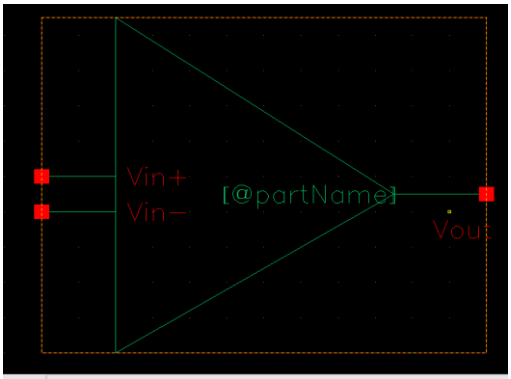

Fig. 9 Symbolic representation of schematic model

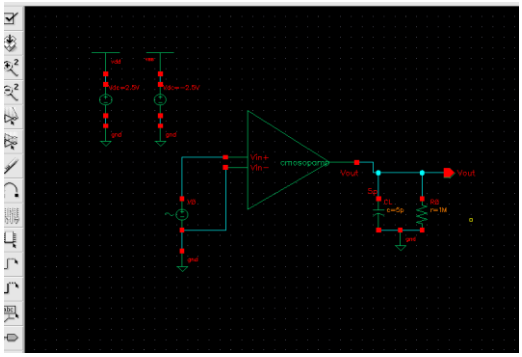

Fig. 10. Frequency response test-bench

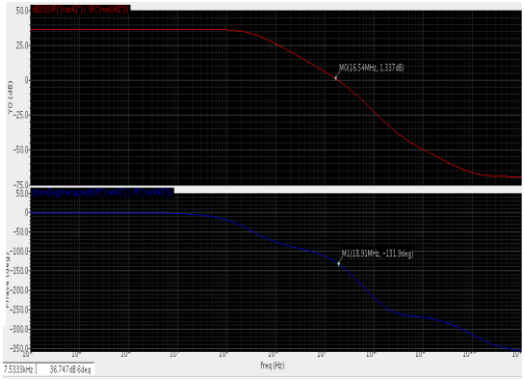

Fig.11 Frequency response simulation result

From above fig we can found that the gain bandwidth is 16.54 MHz (the unity gain frequency, 0dB) The Corresponding phase margin for a 5pF load we can find out as 48.1.° at a frequency of 18.9 MHz. Phase Margin = (180° +Φ) = 180 – 131.9 $^{\circ}$ =48.1 $^{\circ}$ The open-loop voltage gain is36.747dB

Slew rate

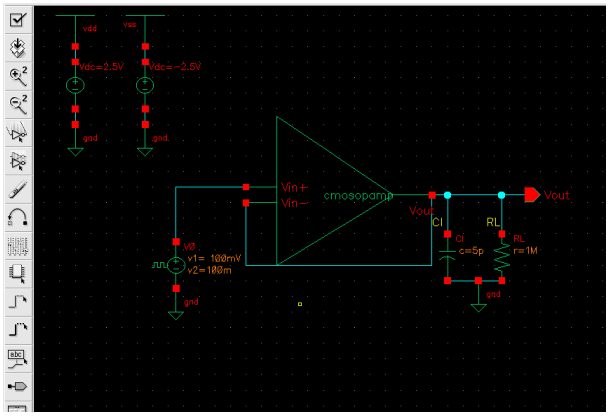

Fig. 12 Slew rate test-bench

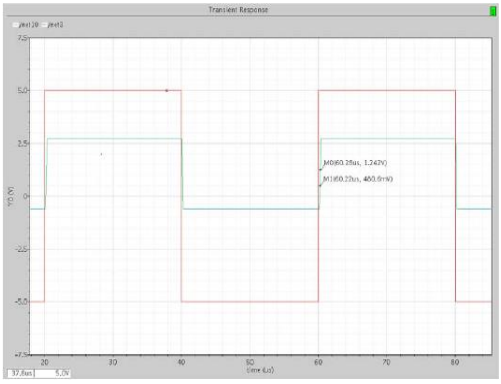

Fig. 13 Slew rate simulation result

Slew rate (SR) = $V_2 - V_1 / T_2 - T_1$ From figure we can find the value is 12.5 V/μ S

CMRR

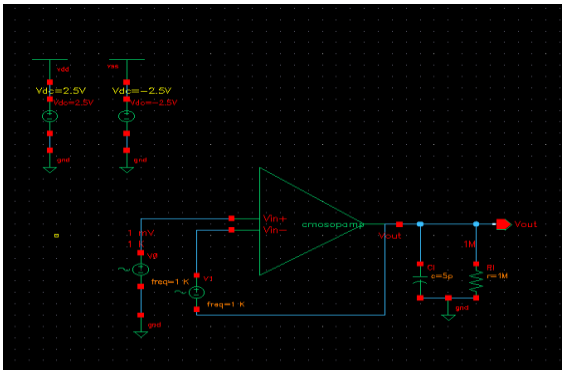

Fig. 14 CMRR test bench

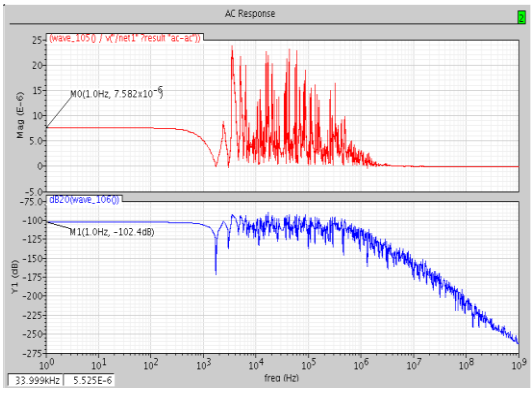

Fig 15 CMRR SIMULATION result

The CMRR can be calculated as

CMRR= $20log_{10} {A_{V,DIFF}}/{A_{V,CM}}$,Where $A_{V,DIFF}$ = Differential Gain

From simulation CMRR can be calculated as, $20\ log_{10} {36.747}/{7.582.10^{-6}}$=$20\ log_{10}$ (4.84× 10^6)

= 133.69 dB

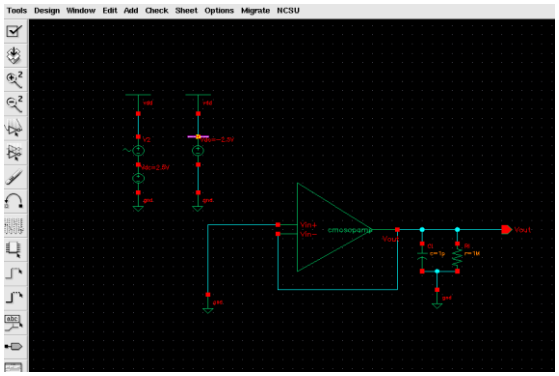

Fig.16 PSRR test bench

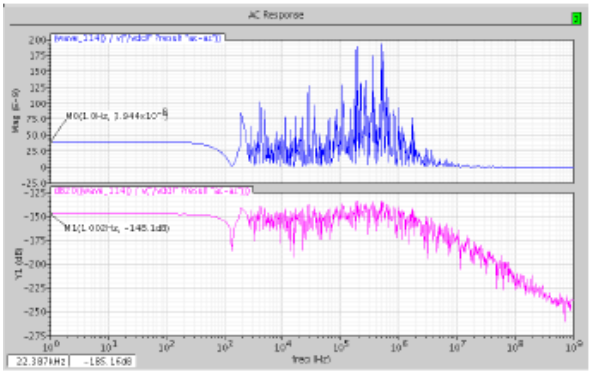

Fig. 17 PSRR SIMULATION result

PSRR = $\left({\Delta V_{DD}}/{\Delta V_{OUT}}\right) A_V = \frac{{V_0}/{V_{IN}}\,(V_{DD}=0)}{{V_0}/{V_{DD}}\,(V_{IN}=0)}$ from simulation result PSRR

= $20log_{10} {A_{V,DIFF}}/{A_{V,PS}}$ = $20\ log_{10}\left({36.747}/{3.94.10^{-8}}\right)$ = $20log_{10}\ (9.32 \times 10^8)$=179.38 dB

Power dissipation:

The power dissipation of this op-amp is calculated as 0.804 mW. using the SPECTRE simulator, have to set up a DC analysis. The power is calculated as the power dissipated by the VDD source. To calculate the power in cadence we simulated the circuit and saved the DC operating points and calculated the power as the product of the total current drawn from the VDD DC voltage source and the total DC potential across the circuit.(VDD + |VSS|) Here we have taken the parameters as VDD = 2.5 V V_{PULSE} = 0 to 2.5 V, pulse width=5us, period = 10us.

TABLE III COMPARISON BETWEEN THEORITICAL AND SIMULATION RESULT

Specification	**Actual Value**	**Simulated Value**
Open loop gain	40 dB	36.747 dB
Gain Bandwidth	➢ 5MHz	16.54 MHz
Phase Margin	60Degree	48.1Degree
Cut off frequency		7.33 KHz
Slew Rate	➢ 10 V/uS	12.5 V/uS
CMRR	➢ 60 dB	133.69 dB
PSRR	➢ 60 dB	179.38 dB
Power dissipation	< 2mW	.804 mW

Compensation Capacitance	2.2 pf	3pf

IV. CONCLUSION

The objective of this work was to implement the full custom design of low voltage and low power operational amplifier**.** In this paper a well-defined method for the design of a two-stage CMOS operational amplifier has been presented. The design has been made through the scaling of device parameters, as it is known that, by maintaining the scaling factor to a minimum value can reduce the current, power consumption and area as well. Now an OPAMP has been described in its negative feedback Configuration, as it can provide a moderate gain as compare to the open loop, but the problem is this case is the stability, which can be reduced by using the compensation techniques. In this thesis Miller Compensation technique is implemented, where this simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage.

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