A New Low Power Symmetric Folded Cascode Amplifier by Recycling Current in 65nm CMOS Technology

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Abstract

A new low power symmetric folded cascode amplifier is presented. The proposed amplifier delivers the same performance as that of the conventional symmetric folded cascode amplifier while consuming only 50% the power. This is achieved by recycling the bias current of idle devices, which results in an enhanced transconductance, gain and slew rate. The proposed amplifier was implemented in SMIC standard 65nm CMOS process. Simulation results show that the proposed amplifier achieves almost twice the bandwidth (313.4MHz versus 158.2MHz), 8.2dB DC gain enhancement (63.4dB versus 55.2dB) and better than twice the slew rate (45.6V/us versus 20.5V/us) compared to the conventional symmetric folded cascode amplifier with the same power. On the other hand, the power consumption of the proposed amplifier can reduce 50% compared to the conventional symmetric folded cascode amplifier with the same performance.

1. Introduction

The operational transconductance amplifier (OTA) is a vital analog building block and for many applications is the largest and most power consuming block. In deep submicron technology, in order to achieve completely symmetric slew rate and high DC gain, the symmetric folded cascode amplifier (SFC) [1], as shown in Figure 1, is widely used. However, the SFC usually consumes more power than other amplifiers because of the cross-connected devices (P5, P8, N11 and P9, P11, N9) between the inverting and non-inverting side of the amplifier, providing the required inverting current mirror operation [2]. Thus it becomes important for the conventional SFC to reduce the power budgets for more and more low power applications [3] [4].

In this paper, a modification to the conventional SFC aims to reduce its power consumption by recycling the bias current of idle transistors (N6 and N8). Additonally, this is achieved at no expense in performance.

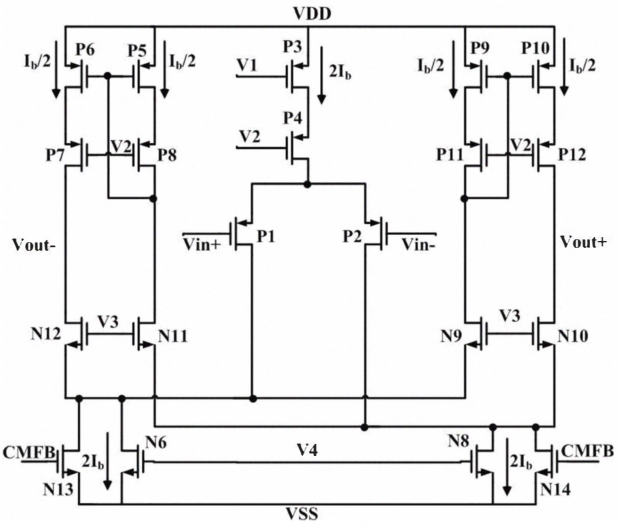

Figure 1. Conventional SFC

This paper is organized as follows. Section II describes the principle and the architecture of the proposed amplifier. Section III presents simulation and results. Section IV concludes the paper along with the performance summary.

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2. Improved Symmetric Folded Cascode Amplifier

The conventional SFC is shown in Figure 1. Transistors N6 and N8 conduct the most current, but only act as current sinks, providing a folding node for the small signal current generated by the input drivers. To address this inefficiency, an improved symmetric folded cascode amplifier (ISFC) to enhance performance over that of the SFC is presented as following.

The newly proposed structure is shown in Figure 2, which intends to use N6 and N8 as driving transistors. First, P1 and P2 in Fig.1 were split in half to produce P1a(b) and P2a(b) in Fig.2, respectively. Next, the diode connected pair N5 and N7 in Fig. 2 is used to make a cross-over and drive N6 and N8, such that the small signal currents added at the sources of N9, N12 and N10, N11 are in phase. Finally, the ratio of the current mirror N6:N5 and N8:N7 is K:1. Additonally, in order to maintain the same DC current as that of the SFC, the current mirror factor K in Fig.2 is chosen to three.

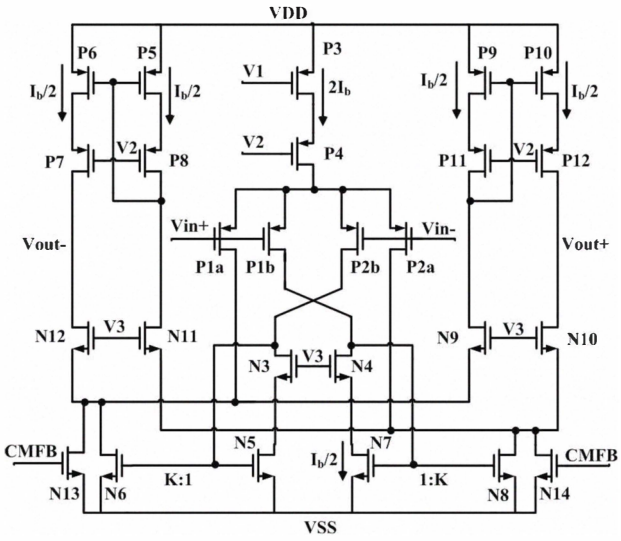


Figure 2. The Proposed ISFC

A. Small Signal Transconductance

For the small signal transconductance, if taking into account that the width of P1 and P2 are twice that of P1a(b) and P2a(b), the equivalent transconductance (G_m) of the SFC can be expressed in equation (1). However, for the ISFC, as the small signal current of P1b and P2b is amplified by K times, the G_m of the newly proposed ISFC is K+1 times that of P1a(b) and P2a(b), expressed in equation (2).

$$G_{mSFC} = 2g_{m1a} \quad (1)$$

$$G_{mISFC} = (K+1)g_{m1a} \quad (2)$$

As a result, with the same power, K=3, the proposed ISFC has almost twice the GBW as that of the SFC. That is to say, the ISFC can achieve the same GBW with only half the power.

B. Low Frequency Gain

Moreover, since the transconductance of the ISFC is twice that of the SFC, a 6dB gain enhancement will be achieved for the same output impedance. However, the output impedance (R_{out}) is also enhanced, which is due to the increased output impedance of P1a, P2a, N6 and N8, conducting less current than that of the SFC. The expressions for R_{outSFC} and $R_{outISFC}$ are represented by equation (3) and (4), respectively.

$$R_{outSFC}=(g_{mP7}r_{dsP7}r_{dsP6})//(g_{mN12}r_{dsN12}(r_{dsP1}//r_{dsN6}//r_{MN9}) \quad (3)$$

$$R_{outISFC}=(g_{mP7}r_{dsP7}r_{dsP6})//(g_{mN12}r_{dsN12}(r_{dsP1a}//r_{dsN6*}//r_{MN9}) \quad (4)$$

Therefore, an overall gain enhancement can be obtained in the ISFC. This added gain has two fundamental benefits. First, static settling errors are reduced because of the increased gain. Second, the power supply rejection ratio (PSRR) performance of the ISFC is improved over its SFC counterpart.

C. Slew Rate

The slew rate is also improved in the ISFC. When a large signal is applied as an input, assuming a load C_L, the slew rate of the SFC can be expressed in (5).

For the ISFC, suppose Vin+ goes high, it follows that P1a and P1b turn off, which forces N7 and N8 to turn off. Consequently, the drain voltage of N8 rises and N10 and N11 are turned off whereas P2a is driven to shut off. This directs the tail current, $2I_b$, into P2b and then is mirrored by a factor K into N6. The current in N6

is consequently split equally into N9 and N12. While half of current in N6 flows into the inverting output through N12, the other half current flows into N9 and consequently into the non-inverting output by the current mirror of P9, P10, P11 and P12.

As a result, the inverting and non-inverting outputs exhibit the symmetric slew rate, which can be described by equation (6).

$$SR_{SFC} = I_b/C_L \quad (5)$$

$$SR_{ISFC} = KI_b/C_L \quad (6)$$

In an actual design, although the devices could not be fully turned off, the slew rate enhancement is still greater than two for K=3.

3. Implementation and Results

The improvements of performance seen in the ISFC are critical when power is of concern. Since the ISFC is capable of delivering twice the transconductance, higher DC gain and better slew rate compared to the SFC for equal power budgets, then it is capable of delivering a similar performance to the SFC for less power.

To validate the theoretical results, three amplifiers (SFC, ISFC1 and ISFC2) were designed in SMIC 65nm CMOS process using a supply voltage of 1.2V. The proposed ISFC1 is biased at the same DC current of the SFC and the ISFC2 has the half DC current of the SFC.

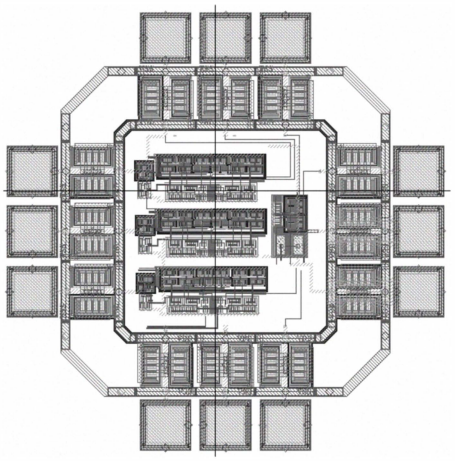


Figure 3. Layout of SFC, ISFC1 and ISFC2

Also, they had the same common-mode feedback circuit (CMFB). Fig.3 shows the layout of the three amplifiers and the biasing circuit.

The three amplifiers were used as a unity gain capacitive amplifier, as seen in Figure 4, driving a total capacitive load of 5pF (C1=1pF, C2=2.5pF). The simulated open-loop AC response is shown in Figure 5, and the simulated transient response to 10MHz 100mVpp step input is shown in Figure 6. The simulation comparison results of key parameters of the three amplifiers are listed in Table 1.

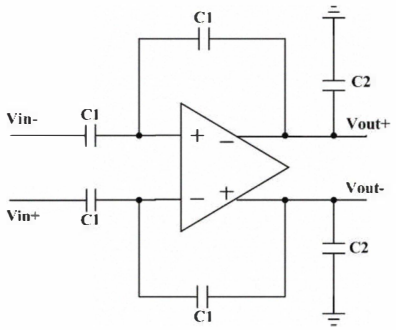
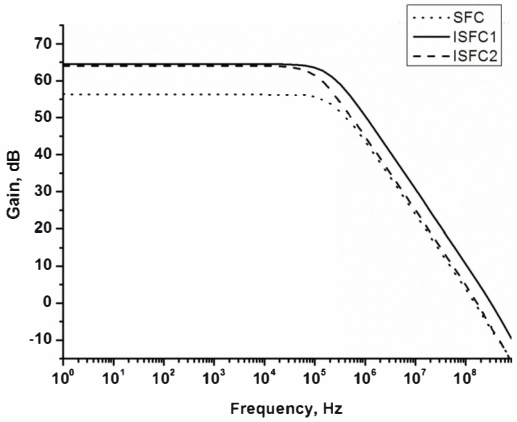
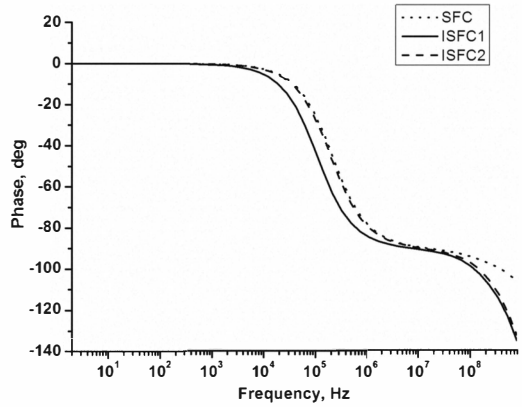


Figure 4. Unity gain capacitive amplifier

Note that the GBW of the SFC, ISFC1 and ISFC2 is 158.2MHz, 313.4MHz and 160.3MHz respectively, which demonstrates the enhanced transconductance of the ISFC. As for the phase margin, the slight degradation in the ISFC is due to the pole-zero pair of current mirror.



(a) Gain



(b) Phase

Figure 5. AC response of SFC, ISFC1 and ISFC2 (a) Gain (b) Phase

The DC gain value is 55.2dB for SFC, 63.4dB for ISFC1 and 62.7dB for ISFC2. The enhanced gain of the ISFC1 over the SFC is still apparent and within the expected range of 8dB. Since the ISFC2 uses less overall current, the output conductance of the transistors is smaller, and that is reflected in an increased DC gain.

The average slew rate of the SFC, ISFC1 and ISFC2 is 20.5V/us, 45.6V/us, and 24.3V/us respectively. The ISFC1 has a clearly improved slew rate over the SFC. Also, the settling time improvement in the ISFC1 is due to the higher GBW.

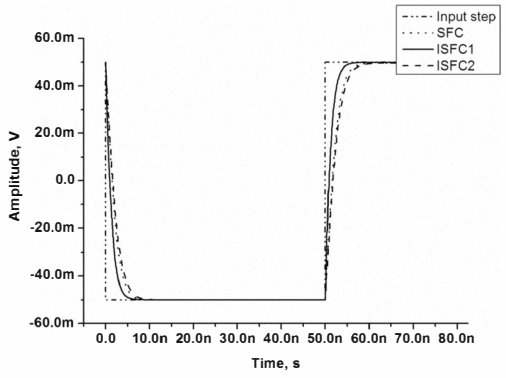


Figure 6. Transient response of SFC, ISFC1 and ISFC2 to differential 10MHz, 100mVpp step

Table 1. Performance results summary

Parameter	SFC	ISFC1	ISFC2
Power (uA)	402	402	201
Supply Voltage (V)	1.2	1.2	1.2
CL (pF)	5	5	5
Gain (dB)	55.2	63.4	62.7
GBW(MHz)	158.2	313.4	160.3
Phase margin (deg)	84.1	71.9	78.3
1%Setting time (ns)	8.3	4.2	8.1
Slew rate [average] (V/us)	20.5	45.6	24.3

4. Conclusion

An improved symmetric folded cascode amplifier was proposed to reduce power budget without sacrificing performance. Simulation results show that the ISFC can achieve the same performance with only 50% the power consumption of the conventional SFC.

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