An Enhanced Folded Cascode Op-Amp in 0.18 µm CMOS Process with 67dB Dc-Gain

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***Abstract*— In this paper a new method is used to increase the dc-gain of the Folded Cascode op-amp (FCO). This method does not limit the range of the output voltage swing, bandwidth, phase margin of FCO.**

I. INTRODUCTION

Speed and accuracy are two of the most important properties of analog circuits, however, optimizing circuits for both aspects leads to contradictory demands. In high performance analog integrated circuits, such as pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as CMOS design scales into low-power, low-voltage and short-channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more and more difficult, since the intrinsic gain of the devices is limited. The high gain requirements leads to multistage designs with long channel devices biased at low current levels, where as the high unity-gain frequency requirements calls for a single stage design with short channel devices biased at high bias current levels. There have been several circuit approaches to circumvent this problem. It is well known that active cascode gain-boosting technique can be used to increase the dc gain of an operational amplifier without degrading its high frequency performance [1]. Unfortunately, the existence of pole-zero doublet will unfavorably affect the settling performance of the gain-boosted op amp [1] and the effort of pushing up the doublet can raise stability problem [2]. Also, in Correlated Double Sampling (CDS) [3] and Correlated Level Shifting (CLS) [4] methods, two clock cycles are needed to amplify, so the speed may be reduced. The new structure proposed in this paper is based on the conventional Folded Cascode amplifier. To increase the dc-gain of the op-amp a new method is presented that uses positive feedback concept. Opposite to conventional techniques this technique does not add extra nodes to the the structure of the op-amp or pole-zero doublet to the transfer function of the op-amp. So applying the proposed technique to the conventional FCO does not increase the settling time of the op-amp in the closed loop configuration. Also the output voltage swing of the proposed op-amp remains equal with that of the conventional FCO.

II. PROPOSED STRUCTURE

To achieve higher dc-gain in the simple FCO, positive feedback method can be used. Fig.1 shows the complete structure of the proposed op-amp. *Mf0-Mf2* devices form a positive feedback loop. The common mode feedback and bias circuits are not shown for simplicity.

A. Differential DC-Gain :

As we can see, the total current injected to the output node is approximately as:

$$i_{out} = (Gm_{in} \times V_{in}) + (Gm_f \times V_{out}) \quad (1)$$

Where Gmin is the transconductance of input differential pair (*M1, M2*) and Gmf is the transconductance of the bulk-driven differential pair of the positive feedback block (PFB).

Output voltage can be calculated as:

$$V_{out} = R_{out} \times i_{out} \quad (2)$$

$$V_{out} = R_{out} \times (G_{m_{in}} \times V_{in} + G_{mf} \times V_{out}) \quad (3)$$

The differential dc-gain of this op-amp can be written as:

$$Av_0 = \frac{V_{out}}{V_{in}} \approx -\frac{Gm_{in} \times R_{out}}{K} \quad (4)$$

$$K = 1 - (G_{mf} \times R_{out}) \quad (5)$$

$$R_{out} = R_{out1} \| R_{out2} \quad (6)$$

$$R_{out1} \approx g_{mM_{7,8}} \times r_{oM_{7,8}} \times r_{oM_{9,10}}$$

$$R_{out2} \approx g_{mM_{5,6}} \times r_{oM_{5,6}} \times (r_{oMf_{1,2}} \| r_{oM_{1,2}} \| r_{oM_{3,4}})$$

It is clear that by reducing K the total value of A_{v0} will increase. A_{v0} can be controlled by choosing appropriate sizes for *Mf0-Mf2*. However, K cannot take a value very close to zero, because it might take a negative value because of process variations, so

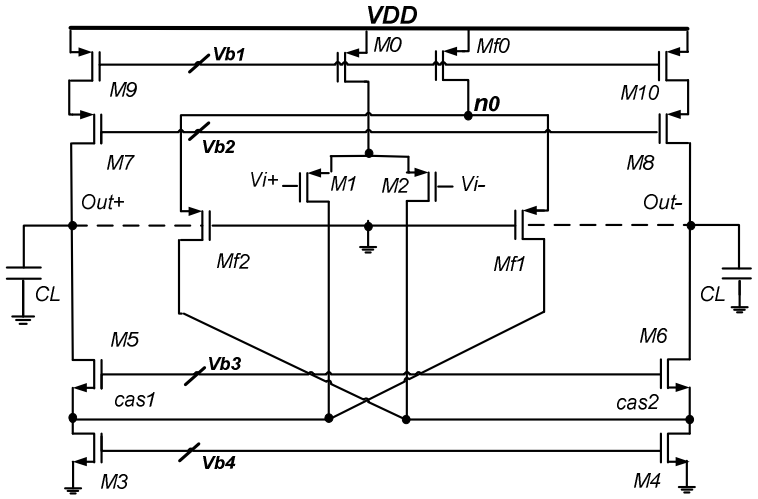

Fig.1. proposed op-amp

before fabrication, the proposed op-amp, must be tested in the corners of fabrication process. It is considerable that in the proposed amplifier , PFB does not limit the output swing range of FCO and output voltage can increase to *Vdd - 2Vds,sat* which is limited by PMOS cascode devices in FCO, not PFB devices. In the opposite side the output voltage can decrease to *2Vds,sat* which is limited by overdrive voltage of NMOS devices of FCO, not PFB devices. It is considerable that the source-well junction of *Mf1,2* device is biased backward in the mentioned output swing range. Since highest possible voltage at the sources of *Mf1* and *Mf2* is *|Vthp|+Vds,sat*, hence maximum voltage difference of Vn_0–*Vout+* (or Vn_0-*Vout-*) becomes *|Vthp|+Vds,sat-2Vds,sat* which is less than 0.25volt in the designed structure. Thus the source-well junctions of *Mf1* and *Mf2* never turn on, and can never restrict output swing compared to a conventional FCO.

B. Frequency Response

The proposed op-amp has many poles and zeros, but two first poles or zeros are important in the frequency response of the op-amp. The output voltage of the proposed op-amp can be estimated as:

$$V_{out} = \frac{((G_{m_{in}} \times V_{in}) + (G_{mf} \times V_{out}))}{(1+\frac{s}{p_2})} \times \frac{R_{out}}{(1+\frac{s}{p_1})} \tag{7}$$

P1 is the first pole of the FCO which occurs in the output node of the FCO and *P2* is the second pole of the FCO which occurs in the cascode node. P_{f1} is the first pole of the proposed op-amp which occurs in the output node of the proposed op-amp and P_{f2} is the second pole of the proposed op-amp which occurs in the cascode node (*cas1,2*).

P1 and *P2* are:

$$P_1 = -\frac{1}{R_{out} \times C_{out}} \qquad P_2 = -\frac{1}{R_{cas} \times C_{cas}} \tag{8}$$

$$C_{out} = C_L + C_{dM_{5,6}} + C_{dM_{7,8}} + C_{bM_{f1,2}} \tag{9}$$

And R_{out} is calculated in Eq.6.

$$R_{cas} \approx r_{oM_{1,2}} \left\| r_{oM_{3,4}} \right\| \frac{1}{g_{mM_{5,6}}} \left\| r_{oMf_{1,2}} \right\| r_{oM_{5,6}} \tag{10}$$

$$C_{cas} = C_{dM_{1,2}} + C_{dM_{3,4}} + C_{sM_{5,6}} + C_{dMf1,2} \tag{11}$$

From Eq.7 we can write:

$$Av_f(s) = \frac{V_{out}}{V_{in}}(s) = \frac{-(Gm_{in} \times R_{out})}{(1+\frac{s}{p_1}).(1+\frac{s}{p_2}) - (G_{mf}.R_{out})} \approx$$

$$\frac{\frac{-Gm_{in} \times R_{out}}{(1-(G_{mf}.R_{out}))}}{(1+\frac{s}{(1-(G_{mf}.R_{out})).p_1}).(1+\frac{s}{p_2})} = \frac{\frac{-Gm_{in} \times R_{out}}{K}}{(1+\frac{s}{K.p_1}).(1+\frac{s}{p_2})} \tag{12}$$

$$Av_f(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_{v0}}{(1+\frac{s}{P_{f1}})(1+\frac{s}{P_{f2}})} \tag{13}$$

So as mentioned before the dc-gain is:

$$Av_0 = \frac{-Gm_{in} \times R_{out}}{(1-(G_{mf}.R_{out}))} = \frac{-Gm_{in} \times R_{out}}{K} \tag{14}$$

Where $-Gm_{in} \times R_{out}$ is the dc-gain of FCO. P_{f1} the first pole which occurs in the output node of the proposed op-amp is:

$$P_{f1} = K \times P_1 = -\frac{K}{R_{out} \times C_{out}} \tag{15}$$

And second pole is:

$$P_{f2} = P_2 = -\frac{1}{R_{cas} \times C_{cas}} \tag{16}$$

Hence the total transfer function of the op-amp can be estimated as:

$$Av(s) \approx \frac{\frac{-Gm_{in} \times R_{out}}{K}}{(1+\frac{s}{K.p_1}).(1+\frac{s}{p_2})} \tag{17}$$

It is clear that the second pole is not affected by additional devices (*Mf1, Mf2*) to a great extent. The Unity gain bandwidth (UGBW) of FCO is:

$$\omega_{u1} = P_1 \times A_{v0} = P_1 \times Gm_{in} \times R_{out} \tag{18}$$

Also UGBW of the proposed op-amp is:

$$\omega_{u2} = P_{f1} \times Av_{f0} = K_1.P_1 \times \frac{Gm_{in} \times R_{out}}{K_1} = \omega_{u1} \tag{19}$$

So the UGBW of the proposed op-amp is equal with the UGBW of the FCO.

C. Common Mode Gain:

In the common mode state, the proposed positive feedback structure decreases the common mode gain of the op-amp opposite to the differential mode, because the positive feedback loop converts to a negative feedback loop. For this reason, common mode gain of the proposed op-amp is slightly less than common mode gain of the FCO. In addition, in the proposed structure the positive feedback structure has a negative feedback role for the output common mode voltage. So the PFB helps the common mode feedback circuit to stabilize the output common mode voltage.

D. Speed:

In the conventional designs (e.g. [1]), some extra node are added to the topology of the op-amp. Also it is clear that introducing additional nodes to the op-amp structure introduces extra poles to the transfer function of the op-amp which increases the settling time of the op-amp in the close loop configuration. Also in [1] introduced pole-zero doublet causes a reduction in the speed of the op-amp in the closed loop configuration. In the proposed op-amp in this paper positive feedback devices do not add any additional node to the FCO topology and pole to the transfer function of the FCO. Furthermore in this design there is not any pole–zero doublet, so opposite to [1] the settling time of the proposed op-amp is not increased in comparison with FCO.

III. Simulation Results :

In this section, the simulation results of the proposed op-amp are shown and the characteristics of proposed op-amp are compared with the conventional FCO. Both the proposed and the conventional FCO, have been designed in a typical 0.18µm CMOS process (Vdd=1.8v) with the same capacitor load and the same power consumption and are simulated by HSPICE software using *level* 49 parameters (BSIM3v3). The closed loop configuration shown in Fig.2 is used to test the step response of both op-amps. AC simulation result of the proposed and FCO is shown in Fig.3. Proposed op-amp has a UGBW of 920MHz with 67° phase margin. As demonstrated in Fig.3, the proposed op-amp achieves a dc-gain of more than 67dB which is 30 dB greater than the dc-gain of the conventional FCO in the approximately same power consumption. Step response of designed op-amps is shown in Fig4. As shown in Fig4 the proposed op-amp has the accuracy of more than 10 bit; but the conventional FCO has the accuracy of less than 6bit in the same output voltage swing and in the approximately same power consumption. Monte-Carlo simulation results for a 20mv variation in the threshold voltage of all of the devices used in the proposed Op-Amp is shown in Fig.5 Also for a 0.5 *Vp–p* input step voltage in the closed loop unity gain configuration of Fig.2, FS and SF corners do not have a significant change in the results compared to TT corner. Settling time of the proposed Op-Amp is increased 15% in SS corner. Accuracy of the proposed op-amp in the closed loop configuration degrades just 1 bit only in FF corner. Finally the characteristics of the designed op-amps are summarized in Table1 for comparison.

Table 1: Specifications of the conventional and proposed op -amps

Parameters	**Folded Cascode**	**Proposed**
Process (µm)	0.18	0.18
Open loop dc-gain	37 dB	67 dB
Phase margin	≈67°	≈ 67°
Power consumption	≈ 3.8 mW	≈ 3.9 mW
UGBW(CL=0.5pF)	≈ 920 MHz	≈ 920 MHz
Maximum swing of Output voltage	$V_{DD} - 4V_{DSsat}$	$V_{DD} - 4V_{DSsat}$

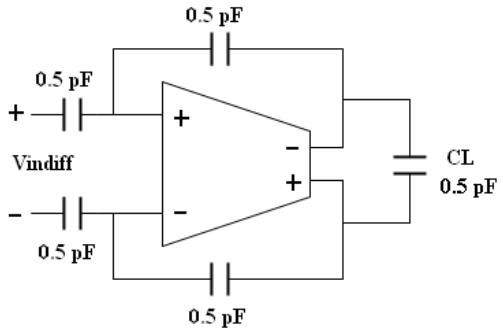

Fig2. Closed loop configuration

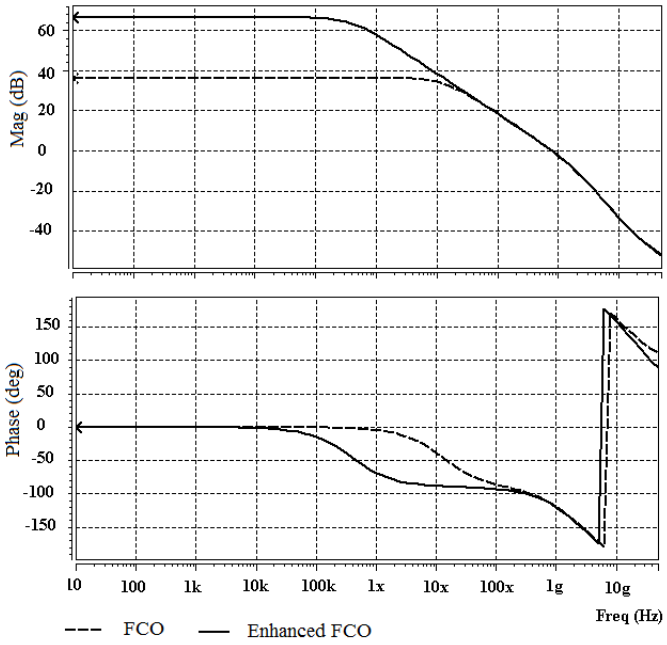

Fig. 3. Frequency response of the Op-Amps

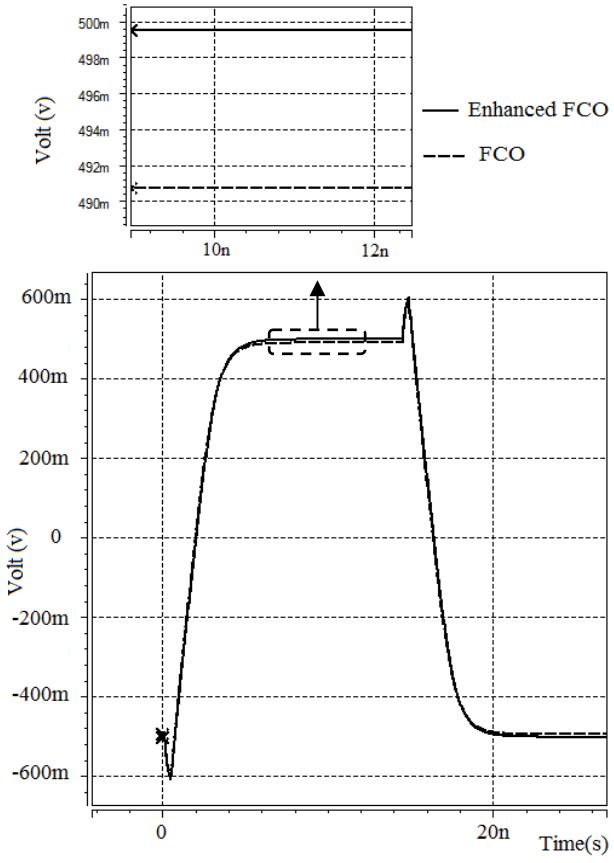

Fig.4 Step response comparison

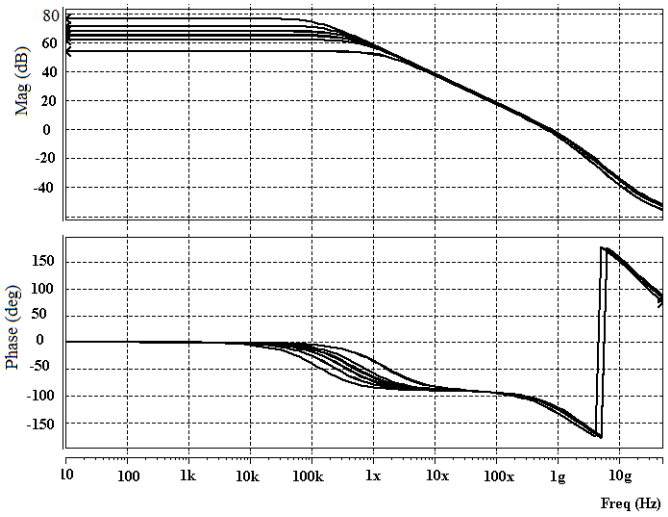

Fig.5 Monte-Carlo simulation for 20mv variation in threshold voltages

IV. CONCLUSION

In this paper, a new op-amp is presented which uses positive feedback and bulk amplification concepts in the conventional FCO to increase the dc-gain of the op-amp. Also by using the presented method without any reduction in the bandwidth the dc-gain of the FCO increases more than 30db. Hspice simulations confirm the theoretical estimated improvements.

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