A Novel Voltage Reference With An Improved Folded Cascode Current Mirror OpAmp Dedicated for Energy Harvesting Application

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Abstract — In this paper, a CMOS ultra-low voltage reference circuit with ultra-low power consumption of 220nW is proposed. The circuit, simulated in 65nm standard CMOS process technology, operates with a supply voltage of 1V. It is based on sub-threshold MOSFETs using the technique of compensating a PTAT-based variable with the gate source voltage of a sub-threshold MOSFET. The novelty of circuit is the use of an improved folded cascode current mirror op-amp operating directly from a 1V power supply. The resulting voltage is equal to the extrapolated threshold voltage of a MOSFET at absolute zero temperature, which was about 435mV for the MOSFETs used. The proposed circuit achieves an average temperature coefficient of 30ppm/°C, 12ppm/V in line regulation for a supply voltage range of 0.6-1.2V, and a power supply rejection ratio (PSRR) of -38dB at 100Hz. The overall power consumption is only 220nW.

I. INTRODUCTION

For the past few years, there has been intensive research carried out in the field of bio-energy harvesting as seen by the recent increase in research publication. The rationale is that it is suitable to be used for portable mobile devices and wireless sensor networks [1, 2]. Voltage reference circuit is one of the most important building blocks for the power management system embedded in a bio-energy harvesting device. Its objective is to generate a temperature compensated, regulated reference voltage [1, 2]. Hence, there is a huge demand to develop an ultra-low power voltage reference circuit yielding a reference voltage of about 0.5V, dedicated for bio-energy harvesting device.

Voltage mode approach entails the use of a bandgap voltage reference with vertical bipolar transistor which can be implemented in a CMOS process. This yields a minimum reference voltage of about 1.25V and therefore requires a minimum supply voltage of 1.4V. Recent research studies involving the use of resistive subdivision methods, known as current mode approach [5], can overcome the design challenge faced above. However, the tradeoff is the use of large value resistors which increase the silicon area overhead. The above tradeoff is evident that conventional bandgap reference circuit is not ideally suitable for ultra-low power application.

Hence, voltage reference circuits based on sub-threshold MOSFETs are proposed [3-4, 6-8]. However, these circuits suffer from a poor line regulation and temperature variation.

In this paper, a new voltage reference circuit is implemented based on the sub-threshold MOSFETs with an improved line regulation and eliminate the use of resistors. Furthermore, an improved folded cascode current mirror is implemented to enhance the line sensitivity and power consumption. The temperature compensated reference voltage yields a value of 435mV which has minimal variation to temperature and supply voltage variation.

The organization of this paper is organized as follows: Section II will discuss the theoretical calculation of the proposed voltage reference circuit. Section III will present the experiment results and give a detailed discussion on its temperature variation performance, line regulation and PSRR. Lastly, section IV will conclude our research work.

II. PROPOSED VOLTAGE REFERENCE CIRCUIT

A. MOSFET in the Subthreshold region

The I-V characteristic of an NMOS transistor in the sub-threshold region has an exponential relationship and given by:

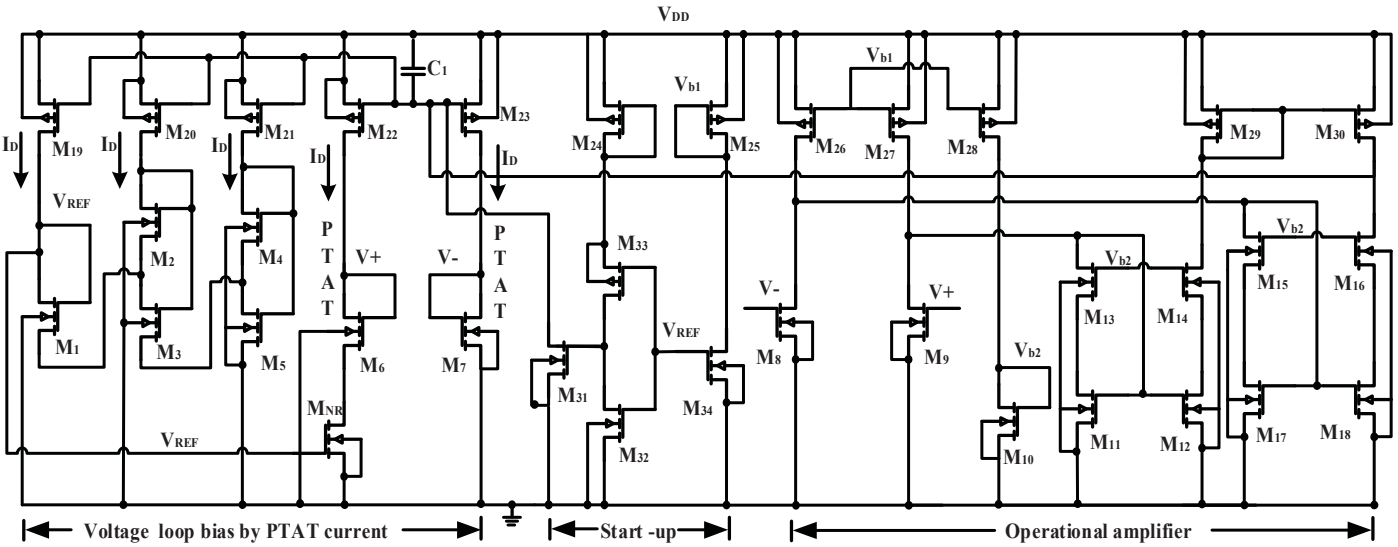

Figure 1. Schematic Level of Proposed Voltage Reference

$$I_D = \mu C_{ox} U_T^{\,2} S \exp\left(\frac{V_{GS}-V_{TH}}{mU_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{U_T}\right)\right) \quad (1)$$

where S is the aspect ratio of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, $U_T = \pi r^2 (k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature and q is the electron charge. V_{TH} is the threshold voltage of MOSFET and m is the sub-threshold slope factor (For V_{DS}>0.1V), the current I_D is almost independent of V_{DS} and is given by:

$$I_D = \mu C_{ox} U_T^{\,2} S \exp\left(\frac{V_{GS}-V_{TH}}{mU_T}\right) \quad (2)$$

$$V_{GS} = mU_T \ln\frac{I_D}{\mu C_{ox} U_T^2 S} + V_{TH} \quad (3)$$

B. Description of Proposed Voltage Reference

The structure of the voltage reference circuit is presented in Fig. 1. All the MOSFETs except for M_{NR} are operated in the sub-threshold region. In addition, the MOS resistor M_{NR} is operated in the deep triode region.

Voltage loop formed by gate source voltage of transistors gives the output voltage of voltage reference circuit hence can be expressed as:

$$V_{REF} = V_{GS5} + V_{GS3} + V_{GS1} - V_{GS4} - V_{GS2} \quad (4)$$

From (2) and (3) the reference voltage can be expressed as:

$$V_{REF} = V_{TH} + mU_T \ln\left(\frac{3I_D}{\mu C_{ox} U_T^2 S_5}\right) + mU_T \ln\left(\frac{2S_4 S_2}{S_3 S_1}\right) \quad (5)$$

Each branch of the voltage loop is biased with same current I_D and this current is defined by the MOS M_{NR} operated in deep triode region. It is also controlled by the output voltage $V_{REF,}$ given that:

$$I_{PTAT} = I_D = S_{NR}\mu C_{OX}(V_{REF} - V_{TH})\, mU_T \ln\left(\frac{S_7}{S_6}\right) \quad (6)$$

Moreover, this is the PTAT current. We assume that the mismatch between the threshold voltages of transistors can be ignored. Approximately, the threshold voltage V_{TH} decreases linearly with temperature:

$$V_{TH}(T) = V_{TH}(T_o) - \varkappa T \quad (7)$$

Where $V_{TH}(T_o)$ is the sub-threshold voltage at 0 K which is temperature independent and $\varkappa$ is the temperature coefficient of V_{TH}. Hence, from (5) and (6), we arrive at:

$$V_{REF} = V_{TH}(T_o) - \varkappa T + mU_T \ln\left\{\frac{6mS_R S_4 S_2 (V_{REF}-V_{TH})}{S_5 S_3 S_1 (m-1) U_T} \times \ln\left(\frac{S_7}{S_6}\right)\right\} \quad (8)$$

Differentiating equation (8) with temperature, we can arrive at the temperature derivative of V_{REF} shown in (9). Assume that $V_{REF} - V_{TH}(T_o) \ll \varkappa T$ and $mU_T \ll \varkappa T$. Therefore, a temperature compensated voltage reference can be obtained by setting the aspect ratios S_i in accordance with (8). Hence, it can be derived that: $V_{REF} = V_{TH}(T_o)$.

$$\frac{\partial V_{REF}}{\partial T} = -\varkappa + \frac{mk_B}{q}\ln\left[\left\{\frac{6mS_R S_4 S_2 (V_{REF}-V_{TH})}{S_5 S_3 S_1 (m-1) U_T}\ln\left(\frac{S_7}{S_6}\right)\right\} + mU_T\left\{\frac{1}{(V_{REF}-V_{TH})}\left(\frac{\partial V_{REF}}{\partial T} + \varkappa\right) - \frac{1}{T}\right\}\right] \quad (9)$$

C. *Operational Amplifier*

Voltage reference circuit has an operational amplifier (OPA) to increase the power supply rejection ratio so that it will reduce the line sensitivity of the circuit. An improved folded cascode current mirror op-amp is implemented as shown in Fig. 1. The bias current is a replica of the current in the voltage reference circuit. Hence, the currents in the input stage of OPA do not need to control its operation. The bias voltage, $V_{b1,}$ is generated within the startup circuit. The signal current generated by the input differential pair is folded and collected by two cascode current mirrors which increased the output impedance to make it more resilient to power supply ripples.

Since the input gain stage is fully symmetrical, its systematic offset and that of the second stage of push-pull circuit are practically zero. This allows excellent power supply and common-mode rejection ratios. The bias current in the operational amplifier matches the current flowing in the voltage reference circuit, which in turn is designed to be ultra-low. However, since the bias current of circuit has a PTAT feature, power consumption will increase proportionally to the absolute temperature. The compensation capacitance C_1 ensures the stability of the whole voltage reference circuit under any operating conditions.

III. SIMULATION RESULTS AND DISCUSSION

The proposed circuit was simulated using Global Foundries 65nm standard CMOS process technology. The simulation results were shown in the following figures.

In Fig 2, the output voltage V_{REF} versus V_{DD} shows that the proposed voltage reference circuit starts working properly with V_{DD}=0.5V. In addition, Fig.2 also shows that the line sensitivity is 12 ppm/V with a supply voltage range from 0.6-1.3V. Fig. 3 shows the output voltage V_{REF} dependence on the temperature for different values of the supply voltage. The measured temperature coefficient at V_{DD}=1V is 30 ppm/°C.

The current drawn from supply voltage as a function of temperature at 1V is measured shown in Fig 5. This shows that the supply current is 220nA at 27°C and its power consumption is 220nW. In Fig.4, the PSRR at room temperature, with a 1pF capacitor, is -38dB at 100Hz and starts to degrade after this frequency.

Table I summaries the measurement results of this work in comparison with [3,4,6]. From the comparison, the proposed voltage reference circuit achieves the lowest power consumption and temperature coefficient of 220nW and 30ppm/°C respectively. Furthermore, this is achieved at a minimal trade-off with line sensitivity, PSRR and silicon area overhead.

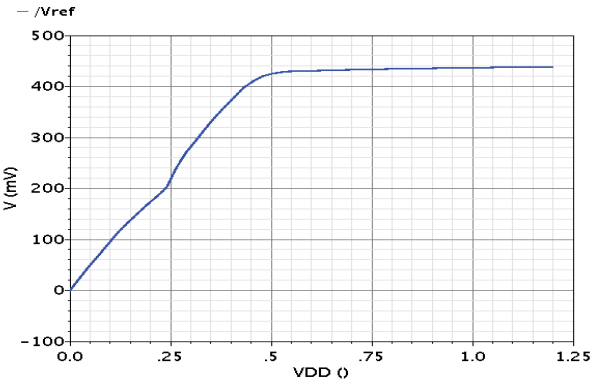

Figure 2. Measured V_{REF} with Supply Voltage

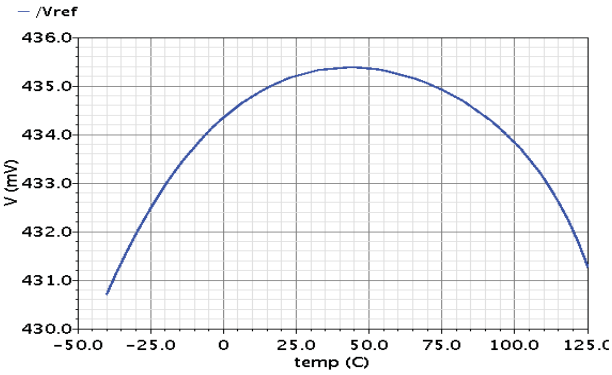

Figure 3. Measured V_{REF} with Temperature

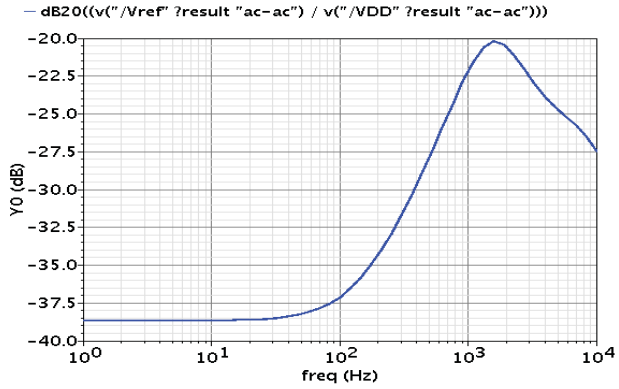

Figure 4. Power Supply Rejection Ratio (PSRR)

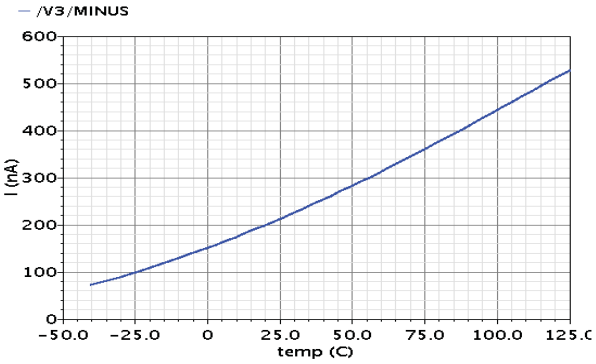

Figure 5. Supply Current with Temperature under 1V supply

TABLE I COMPARISON WITH PAST VOLTAGE REFERENCES

	VLSIC [3]	JSSC [4]	JSSC [6]	**This Work**
Tech [nm]	130	130	130	65
V_{DD} [V]	0.7 - 1.8	> 0.75	0.7 - 1.8	0.6 - 1.2
V_{REF} [mV]	501	256	548	435
Temp Range [°C]	-50 to 130	-20 to 85	-40 to 120	-40 to 125
TC [ppm/°C]	29.3	40.0	114.0	**30.0**
Line Sensitivity [ppm/V]	337.0	50.0	16.1	12.0
PSRR [dB] @100 Hz	-	-	-56	-38
Power [nW]	210	170	52	**220**
Die Area [mm^2]	0.023	0.070	0.0246	0.024

IV. CONCLUSION

In this brief, a novel 65nm CMOS ultra-low voltage reference circuit with a temperature coefficient of 30ppm/°C and an ultra-low power consumption of 220nW is proposed and implemented. Furthermore, it yields a line regulation of 12ppm/V with a supply voltage ranging from 0.6V to 1.2V. This is possible with the use of an improved folded cascode current mirror op-amp.

REFERENCES

[1] E. J. Carlson, *et al.*, "A 20 mV Input Boost Converter With Efficient Digital Control for Thermoelectric Energy Harvesting," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 741-750, 2010.

[2] C. Himes, *et al.*, "Ultralow Voltage Nanoelectronics Powered Directly, and Solely, From a Tree," *Nanotechnology, IEEE Transactions on,* vol. 9, pp. 2-5, 2010.

[3] L. Junghyup and C. SeongHwan, "A 210 nW 29.3 ppm/ºC 0.7 V voltage reference with a temperature range of -50 to 130 ºC in 0.13 um CMOS," in *VLSI Circuits (VLSIC), 2011 Symposium on*, 2011, pp. 278-279.

[4] V. Ivanov, *et al.*, "An Ultra Low Power Bandgap Operational at Supply From 0.75 V," *Solid-State Circuits, IEEE Journal of,* vol. 47, pp. 1515-1523, 2012.

[5] L. Ka Nang and P. K. T. Mok, "A CMOS voltage reference based on weighted difference of gate-source voltages between PMOS and NMOS transistors for low dropout regulators," in *Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th European*, 2001, pp. 61-64.

[6] Y. Osaki, *et al.*, "1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs," *Solid-State Circuits, IEEE Journal of,* vol. 48, pp. 1530-1538, 2013.

[7] C. Popa, "A new curvature-corrected voltage reference based on the weight difference of gate-source voltages for subthreshold-operated MOS transistors," in *Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on*, 2003, pp. 585-588 vol.2.

[8] G. Giustolisi, *et al.*, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 151-154, 2003.