A 116-dB CMOS Op Amp with Repetitive Gain Boosting and Subthreshold Operation

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***Abstract*—This work proposes a simple high-gain single-stage op amp design that operates at low power (~100 µW) and low voltage (±1 V) without severely sacrificing unity gain frequency and slew rate. Simulation results that demonstrate the performance of this design are also presented.**

Keywords—op amp, high open-loop gain, low power, low voltage, repetitive gain boosting technique, subthreshold operation.

I. INTRODUCTION

Designing high-performance analog circuits is becoming incrementally challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifiers that are widely used in various analog systems and VLSI systems [1], [2]. Although multi-stage amplifiers can achieve very high gain, it suffers from enhanced noise, slow speed and poor stability [3]. The unity gain frequency (UGF) is subjected to the trade-off between power consumption and performance.

This paper proposes a low-voltage low-power CMOS op amp design to remarkably enhance the open-loop gain other than multi-stage structure without influencing other features, such as UGF and slew rate (SR). Section II introduces the employed technology and presents the circuit implementation. Section III addresses the simulation results of the amplifier and section IV presents the conclusion.

II. PROPOSED CIRCUIT

A. Repetitive Gain Boosting Technique

Differing from the multi-stage method, the open-looped gain can be increased by gain boosting technique which uses an auxiliary amplifier to form negative feedback and enhance the output impedance of a cascode stage [3]. When a cascode stage is used to be the auxiliary amplifier, gain boosting technique can also be applied to this stage. In this way, an *N*-stage auxiliary amplifier can be implemented and can further enhance the gain [4]. The transfer function of a cascode stage with an *N*-stage auxiliary amplifier is

$$A(s) = \frac{A_0 \prod_{k=1}^{N} A_k}{1 + s g_{m2} r_{o1} r_{o2} C_0 \prod_{k=1}^{N} A_k} \qquad (1)$$

where A_0 is the gain of the cascode stage, A_k is the gain of the k^{th} stage of the auxiliary amplifier, C_0 is the loading capacitance and $g_{m2} r_{o1} r_{o2}$ is original output impedance of the cascode stage. The gain has been exponentially boosted while the UGF remains unchanged (g_{m1}/C_0).

B. Subthreshold Operation

The impedance of a transistor is inversely proportional to the drain-to-source current I_D [3] and it can be increased by applying lower gate-to-source voltage V_{GS} which results in smaller I_D. For a transistor in the saturation region, a continuously decaying V_{GS} will drive this device to the linear region and finally to the subthreshold region, which causes huge increase in output impedance. The transconductance of a transistor in the subthreshold region is given by

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{q}{nkT} I_D \qquad (2)$$

where n is a nonlinearity factor, and (2) suggests that the transconductance to drain current ratio is maximized in subthreshold operation since there is no square root effect on I_D that exists in the saturation mode [5]. While the voltage gain of a cascode stage with both transistors in the saturation region is less than the maximum value [5], a properly designed stage in the subthreshold region can approach the maxima by enhancing the output impedance and providing an optimized g_m.

C. Circuit Implementation

Fig. 1 shows the implementation of the proposed design based on a conventional telescopic amplifier, where A_1 and A_2 are the two *N*-stage cascode auxiliary amplifiers that boost the open-loop gain of the telescopic amplifier. Instead of applying the subthreshold operation to the main amplifier which results in smaller g_m (hence lower UGF) and lower I_{TAIL} (hence lower SR), this work employs the subthreshold operation in repetitive cascode gain boosting stages. The idea is to increase the gain of the cascode stages in A_1 and A_2 by the subthreshold operation so that they can provide higher gain than normal auxiliary amplifiers while the power consumption only increases slightly since the current across the two auxiliary amplifiers is small.

Fig. 2 gives the configuration of the auxiliary amplifier. In order to increase the drain-to-source impedance of M_{A1} to M_{AN}, i.e. r_{dsA1} to r_{dsAN}, and thus the overall gain, the aspect ratio of devices M_{A1} to M_{AN} is much smaller than that of M_{B1} to M_{BN}, which enables M_{A1} to M_{AN} to operate in the saturation region at low current. Although g_{mAN} decreases with decreasing drain current, this decline is lower than the increase in r_{dsAN} [6]. For the N^{th} stage, the gate voltage of M_{AN} is V_{GN} and the bias voltage of M_{BN} is $V_{GSBN} = V_{GN} - V_{DSAN}$ which greatly falls off due to significantly aggrandized V_{DSAN} caused by large r_{dsAN}.

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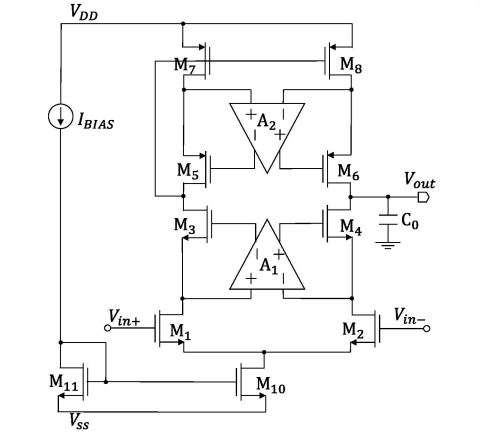

Figure 1. Telescopic op amp with gain boosting

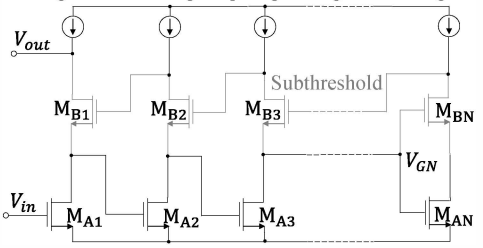

Figure 2. Repetitive gain boosting stages employing subthreshold operation

Consequently, M_{B1} to M_{BN} enter the subthreshold region and therefore provide more gain while requiring little current.

Fig. 3 gives the complete implementation of the proposed circuit based on the concepts of Fig. 1 and Fig. 2, in which the configurations of A_1 and A_2 are shown. The current sources are replaced by cascode loads. In this design, only 2 cascode stages are used in the auxiliary amplifiers since the gain has already reached the maximum value. All devices operate in the saturation region except M_1 to M_{16} which have larger aspect ratio than the other transistors in the two auxiliary amplifiers.

III. Simulation Results

Both proposed op amp and conventional telescopic amplifier without auxiliary amplifiers are simulated at I_{BIAS} = 14 µA and load capacitance = 10 pF. Detailed results of performance are summarized in Table I. Compared with the conventional telescopic amplifier, the slew rate of the proposed op amp is SR_+ = 2.85 V/µs and SR_- = 3.88 V/µs and it is quite close to the conventional one and so is the UGF. The power consumption is 11.85 µW higher. Since the conventional one has an open-loop gain of only 36.31 dB, it is found that each additional stage in the subsidiary amplifiers only increases the power dissipation by 5.93 µW in exchange for an extra gain of 41.77 dB without sacrificing either the UGF or the SR. The performance is also better than that in [7].

IV. Conclusion

In this paper, an op amp design adopting gain boosting technique and subthreshold operation has been proposed. Due to the property of subthreshold operation, it greatly enhances the open-loop gain at the expense of very little increase in power consumption. If needed, the number of gain boosting stages can be more and results in even higher open-loop gain.

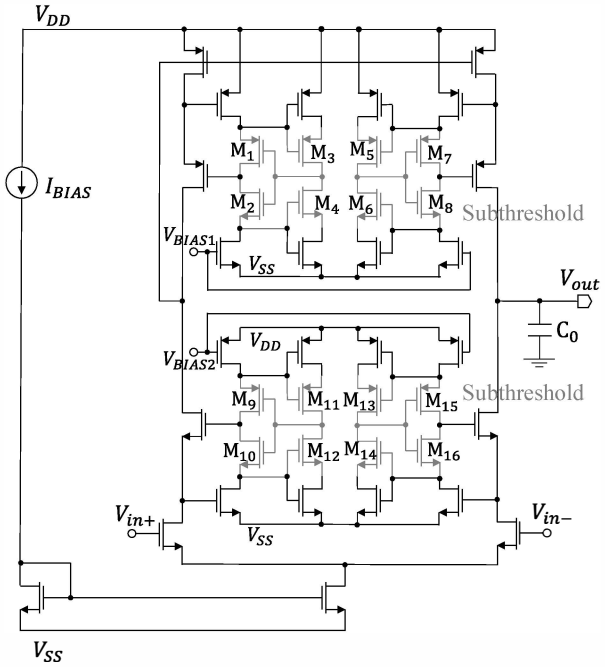

Figure 3. Circuit diagram of the proposed op amp using repetitive gain boosting and subthreshold operation

TABLE I. Summary of Circuit Performance

	Conventional Telescopic	Reference [7]	Proposed
Open-loop Gain	36.31 dB	62-69 dB	116.48 dB
UGF	4.0 MHz	2.0 MHz	5.6 MHz
Supply Voltage	±1 V	1 V	±1 V
Load Capacitance	10 pF	20 pF	10 pF
Phase Margin	90º	57º	90º
Slew Rate	+2.29 V/µs -3.85 V/µs	0.5 V/µs	+2.85 V/µs -3.88 V/µs
Power Dissipation	121.10 µW	N/A	132.95 µW

Moreover, the proposed methodology can be adopted to other op amp designs without causing performance degradation.

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