A High-Voltage-Enabled Recycling Folded Cascode OpAmp for Nanoscale CMOS Technologies

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Abstract

This paper describes a high-voltage-enabling circuit technique for enhancing the gain precision and linearity of OpAmp-based analog circuits. Without resorting from specialized devices, a 2xV_{DD}-enabled recycling folded cascode (RFC) OpAmp optimized in 1V GP 65-nm CMOS achieves, when compared with its 1xV_{DD} counterpart, 25-dB higher open-loop DC gain and 30-dB higher IM3 (in closed loop), under a similar power budget. These joint improvements save the need of a 2nd stage in the OpAmp when high precision and high linearity are the priorities. A voltage-conscious bias scheme and gate-drain-source engineering ensure that all devices are consistently operated within the reliability limits.

I. Introduction

Rapid downscaling of CMOS has led to more compact and faster analog circuits but with deteriorated linearity and accuracy due to the associated low-voltage constraints. The value of the supply voltage (V_{DD}) predominantly defines the number of transistors that can be cascoded in an amplifier. Entered into the sub-1V nanoscale regime, the downsizing of threshold voltage (V_T) is decelerated due to variability, matching and leakage issues. Insufficient voltage headroom makes stacking of transistors no longer efficient. Cascading of transistors, on the other hand, demand more power and achieve lower operating speed. Innovative techniques befitting sub-1V nanoscale processes must be investigated in order to keep driving up circuit performances along with technology advancements.

Thus, instead of blindly tracking the downsizing of V_{DD} in technology scaling, V_{DD}-elevated analog circuits with *design for reliability* have emerged as a prospective circuit solution [1, 2]. An elevated V_{DD} directly opens up much more voltage headroom (Fig. 1), while maintaining the speed and area benefits of fine linewidth processes.

In this paper, a high-voltage-enabling circuit technique is proposed for realizing a 2xV_{DD}-enabled recycling folded cascode (RFC) OpAmp. Without resorting from a two-stage or multi-stage OpAmp, this new RFC OpAmp can offer sufficient open-loop gain to realize *high-precision* and *high-linearity* analog functions, when they are the priorities. The reliability of the circuit is ensured via voltage-conscious biasing and gate-drain-source engineering. It is worth to mention that the true value of 2xV_{DD} is within 2 V at nanoscale CMOS, when V_{DD} is roughly 1 V, which can be easily generated via a 3.6/3.7-V Li-ion battery in typical portable systems.

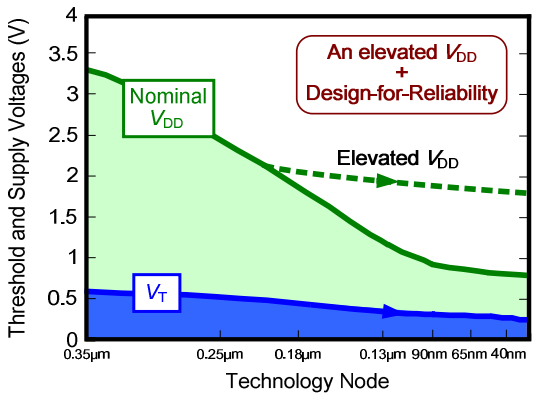


Fig. 1. Increase the design headroom via elevating the V_{DD} plus design for reliability [1, 2].

II. 1xV_{DD} and 2xV_{DD} RFC OpAmps

A. Typical RFC OpAmp

The single-stage RFC OpAmp [3] is shown in Fig. 2. It is selected as the basis of our 2xV_{DD} design for its high performances. The RFC OpAmp employs *M1b*, *M2b*, *M11*, *M12*, *M3b* and *M4b* to improve concurrently the gain and speed. By controlling the current mirror gain K, the small signal transconductance can be boosted, i.e., $g_{mRFC} = g_{m1a}(1 + K)$. Thus, under a fixed power budget, the RFC shows a higher gain-bandwidth product (GBW) than the conventional folded cascode (FC) structure. Furthermore, the RFC OpAmp also exhibits larger output resistance than its FC counterpart, leading to further gain enhancement.

B. 2xV_{DD}-Enabled RFC OpAmp with Design for Relaiblity

The proposed 2xV_{DD} RFC OpAmp is depicted in Fig. 3. The aim of doubling the supply is to enhance certain performance metrics that cannot be simply obtained by doubling the bias current at 1xV_{DD} under a similar power budget. By appropriately doing transistor stacking and biasing, the output resistance of the devices can be boosted while the voltage stress on them can also be shared to meet the reliability limits. For instance, under a 2xV_{DD}, *M0*' can be added to share the voltage stress on the current source *M0* and improve its output resistance, thereby the OpAmp's common-mode rejection ratio (CMRR). On the other hand,

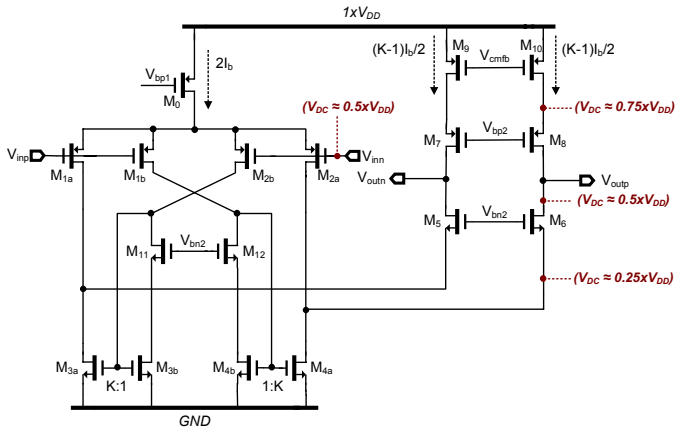


Fig. 2. Typical RFC OpAmp (1xV_{DD} design).

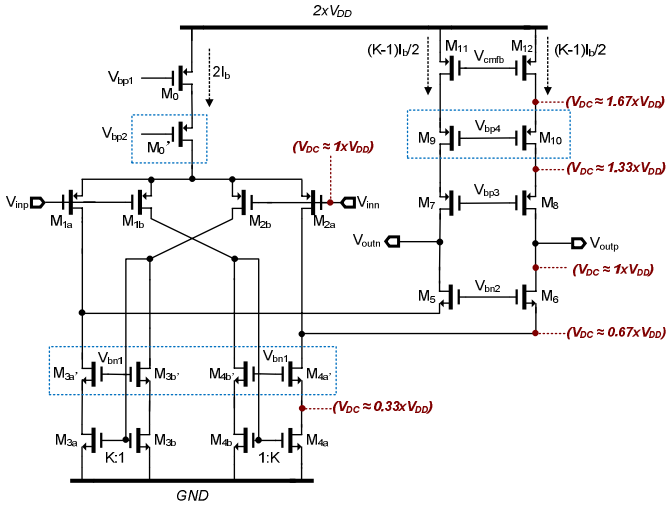


Fig. 3. Proposed 2xV_{DD}-enabled RFC OpAmp.

the current mirrors (*M3a*, *M3b*, *M4a*, *M4b*) are cascoded with (*M3a*', *M3b*', *M4a*', *M4b*'), whereas the current sources of the output stage (*M11*, *M12*) are cascoded with (*M9*, *M10*). Thus, the overall DC gain should be enhanced due to the boosted output resistance $R_{O,RFC\text{-}2V}$ by comparing it with the $R_{O,RFC\text{-}1V}$ given by the 1xV_{DD} RFC OpAmp:

$$R_{o,RFC-1V} \cong g_{m6} r_{ds6} (r_{ds2a} \,\|\, r_{ds4a}) \,\|\, (g_{m8} r_{ds8} r_{ds10}) \tag{1}$$

$$R_{o,RFC-2V} \cong g_{m6} r_{ds6} (r_{ds2a} \,\|\, g_{m4a'} r_{ds4a'} r_{ds4a}) \,\|\, (g_{m8} r_{ds8} g_{m10} r_{ds10} r_{ds12}) \tag{2}$$

The bias and common-mode feedback circuits (CMFB) are tailored to include extra cascode devices to ensure all node voltages are within the reliability limits as shown in Fig. 4.

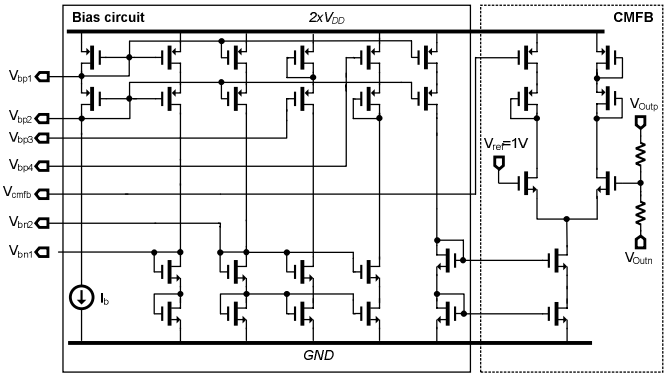


Fig. 4. Bias and CMFB circuits for the 2xV_{DD}-enabled RFC OpAmp.

III. Circuit Reliability Considerations

A 2xV_{DD} may generate reliability risk if inappropriately designed in a standard CMOS process. The key reliability issues are related with several effects that will limit the lifetime of MOSFETs. The technology design rule manual outlines the following most critical parameters: absolute maximum rating (AMR); hot carrier injection (HCI); electrostatic discharge (ESD); time dependent dielectric breakdown (TDDB); bias temperature instability (BTI) and punchthrough effect.

The AMR corresponds to the maximum voltage applied to a minimum-gate-length device with no unrecoverable hard failure. AMR is concerned mainly with the gate-oxide breakdown voltage as it is 3 to 4 times smaller than the junction breakdown voltage. A device biased close to the AMR limit may also lead to a deviation in device parameters, degrading the long-term reliability. The AMR is continuously reducing with the technologies, but mostly it is not the decisive breakdown limit.

Degradation of MOS device characteristics occurs as a result of exposure to a high V_{DS} with a large drain current. Examples of degradation are a shift of V_T and a shorter gate-

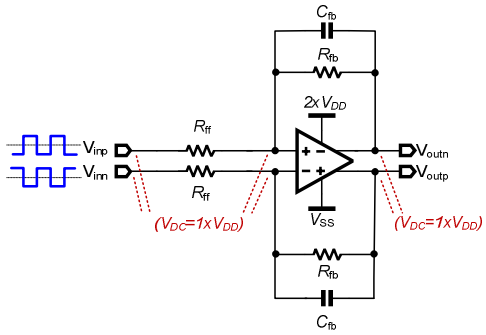


Fig. 5. 1st-order active-*RC* lowpass filter for assessing the performance and reliability of a 2xV_{DD}-enabled RFC OpAmp. The input and output dc-levels are 1xV_{DD} to maximize the signal swing and allow ease of cascading.

oxide breakdown lifetime. HCI normally happens in high-power circuits such as the power amplifier, where the worst HCI bias conditions: $V_{DS} \geqq V_{GS} \geqq V_T$ and $V_{DS} \geqq V_{DD}/2$ are concurrently satisfied. HCI degradation can be reduced by lowering the drain current or increasing the device channel length (*L*).

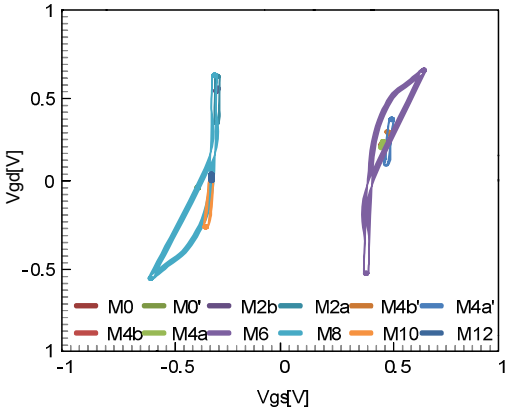


Fig. 6 V_{gs}-V_{gd} trajectories of all key devices when a square-wave input is applied with a signal swing of 1.2 V_{pp}.

TDDB is the wear-out of insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. In order to protect the circuit against TDDB the catastrophic destruction of gate oxides induced by the maximum DC gate oxide voltage at different temperatures must be considered. According to the maximum DC gate oxide voltages of 65-nm CMOS, NMOS has a higher voltage standing capability than PMOS for all cases to prevent TDDB. Thus, NMOS is preferable when considering TDDB in circuit design.

BTI degradation happens under steady-state conditions. It is design dependent in analog circuits and primarily only PMOS devices are subjected to BTI stress, namely negative BTI (NBTI). In a V_{DD}-upscaled design, analyzing NBTI involves detecting, in all modes of operation (DC and small signal), which PMOS device is exposed to a peak or rms voltage value exceeding the standard V_{DD}, which is around 1 V in 65-nm CMOS. Thus, NMOS is also preferred in terms of BTI.

Complying with all of them in the design indeed translates the term *design for reliability* into *voltage-conscious design*, highly simplifying the design and verification methodologies [4]. Furthermore, in the topology formation phase, their implications to the circuits can be easily justified in circuit simulations as presented next.

The test circuit for assessing the performances of the 2xV_{DD} RFC OpAmp is a 1st-order active-*RC* lowpass filter with unity gain, as shown in Fig. 5. To check the reliability of all devices inside the OpAmp, a large square-wave input at a common-mode voltage of 1 V is applied. Fig. 6 shows the V_{gs}-V_{gd} relationship at an input swing of 1.2 V_{pp}. Since the circuit is differential, we just show the half-circuit results. It can be observed that both V_{gs} and V_{gd} vary within the ±1-V boundary and the variation is indeed small. Next, the V_{ds} trajectory is checked. Fig. 7(a)-(c) show that the V_{ds}, in a period of square-wave input under an input swing of 1.2, 1.6 and 2 V_{pp}, respectively. When the input swing is 1.2 V, all V_{ds} are within the ±1-V boundary. When the input swing is enlarged, some of the V_{ds} exceed 1 V, reached 1.13 and 1.25 V for 1.6- and 2-V_{pp} inputs, respectively. According to

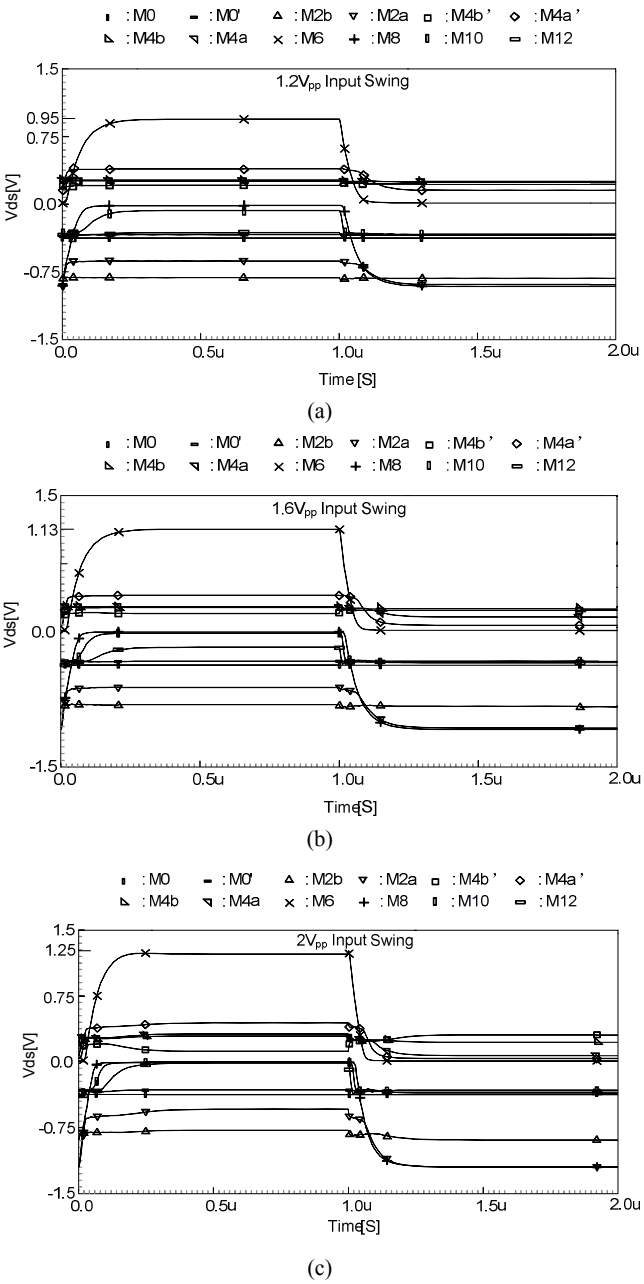
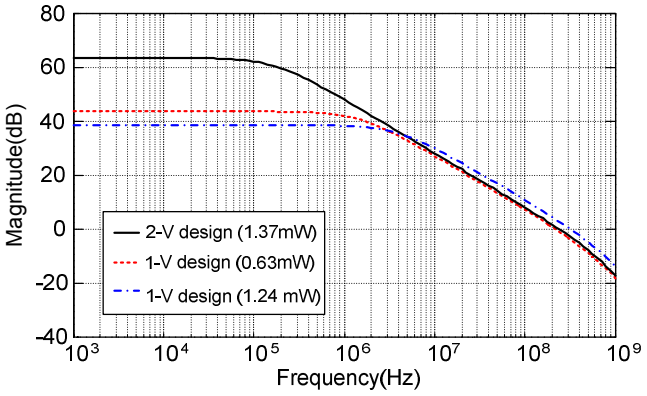


Fig. 7. V_{ds} variation versus time at an input swing of (a) 1.2 V, (b) 1.6 V and (c) 2 V. The notations correspond to Fig. 3. The maximum V_{ds} is within 0.95/1.13/1.25 V, respectively.

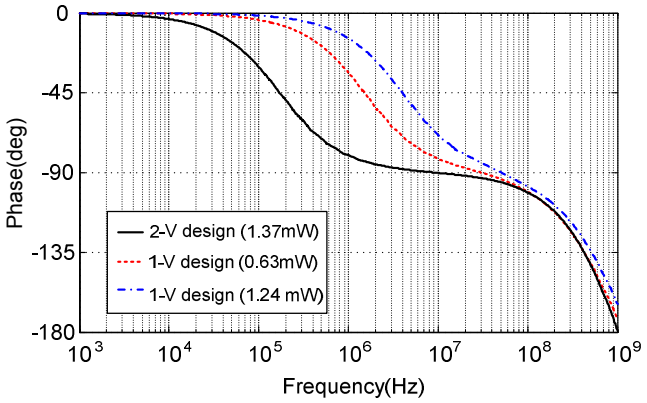
the liftime targets discussed in [5], V_{ds} > 1 V may still be acceptable for some applications.

IV. Simulation Results

In order to compare the performances between 1xV_{DD} and 2xV_{DD} RFC OpAmps fairly, two 1xV_{DD} RFC OpAmps are designed. The power budget of the 1-V RFC OpAmp #1 is roughly half of the 2xV_{DD} design, whereas the 1-V RFC OpAmp #2 consumes roughly the same power as the 2xV_{DD} one. Designed in a 65-nm CMOS process with 1-V GP



(a)



(b)

Fig. 8. (a) Gain and (b) phase responses of 1-V and 2-V RFC OpAmps.

transistors, the open-loop gain and phase responses are obtained as shown in Fig. 8(a) and (b), respectively. With similar power consumption, the 2xV_{DD} design attains 25-dB higher open-loop DC gain, reached 63.4 dB, which is adequate for building most analog functions. This benefit avoids the need of a 2nd stage that is highly necessary in the 1xV_{DD} designs due to their insufficient gain. The GBW of the 2xV_{DD} design, as expected, is less than that in the 1xV_{DD} design under a similar power budget, but is fairly adequate for most analog functions with signal bandwidth of less than 20 MHz. Table I summarizes their simulation results. In addition to the gain enhancement that can highly enhance the closed-loop gain precision, the 2xV_{DD} design also achieves 30-dB better intrinsic CMRR and IM3 comparing with its 1xV_{DD} counterpart after closed-loop use as a 1st-order active-*RC* filter (see Fig. 5). The values are $R_{ff} = R_{fb} = 10$ kΩ and $C_{fb} = 1.59$ pF for a cutoff frequency of 10 MHz. The IM3 test is obtained by injecting a 2-tone input at 5 and 6 MHz. These results reveal that the 2xV_{DD} OpAmp is more feasible in improving the gain precision, CMRR and linearity than its 1xV_{DD} counterpart in building analog baseband circuits.

V. Conclusions

A high-voltage-enabling circuit technique for enhancing the performance of RFC OpAmp in nanoscale CMOS is proposed. No specialized process option is entailed. The design example, under a 2-V supply in 65-nm CMOS process, achieves 25-dB higher open-loop DC gain and 30-dB better IM3 (in closed loop) than its 1xV_{DD} counterpart, avoiding the need of extra gain stages. These joint improvements cannot be simply achieved in a 1xV_{DD} design even with the same power budget, as there is inefficient voltage headroom. A high-voltage-enabled OpAmp, hence, appears as a perspective solution that can enhance the gain precision, CMRR and linearity of analog functions in nanoscale CMOS with no extra manufacturing cost or reliability risk.

Table I.
Summary of performances for 1-V and 2-V RFC OpAmps.

Parameters	1 V RFC OpAmp #1	1 V RFC OpAmp #2	2 V RFC OpAmp
Technology	65-nm CMOS		
Open-Loop DC Gain [dB]	43.6	38.4	**63.4**
IM3 (dB) (closed loop)	62.5	55.4	**86.1**
Gain Precision (closed loop, ideal case is 1)	0.66	0.5	**0.94**
Intrinsic CMRR (dB) (closed loop, no mismatch)	254	301	**331**
I/O swing (V) (closed loop as a filter)	1	1	1.2
GBW [MHz]	215.8	312	236
Open Loop PM [deg]	65.4	61.1	63.6
Capacitive load [pF]	1	1	1
Slew Rate (average) [V/μs]	19.1	18.2	19.0
Input Referred Noise (1Hz-10 MHz) [μV_{rms}]	39	30.8	36
Power Consumption [mW]	0.63	1.24	1.37

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