HIGH PERFORMANCE CMOS OPERATIONAL-AMPLIFIER

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ABSTRACT

The design of a high performance CMOS operational-amplifier (op-amp) in 3 micron, double level metal technology is presented. The amplifier makes use of stacked (cascode) current source techniques and an enhanced push-pull output stage. This op-amp will be used for the realization of high-frequency switched-capacitor (SC) filters. Spice simulations of the op-amp shows a unity gain bandwidth of 40 MHz and a DC gain of 72 dB, when using a bias current of 100 microamperes and a load capacitance of 15 pF. A test chip implementing the operational-amplifier and other analog test cells was fabricated through the Canadian Microelectronics Corporation (CMC). Test results from the fabricated device demonstrate a DC gain of about 67 dB, with a unity gain bandwidth of about 40 MHz and a 36 volt per microsecond slew rate when using a bias current of about 100 microamperes and a 15 pF load.

I. INTRODUCTION

Monolithic SC filters can be very accurate, and allow more complete system integration due to their compatibility with current MOS technologies [1], [2] and [3]. The requirement for high performance CMOS op-amps increases as more applications and systems are realized in SC forms using CMOS VLSI technologies. Most of these applications make use of short-channel MOS processes to allow maximum systems integration. The use of short-channel devices also improves the frequency at which these circuits may be clocked.

The high clock rates attainable using current short-channel MOS processes imposes severe design constraints on the op-amps required to implement high frequency switched-capacitor filters. These can be summarized as follows:

- provide maximum possible gain
- provide the maximum possible unity gain bandwidth
- provide maximum possible slew rate
- provide minimum possible settling time
- provide reasonable output drive capabilities

The op-amp described in this paper takes advantage of the short-channel MOS processes, while providing reasonably high DC gain, unity gain bandwidth, slew rate and output drive capabilities. The op-amp was developed using design techniques described by Milkovic [4], [5] and Salama et al [8]. Milkovic's single-ended stacked (cascode) current mirror op-amp was chosen due to its compatibility with short-channel MOS technologies and ability to overcome the channel-length modulation problem which is the major factor limiting the open-circuit voltage gain of short-channel MOS transistors.

Salama's output driver stage was chosen for its high drive capability, fast slew rate and short settling time. The principle application for the high performance op-amp to be discussed is in high frequency switched-capacitor filters operating with clock rates in the tens of megahertz.

II. SINGLE ENDED STACKED MIRROR OPERATIONAL-AMPLIFIER

The basic amplifier approach is to use an input stage followed by a current gain stage. In high frequency op-amp designs, the output stage is designed to be the dominant pole of the amplifier thus making the poles associated with the input stages higher in frequency [7]. This is generally possible since the load capacitance is larger than the internal stray capacitance located between stages in the amplifier. When using this technique, great care must be taken since compensation is typically provided by the load capacitance.

The dominant pole p_1 is located at a frequency ω_1 determined by the total output resistance Ro and the load capacitance C_L. The ω_1 frequency is determined as

$$\omega_1 = \frac{1}{R_o C_L}$$

The non-dominant pole p_2 is determined by the first stage input resistance R_i, and the input capacitance to the current gain stage C_i. The non-dominant pole frequency ω_2 is approximately determined by

$$\omega_2 = \frac{1}{R_i C_i}$$

provided $r_o >> R_i$, where r_o is the output resistance of the input stage.

The current gain stage can be designed using basic current mirror techniques [2]. The underlying problem with basic current mirrors is that they are susceptible to channel-length modulation (λ) effects, especially when short-channel MOS processes are used. A more suitable circuit for the current gain stage is the stacked current mirror.

The stacked current mirror on the other hand, provides a large output resistance. The output resistance is large because of the local feedback action in the lower and upper transistors. The net effect of this is to reduce the λ-effect. The drain current in each branch of the mirror is only dependent on the ratio of the lower transistor gate widths, assuming that their channel lengths are equal. This simplifies the DC design of the circuit. The drawbacks to

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the stacked current mirror are a reduced voltage swing for large currents, and a slower response than the basic current mirror.

The single ended op-amp is shown in Figure 1. The input voltage is converted to a current in the differential input stage through M1 and M2. The PMOS stacked current mirror M15, M5, M6, and M7 provide a current gain of two and a high output resistance. The unity current mirror M14, M8, M9, M13 provides the current for the NMOS mirror M16, M10, M11, and M12 which also has a current gain of two and a high output resistance. The capacitor C_{cmp} provides frequency compensation.

The single-ended stacked (cascode) current mirror op-amp was first simulated and then implemented and tested using 3 micron CMOS design rules [6]. The test results demonstrated that the major disadvantage with this design is the poor drive capability of the current gain stage, and that the load capacitance provides frequency compensation limiting the minimum load. The minimum value for the load capacitance which provides dominant pole compensation, is given by

$$C_L = C_i R_i g_{m1} A_i$$

where g_{m1} is the transconductance of the first stage, and A_i is the current gain in the current gain stage.

The full bandwidth of the amplifier can be used on chip were minimum loads can be placed on the output. The output load is considerably larger when driving signals off chip, thus reducing the bandwidth of the amplifier. In order to enhance the performance of the op-amp so that it could easily drive signals off chip, a high drive class AB output stage was incorporated into the design.

III. HIGH DRIVE CLASS AB OUTPUT STAGE

Salama et al [8] designed a CMOS class AB high drive buffer which is suitable for driving large capacitive and moderate resistive loads. The main features of this design are its ability to drive large capacitive loads, have a low quiescent power dissipation, occupy a small silicon area, operate at high speed, and provide an adequate phase margin for good stability.

The design consisted of a two stage operational transconductance amplifier (OTA). Generally it consisted of a differential input stage followed by a class AB push-pull output stage. The voltage gain of the input stage was kept low to maintain a broadband frequency response. This is usually adequate for most buffering applications, where the overall gain is generally lower than that of conventional designs having a high input stage gain. This amplifier is also compensated by the load capacitor. The design combined a conventional OTA with an output stage which provides maximum drive capability during the slewing period, but is allowed to return to a wide-band low power mode of operation during the settling period.

A schematic of the high drive output stage is shown in Figure 2. It consists of an intermediate stage M17, M18, M19, M20, and M23 driving a push-pull class AB output stage M21, M22. Transistor M23 is given a low W/L ratio forcing it to operate in the linear mode and behave essentially as a large linear resistor. During quiescent operation, M18 and M19 remain on minimizing the current through the output stage, as well as maintaining a low impedance level on the gates of M21 and M22, thereby avoiding low order poles being created by the Miller capacitances. During the slewing period, either M17 and M18 are fully on while M19 and M20 are turned off, or M19 and M20 are fully on while M17 and M18 are turned off. In either case, large currents are available from M21 or M22 to discharge or charge the load capacitance.

A small signal analysis of the circuit demonstrates that the overall gain bandwidth of the amplifier is given by

$$GBW = g_m/C_L$$

where g_m is the effective transconductance of the amplifier and C_L is the load capacitance. The remaining poles and zeros are ratios of transconductance to parasitic capacitance, and have values in the high megahertz range. The design was capable of driving very large loads, 5000 pF, at over 100 KHz clock frequency, and had a bandwidth of 6 MHz with 100 pF load.

IV. HIGH PERFORMANCE OP-AMP

A high performance op-amp was developed by merging the single-ended stacked mirror op-amp and the high drive class AB output stage described above. The complete transistor schematic of the enhanced op-amp is shown in Figure 3a. It comprises the circuit shown in Figure 1, which has a large output resistance and thus a high gain, and the output buffer stage shown in Figure 2. Transistors M17 and M20 bias M18 and M19 which drive the push-pull class AB output stage M22 and M21. M23 has a low W/L ratio and essentially acts as a large linear resistor. Ideally the gate voltages of M18 and M22, and M19 and M21 compensate each other, and therefore, the output voltage is ideally zero for a 0 volt input. The output buffer stage is biased such that the current flowing through M22 is matched by the current in M21 during quiescent operation. The biasing transistors are controlled by the high frequency gain stage and provides the necessary inputs for the push-pull output stage. This quickly provides large currents to charge or discharge the load capacitance. M23 helps stabilize the output stage and allow fast settling of the amplifier.

Figure 3b is the layout for the high performance op-amp. Special layout considerations were taken in order to avoid large parasitic source and drain capacitances and resistances. Quickly changing signal paths were also kept as far apart as possible within the circuit. The op-amp was implemented using a 3 micron, double level metal CMOS process available through the Canadian Microelectronics Corporation (CMC). The layout occupies an area of 295 microns by 380 microns or about 174 mils square. Figure 4 shows the SPICE results for the small signal frequency response for the high performance op-amp circuit shown in Figures 3a and 3b. With a bias current of 100 microamperes and a load capacitance of 15 pF, a unity gain bandwidth of 40 MHz is achieved, and a DC gain of about 72 dB is obtained. Notice that the frequency response remains flat to about 100 KHz. Figure 5 shows the SPICE results for the AC response of the op-amp with varying capacitive loads ranging from 1 pF to 50 pF. Varying the load capacitance will vary the unity gain bandwidth as predicted, but does little affect the 3 dB bandwidth of the amplifier.

V. TEST RESULTS

Figure 4 also shows the measured small frequency response of the high performance op-amp. Measured and simulated device parameters are listed in Table1. At a bias current of approximately 100 microamperes and a load capacitance of 15 pF, a unity gain bandwidth of about 40 MHz was achieved, with a DC open-loop gain of about 67 dB. The large signal open-loop transient response indicates a slew rate of about 35 volts per microsecond for a load capacitance of 15 pF, and using a bias current of about 100 microamperes. Under these conditions, the output was well compensated, and no ringing was observed. Various loads were placed on the output with little apparent deterioration of the output when the amplifier was configured as a unity gain buffer.

Results presented by Milkovic using a 1.5 micron CMOS process, demonstrated a unity gain bandwidth of about 70 MHz and a DC voltage gain of 69 dB using a bias current of 50 microamperes and a load of 1 pF, for the single ended gain stage. The implementation of this circuit in a 3 micron process resulted in a unity gain bandwidth of 50 MHz and a DC voltage gain of 50 dB using a bias current of 100 microamperes and a load of 1 pF. Under the same conditions, and with a load of 15 pF, the unity gain bandwidth was reduced to about 6 MHz. Results presented by Salama demonstrated a bandwidth of 8 MHz for a 100 pF load. Results obtained by combining these circuits demonstrate a unity gain bandwidth of 63 MHz for a 1 pF load and 20 MHz for a 100 pF load. These results also compare favorably well with results obtain recently by C.L. Laber and P.R. Gray [9]. Their design of a positive-feedback transconductance amplifier achieved an open loop gain of about 80 dB with a gain bandwidth product of 25 MHz, and a slew rate of 18 volts per microsecond.

VI. CONCLUSION

A high performance op-amp has been presented. It was developed by combining a high frequency CMOS op-amp which uses short-channel MOS transistors, with a CMOS class AB high drive buffer suitable for driving large capacitive loads. Key advantages of both designs were used to implement a high performance op-amp suitable for use in analog integrated circuits and the development of high frequency switch-capacitor filters. A fully differential op-amp is currently being developed using similar design techniques.

VII. REFERENCES

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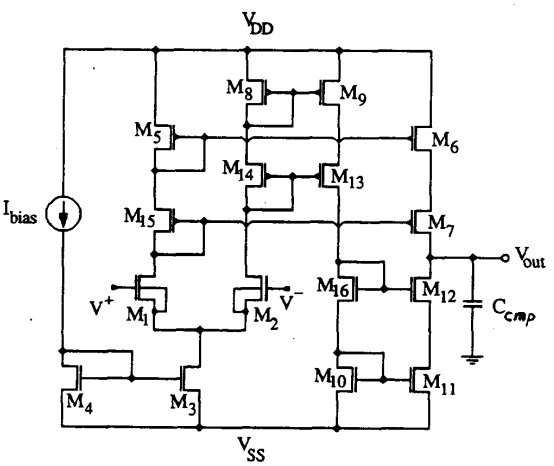

Figure 1. Single-ended CMOS op-amp using stacked current mirror

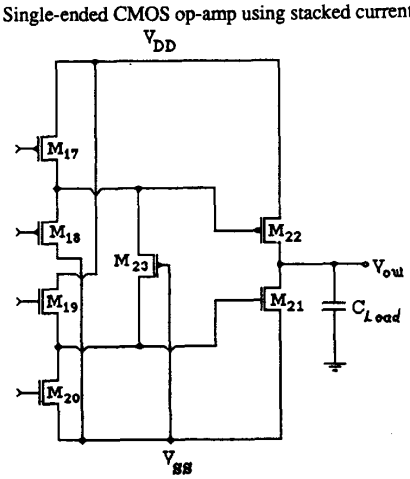

Figure 2. Output drive of the operational amplifier

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Further information can be obtained from Dr. W. Kenneth Jenkins.

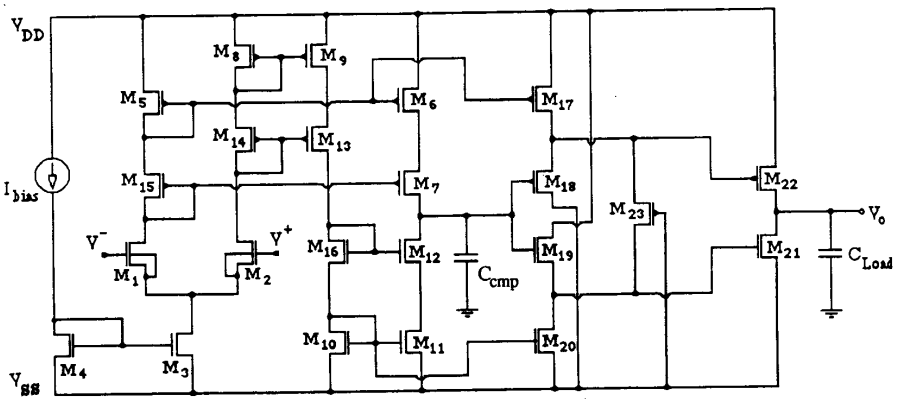

Figure 3(a). Complete schematic of the proposed CMOS op amp

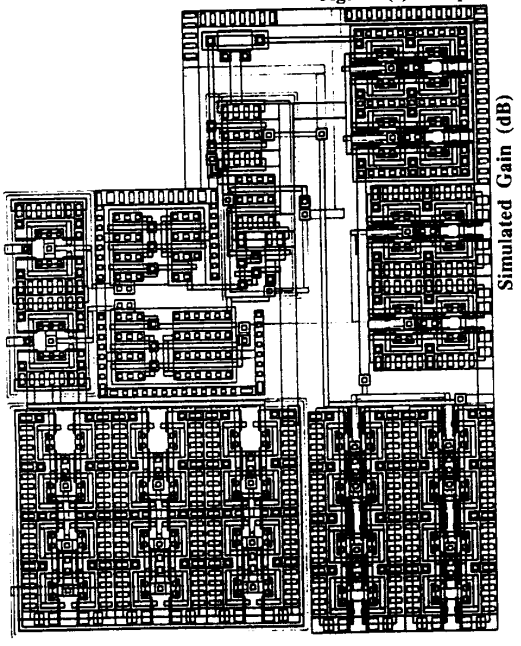

Figure 3(a). Layout of the proposed CMOS op amp

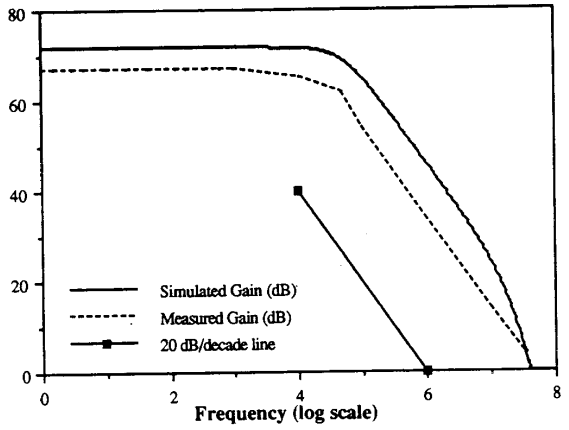

Figure 4. Simulated and measured open-loop gain (V_{DD} = +5V, V_{SS} = -5 V, I_{bias} 100 μA and C_L = 15 pF)

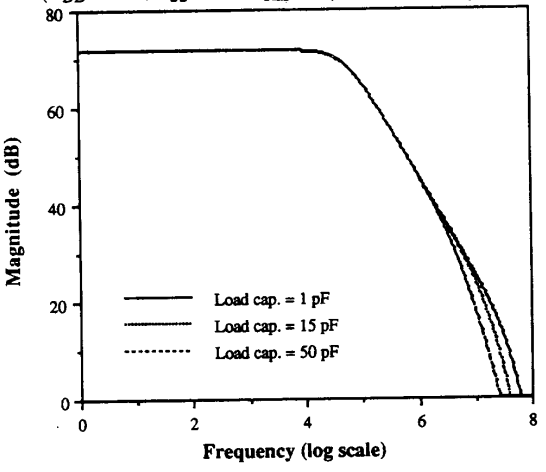

Figure 5. Simulated open-loop gain for different capacitive loads

Table 1. Amplifier parameters
V_{DD} = +5 V, V_{SS}= -5 V, I_{bias} = 100 μA and C_{cmp} = 15 pF

Parameter	Simulation Result	Measured Results
DCgain	71.69 dB	67 dB
Unity gain bandwidth	40 MHz	40 MHz
Phase margin	40°	N/A
Slew rate	200 V/μsec	35 V/μsec
I/p offset voltage	1.0 mV	N/A
O/p voltage swing	5.0 V	4.8 V
DC power dissipation	23 mW	N/A