# Title Here

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March 15, 2013

**Abstract**

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## Contents

# 1 Notch Filter

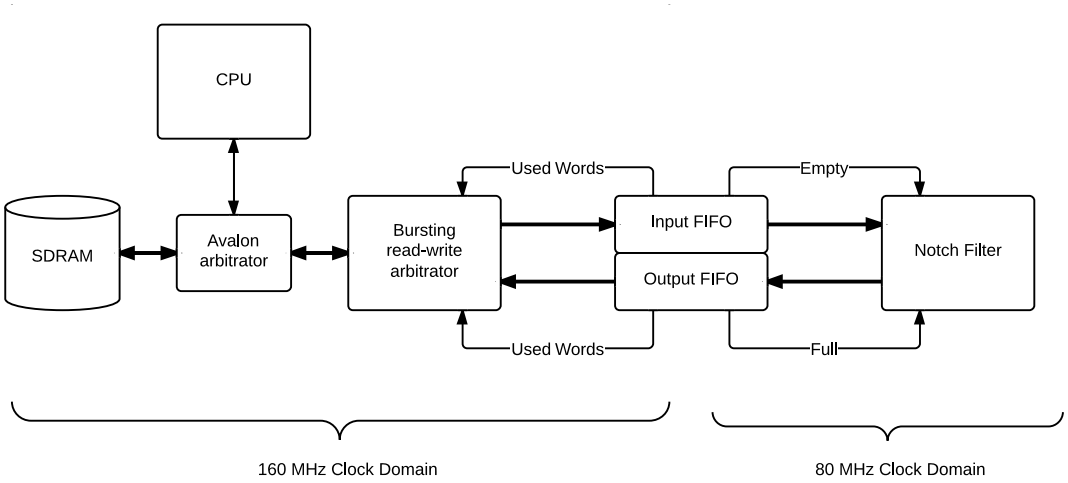


Figure 1: Block diagram of the Notch Filter hardware. FIFO buffers are used to allow efficient interleaved reads and writes to SDRAM. The buffers also serve as Clock Domain Crossing interfaces.

architecture implementation performance and timing (benchmarking) results

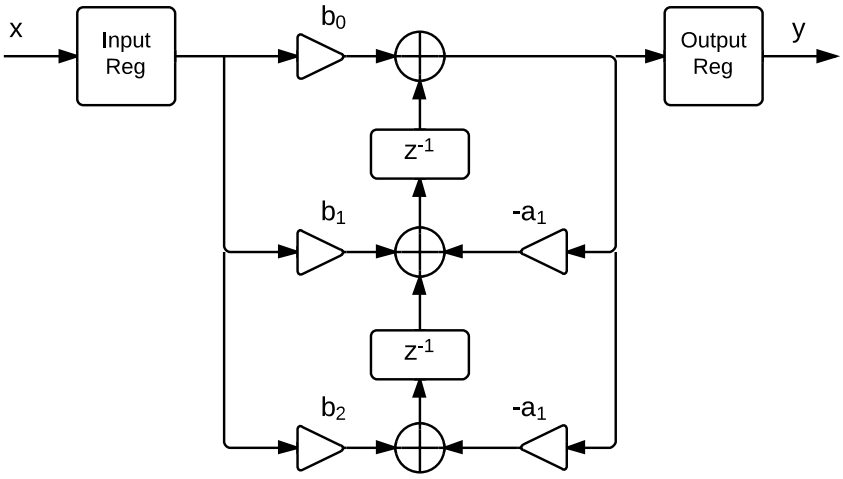


Figure 2: Second order Direct Form II Transposed filter architecture

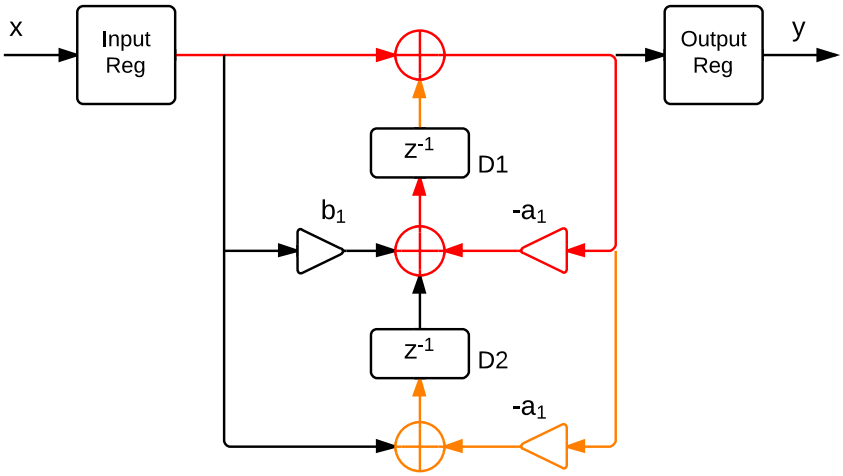


Figure 3: Annotated version of Figure 2, showing the main critical paths in the filter core. Shown in red is the path from the input register to the delay register D1. Shown in orange are the alternative paths that have almost as little slack as the red path.