ISC0404
Standard 1k x 1k, 16 Output ROIC

User's Guide

November 21, 2006

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

Document Revision History

- **Version 1.00, November 21, 2006**
  - Initial Release

ISC0404
Standard 1k x 1k, 16 Output ROIC

Design Overview

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

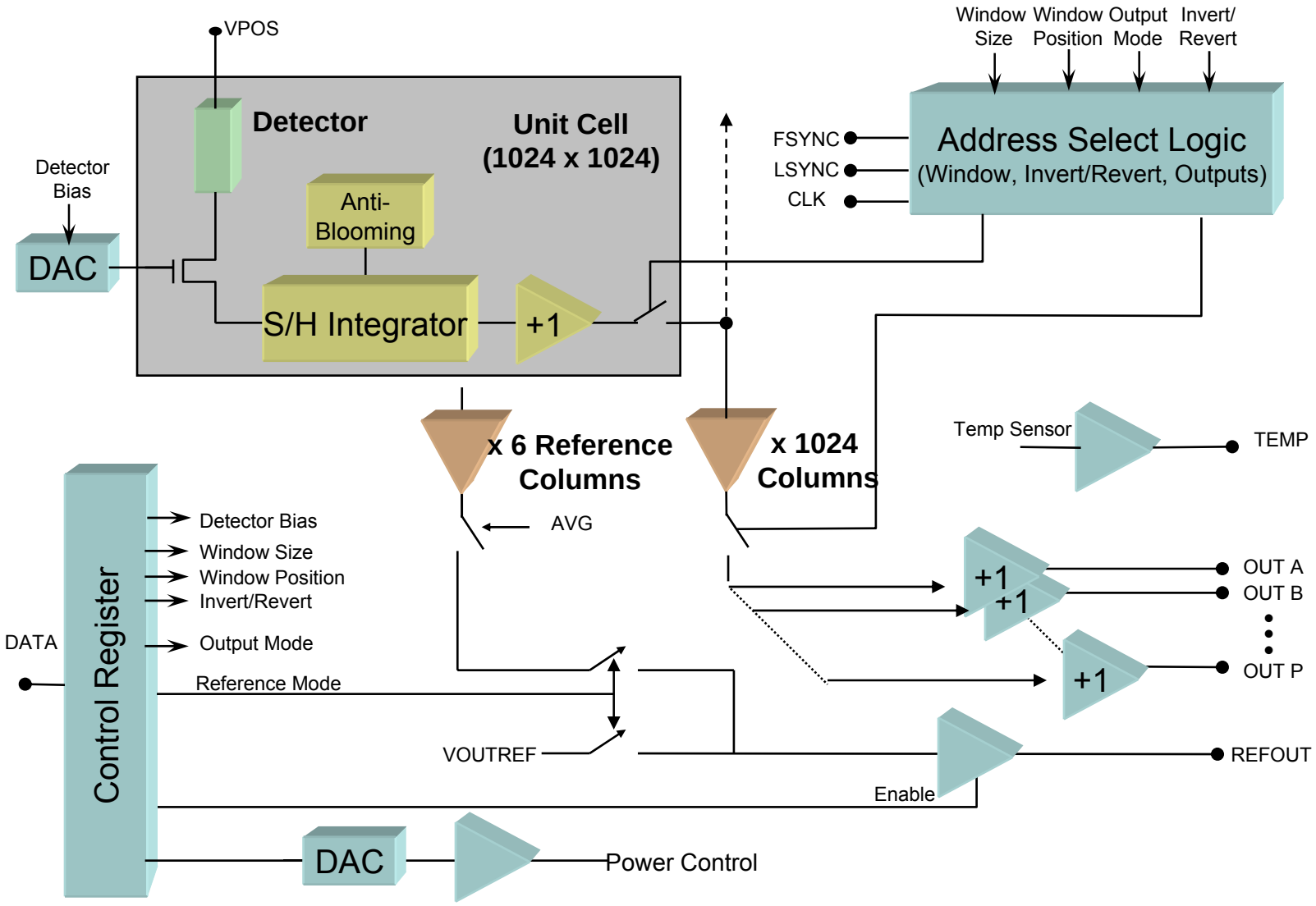
ISC0404 1k x 1k ROIC Overview (1 of 2)

- **18um x 18um unit cell**
- **Die size: 20.8mm x 22.42mm**
- **P-channel direct injection for P-on-N detectors**
- Two Versions of the Chip for Input Charge Handling:
  - Option 1: ≥ 10 x 10^6 carriers
  - Option 2: 2 ± 0.5 x 10^6 carriers
- **Voltage mode column multiplexer architecture**
- **Supports multiple readout modes**
  - Snap shot integrate-while-read (IWR)
  - Snap shot integrate-then-read (ITR)
  - Non-destructive readout (IWR or ITR)
    - Multiple readouts from single integration
  - Integration controlled by frame sync (FSYNC) duty cycle
- **Interface**
  - 5 clocks
  - 2 biases
  - 4, 8 or 16 outputs with optional reference output
  - Temperature sensor & programmable test

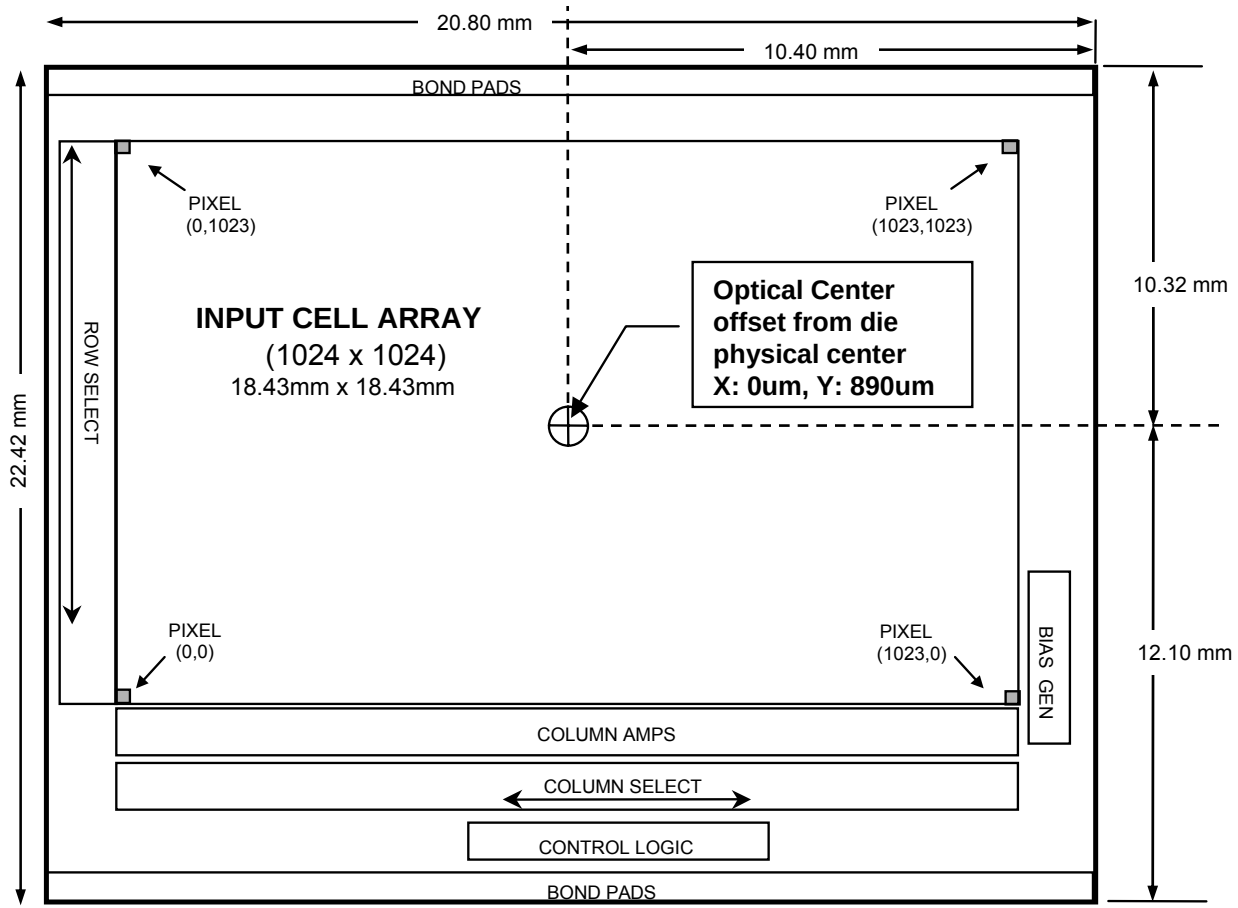
ISC0404 1k x 1k ROIC Overview (2 of 2)

- **Serial data interface (control register)**
  - Windowing
  - Power adjustment for frame rate compensation
  - Adjustable detector bias
  - Programmable test modes
  - Invert / Revert
  - 4, 8 or 16 outputs
  - Internal or external reference
  - Reference output enable
  - Integrate Then Read or Integrate While Read modes
  - Non-destructive readout mode
    - Multiple window readouts per integration
  - Global reset

ISC0404 Block Diagram

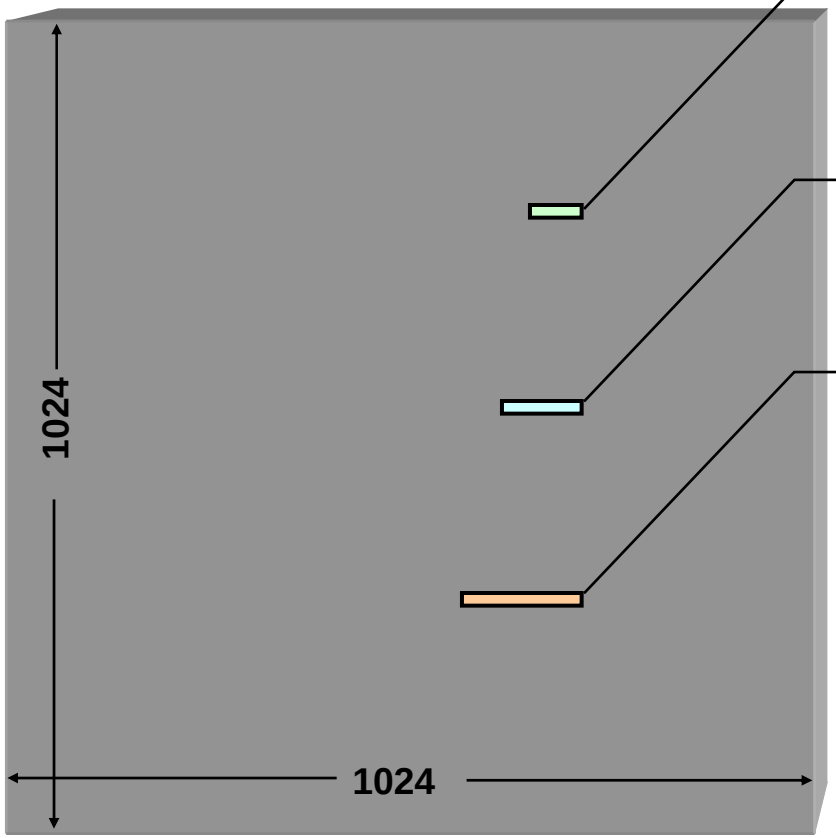


ISC0404 ROIC Layout



ISC0404 Windowing Operation
IWR, 12.5MHz Pixel Rate, T=80K

- **Conditions:**
  - **Integrate While Read**
  - **12.5 MHz Pixel Rate**
  - **T = 80K**



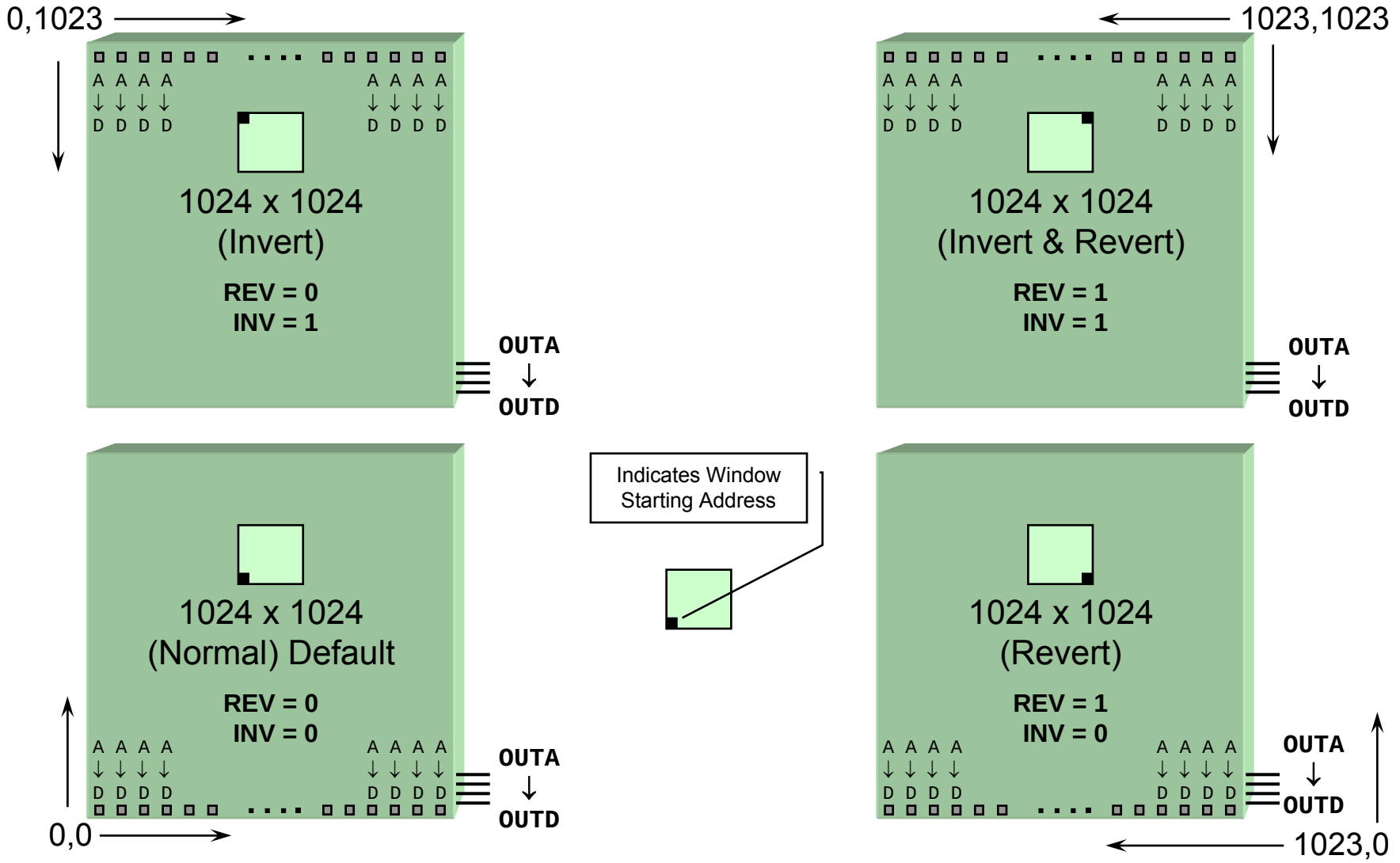
Smallest Window in 4 Output Mode
12.5MHz @ 80K
16x8 @ 4.16 kFPS

Smallest Window in 8 Output Mode
12.5MHz @ 80K
32x8 @ 4.16 kFPS

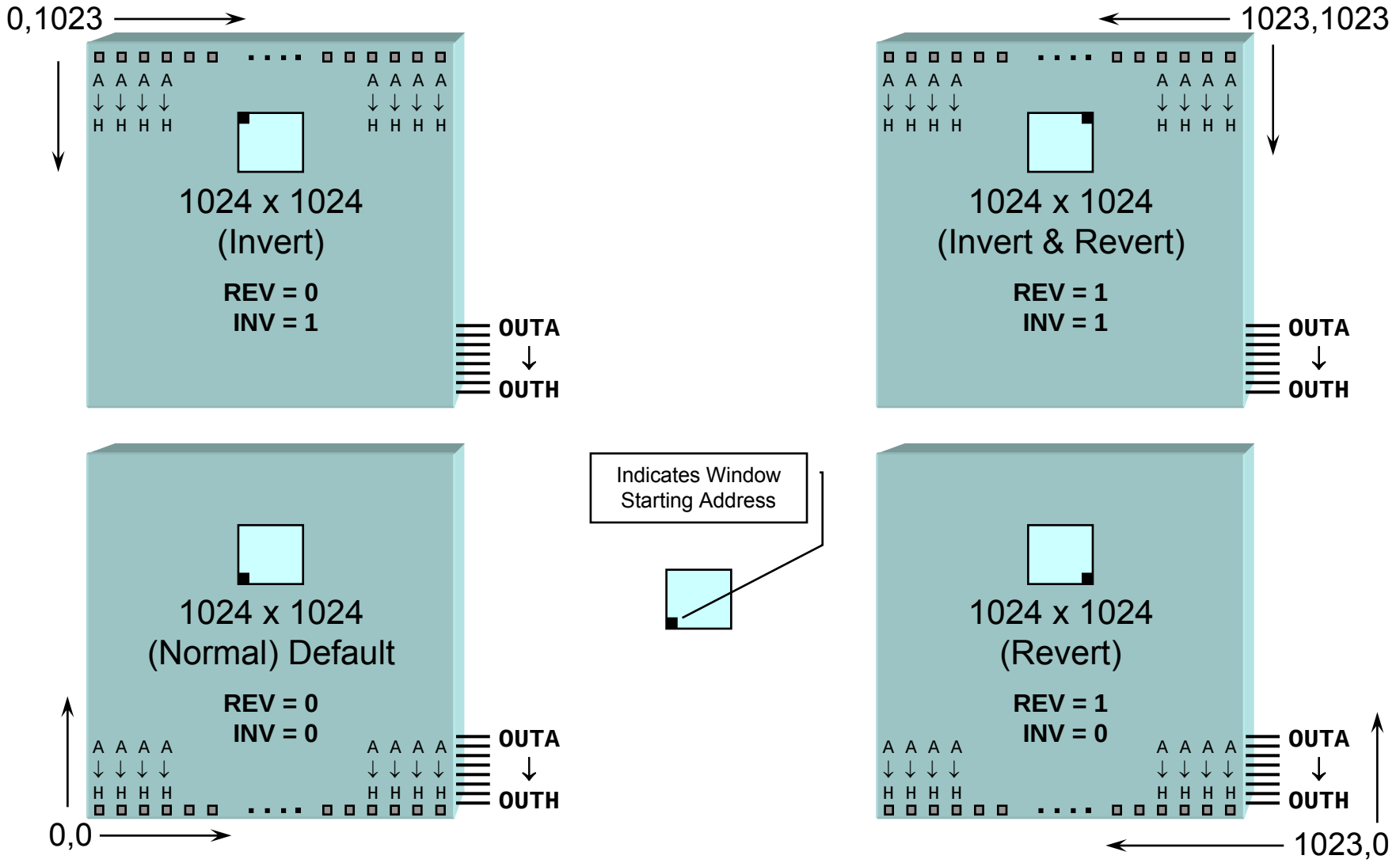
Smallest Window in 16 Output Mode
12.5MHz @ 80K
64x8 @ 4.16 kFPS

Output Configuration	Horizontal Window Resolution (Size and Position)	Vertical Window Resolution (Size and Position)
4 Outputs	16 Pixels	8 Pixels
8 Outputs	32 Pixels	8 Pixels
16 Outputs	64 Pixels	8 Pixels

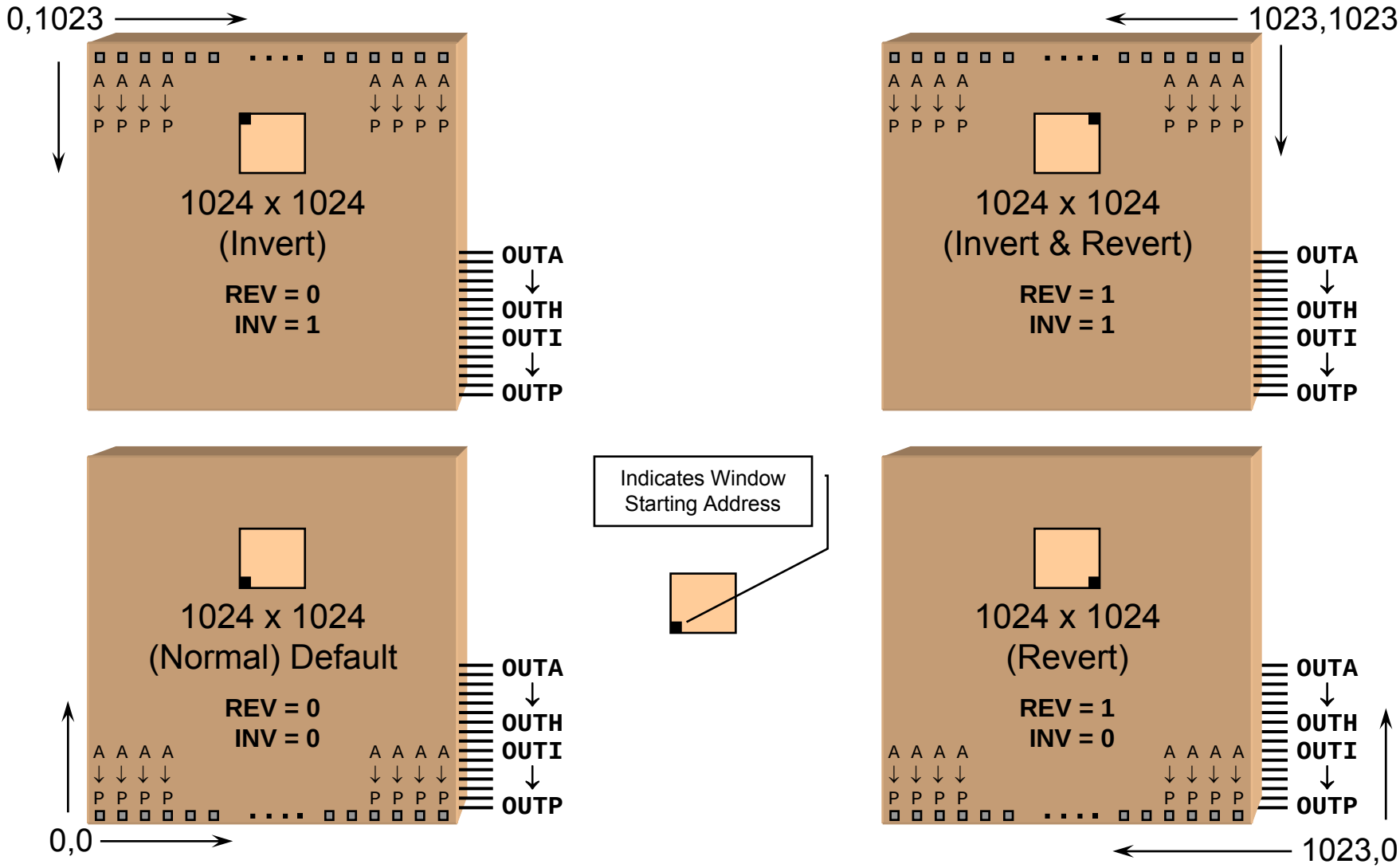
ISC0404 Readout Order
4 Output Mode (OUT=0x)



ISC0404 Readout Order
8 Output Mode (OUT=10)

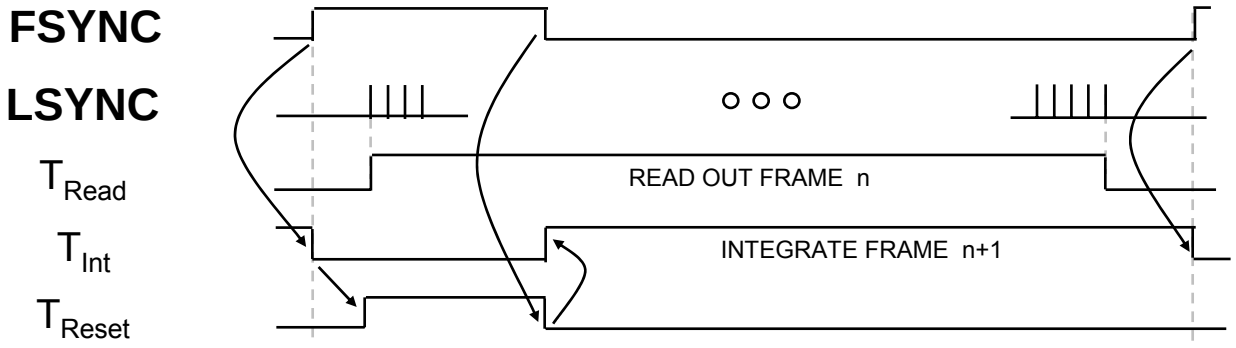


ISC0404 Readout Order
16 Output Mode (OUT=11)

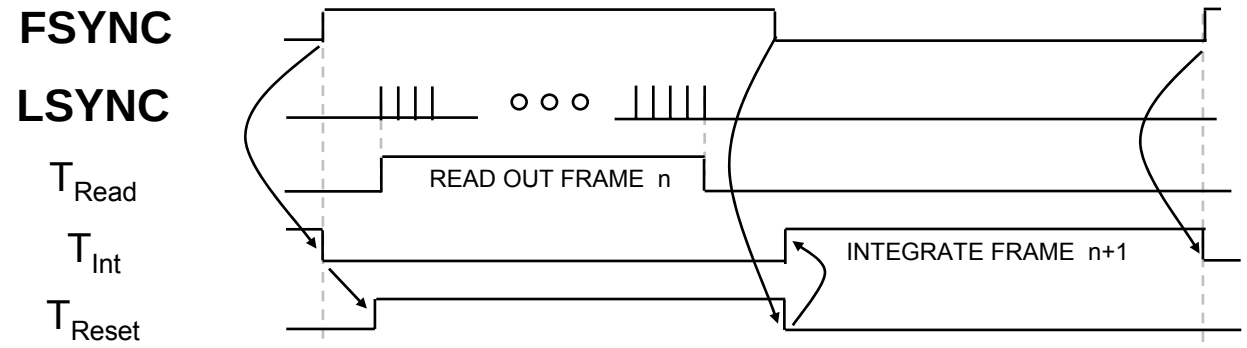


ISC0404
Integration / Readout Modes

- **Integrate While Read: $T_{Frame} = T_{Lsydel} + T_{Read} + T_{Intsample}$**



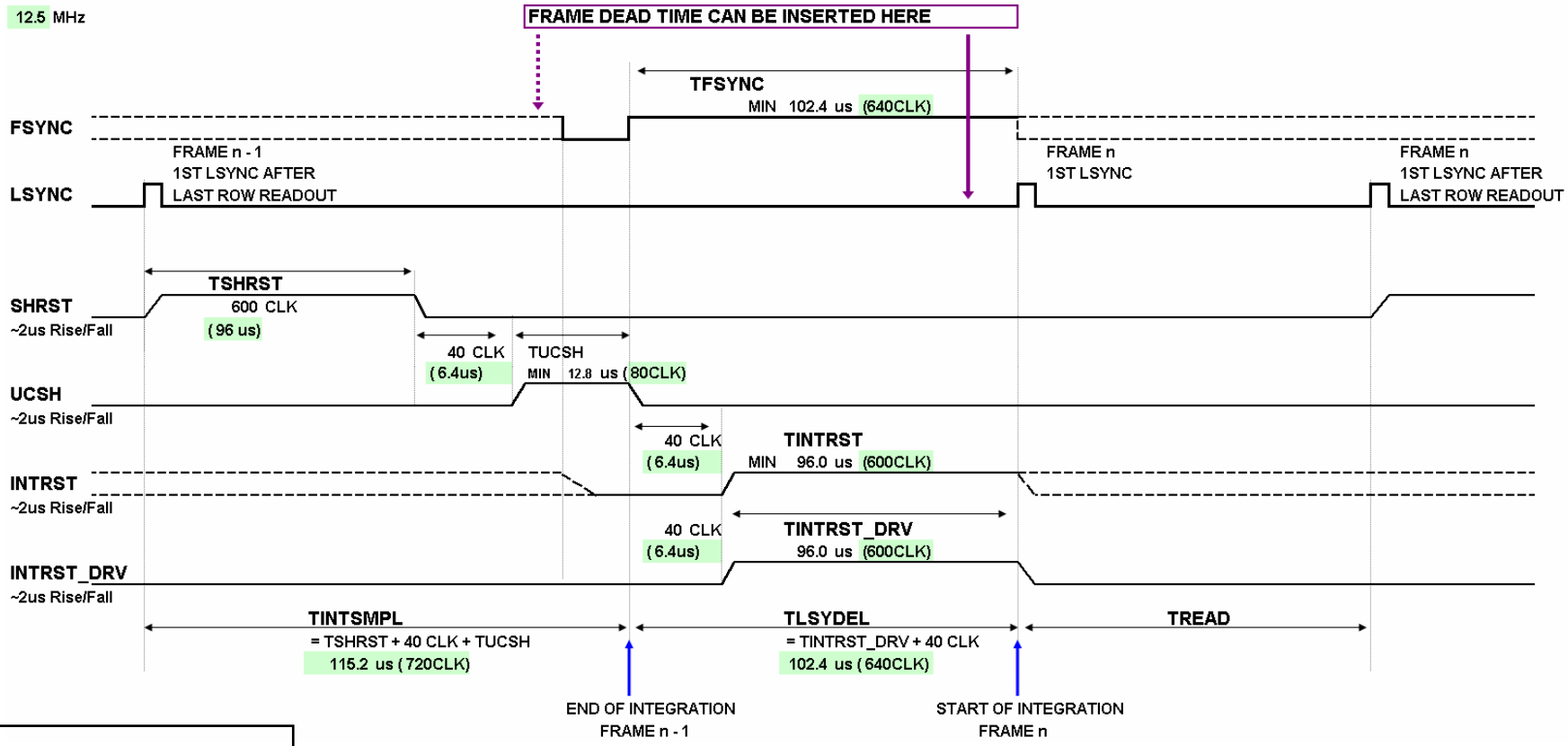
- **Integrate Then Read: $T_{Frame} = T_{Lsydel} + T_{Read} + T_{Intrst} + T_{Int}$**



ISC0404 IWR
Integration Sample Timing

- **Integration process ends at FSYNC rising edge**
- **TFRAME = TLSYDEL + TREAD + TINTSMPL**

(96us + 40 CLK) + TREAD + (96us + 40 CLK + min 12.8us)



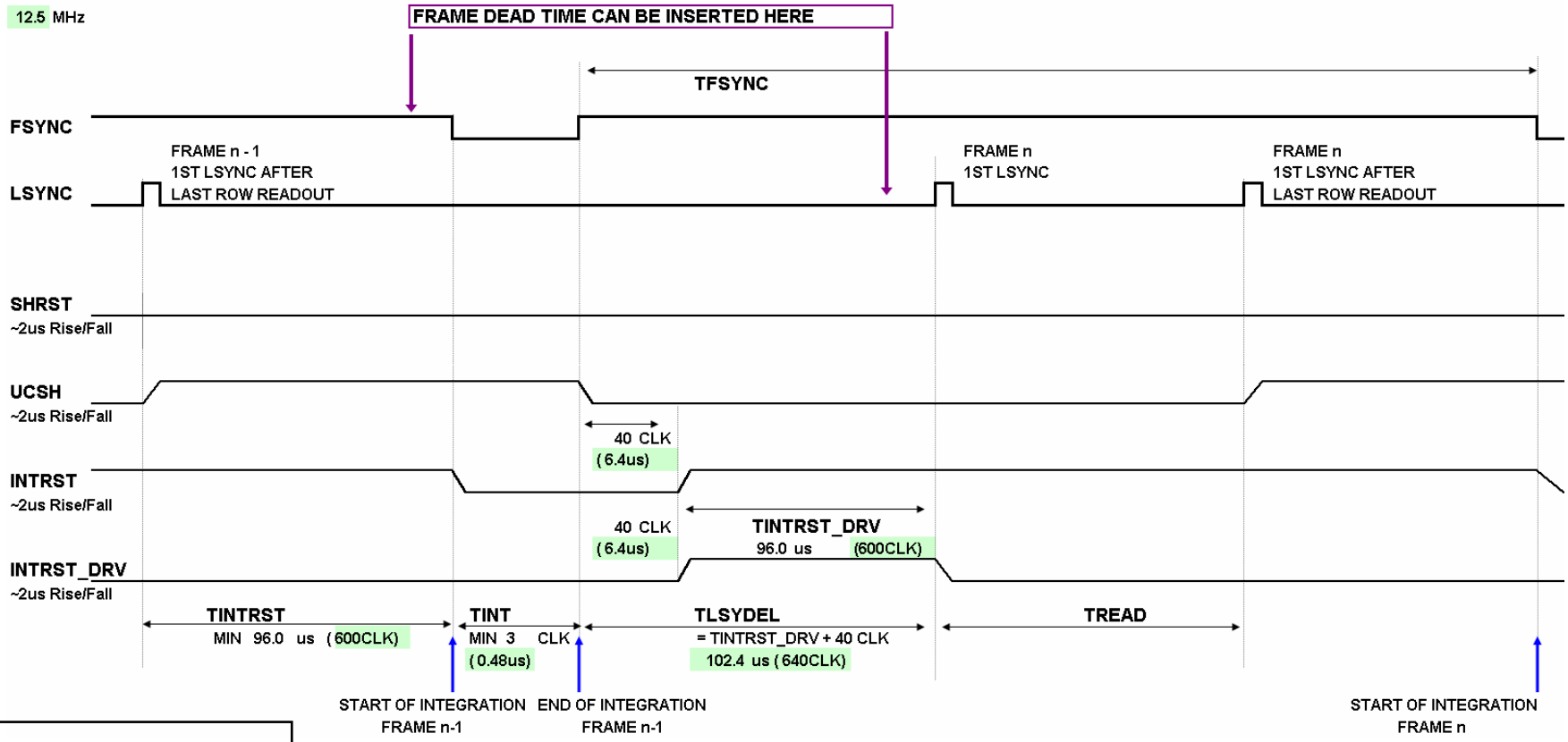
Times shown are for 12.5MHz Pixel Rate

➔1st LSYNC delay minimum 96us + 40 CLKS after FSYNC rising edge,
•TLSYDEL not directly related to non-minimum TFSYNC

ISC0404 ITR
Integration Sample Timing

- **Integration process ends at FSYNC rising edge**
- **TFRAME = TLSYDEL + TREAD + TINTRST + TINT**

(96us + 40 CLK) + TREAD + (min 96us) + (min 3 CLK)



Times shown are for 12.5MHz Pixel Rate

➔1st LSYNC delay minimum 96us + 40 CLKS after FSYNC rising edge

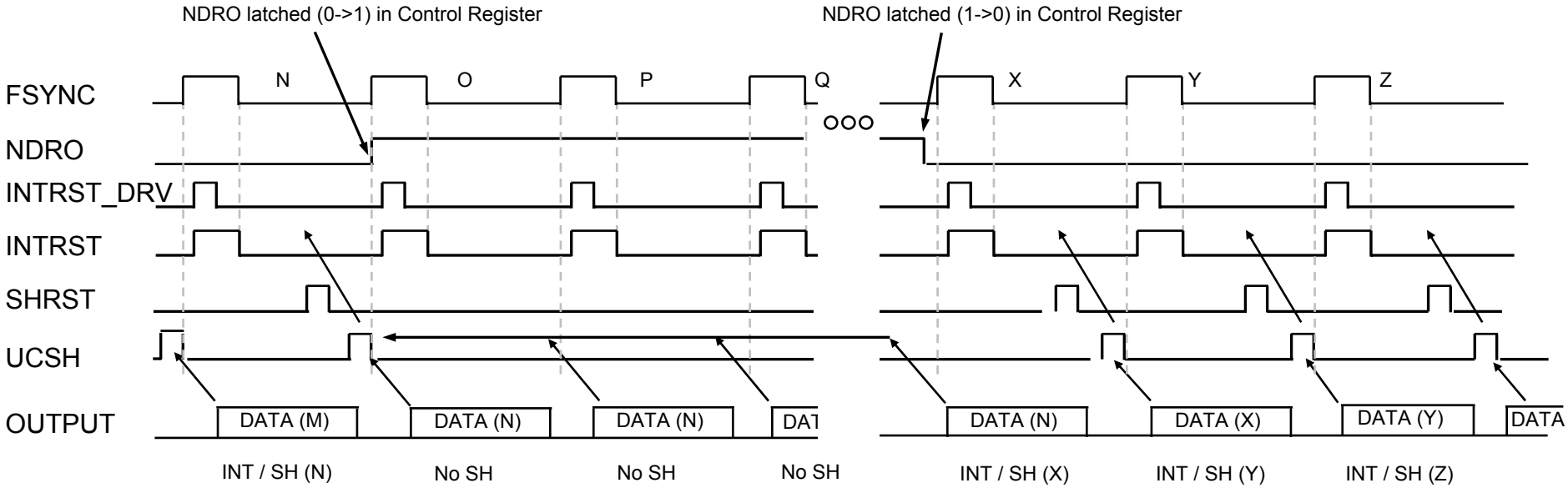
ISC0404
IWR Integration Time Control

- **Simultaneous Reset and Integration of All Pixels**
- **Integration Time Controlled by FSYNC Width:**
  - TINT Start: Falling Edge of FSYNC releases CINT Reset
  - TINT End: Rising Edge of FSYNC triggers End Of Global Sample/Hold
- **Actual Tint Is Defined By Rise And Fall Times Of ROIC Internal Signals**
  - Assume 50% Level Triggers On/Off Condition For Global Clocks
  - TINT Start ≈ 1.0uSec After Falling FSYNC Edge
  - TINT End ≈ 1.0uSec After Rising FSYNC Edge
- **TINT = TFRAME - TFSYNC Clocks**
  - Maximum TINT = TFRAME - 640 Clock Cycles
  - Minimum TINT = 3 Clock Cycles
  - Note: For Integration With Very Small Periods of FSYNC LOW, Non-Linear Behavior Of TINT vs. TFSYNC Is Likely To Occur.

ISC0404
ITR Integration Time Control

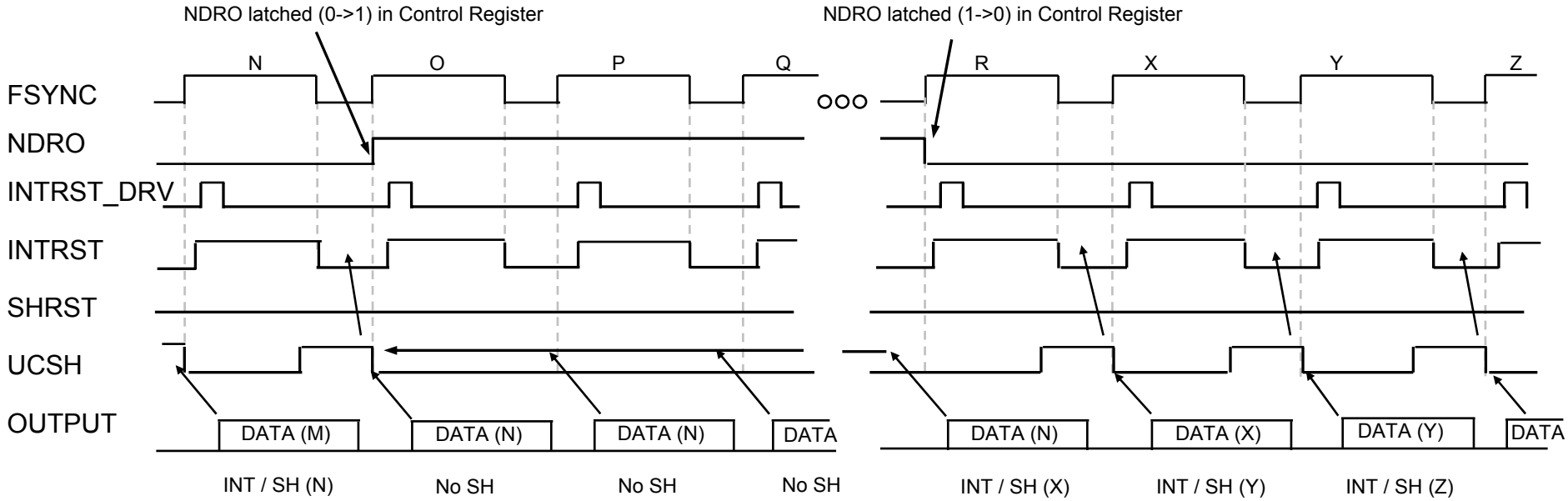
- **Simultaneous Reset and Integration of All Pixels**
- **Integration Time Controlled by FSYNC Width:**
  - TINT Start: Falling Edge of FSYNC releases CINT Reset
  - TINT End: Rising Edge of FSYNC triggers End Of Global Sample/Hold
- **Actual Tint Is Defined By Rise And Fall Times Of ROIC Internal Signals**
  - Assume 50% Level Triggers On/Off Condition For Global Clocks
  - TINT Start ≈ 1.0uSec After Falling FSYNC Edge
  - TINT End ≈ 1.0uSec After Rising FSYNC Edge
- **TINT = TFRAME - TFSYNC Clocks**
  - TFSYNC = TINTRST + TREAD + TLSYDEL
  - Maximum TINT = TFRAME - TREAD - 1240 Clock Cycles
  - Minimum TINT = 3 Clock Cycles
  - Note: For Integration With Very Small Periods of FSYNC LOW, Non-Linear Behavior Of TINT vs. TFSYNC Is Likely To Occur.

ISC0404 Frame Integration Timing For NDRO Mode: IWR



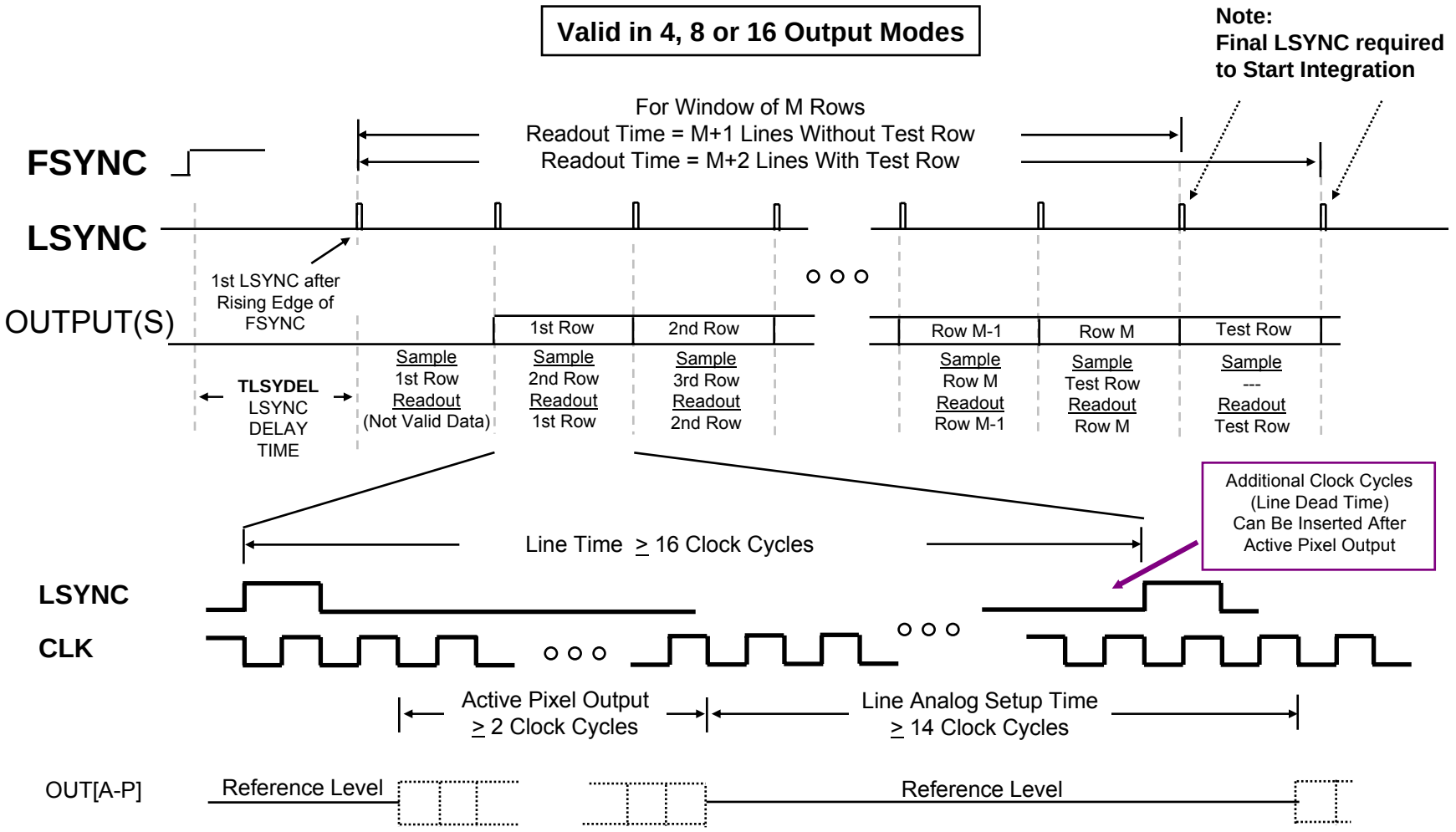
- **When Rising Edge FSYNC Latches NDRO bit transition 0->1**
  - UCSH Falling Edge Ends Integration, Integrated Signal Is Read Out
  - Subsequent Rising Edges Of FSYNC
    - No SHRST or UCSH Pulses Occur. Previously Integrated Signal Is Retained
    - Previously Integrated Signal Is Read Out
    - New Windows Can Be Programmed For Each Frame
- **When Rising Edge FSYNC Latches NDRO bit transition 1->0**
  - Previously Integrated Signal Is Read Out
  - Integration and Sample/Hold Occur Normally
  - Subsequent Rising Edges Of FSYNC
    - Integration, Sample/Hold And Readout Occur As For Normal (Not NDRO) Mode

ISC0404 Frame Integration Timing For NDRO Mode: ITR

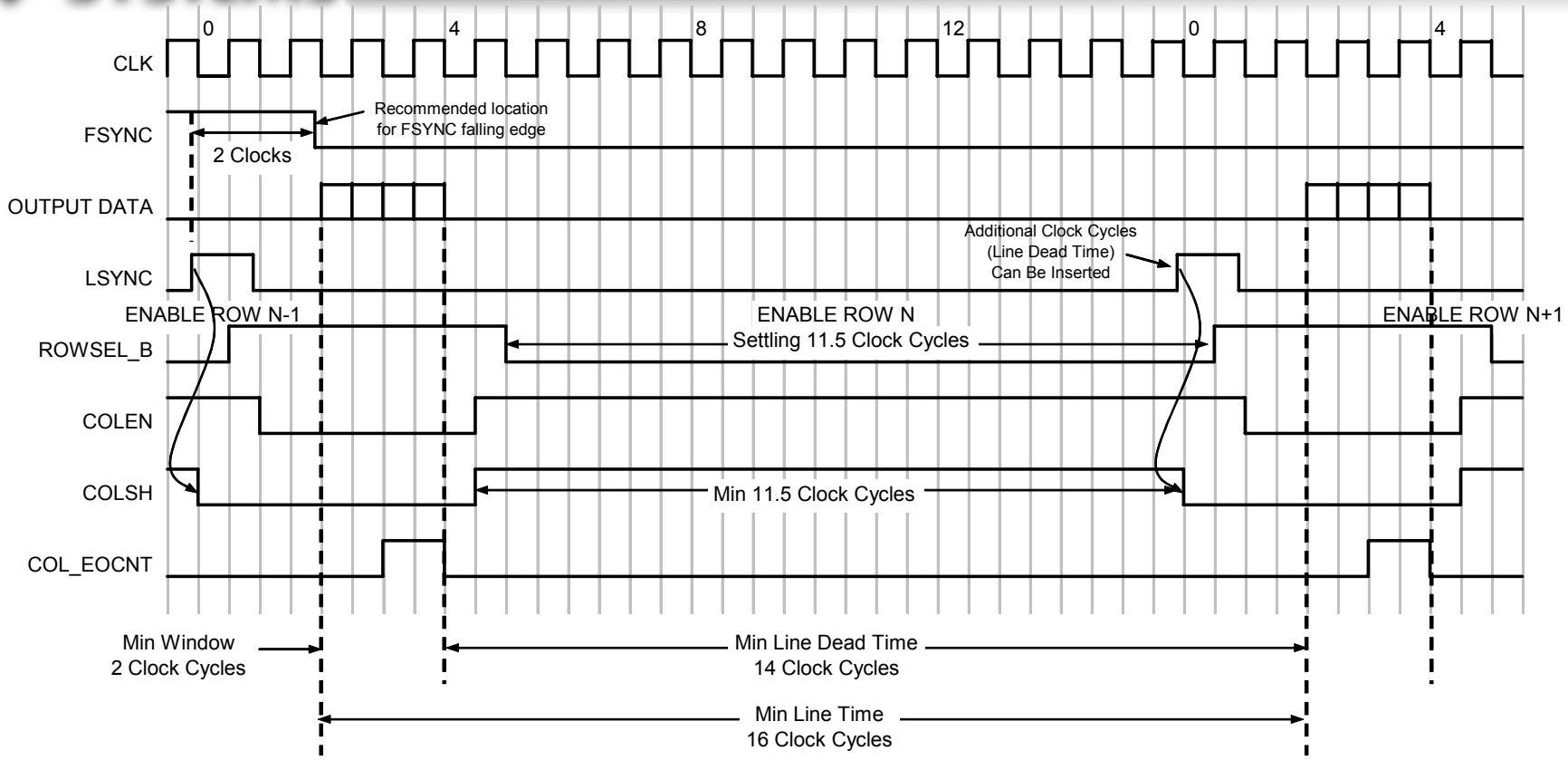


- **When Rising Edge FSYNC Latches NDRO bit transition 0->1**
  - UCSH Falling Edge Ends Integration, Integrated Signal Is Read Out
  - Subsequent Rising Edges Of FSYNC
    - No UCSH Pulse Occurs. Previously Integrated Signal Is Retained
    - Previously Integrated Signal Is Read Out
    - New Windows Can Be Programmed For Each Frame
- **When Rising Edge FSYNC Latches NDRO bit transition 1->0**
  - Previously Integrated Signal Is Read Out
  - Integration and Sample/Hold Occur Normally
  - Subsequent Rising Edges Of FSYNC
    - Integration, Sample/Hold And Readout Occur As For Normal (Not NDRO) Mode

ISC0404
Frame Readout Detail



ISC0404 Analog Control Timing



- Column buffers turned on only 12.5 clock cycles during each line time
  - Line time = $N_{COL}/2/N_{OUTPUT}$ + Line dead time
  - Low power for full frame
- Recommended location for FSYNC falling edge (start of integration) shown above
  - Based on ISC0403 test results
  - FSYNC latched on falling edge of CLK

ISC0404
Readout Line Time

- **Line Time = Analog Setup Time + Active Pixel Time**
  - Minimum Analog Setup Time = 14 Clock Cycles
  - Analog Setup Time May Be Extended By Adding Line Dead Time
    - Whole Additional Clock Cycles
  - Minimum Active Pixel Time = 2 Clock Cycles
  - Therefore Minimum Line Time = 16 Clock Cycles
- **Active Pixel Time Depends on # Outputs, Window Size**
  - Active Pixel Time (Clock Cycles) =
    - 4 Output Mode: Window Size (# Columns) / 8
    - 8 Output Mode: Window Size (# Columns) / 16
    - 16 Output Mode: Window Size (# Columns) / 32
  - Minimum Window Size (# Columns)
    - 4 Output Mode: Window Size (# Columns) / 16
    - 8 Output Mode: Window Size (# Columns) / 32
    - 16 Output Mode: Window Size (# Columns) / 64

ISC0404
Readout Data Timing

- **Minimum Required Number of LSYNC pulses for a Window of M Rows**
  - = M+2 If Test Row Readout Not Enabled
  - = M+3 If Test Row Readout Enabled
  - Note: 1 LSYNC Pulse Required After Last Row Readout (Valid Data Row or Test Row if Enabled) To Begin Integration Sampling Process
- **Start of Data Readout**
  - First Valid Line Follows 2nd LSYNC Pulse After the Rising Edge of FSYNC
- **End of Data Readout**
  - For Window Size of M Rows:
    - Last Valid Line Follows (M + 1)th LSYNC Pulse After the Rising Edge of FSYNC
- **Test Row Readout**
  - Follows Next LSYNC (M+2) After End Of Data Readout
  - Test Row Read Out Only If TR Command Bit = 1

ISC0404
Readout Time / Frame Rate

- **Frame Time in Integrate While Read Mode (IWR)**
  - **Frame Time = LSYNC Delay + Readout + Integration Sample Time**
    - Frame Dead Time Can Be Added By Increasing:
      - LSYNC Delay Time
      - Integration Sample Time
- **Frame Time in Integrate Then Read Mode (ITR)**
  - **Frame Time = LSYNC Delay + Readout + Integration Reset + Integration Time**
    - Frame Dead Time Can Be Added By Increasing
      - LSYNC Delay Time
      - Integration Reset Time
- **Readout Time Depends on:**
  - Pixel Rate, # Outputs, Window Size, Line Dead Time
  - For Window Size of M Rows, Minimum Readout Time =
    - M + 1 Line Times (Test Row Readout Disabled)
    - M + 2 Line Times (Test Row Readout Enabled)

ISC0404 Readout Timing
Max Frame Rate Equations (IWR)

- **Max Frame Rate Equations For IWR Mode:**
  - Rows = # Rows in Readout Window
  - Cols = # Columns in Readout Window
  - Rate = Pixel Rate (Hz) (= CLK Rate *2)
  - Line_ASU = Line Analog Setup Time in CLK Cycles
  - TLSYDEL = FSYNC to LSYNC Delay Time in CLK Cycles
  - TINTSMPL = Integration Sample Time In CLK Cycles
  - Frame Dead Time Can Be Added By Increasing:
    - LSYNC Delay Time (TLSYDEL)
    - Integration Sample Time (TINTSMPL)

# Outputs	Max Frame Rate for IWR Mode =
4	Rate / (2*((Rows + 1)*(Cols/8 + Line_ASU) + TLSYDEL+ TINTSMPL))
8	Rate / (2*((Rows + 1)*(Cols/16 + Line_ASU) + TLSYDEL+ TINTSMPL))
16	Rate / (2*((Rows + 1)*(Cols/32 + Line_ASU) + TLSYDEL+ TINTSMPL))

ASSUMES NO TEST ROW READOUT

ISC0404 Readout Timing
Max Frame Rate Equations (ITR)

- **Max Frame Rate Equations For ITR Mode:**
  - Rows = # Rows in Readout Window
  - Cols = # Columns in Readout Window
  - Rate = Pixel Rate (Hz) (= CLK Rate *2)
  - Line_ASU = Line Analog Setup Time in CLK Cycles
  - TLSYDEL = FSYNC to LSYNC Delay Time in CLK Cycles
  - TINTSMPL = Integration Sample Time In CLK Cycles
  - TINT = Integration Time In CLK Cycles
  - Frame Dead Time Can Be Added By Increasing:
    - LSYNC Delay Time (TLSYDEL)
    - Integration Sample Time (TINTSMPL)

# Outputs	**Max Frame Rate for ITR Mode =**
4	Rate / (2*((Rows + 1)*(Cols/8 + Line_ASU) + TLSYDEL + TINTRST + TINT))
8	Rate / (2*((Rows + 1)*(Cols/16 + Line_ASU) + TLSYDEL + TINTRST + TINT))
16	Rate / (2*((Rows + 1)*(Cols/32 + Line_ASU) + TLSYDEL + TINTRST + TINT))

ASSUMES NO TEST ROW READOUT

ISC0404 Frame Rate Computation Examples

- **640 x 512, 4 Output Mode, IWR Mode, No Additional Dead Time, 12.5MHz Pixel Rate**
  - Line Time = (640 / 8) + 14 = 94 Clock Cycles
  - Readout Time = ((512 + 1) * 94) = 48,222 Clock Cycles
  - Integration Sample Time = 720 Clocks
  - LSYNC Delay Time = 640 Clocks
    - Frame Time = 7.93 mSec
    - Frame Rate = 126.05 Hz
- **1024 x 1024, 8 Output Mode, IWR Mode, No Additional Dead Time, 12.5MHz Pixel Rate**
  - Line Time = (1024 / 16) + 14 = 78 Clock Cycles
  - Readout Time = ((1024 + 1) * 78) = 79,950 Clock Cycles
  - Integration Sample Time = 720 Clocks
  - LSYNC Delay Time = 640 Clocks
    - Frame Time = 13.01 mSec
    - Frame Rate = 76.87 Hz
- **1024 x 768, 16 Output Mode, IWR Mode, No Additional Dead Time, 12.5MHz Pixel Rate**
  - Line Time = (1024 / 32) + 14 = 46 Clock Cycles
  - Readout Time = ((768 + 1) * 46) = 35,374 Clock Cycles
  - Integration Sample Time = 720 Clocks
  - LSYNC Delay Time = 640 Clocks
    - Frame Time = 5.88 mSec
    - Frame Rate = 170.14 Hz

ISC0404 Frame Rates

- **Operating Conditions for Examples**
  - –Integration Mode & Timing
    - IWR Integration Sample Time = 720 CLK
    - ITR Integration Reset + Integration Time = 720 CLK
  - – Line Dead Time = 14 CLK
  - – CLK= 6.25 MHz

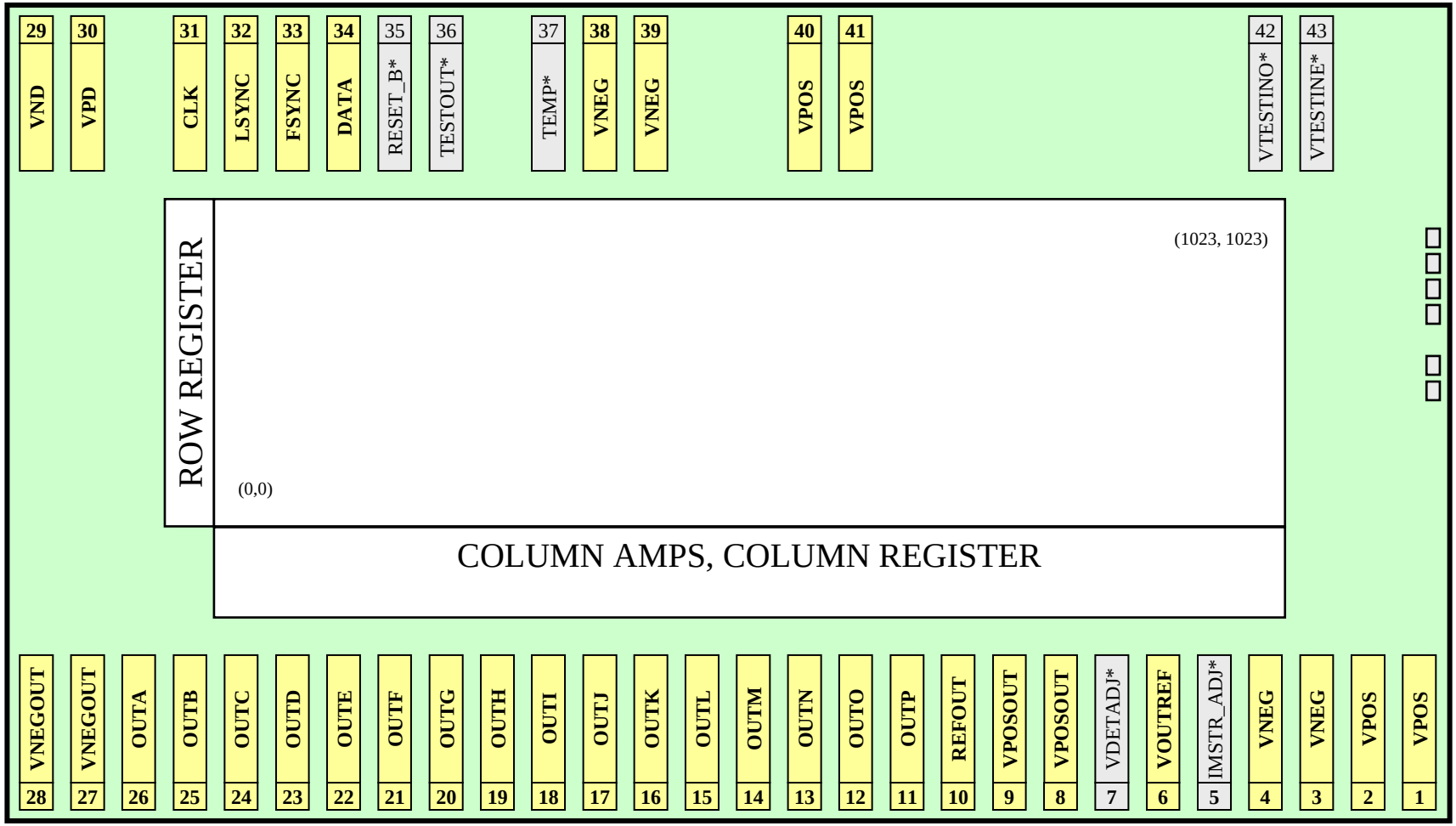
MODE	1024 x 1024 Full Frame	640 x 480	320 x 256	160 x 128	80 x 64
4 Output Mode	42.5 Hz	134.2 Hz	410 Hz	1088 Hz	2140 Hz
8 Output Mode	76.9 Hz	228.7 Hz	619 Hz	1402 Hz	2408 Hz
16 Output Mode	128.8 Hz	352.8 Hz	830 Hz	1640 Hz	2569 Hz

–CLK= 5.00 MHz

MODE	1024 x 1024 Full Frame	640 x 480	320 x 256	160 x 128	80 x 64
4 Output Mode	34.0 Hz	107.4 Hz	328 Hz	870 Hz	1712 Hz
8 Output Mode	61.5 Hz	182.9 Hz	495 Hz	1122 Hz	1927 Hz
16 Output Mode	103.1 Hz	282.3 Hz	664 Hz	1312 Hz	2055 Hz

***Note: To achieve 16 Output Full Frame = 120 Hz, CLK can be reduced to 5.83MHz -- (Pixel Rate = 11.65MHz)**

ISC0404 Pad Placement



* Pads in grey are optional

ISC0404
Standard 1k x 1k, 16 Output ROIC

Analog Operational Overview

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404 Analog Controls

- **Pads**
  - IMSTR_ADJ — Master Bias Current Adjust
  - VDET_ADJ — Detector Bias Adjust
  - VOUTREF — Output Voltage Level During Blanking Period
  - VTESTINE, VTESTINO — Unit Cell Test Input Voltages (Even, Odd)
- **Control Bits (All Digital)**
  - PT — Master Bias Current Temperature Setting
  - IM[2-0] — Master Bias Current Adjust
  - CP[2-0] — Column Buffer Bias Adjust
  - CL[2-0] — Column Bus Clamp Level Adjust
  - MP[1-0] — Mux Buffer Bias Adjust
  - DP[1-0] — Output Driver Bias Adjust
  - BP[1-0] — Detector Bias and Anti-Blooming Bias Buffer Adjust
  - DE[6-0] — Detector Bias Adjust
  - BLM_E — Even Column Test Enable
  - BLM_O — Odd Column Test Enable
  - LP[2-0] — Unit Cell Clock Rise / Fall Time Adjust
  - LPD[1-0] — Current Limited Logic Driver Current Adjust
  - REF[1-0] — Selects Reference Column vs. Reference Buffer
  - NDRO — Selects Non-Destructive Readout

ISC0404 Power Adjust Circuit Functions

- **Optimize power while achieving desired performance at operating speed at various operating temperatures**
- **Use adjustment of currents to:**
  - Adjust bias chain for temperature (PT)
  - Signal channel slewing and settling time requirements (CP)
  - Multiplexer buffer drive requirements (MP)
  - Output amplifier drive requirements (DP)
  - Use IM, CP and PT bits to adjust master bias current and signal path currents
  - IMSTR_ADJ pad may also be used to adjust master bias current
- **Recommended settings provided for the most common operating modes**

ISC0404 Master Current Adjust Bits for Temperature Adjust

- **PT adjusts the master current source**
  - Accounts for internal master resistor changes vs. temperature
  - PT defaults to PT = 0 at reset which should correspond to 50uA in master current source at T = 77K
  - A programmed PT = 1 will increase all currents by 1.35x
    - Recommend using PT = 1 when operating at 300K

PT	Target Current
0	50uA at 77K (Default)
1	50uA at 300K

Note: The above bias current values correspond to the default settings for the Chip Master Bias set with the IM[2-0] bits

ISC0404 Master Current Adjust Bits IM[2-0]

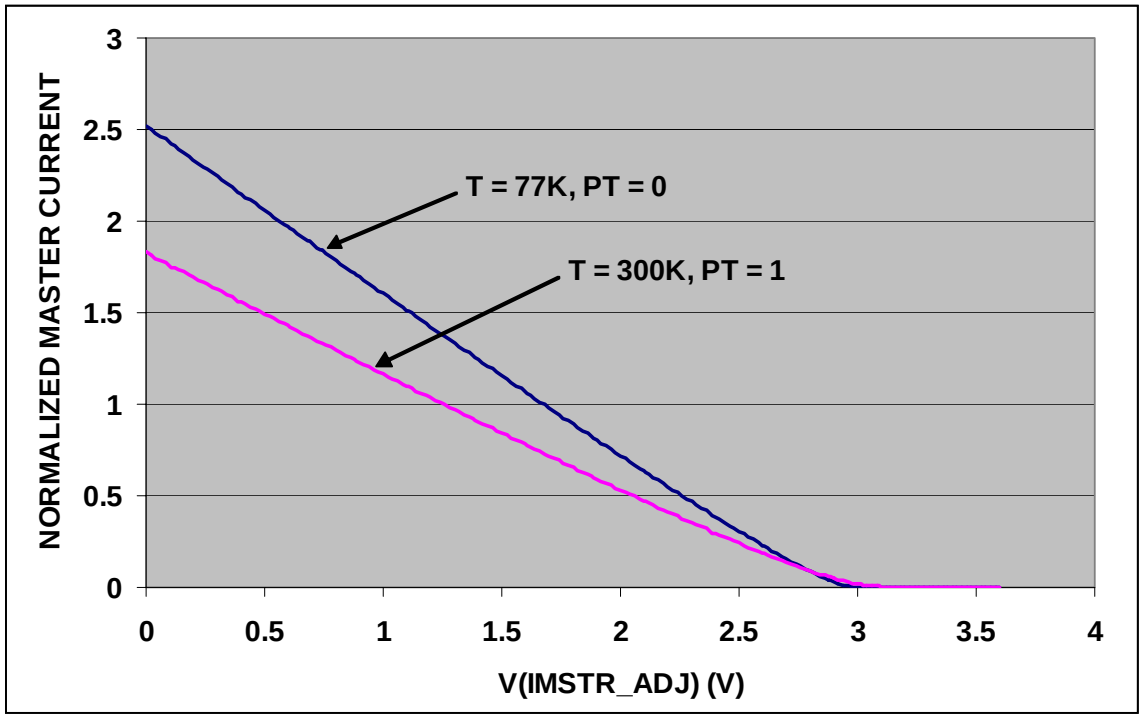
- **IM[2-0] adjusts the master current source**
  - Accounts for internal master resistor process variations
  - IM[2-0] defaults to [011] at reset which should correspond to 50uA in master current source
  - A programmed [000] will decrease all currents to about 0.70x
  - A programmed [111] will increase all currents to about 1.40x

IM2	IM1	IM0	Target Current	%
0	0	0	35uA	70
0	0	1	40uA	80
0	1	0	45uA	90
0	1	1	50uA (Default)	100
1	0	0	55uA	110
1	0	1	60uA	120
1	1	0	65uA	130
1	1	1	70uA	140

Note: The above bias current values are for PT set to appropriate level

ISC0404 Power Adjust External Pad Control (IMSTR_ADJ)

- **Power is also adjustable by applying a voltage to the IMSTR_ADJ pad with V_{POS} = 3.6V**
  - Provides fine adjustment of the master internal current source
  - Can be used in conjunction with IM[2-0] control
  - IM[2-0] = [011] – Default value for graph below



ISC0404 Unit Cell, Column Buffer Current Adjust Bits CP[2-0]

- **CP[2-0] adjusts the unit cell source follower and column buffer bias currents**
  - Accounts for various operating conditions
  - CP[2-0] defaults to [011] at reset
  - A programmed [000] will decrease all currents to about 0.625x
  - A programmed [111] will increase all currents to about 1.50x

CP2	CP1	CP0	Target Current	%
0	0	0	18.75uA	62.5
0	0	1	22.50uA	75.0
0	1	0	26.25uA	87.5
0	1	1	30uA (Default)	100.0
1	0	0	33.75uA	112.5
1	0	1	37.50uA	125.0
1	1	0	41.25uA	137.5
1	1	1	45.00uA	150.0

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 Column Clamp Level Adjust Bits CL[2-0]

- **CL[2-0] adjusts column buffer clamp level**
  - Accounts for various operating conditions
  - CL[2-0] defaults to [011] at reset
    - Corresponds to ~2.21V dynamic range
  - A programmed [000] will increase the clamping level by about 0.11V
  - A programmed [111] will decrease the clamping level by about 0.14V

CL2	CL1	CL0	Target Clamp Level
0	0	0	2.32V
0	0	1	2.30V
0	1	0	2.25V
0	1	1	2.21V (Default)
1	0	0	2.18V
1	0	1	2.14V
1	1	0	2.11V
1	1	1	2.07V

Note: The above clamp levels are for the default settings for IM, PT and CP bits

ISC0404 Output Multiplexer Buffer Bias Current Adjust Bits MP[1-0]

- **MP[1-0] adjusts the output multiplexer buffer bias current**
  - Accounts for various operating conditions
  - MP[1-0] defaults to [01] at reset
  - A programmed [00] will decrease all currents to about 0.75x
  - A programmed [11] will increase all currents to about 1.5x

MP1	MP0	Target Current	%
0	0	22.5uA	75
0	1	30uA (Default)	100
1	0	37.5uA	125
1	1	45uA	150

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 Output Driver Bias Current Adjust Bits DP[1-0]

- **DP[1-0] adjusts the output driver bias current**
  - Accounts for various operating conditions
  - DP[1-0] defaults to [01] at reset
  - A programmed [00] will decrease all currents to about 0.75x
  - A programmed [11] will increase all currents to about 1.5x

DP1	DP0	Target Current	%
0	0	225uA	75
0	1	300uA (Default)	100
1	0	375uA	125
1	1	450uA	150

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 Detector and Anti-Blooming Buffers Bias Current Adjust Bits BP[1-0]

- **BP[1-0] adjusts the detector and anti-blooming buffers bias current**
  - BP[1-0] defaults to [01] at reset
  - A programmed [00] will decrease all currents to about 0.66x
  - A programmed [11] will increase all currents to about 1.66x

BP1	BP0	Target Current	%
0	0	13.3uA	66
0	1	20uA (Default)	100
1	0	26.7uA	133
1	1	33.3uA	166

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 Detector Bias Definition DE[6-0]

- **DE[6-0] adjusts the detector bias**
  - DE[6-0] defaults to [000 0000] at reset
    - Generates 11 levels of adjustment DE_B[10-0]
  - Detector bias adjustable in about 5mV steps with VPOS = 3.6V and VDET_ADJ floating

	DE[6-0]	Detector Bias T = 77K I_{DET} = 1nA	Detector Bias T = 300K I_{DET} = 1nA
Default →	000 0000	146mV (forward biased)	45mV (forward biased)
	111 1111	-516mV (reverse biased)	-590mV (reverse biased)

~5mV adjustment step with DE[6-0] at 77K

~5mV adjustment step with DE[6-0] at 300K

ISC0404 Detector Bias External Pad Control

- **Detector bias is also adjustable with VDET_ADJ pad**
  - Table below assumes default DE[6-0] setting of [000 0000]

VDET_ADJ	Detector Bias T = 77K I_{DET} = 1nA	Detector Bias T = 300K I_{DET} = 1nA
0.0V	-889mV	-988mV
0.5V	-739mV	-838mV
1.0V	-589mV	-689mV
1.5V	-440mV	-539mV
2.0V	-290mV	-390mV
2.5V	-141mV	-242mV
3.0V	8mV	-94mV
3.6V	185mV	83mV

ISC0404 Anti-Blooming Disable / Injection FET Enable

- **BLM_E and BLM_O perform two functions**
  - BLM_E and BLM_O default is 0 at reset
    - Corresponds to enabling the anti-blooming function
  - A programmed BLM_E = 1 (BLM_O = 0)
    - Disables the anti-blooming function
    - Enables the test injection function of the bloom FET on 16 even columns
  - A programmed BLM_O = 1 (BLM_E = 0)
    - Disables the anti-blooming function
    - Enables the test injection function of the bloom FET on 16 odd columns
  - A programmed BLM_E = 1 and BLM_O = 1
    - Disables the anti-blooming function
    - Enables the test injection function of the bloom FET on all columns

BLM_E	BLM_O	Function
0	0	Anti-Blooming ON (Default)
0	1	BLM FET Injection on 16 Odd Columns
1	0	BLM FET Injection on 16 Even Columns
1	1	BLM FET Injection on All Columns

ISC0404 SHRST, INTRST Reset Current Adjust Bits LP[2-0]

- **LP[2-0] adjusts the current limited clock driver (SHRST, INTRST) bias currents**
  - LP[2-0] defaults to [100] during reset which should correspond to 50uA in master current
  - A programmed [000] will decrease all currents to about 0.20x
  - A programmed [111] will increase all currents to about 1.60x

LP2	LP1	LP0	Target Current	I_{SHRST}	I_{INTRST}
0	0	0	10uA	27nA	34nA
0	0	1	20uA	54nA	68nA
0	1	0	30uA	81nA	102nA
0	1	1	40uA	108nA	136nA
1	0	0	50uA (Default)	135nA	170nA
1	0	1	60uA	162nA	204nA
1	1	0	70uA	189nA	238nA
1	1	1	80uA	216nA	272nA

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 UCSH Rising and Falling Edge Adjust Bits LPD[1-0]

- **LPD[1-0] adjusts the current limited clock driver (UCSH) bias currents**
  - LPD[1-0] defaults to [01] during reset which should correspond to 20uA in master current
  - A programmed [00] will decrease all currents to about 0.50x
  - A programmed [11] will increase all currents to about 2.00x

LPD1	LPD0	Target Current	Approx. T_{RISE}/T_{FALL}
0	0	20uA	4.00us
0	1	40uA (Default)	2.00us
1	0	60uA	1.33us
1	1	80uA	1.00us

Note: The above bias current values are for the default settings for IM and PT bits

ISC0404 Reference Control Bits REF[1-0]

- **REF[1-0] selects reference mode and dead time output level**
  - REF[1] controls power to reference output driver
    - Set REF[1] = 0 if not used
  - REF[0] selects input to reference output
    - Set REF[0] = 0 to select VOUTREF bias from pad
      - Provides common mode system noise from V_{POSOUT}/V_{NEGOUT} supplies
    - Set REF[0] = 1 to select average of 6 reference columns
      - Reference column buffer includes signal path circuitry from unit cell sample / hold node
      - Provides common mode system noise from V_{POSOUT}/V_{NEGOUT} and V_{POS}/V_{NEG} supplies

	REF1	REF0	Reference Output	Reference Source	Dead Time Output Level Source
Default →	0	0	Disabled	N/A	VOUTREF pad
	0	1	Disabled	N/A	Ref Columns
	1	0	Enabled	VOUTREF pad	VOUTREF pad
	1	1	Enabled	Ref Columns	Ref Columns

ISC0404 Non-Destructive Readout

- **NDRO bit selects non-destructive readout operation**
  - Provides a snapshot with multiple readouts of the same scene
  - Unit cell S/H capacitor reset is disabled
  - Unit cell sample and hold is disabled
  - Unit cell reset is not affected

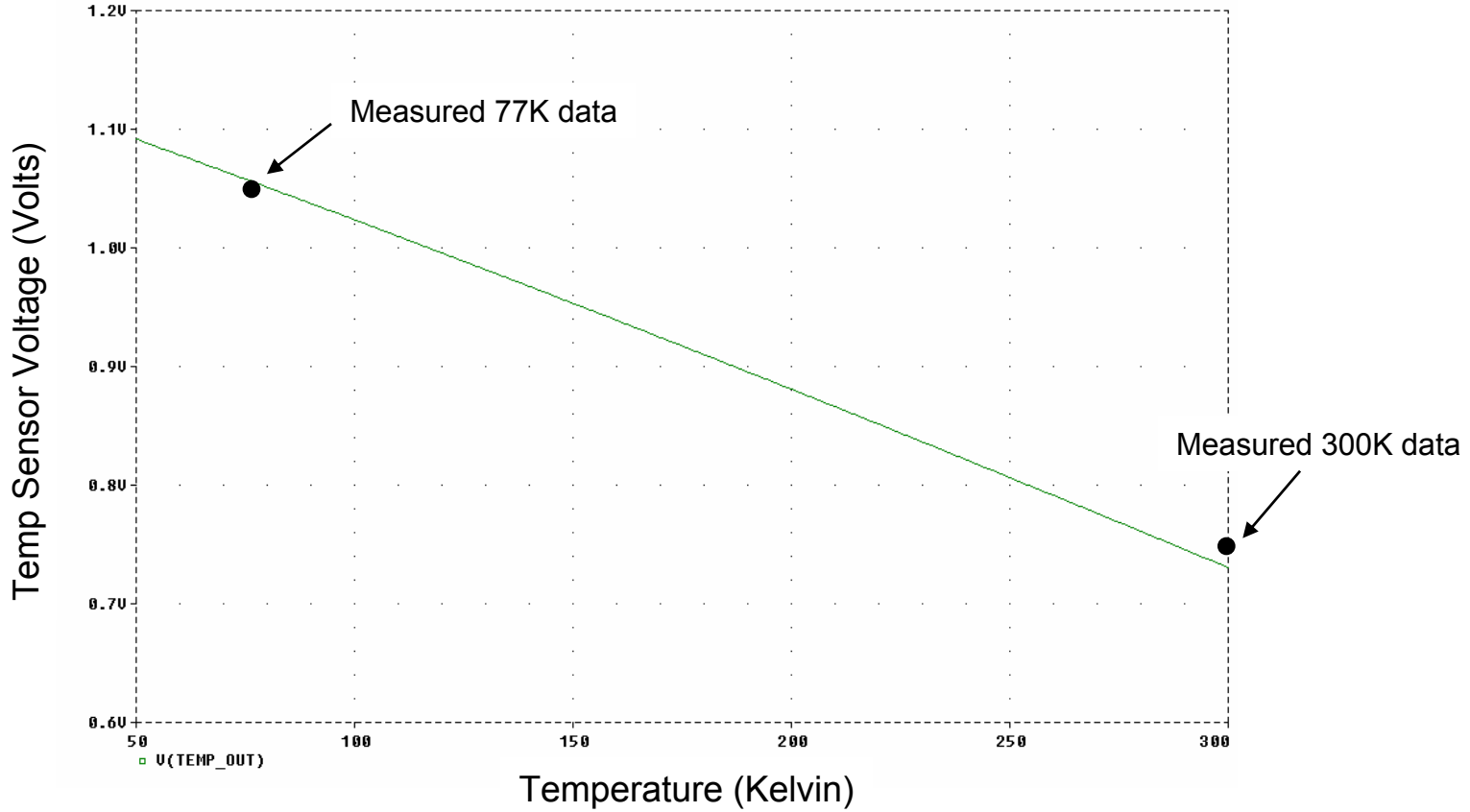
ISC0404 Output Reference

- **Output reference for differential subtraction of common mode noise**
  - N additional columns to average signal path noise
  - Supply induced noise correlated ➔ not averaged down
  - RMS noise reduced by √N with N = number of ref columns
- **REF[1-0] control bits**
  - Bit to switch to external reference voltage if desired REF[0]=1
  - Bit to disable the reference output buffer REF[1]=0
- **Supply induced noise can be reduced externally (if needed)**
  - Subtraction of the reference voltage
  - Reference noise added to signal

$$N_{UCeq.} = \sqrt{N_{UC}^2 + \frac{N_{UCREF}^2}{n}}$$

ISC0404 Temperature Sensor

- **Integrated temperature sensor**
  - Forward biased diode with buffered output
  - V(TEMP) ~ 0.73V at 300K Measured: 0.748V
  - V(TEMP) ~ 1.055V at 77K Measured: 1.05V



ISC0404 Interline Deadtime Reference (OUTA – OUTP)

- During the interline deadtime, either V_{OUTREF} or V_{REF_INT} on OUTA-P
  - REF0 = 0 ➔ V_{OUTREF}(Pad) used
  - REF0 = 1 ➔ V_{REF_INT} used

ISC0404 Camera Level Effects vs. Analog Control (1 of 2)

- **Analog controls optimize power to achieve desired performance at various speeds and temperatures**
  - It is assumed that desired performance is achieved with default conditions
  - Effects described in table for extreme settings

Analog Control	Bits	Camera Level Effects
Temperature Bit PT = 0 default	0 at 77K	Normal operation at 77K (default current settings)
	1 at 300K	Normal operation at 300K (default current settings) ➔ Recommended clock rate = 2.5MHz
	0 at 300K	Currents reduced by 35% ➔ degraded overall performance at clock rate = 2.5MHz (suggest clock rate set at 1MHz)
	1 at 77K	Total power increased by 35% ➔ Overall performance should not be affected ➔ 14MHz data rate operation (not verified)
Master Current IM[2-0] = [011] default	000	Total power reduced by 30% Settling time might not be achieved ➔ Frame to frame crosstalk, dynamic range and linearity will be degraded
	111	Total power increased by 40% ➔ Overall performance should not be affected ➔ 14MHz data rate operation (7MHz clock rate) (not verified)
Column Buffer Currents CP[2-0] = [011] default	000	Column buffer power reduced by about 38% ➔ Frame to frame crosstalk, dynamic range and linearity will be degraded
	111	Column buffer power increased by about 50% ➔ Overall performance should not be affected

ISC0404 Camera Level Effects vs. Analog Control (2 of 2)

Analog Control	Bits	Camera Level Effects
Clamp Level CL[2-0] = [011] default	000	Clamping level increased by about 0.11V ➔ Dynamic range might increase by 0.11V (depending on other dynamic range limits)
	111	Clamping level decreased by about 0.13V ➔ Dynamic range might be reduced by 0.13V (depending on other dynamic range limits)
Column Multiplexer Bias Current MP[1-0] = [01] default	00	Column multiplexer power reduced by 25% Settling time might not be achieved ➔ Frame to frame crosstalk, dynamic range and linearity will be degraded
	11	Column multiplexer power increased by 50% ➔ Overall performance should not be affected
Output Driver Bias Current DP[1-0] = [01] default	00	Output driver power reduced by 25% Output voltage slew and settling time might not be achieved Depending on the output load ➔ Frame to frame crosstalk, dynamic range and linearity will be degraded
	11	Output driver power increased by 50% ➔ Overall performance should not be affected
Detector Bias and Anti-Blooming Buffers Bias Current BP[1-0] = [01] default	00	IG and BLM buffers power reduced by 33% ➔ The detector bias voltage and anti-blooming levels will require more time to settle in the ROIC (the frame to frame modification of the detector bias might be affected)
	11	IG and BLM buffers power increased by 66% ➔ Overall performance should not be affected

- **Performance will be verified during the characterization (default settings)**
- **If needed, other bias settings will be verified for normal operation**

ISC0404
Standard 1k x 1k, 16 Output ROIC

Performance Predictions

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404 Option 1
Noise Performance, 77K

Condition	ROIC Noise		
	Input Referred	Output Referred	Dynamic Range
Requirement	--	--	*≥ 80dB*
Nominal	849e-	150uV	83.1dB
With reference circuitry	965e-	170uV	82.0dB
Worst case 1/f noise parameters, with ref.	1026e-	181uV	81.5dB

- **Temperature = 77K**
- **UC Capacitor $C_{INT}+C_{SH}$ = 884fF**
- **R_OA_D = 1.0E4 Ω-cm^2, C_{DET} = 100fF**
- **15% margin added to transistor noise sources**

ISC0404 Option 2
Noise Performance, 77K

Condition	ROIC Noise		
	Input Referred	Output Referred	Dynamic Range
Requirement	--	--	--
Nominal	245e-	210uV	80.2dB
With reference circuitry	271e-	232uV	79.3dB
Worst case 1/f noise parameters, with ref.	282e-	241uV	79.0dB

- **Temperature = 77K**
- **UC Capacitor $C_{INT}+C_{SH}$ = 182fF**
- **R_OA_D = 1.0E4 Ω-cm^2, C_{DET} = 100fF**
- **15% margin added to transistor noise sources**

ISC0404
Standard 1k x 1k, 16 Output ROIC

Test Plan

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404 Characterization and Wafer Probe Tests (1 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C, W	Full Scale Swing Four Outputs	Test the full scale swing of every pixel.	Set control register anti-bloom bits to current injection on all channels BLM[1-0]=11, four output mode.	Set VDET_ADJ to 3.6V. Acquire full frame data. Set VDET_ADJ to get about 1.9V at output (95% dynamic range). Acquire full frame data.	Subtract the data to determine the delta voltage for each pixel	Compare delta voltage to Pass/Fail criteria
C, W	Shorted Columns Test 1	Check for shorted columns by driving odd and even test channels separately.	Default settings. Operate the chip with two different voltage sources on VTESTINO and VTESTINE input pads.	Initially set VTESTINO and VTESTINE to a low voltage. Acquire output data. Then change VTESTINO to a large voltage(<VPOS). Acquire output data. Then change VTESTINE to the same large voltage as VTESTINO. Acquire output data.	Subtract acquisitions to determine if there is a short (improper response to opposite input voltage) between any even and odd column.	Compare with Pass/Fail criteria
C, W	Multiple Output Test	Test the full array in 4, 8 and 16 output modes and verify outputs and pixel multiplexing.	Set control register anti-bloom bits to current injection on all columns BLM[1-0]=11.	Adjust VDET_ADJ where anti-bloom FETs show noticeable threshold variations. Take frame data in 4, 8 and 16 output modes.	Correlate the full frame data in the 3 output modes.	Compare delta voltage to Pass/Fail criteria
C, W	Invert/Revert Test	Test the invert/revert modes.	Same as multiple output test but with 4 outputs.	Adjust VDET_ADJ where anti-bloom FETs show noticeable threshold variations. Take 4 output frame data in all invert/revert combinations.	Correlate the full frame data in all 4 invert/revert modes.	Compare delta voltage to Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404 Characterization and Wafer Probe Tests (2 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C, W	Power Dissipation	Check power dissipation.	Set anti-bloom mode ON BLM[1-0]=00. VDET_ADJ floating.	Measure all bias supply and total clock current and voltages.	Calculate power.	Compare with Pass/Fail criteria
C, W	Power Dissipation DAC	Check internal bias generation adjustability.	Same as power dissipation test.	Set a different power setting IM[2-0] in the power adjust DAC. Measure all bias supply and total clock current and voltages.	Calculate power.	Compare with Pass/Fail criteria
C, W	Power Dissipation Adjustability	Check power dissipation with external drive pin IMSTR_ADJ	Same as power dissipation test.	Adjust voltage IMSTR_ADJ pad. Measure all bias supply and total clock current and voltages.	Calculate power.	Compare with Pass/Fail criteria
C, W	Window Test	Test the windowing modes.	Same as invert / revert test.	Adjust VDET_ADJ where anti-bloom FETs show noticeable threshold variations. Set WAX[5-0] and WSX[5-0] patterns in the windowing registers, collect frame data and observe the output. Repeat for WAY[6-0] and WSY[6-0].	Correlate the window data to the full frame data.	Compare delta voltage to Pass/Fail criteria.
C, W	Threshold Variation Test	Test injection FET threshold variation by similarity.	Set control register anti-bloom bits to current injection on all channels BLM[1-0]=11. Four output mode.	Sweep VDET_ADJ across range and record the voltage where each pixel turns on.	Find the peak to peak variation in threshold voltage.	Compare delta voltage to Pass/Fail criteria
C, W	Offset Uniformity Test	Test signal path offset uniformity.	Default settings. No injection of signal. Four output mode.	Record the output voltage level of each pixel.	Find the peak to peak variation in output offset.	Compare with Pass/Fail criteria
C, W	Integration Mode Test	Test the ability to switch between IWR and ITR modes.	Set INT mode bit to 0 (IWR), then 1 (ITR).	Take 1 frame of data.	See that each line is repeated by subtracting them from four output, normal mode test data.	Compare delta voltage to Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404 Characterization and Wafer Probe Tests (3 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C, W	Detector Bias DAC	Check internal detector bias adjustability.	Run chip with default settings.	Adjust DE[6-0] and read back VDET_ADJ voltage.	Verify input vs. output changes.	Compare with Pass/Fail criteria
C, W	Temperature Diode Test	Check the on chip temperature diode operability.	Run chip with default settings at room temperature (300K) and at cryogenic temperature (77K).	Read diode voltage on TEMP pad.	--	Compare with Pass/Fail criteria
C, W	Default Operation	Check defaults on control register.	Run chip with default settings.	Acquire full frame data with a [BLM[1-0]=11] source on, then off.	Subtract the data to determine the delta voltage for each pixel.	Compare delta voltage to Pass/Fail criteria
C, W	Reset Test	Check that chip resets to default after initiating a global RST in control register or after applying RESET_B pad voltage	Change chip settings from default.	Acquire data before and after initiating soft reset from control register. Acquire data before and after initiating hard reset from pad.	Compare both data sets taken in default mode (before and after reset).	Compare delta voltage to Pass/Fail criteria
C	Global UCSH Clock Transition Time Adjustability	Check adjustability of current controlled clock UCSH.	Same as power dissipation test.	Change LPD[1-0] through all counts measuring transition location of UCSH clock using the VET	Compare shift in transition point for each LPD[1-0] count.	Compare with Pass/Fail criteria
C	Reset Current Control (Test 1)	Check the control of the unit cell limited current reset looking at the reset current return.	Set control register anti-bloom bits to current injection on all channels BLM[1-0]=11. Observe the transient reset current return through VNEG.	Adjust VDET_ADJ for a full output voltage range. Repeat for all LP[2-0] counts.	Observe the reset current return through VNGE for each LP[2-0] count.	Compare with Pass/Fail criteria
C	Reset Current Control (Test 2)	Check the control of the unit cell limited current reset looking at the residual offset.	Default settings (no injection) . Acquire an image (dark image). Set control register anti-bloom bits to current injection on all channels BLM[1-0]=11. Then remove BLM FET current injection by setting BLM[1-0]=00. Acquire the no-signal image the next frame.	Adjust VDET_ADJ for a full output voltage range. Repeat for all LP[2-0] counts.	Compare the frame acquired right after having removed the signal with the dark image for each LP[2-0] count.	Compare with Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404 Characterization and Wafer Probe Tests (4 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C	Noise	Check noise after integration capacitor.	Operate chip with no current flowing to integration capacitor (default settings).	Acquire data in 4, 8 and 16 output modes.	Calculate sigma for each pixel.	Compare with Pass/Fail criteria
C	Linearity	Check device linearity and integration time control.	Operate chip with a [signal] source so that all devices are at or above 80% full well with a long integration time.	Reduce the integration time and acquire full frame data at each step, with the last step at an integration time of zero.	Calculate pixel means at each integration time. Subtract the zero integration time frame from each pixel. Verify that the delta voltage ratios match the integration time ratios.	Compare with Pass/Fail criteria
C, W	Output Reference Test (1)	Check the operation of the reference output.	Same as power dissipation test. Load the REFOUT pin with 100kOhm to ground.	Set REF[1-0] =00 and 01. Observe that REFOUT goes to ground. Set REF[1-0]=10. Observe that REFOUT follows VREF voltage. Set REF[1-0]=11. Observe REFOUT.	The REFOUT pad voltage should float to ground with REF[1-0]=0X, and to VREF voltage with REF[1-0]=10.	Compare delta voltage to Pass/Fail criteria
C, W	Output Reference Test (2)	Check the operation of the averaged reference columns output.	Inject through bloom circuit on even channels (or odd) to get about 1 Volt output swing.	Set REF[1-0]=11. Set current injection on even (or odd) channels BLM[1-0]=01 or 10.	The REFOUT pad voltage should read the average of the 6 reference columns = (Even+Odd)/6	Compare delta voltage to Pass/Fail criteria
C, W	Clamp Level Test	Check clamp level adjustability.	Operate chip with a [signal] source so that all devices are at full well with a long integration time with CL[2-0]=111	Acquire full frame data for each CL[2-0] setting.	Calculate pixel means at each CL[2-0] setting.	Compare with Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404 Characterization and Wafer Probe Tests (5 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C	FSYNC Boundary Tests	Check that the internal clocks are operating at the documented FSYNC boundary points.	Same as invert / revert test.	Check boundary conditions in both ITR and IWR modes.	Verify that appropriate clocks are operating as expected using the VET.	Compare with Pass/Fail criteria (minimum perturbation at the output)
C	Valid Falling FSYNC Location Test	Check valid region where FSYNC can fall and not create an offset.	Same as invert/revert test. Set chip in IWR mode.	Change location of falling edge of FSYNC with respect to rising edge of LSYNC and acquire full frame data at each step within a line time.	Calculate pixel means at each falling FSYNC location. Process data to verify optimum falling edge location of FSYNC.	Compare with Pass/Fail criteria
C	Inserted Line Dead Time Test	Check that inserting line dead time modified the appropriate edges of internal analog control timing clocks.	Same as invert / revert test.	Insert line dead time. Verify that the appropriate internal clock locations or pulse widths are as predicted.	One at a time, set VET to observe internal analog control clocks for each inserted dead time.	Compare with Pass/Fail criteria
C	End Of Readout To Analog Control Clocks Test	Check that changing the window size (and thereby changing the end of readout location) modifies the appropriate edges of internal analog control timing clocks.	Same as invert / revert test.	Modify readout window size. Verify that the appropriate internal clock locations or pulse widths are as predicted.	One at a time, set VET to observe internal analog control clocks for each inserted dead time.	Compare with Pass/Fail criteria
C	Crosstalk Test	Characterize the crosstalk effect for different BLM FET injection currents.	Default settings (no injection). Acquire an image (dark image). Set control register anti-bloom bits to current injection on all channels BLM[1-0]=11. acquire image. Repeat for injection on odd and even channels.	Set VDET_ADJ to 3.6V. Acquire full frame data. Set VDET_ADJ to get about 1.9V at output (95% dynamic range).	Subtract flat field from dark image and observe dispersion. Subtract odd injection image from dark image and observer crosstalk on even columns. Repeat for even injection.	Compare with Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404 Characterization and Wafer Probe Tests (6 of 6)

Test Phase*	Test Name	Description	Setup	Stimulus and Data Acquisition	Data Reduction	Pass / Fail
C	Input Clock Levels	Determine clock level operation minimums.	Run chip with default settings.	Observe operation while decreasing high level of input CLK.	Record minimum clock level of input CLK which results in normal operation.	Compare with Pass/Fail criteria
C	Maximum Pixel Rate	Determine maximum rate chip runs at.	Run chip with default settings.	Observe operation while increasing CLK frequency.	Record maximum CLK frequency which results in normal operation.	Compare with Pass/Fail criteria
C	Internal Pull Up	Check internal pull-up current levels.	Run chip with default settings.	Measure current draw on RESET_B pad.	Record current level.	Compare with Pass/Fail criteria
C, W	NDRO Mode Test	Test the ability to switch into NDRO mode.	Set NDRO mode bit to 0 (normal). Inject signal into array with BLM_E, BLM_O =1. Set NDRO bit to 1 (NDRO). Change injected signal.	Observe change in operation of UCSH_VP between modes at VET output.	Verify that change in injected signal causes no change at output in NDRO mode.	Compare with Pass/Fail criteria
C, W	Window Overflow Test	Check operation of window overflow.	Run chip with default settings. Program window size that exceeds edge of chip.	Acquire before (full frame) and after window programming images.	Verify that window programming does not cause faulty data to appear at output.	Compare with Pass/Fail criteria
C	Test Row Readout	Check operation of test row.	Run chip with default settings. Set TR = 1. Change VTESTINE, VTESTINO voltages.	Observe data output on scope.	Verify variation of voltage levels of last line of data with VTESTINE and VTESTINO inputs.	Compare with Pass/Fail criteria
C	IWR Mode Column 2 Pt. Corrected Response Uniformity	Characterize the column 2pt corrected response uniformity for IWR mode.	REF[1-0]=[00], INT=0. Drive VTESTINO and VTESTINE with the same stimulus “VTESTIN” (calibrated-measured) from 0 to 3.6V by TBD mV.	Acquire mean and sigma (noise) during the line active time for all outputs including REFOUT during the test row data readout	Calculate instantaneous deviation from data to a 2 point line fit of data. Compute max-min of deviation over output range for all channels.	Compare with Pass/Fail criteria
C	ITR Mode Column 2 Pt. Corrected Response Uniformity	Characterize the column 2pt corrected response uniformity for ITR mode.	REF[1-0]=[00], INT=1. Drive VTESTINO and VTESTINE with the same stimulus “VTESTIN” (calibrated-measured) from 0 to 3.6V by TBD mV.	Acquire mean and sigma (noise) during the line active time for all outputs including REFOUT during the test row data readout	Calculate instantaneous deviation from data to a 2 point line fit of data. Compute max-min of deviation over output range for all channels.	Compare with Pass/Fail criteria

* Test Phase C: Characterization Test W: Wafer Probe Test

ISC0404
Standard 1k x 1k, 16 Output ROIC

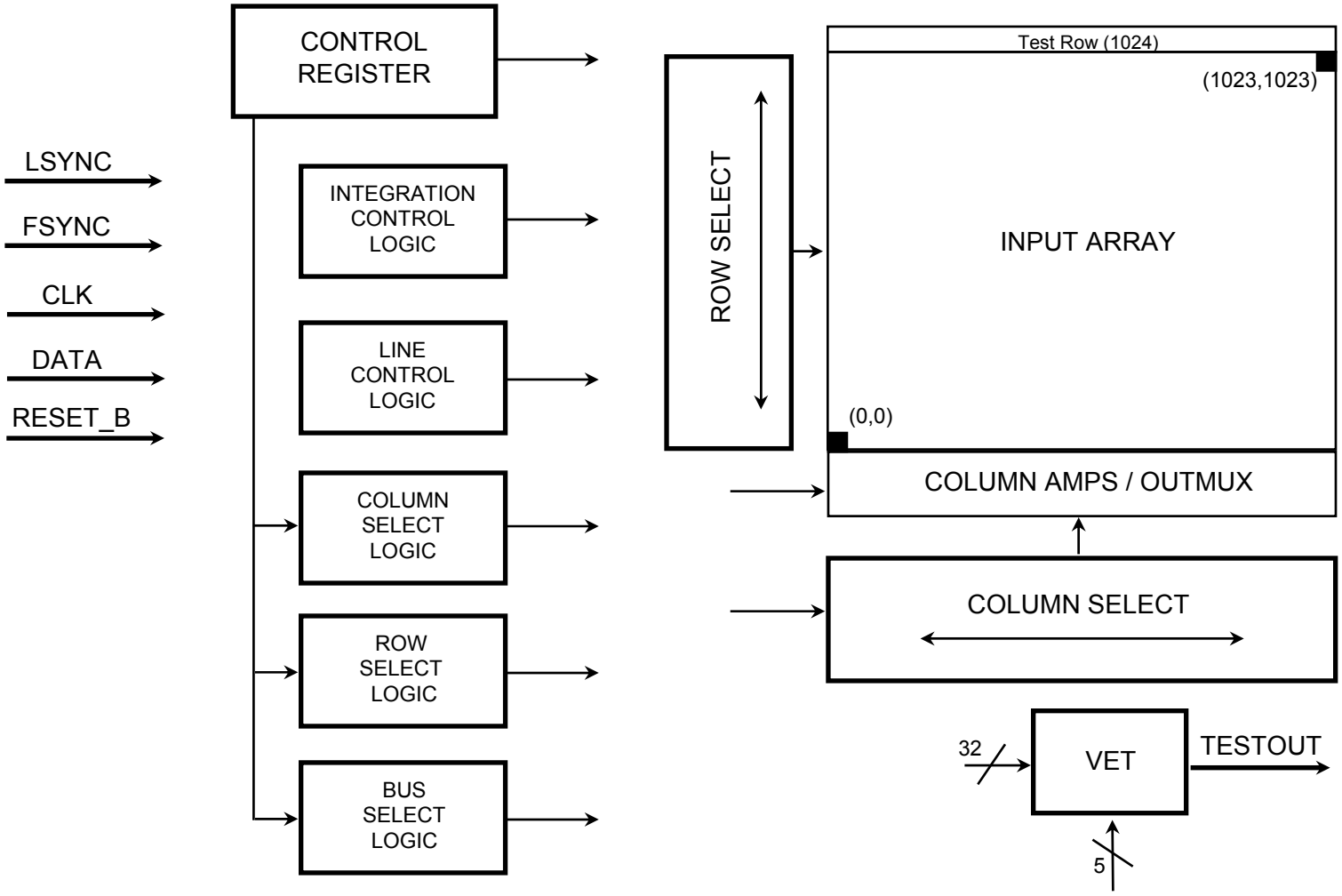
Digital Design

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404
Logic Summary

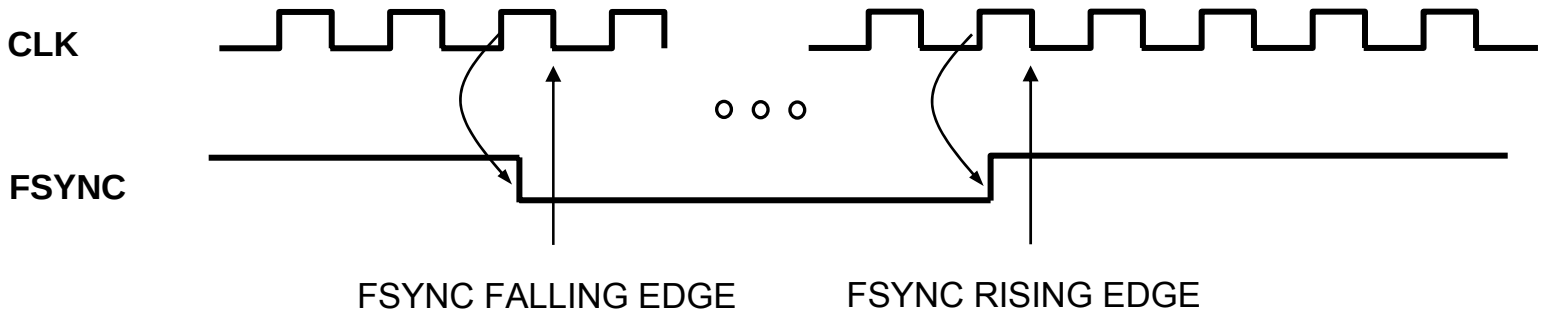
- **Serial Control Interface**
- **Variable Integration Time**
- **Snapshot Integration**
  - Integrate Then Read **OR** Integrate While Read
  - Non-Destructive Readout (IWR or ITR)
    - Multiple Window Readouts From Single Integration (NDRO)
- **Invert / Revert**
  - Bidirectional Scan in both X and Y Dimensions
- **4, 8 or 16 Output Modes**
- **Windowing**
- **Flexible Frame, Line Timing**
  - Controlled by FSYNC, LSYNC Clocks
  - Dead time can be inserted at end of line and end of frame

ISC0404
Logic Block Diagram



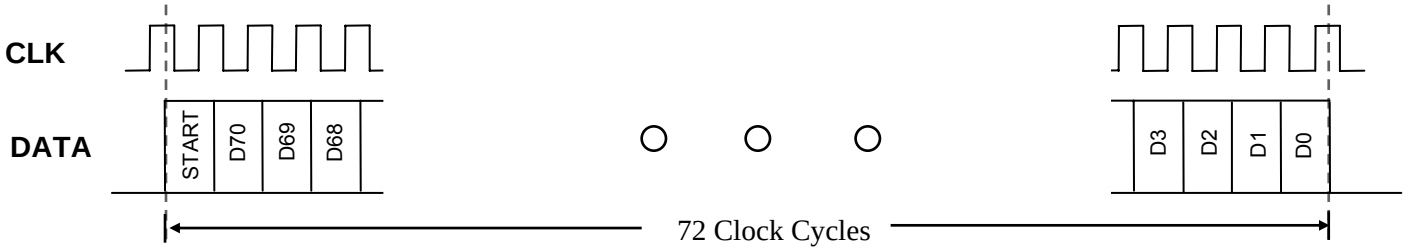
ISC0404
Signal Timing Definition

- DATA, LSYNC and FSYNC Signals Are Internally Synchronized on CLK Falling Edge
- By Definition FSYNC and LSYNC Rising or Falling Edge Refer To The Falling CLK Edge Where The Internally Synchronized Signals Transition
- Most Robust Timing Would Be For The System Electronics To Change Signals With The Previous Rising Edge Of The CLK



ISC0404
Control Register

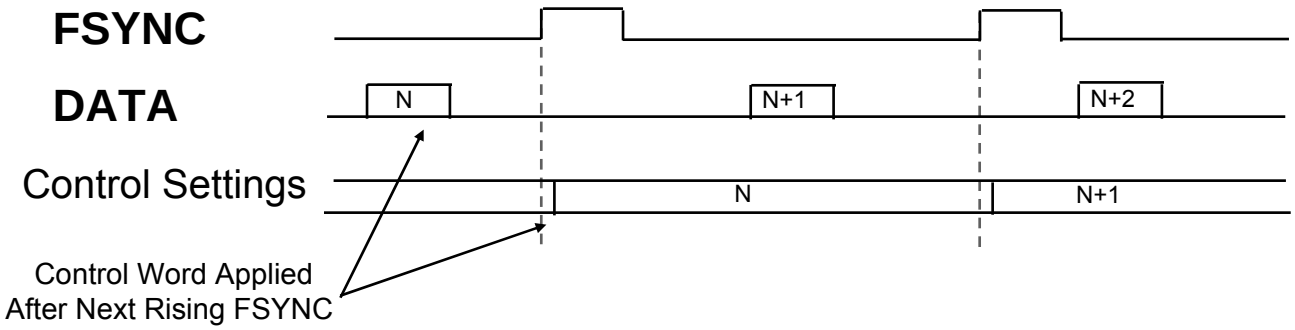
- **Serial Data Interface for Controlling Operation Modes, Gain, etc.**
- **Programming Clock Definition:**



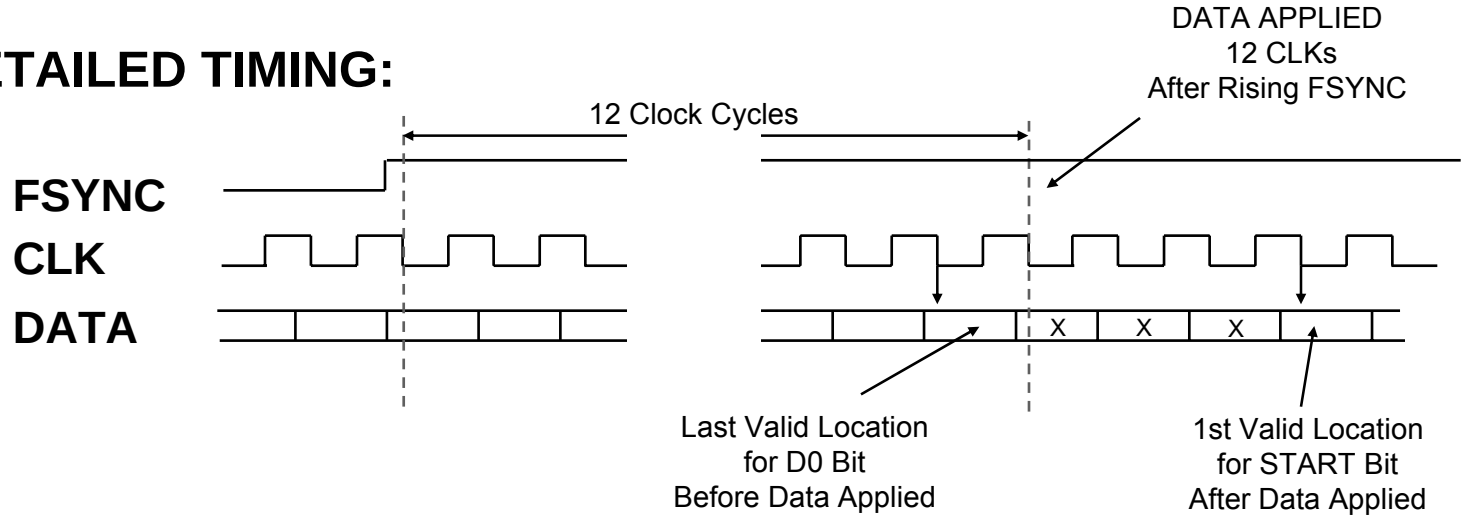
- **Control Data only Required when Settings Are Changing**
- **START Bit Always = 1**
- **71 Data Bits (D70-D0) Control ROIC Functions.**
- **DATA Sampled Internally On Falling CLK Edge**
- **Data is held and Applied After Next Rising Edge of FSYNC**

ISC0404
Control Register Timing (1 of 2)

FRAME TIMING:



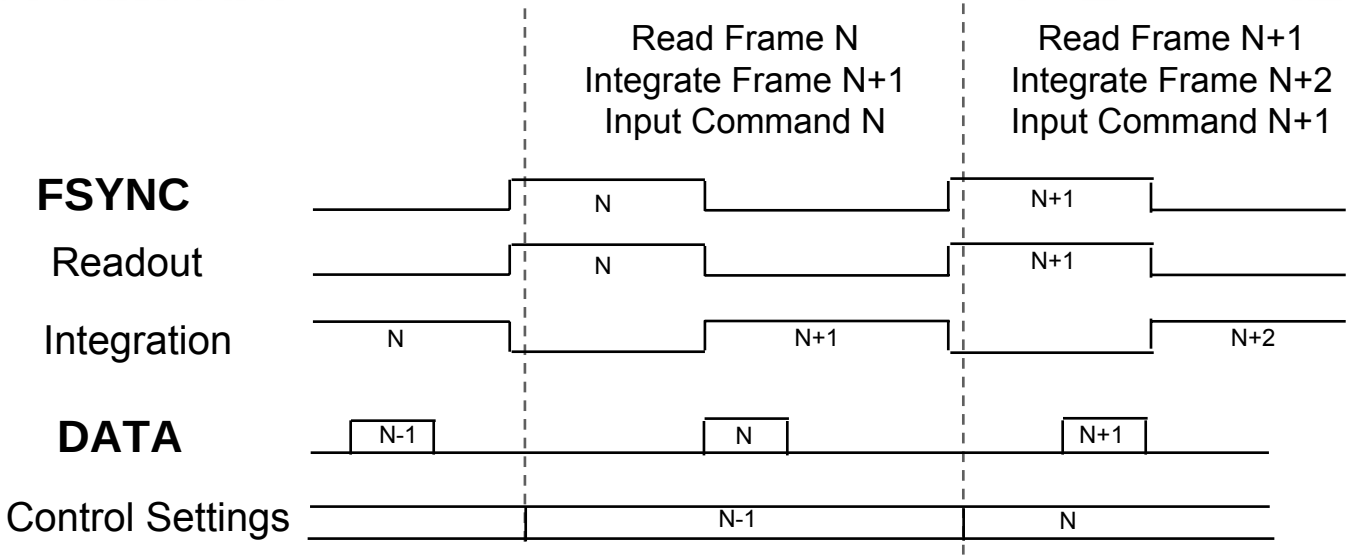
DETAILED TIMING:



ISC0404
Control Register Timing (2 of 2)

- **Valid Control Word has Rising Edge of START Bit:**
  - > 72 Clock Cycles Before Data Applied
  - > 3 Clock Cycles After Data Applied
- **If New Control Word Has Not Been Completed By Time Data Is Applied, Existing Settings Are Used**
  - DATA Bits Sent Before Data Application Are Ignored.
  - DATA Bits Seen At Or After 1st Valid Location For START Bit Will Be Seen As New Control Word

ISC0404
Control Register Setting Latency



SETTING(S)	DATA SENT	SETTINGS AFFECT
Integration (Det Bias, Bloom Ctl, Etc.)	**N**	**Integration N+2 Readout N+2**
Readout (Windowing, Direction, Outputs, Etc.)	**N**	**Readout N+1**

ISC0404
Control Bit Definition (1 of 3)

- **Control Register Controls The Following Functions:**
  - Window Size and Location
  - Readout Direction
  - Power Control
  - Detector Bias
  - Integration Mode (IWR or ITR)
  - Non-Destructive Readout Mode
  - Test Modes
  - 4, 8 or 16 Outputs
  - Reference Output Enable
  - Global Reset

									D 70	D 69	D 68	D 67	D 66	D 65	D 64
									WAX5	WAX4	WAX3	WAX2	WAX1	WAX0	WAY6
D 63	D 62	D 61	D 60	D 59	D 58	D 57	D 56	D 55	D 54	D 53	D 52	D 51	D 50	D 49	D 48
WAY5	WAY4	WAY3	WAY2	WAY1	WAY0	WSX5	WSX4	WSX3	WSX2	WSX1	WSX0	WSY6	WSY5	WSY4	WSY3
D 47	D 46	D 45	D 44	D 43	D 42	D 41	D 40	D 39	D 38	D 37	D 36	D 35	D 34	D 33	D 32
WSY2	WSY1	WSY0	PT	IM2	IM1	IM0	CP2	CP1	CP0	CL2	CL1	CL0	MP1	MP0	DP1
D 31	D 30	D 29	D 28	D 27	D 26	D 25	D 24	D 23	D 22	D 21	D 20	D 19	D 18	D 17	D 16
DP0	BP1	BP0	DE6	DE5	DE4	DE3	DE2	DE1	DE0	BLM_E	BLM_O	LP2	LP1	LP0	LPD1
D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
LPD0	REF1	REF0	NDRO	INT	INV	REV	TR	OM1	OM0	VET4	VET3	VET2	VET1	VET0	MRST

ISC0404
Control Bit Definition (2 of 3)

BIT #	BIT NAME	FUNCTION	DEFINITION	DEFAULT
70-65	WAX[5-0]	Column Window Start Address	See Window Address Definition	00 0000 (Full Window)
64-58	WAY[6-0]	Row Window Start Address	See Window Address Definition	000 0000 (Full Window)
57-52	WSX[5-0]	Column Window Size	See Window Address Definition	11 1111 (Full Window)
51-45	WSY[6-0]	Row Window Size	See Window Address Definition	111 1111 (Full Window)
44	PT	Global Power Adjust (Temperature)	See Analog Section	0
43-41	IM[2-0]	Master Bias Current Adjust	See Analog Section	0 1 1
40-38	CP[2-0]	Column Buffer Bias Adjust	See Analog Section	0 1 1
37-35	CL[2-0]	Column Bus Clamp Level Adjust	See Analog Section	0 1 1
34-33	MP[1-0]	Mux Buffer Bias Adjust	See Analog Section	0 1
32-31	DP[1-0]	Output Driver Bias Adjust	See Analog Section	0 1
30-29	BP[1-0]	Det. Bias & Anti-Bloom Bias Buffer Adjust	See Analog Section	0 1
28-22	DE[6-0]	Det. Bias Adjust	See Analog Section	000 0000
21	BLM_E	Even Column Test Enable	See Analog Section	0
20	BLM_0	Odd Column Test Enable	See Analog Section	0
19-17	LP[2-0]	Unit Cell Clock Rise / Fall Adjust	See Analog Section	1 0 0
16-15	LPD[1-0]	Global Driver Adjust	See Analog Section	0 1
14-13	REF[1-0]	Reference Column / Refernce Buffer	See Analog Section	0 0

- **Default Values Occur:**
  - At Power-Up
  - When RESET_B Pad Is Pulsed Low
  - After Master Reset Command

ISC0404
Control Bit Definition (3 of 3)

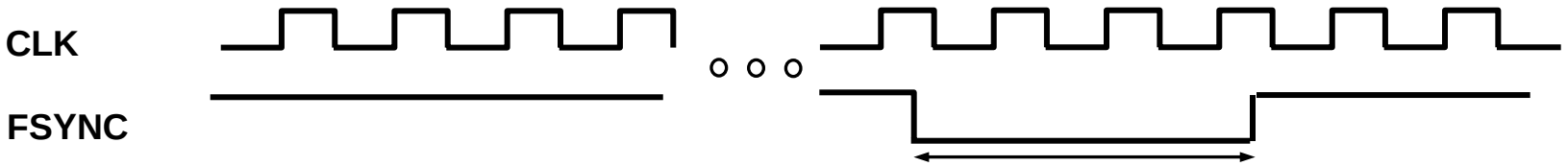
BIT #	BIT NAME	FUNCTION	DEFINITION	DEFAULT
12	NDRO	Enable Non-Destructive Readout	0 = Disable Non-Destructive Readout 1 = Enable Non-Destructive Readout	0 = Disable Non-Destructive Readout
11	INT	Select Integration Mode	0 = Integrate While Read (IWR = 1) 1 = Integrate Then Read (ITR = 1)	0 = Integrate While Read (IWR = 1)
10	INV	Row Readout Direction	0 = Row Scan 0 --> 1023 (UP = 1) 1 = Row Scan 1023 --> 0 (DN = 1)	0 = Row Scan 0 --> 1023 (UP = 1)
9	REV	Column Readout Direction	0 = Column Scan 0 --> 1023 (LR = 1) 1 = Column Scan 1023 --> 0 (RL = 1)	0 = Column Scan 0 --> 1023 (LR = 1)
8	TR	Enable Test Row Readout	0 = Disable Test Row Readout 1 = Enable Test Row Readout	0 = Disable Test Row Readout
7-6	OM[1-0]	Select Number of Outputs	00 , 01 = 4 Outputs 10 = 8 Outputs 11 = 16 Outputs	0 0 - 4 Outputs
5-1	VET[4-0]	Vector Enabled Test Address	Binary Address 0-31	0 0 0 0 0
0	MRST	Reset to Power Up Condition		N / A

- **Default Values Occur:**
  - At Power-Up
  - When RESET_B Pad Is Pulsed Low
  - After Master Reset Command

Note: VET ADDR Reset ONLY BY Commanded Reset OR PWRUP

ISC0404
FSYNC Pulse Timing

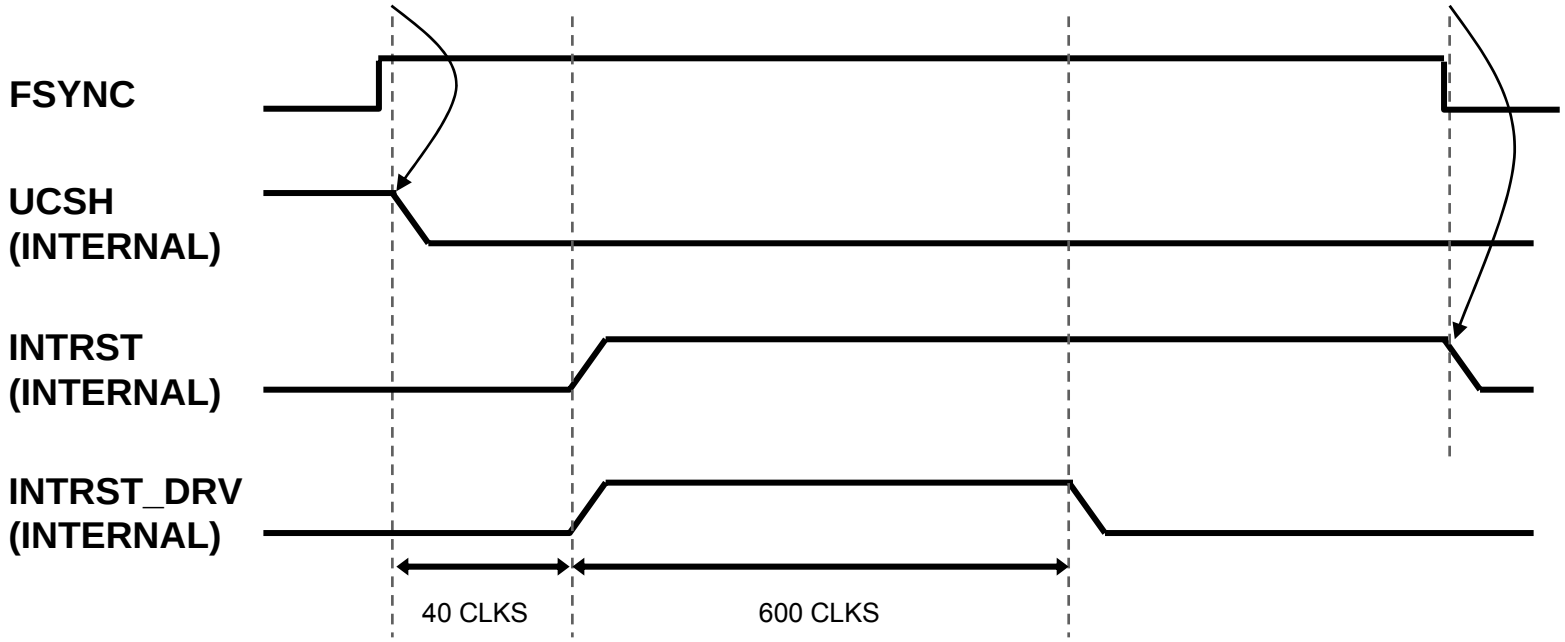
- **IWR or ITR Modes**



Min Delay: Falling Edge FSYNC to Rising Edge FSYNC = 3 CLK CYCLES
- 480nSec @ 12.5MHz Pixel Rate
- 600nSec @ 10.0MHz Pixel Rate

ISC0404 FSYNC Pulse Timing: Rising Edge

IWR or ITR Modes

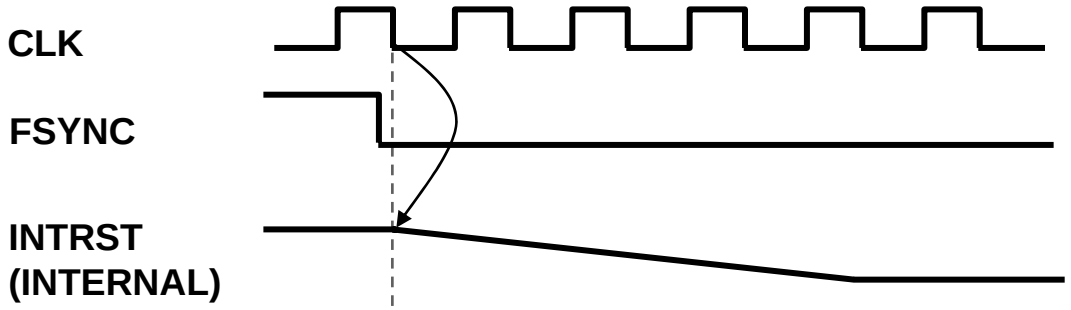


ISC0404 FSYNC Pulse Timing: Falling Edge

IWR or ITR Modes

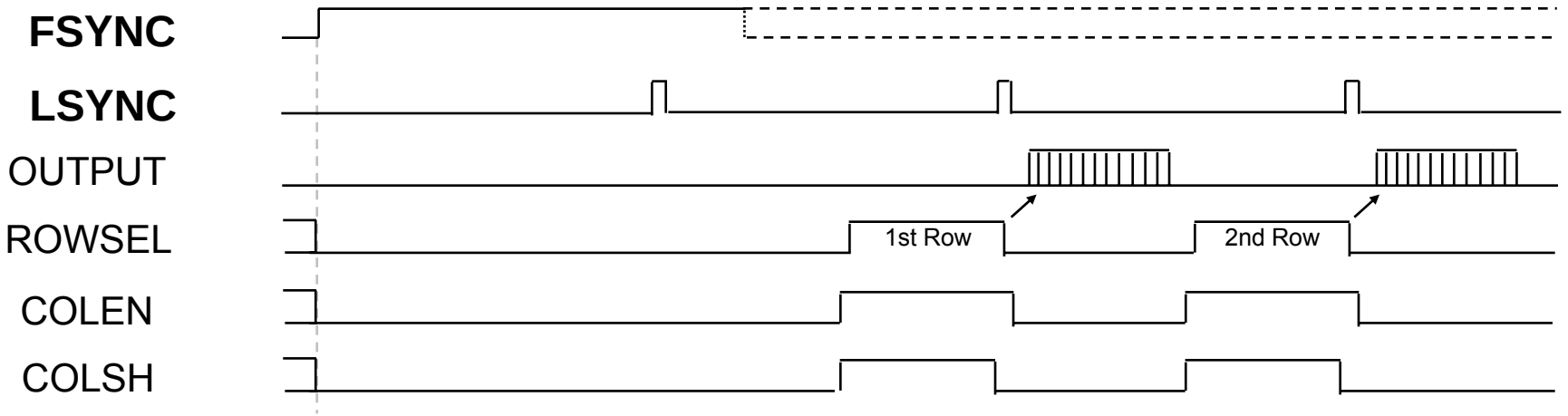
SEE ANALOG CONTROL TIMING FOR RECOMMENDED PLACEMENT OF FSYNC FALLING EDGE WITHIN A LINE TIME

FSYNC SETUP TIME > 0

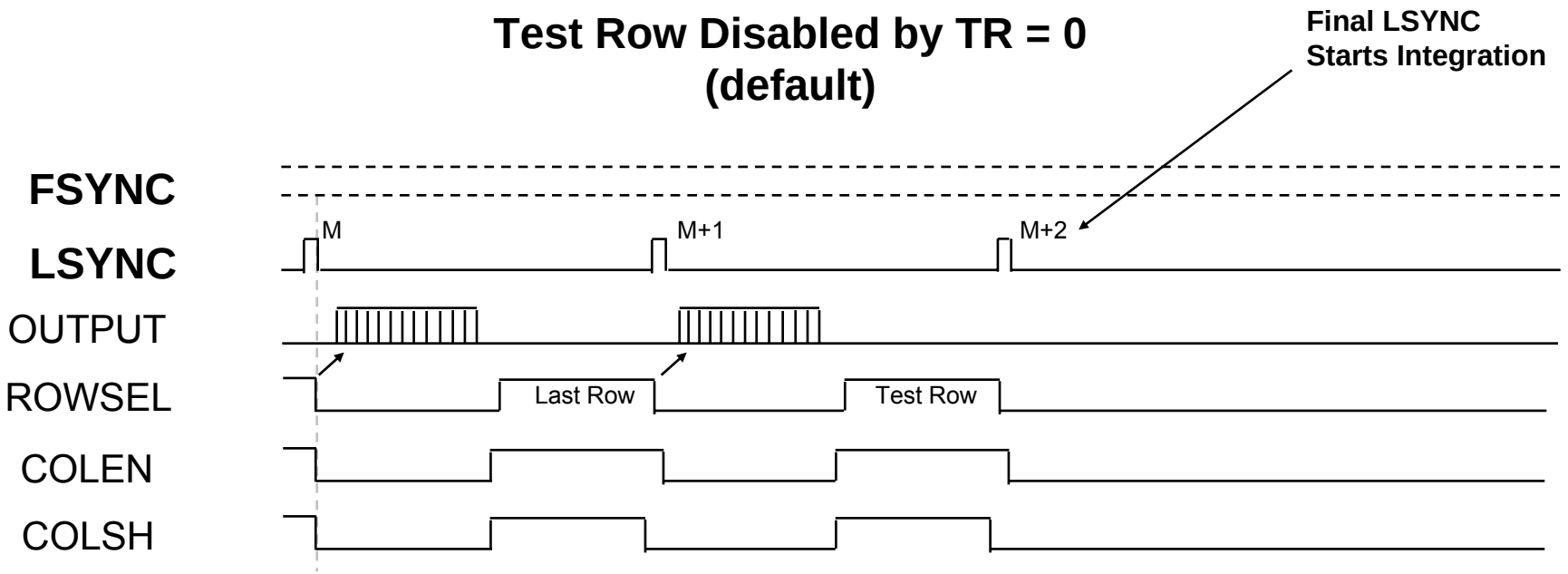


INTRST PULSE BEGINS FALL ON 1ST CLK FALLING EDGE AFTER FSYNC FALLING EDGE

ISC0404
Frame Readout Start



ISC0404
Frame Readout End no Test Row

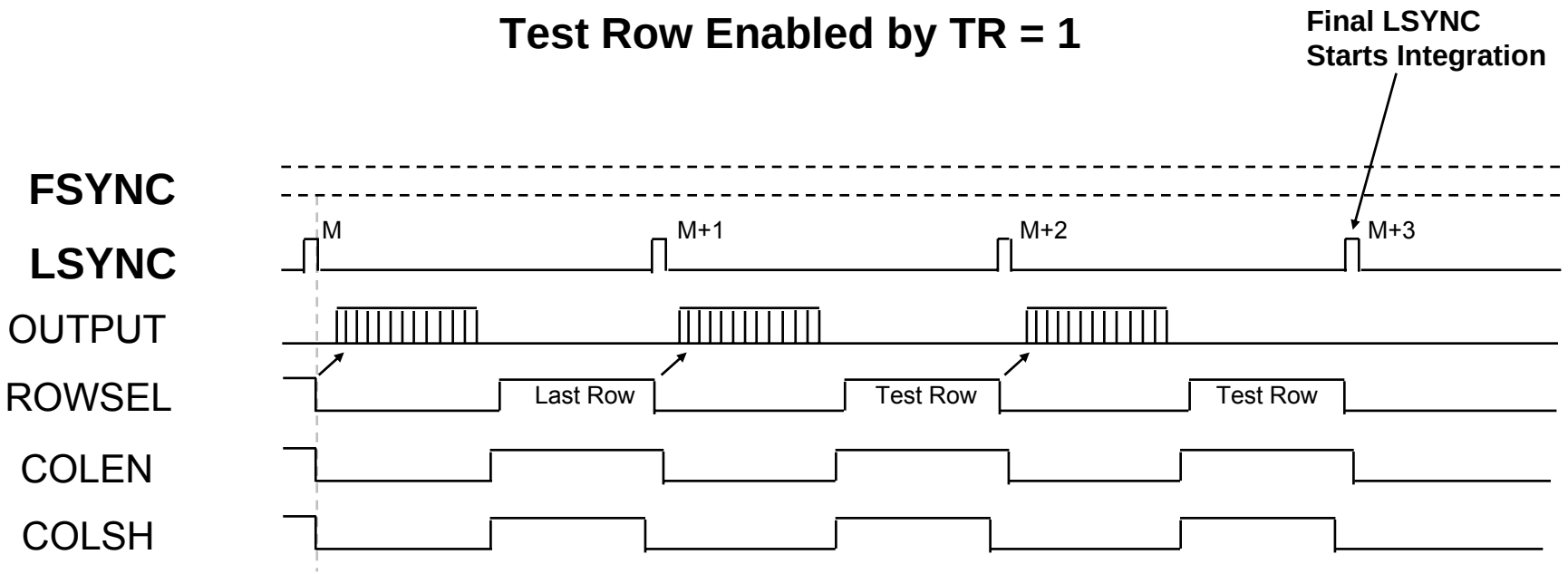


Window of M Rows

Readout Time = M+1 Lines

LSYNCs Required = M+2

ISC0404
Frame Readout End w/ Test Row

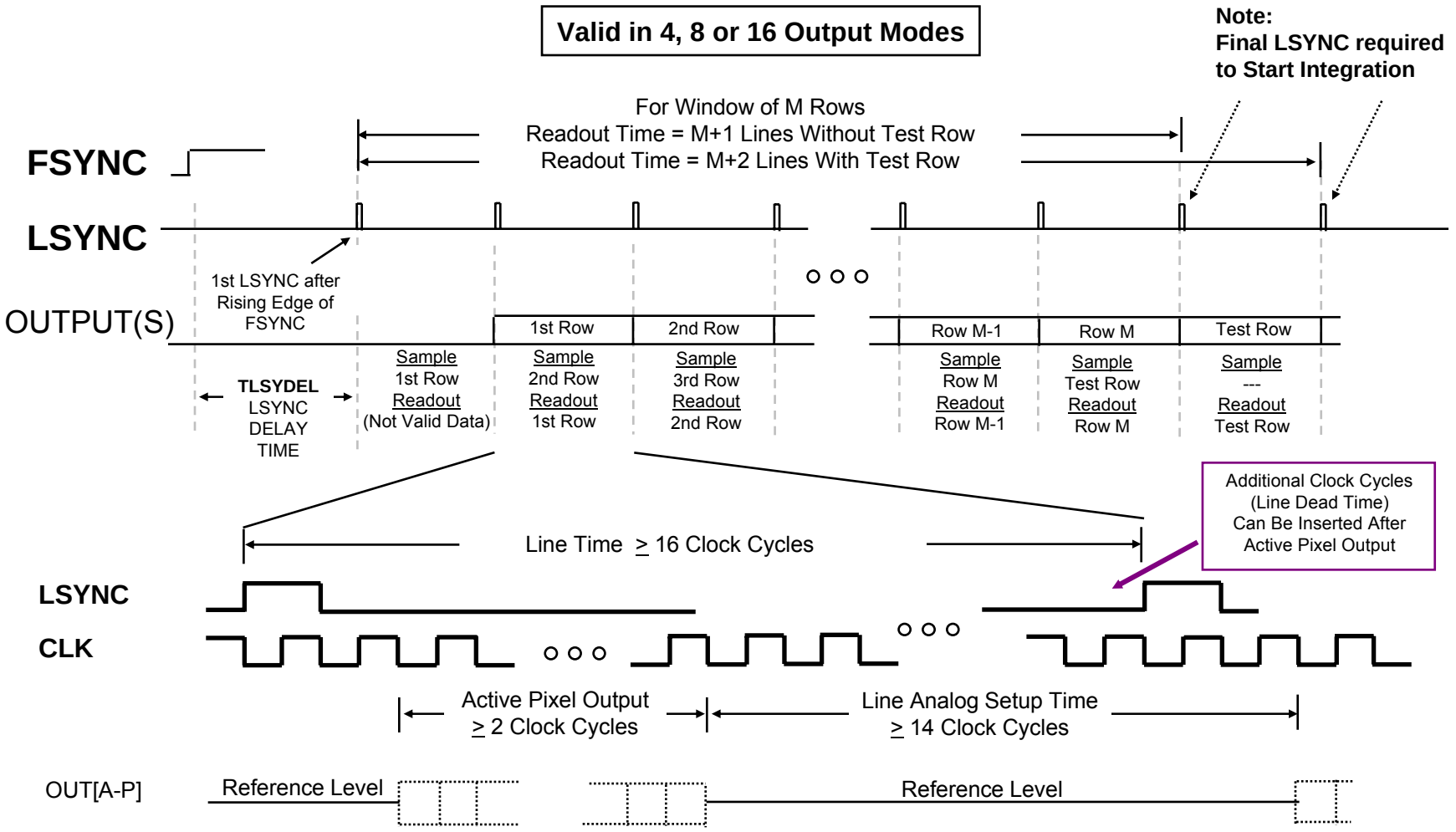


Window of M Rows

Readout Time = M+2 Lines

LSYNCs Required = M+3

ISC0404
Frame Readout Detail



ISC0404
Column Readout Order (1 of 3)

4 Outputs, Full Window, LR Readout Direction
OM[1-0]= 0 0 & REV=0

–OUTA	0	4	…	1016	1020
–OUTB	1	5	…	1017	1021
–OUTC	2	6	…	1018	1022
–OUTD	3	7	…	1019	1023
–OUTE	X	X	…	X	X
–OUTF	X	X	…	X	X
–OUTG	X	X	…	X	X
–OUTH	X	X	…	X	X
–OUTI	X	X	…	X	X
–OUTJ	X	X	…	X	X
–OUTK	X	X	…	X	X
–OUTL	X	X	…	X	X
–OUTM	X	X	…	X	X
–OUTN	X	X	…	X	X
–OUTO	X	X	…	X	X
–OUTP	X	X	…	X	X

4 Outputs, Full Window, RL Readout Direction
OM[1-0]= 0 0 & REV=1

–OUTA	1020	1016	…	4	0
–OUTB	1021	1017	…	5	1
–OUTC	1022	1018	…	6	2
–OUTD	1023	1019	…	7	3
–OUTE	X	X	…	X	X
–OUTF	X	X	…	X	X
–OUTG	X	X	…	X	X
–OUTH	X	X	…	X	X
–OUTI	X	X	…	X	X
–OUTJ	X	X	…	X	X
–OUTK	X	X	…	X	X
–OUTL	X	X	…	X	X
–OUTM	X	X	…	X	X
–OUTN	X	X	…	X	X
–OUTO	X	X	…	X	X
–OUTP	X	X	…	X	X

ISC0404
Column Readout Order (2 of 3)

8 Outputs, Full Window, LR Readout Direction
OM[1-0]= 0 1 & REV=0

–OUTA	0	8	…	1008	1016
–OUTB	1	9	…	1009	1017
–OUTC	2	10	…	1010	1018
–OUTD	3	11	…	1011	1019
–OUTE	4	12	…	1012	1020
–OUTF	5	13	…	1013	1021
–OUTG	6	14	…	1014	1022
–OUTH	7	15	…	1015	1023
–OUTI	X	X	…	X	X
–OUTJ	X	X	…	X	X
–OUTK	X	X	…	X	X
–OUTL	X	X	…	X	X
–OUTM	X	X	…	X	X
–OUTN	X	X	…	X	X
–OUTO	X	X	…	X	X
–OUTP	X	X	…	X	X

8 Outputs, Full Window, RL Readout Direction
OM[1-0]= 0 1 & REV=1

–OUTA	1016	1008	…	8	0
–OUTB	1017	1009	…	9	1
–OUTC	1018	1010	…	10	2
–OUTD	1019	1011	…	11	3
–OUTE	1020	1012	…	12	4
–OUTF	1021	1013	…	13	5
–OUTG	1022	1014	…	14	6
–OUTH	1023	1015	…	15	7
–OUTI	X	X	…	X	X
–OUTJ	X	X	…	X	X
–OUTK	X	X	…	X	X
–OUTL	X	X	…	X	X
–OUTM	X	X	…	X	X
–OUTN	X	X	…	X	X
–OUTO	X	X	…	X	X
–OUTP	X	X	…	X	X

ISC0404
Column Readout Order (3 of 3)

16 Outputs, Full Window, LR Readout Direction
OM[1-0]= 1 X & REV=0

–OUTA	0	16	…	992	1008
–OUTB	1	17	…	993	1009
–OUTC	2	18	…	994	1010
–OUTD	3	19	…	995	1011
–OUTE	4	20	…	996	1012
–OUTF	5	21	…	997	1013
–OUTG	6	22	…	998	1014
–OUTH	7	23	…	999	1015
–OUTI	8	24	…	1000	1016
–OUTJ	9	25	…	1001	1017
–OUTK	10	26	…	1002	1018
–OUTL	11	27	…	1003	1019
–OUTM	12	28	…	1004	1020
–OUTN	13	29	…	1005	1021
–OUTO	14	30	…	1006	1022
–OUTP	15	31	…	1007	1023

16 Outputs, Full Window, RL Readout Direction
OM[1-0]= 1 X & REV=1

–OUTA	1008	992	…	16	0
–OUTB	1009	993	…	17	1
–OUTC	1010	994	…	18	2
–OUTD	1011	995	…	19	3
–OUTE	1012	996	…	20	4
–OUTF	1013	997	…	21	5
–OUTG	1014	998	…	22	6
–OUTH	1015	999	…	23	7
–OUTI	1016	1000	…	24	8
–OUTJ	1017	1001	…	25	9
–OUTK	1018	1002	…	26	10
–OUTL	1019	1003	…	27	11
–OUTM	1020	1004	…	28	12
–OUTN	1021	1005	…	29	13
–OUTO	1022	1006	…	30	14
–OUTP	1023	1007	…	31	15

ISC0404
Window Register Summary

* Note - WAX & WAY Starting addresses are relative to the selected readout order.

Programmable Window Definition

	Window Address X (WAX) *Column Starting Address						Window Address Y (WAY) *Row Starting Address							Window Size X (WSX) Size in Columns						Window Size Y (WSY) Size in Rows						
	5	4	3	2	1	0	6	5	4	3	2	1	0	5	4	3	2	1	0	6	5	4	3	2	1	0
4 Output Mode																										
Valid Bits	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
Binary Value Represents	Start Column / 16						Start Row / 8							(Column Size/ 16) -1						(Row Size / 8) -1						
8 Output Mode																										
Valid Bits	V	V	V	V	V	x	V	V	V	V	V	V	V	V	V	V	V	V	x	V	V	V	V	V	V	V
Binary Value Represents	Start Column / 32						Start Row / 8							(Column Size/ 32) -1						(Row Size / 8) -1						
16 Output Mode																										
Valid Bits	V	V	V	V	x	x	V	V	V	V	V	V	V	V	V	V	V	x	x	V	V	V	V	V	V	V
Binary Value Represents	Start Column / 64						Start Row / 8							(Column Size/ 64) -1						(Row Size / 8) -1						

ISC0404
Window Address Columns

- **Control Word WAX[5-0] Represents Window Column Starting Address**
- **Window Starting Address is Relative to Origin for Selected Readout Order**
  - LR Readout (REV=0) : Origin Column = 0
  - RL Readout (REV=1) : Origin Column = 1023
- **X-Dimension Address Resolution Output Mode Dependent**
  - 4 Output Mode (OM[1-0]=00): Resolution = 16 Columns
  - 8 Output Mode (OM[1-0]=01): Resolution = 32 Columns
  - 16 Output Mode (OM[1-0]=1x): Resolution = 64 Columns
- **Address is Defined As Follows:**
  - 4 Output Mode: Start Address = WAX[5-0], Multiply x 16
    - Example: WAX[5-0] = 01 0000, (Decimal Value = 16) Start Address = Column 256
    - LR Readout : First Column = 256.
    - RL Readout : First Column = 1023-256 = 767
  - 8 Output Mode: Start Address = WAX[5-1], Multiply x 32
    - Example: WAX[5-0] = 01 000x, (Decimal Value = 8) Start Address = Column 256
    - LR Readout : First Column = 256.
    - RL Readout : First Column = 1023-256 = 767
  - 16 Output Mode: Start Address = WAX[5-2], Multiply x 64. WAX[0] = Don't Care
    - Example: WAX[5-0] = 00 01xx, (Decimal Value = 1) Start Address = Column 64
    - LR Readout : First Column = 64
    - RL Readout : First Column = 1023-64 = 959
- **Valid WAX[5-0] Range**
  - 4 Output Mode: 00 0000 (Column 0 : LR) to 11 1111 (Column 1008 : LR)
  - 8 Output Mode: 00 000x (Column 0 : LR) to 11 111x (Column 992 : LR)
  - 16 Output Mode: 00 00xx (Column 0 : LR) to 11 11xx (Column 960 : LR)

ISC0404
Window Address Rows

- **Control Word WAY[6-0] Represents Window Row Starting Address**
- **Window Starting Address is Relative to Origin for Selected Readout Order**
  - UP Readout (INV=0) : Origin Row = 0
  - DN Readout (INV=1) : Origin Row = 1023
- **Y-Dimension Address Resolution is NOT Output Mode Dependent**
  - Resolution = 8 Rows
- **Address is Defined As Follows:**
  - Start Address = WAY[6-0], Multiply x 8
    - Example: WAY[6-0] = 000 1010, (Decimal Value = 10) Start Address = Column 80
    - UP Readout : First Column = 80
    - DN Readout : First Column = 1023 - 80 = 943
- **Valid WAY[6-0] Range**
  - WSY[6-0] = 000 0000 (Row 0 : UP) to 111 1111 (Row 1016 : UP)

ISC0404
Window Size Columns

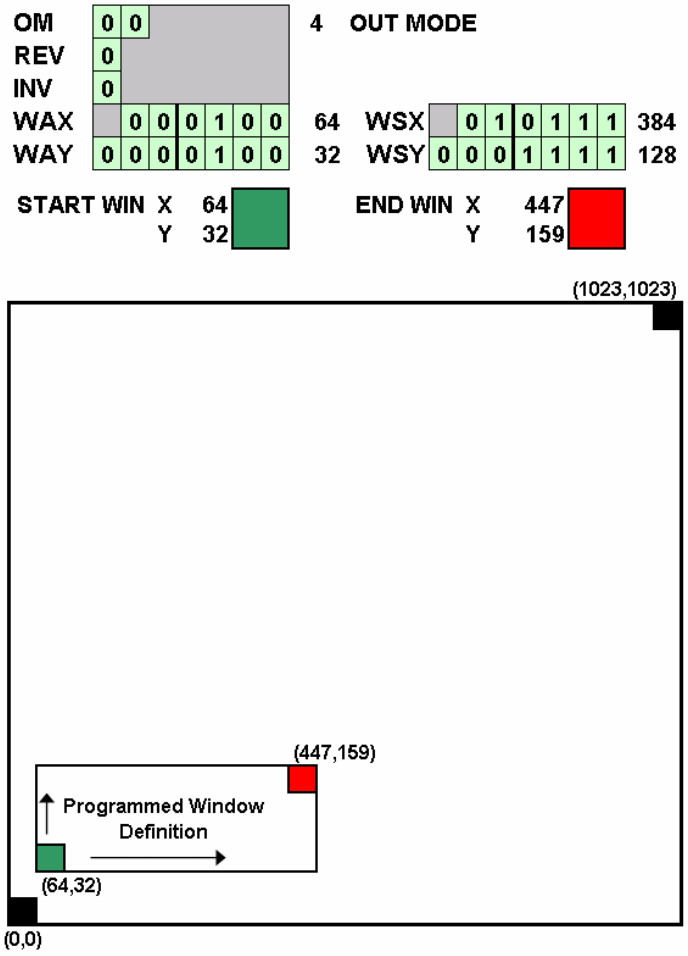
- **Control Word Field WSX[5-0] Represents Window Size in Columns**
- **X-Dimension Size Resolution Output Mode Dependent**
  - 4 Output Mode (OM[1-0]=00): Resolution = 16 Columns
  - 8 Output Mode (OM[1-0]=01): Resolution = 32 Columns
  - 16 Output Mode (OM[1-0]=1x): Resolution = 64 Columns
- **Size is Defined As Follows:**
  - 4 Output Mode: Window Size = WSX[5-0] + 1, Then Multiply x 16
    - Example: WSX[5-0] = 00 1111, (Decimal Value = 15)
    - Add 1 = 01 0000, (Decimal Value = 16)
    - Multiply x 16 = 256 Columns Window Size
  - 8 Output Mode: Window Size = WSX[5-1] + 1, Then Multiply x 32
    - WSX[0] = Don't Care
    - Example: WSX[5-1] = 00 111x, (Decimal Value = 7)
    - Add 1 = 01 000x, (Decimal Value = 8)
    - Multiply x 32 = 256 Columns Window Size
  - 16 Output Mode: Window Size = WSX[5-2] + 1, Then Multiply x 64.
    - WSX[1-0] = Don't Care
    - Example: WSX[5-2] = 01 00xx, (Decimal Value = 4)
    - Add 1 = 01 01xx, (Decimal Value = 5)
    - Multiply x 64 = 320 Columns Window Size
- **Valid WSX[5-0] Range**
  - Note Min active Window = 4 Pixel Periods
    - 4 Output Mode: 00 0000 (16 Cols) to 11 1111 (1024 Cols)
    - 8 Output Mode: 00 000x (32 Cols) to 11 111x (1024 Cols)
    - 16 Output Mode: 00 00xx (64 Cols) to 11 11xx (1024 Cols)

ISC0404
Window Size Rows

- **Control Word Field WSY[6-0] Represents Window Dimension in Rows**
- **Y-Dimension Size Resolution is NOT Output Mode Dependent**
  - Resolution = 8 Rows
- **Size is Defined As Follows:**
  - Window Size = WSY[6-0] + 1, Then Multiply x 8
    - Example: WSY[6-0] = 000 1110, (Decimal Value = 14)
    - Add 1 = 000 1111, (Decimal Value = 15)
    - Multiply x 8 = 120 Rows Window Size
- **Valid WSY[6-0] Range**
  - Note Min active Window = 8 Rows
  - WSY[6-0] = 000 0000 (8 Rows) to 111 1111 (1024 Rows)

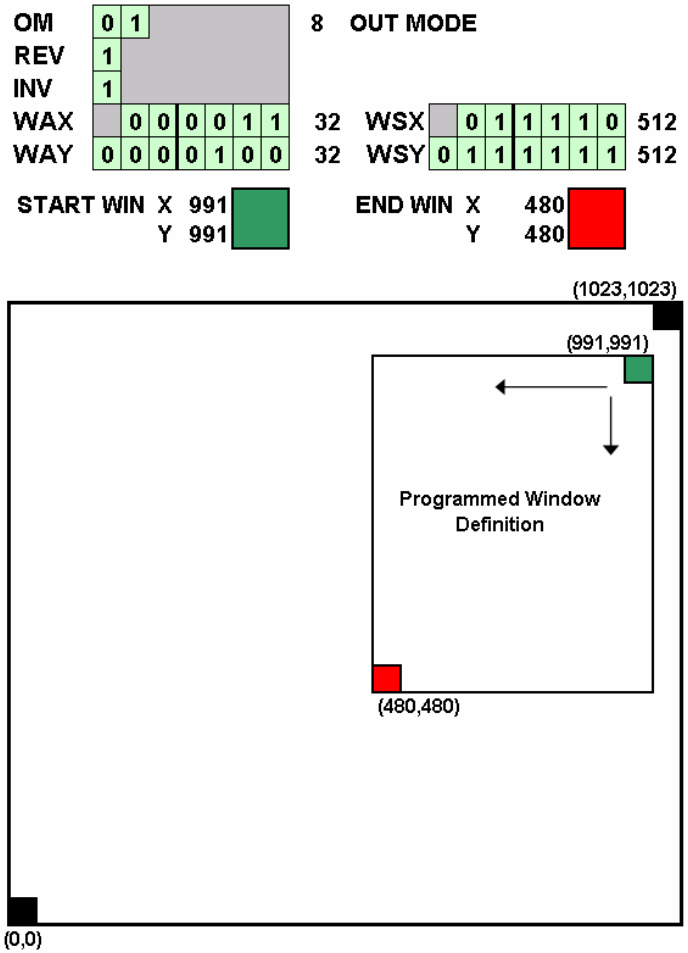
ISC0404
Window Example: Normal Readout

- **Example:**
  - **4 Output Mode, Normal Readout Direction**
    - **OM[1-0]=00 , REV=0 , INV=0**
    - **X-Resolution = 16 Cols**
    - **Y-Resolution = 8 Rows**
  - **Starting Address:**
    - **WAX[5-0] = 00 0100 (Col 64) -- (4 x 16)**
    - **WAY[6-0] = 000 0100 (Row 32) -- (4 x 8)**
  - **Window Size:**
    - **WSX[5-0] = 01 0111 (384 Cols) -- ((23+1) x 16)**
    - **WSY[6-0] = 000 1111 (128 Rows) -- ((15+1) x 8)**
  - **Window Read Out :**
    - **From (64,32) to (447,159)**
  - **Row Readout Order:**
    - **Row 32,33,34, … ,158,159**
  - **Column Readout Order Within Each Row:**
    - **OUTA: 64 , 68 , 72 , …, 436 , 440 , 444**
    - **OUTB: 65 , 69 , 73 , …, 437 , 441 , 445**
    - **OUTC: 66 , 70 , 74 , …, 438 , 442 , 446**
    - **OUTD: 67 , 71 , 75 , …, 439 , 443 , 447**
    - **OUT[E-P]: N/A**



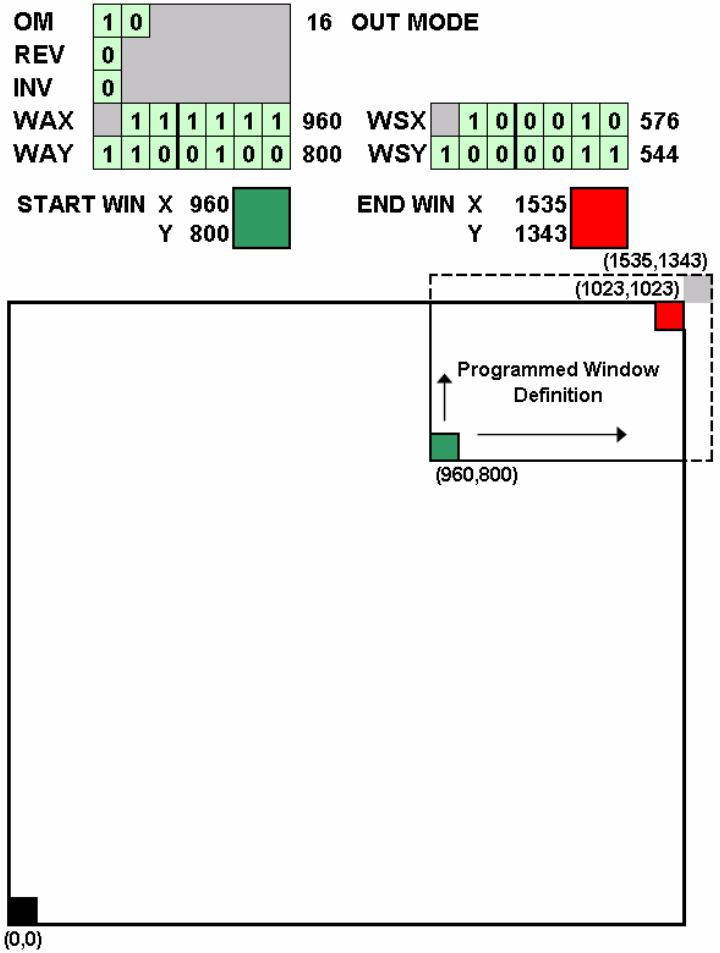
ISC0404
Window Example: INV & REV

- **Example:**
  - **8 Output Mode, Invert & Revert Readout Directions**
    - **OM[1-0]=01 , REV=1 , INV=1**
    - **X-Resolution = 32 Cols**
    - **Y-Resolution = 8 Rows**
  - **Starting Address:**
    - **WAX[5-0] = 00 0011 (Col 991) -- (1024 - (1 x 32))**
    - **WAY[6-0] = 000 0100 (Row 991) -- (1024 - (4 x 8))**
  - **Window Size:**
    - **WSX[5-0] = 01 1110 (512 Cols) -- ((15+1) x 32)**
    - **WSY[6-0] = 011 1111 (512 Rows) -- ((63+1) x 8)**
  - **Window Read Out :**
    - **From (991,991) to (480,480)**
  - **Row Readout Order:**
    - **Row 991,990,989, … ,481,480**
  - **Column Readout Order Within Each Row:**
    - **OUTA: 984 , 976 , 968 , …, 496 , 488 , 480**
    - **OUTB: 985 , 977 , 969 , …, 497 , 489 , 481**
    - **OUTC: 986 , 978 , 970 , …, 498 , 490 , 482**
    - **OUTD: 987 , 979 , 971 , …, 499 , 491 , 483**
    - **OUTE: 988 , 980 , 972 , …, 500 , 492 , 484**
    - **OUTF: 989 , 981 , 973 , …, 501 , 493 , 485**
    - **OUTG: 990 , 982 , 974 , …, 502 , 494 , 486**
    - **OUTH: 991 , 983 , 975 , …, 503 , 495 , 487**
    - **OUT[I-P]: N/A**



ISC0404
Window Example: Overflow

- **If the programmed window address and size result in a window definition that does not lie entirely within the ROIC (either in the Row or Column dimension), the window readout will be truncated by the Readout Logic.**
  - # Active Cols / Line is the Truncated Window Size
  - # Active Rows / Frame is the Truncated Window Size
- **Example:**
  - **16 Output Mode, Normal Readout Direction**
    - **OM=10 , REV=0 , INV=0**
    - **X-Resolution = 64 Cols**
    - **Y-Resolution = 8 Rows**
  - **Starting Address:**
    - **WAX[5-0] = 11 1111 (Col 960) -- (15 x 64)**
    - **WAY[6-0] = 110 0100 (Row 800) -- (100 x 8)**
  - **Window Size:**
    - **WSX[5-0] = 10 0010 (576 Cols) -- ((8+1) x 64)**
    - **WSY[6-0] = 001 0111 (544 Rows) -- ((67+1) x 8)**
  - **Window Read Out :**
    - **Programmed: From (960,800) to (1535,1343)**
    - **Actual Window: From (960,800) to (1023,1023)**
      - **Truncated Window Size 64 Cols x 224 Rows**



ISC0404
Logic Reset Mechanisms (1 of 2)

- **Power-On Reset**
  - Generates Global Logic Reset At Device Power-On
  - Functions for VPD Rise Times of ~0 to At Least 1 Sec
  - Resets Control Register Bits to Default States
- **RESET_B Pad**
  - Active Low Signal
  - Asynchronous Global Logic Reset
  - Resets Control Register Bits to Default States
    - Exception: Does NOT Reset the VET Address Bits
  - Does Not Reset Analog S/H Values
  - Use is optional, Pad has an on-chip Pull-up
  - If used, suggested that RESET_B be Held Low During Power Up

ISC0404
Logic Reset Mechanisms (2 of 2)

- **Commanded Master Reset**
  - Synchronous Global Logic Reset
  - Reset Occurs When Control Data is Applied and MRST Bit = 1
  - Resets Command Bits to Default States
    - Including the VET Address Bits
  - Does Not Reset Analog S/H Values
  - Interrupts Integration Cycle for this frame
    - Valid Output data in this Frame (from previous Integration)
    - NOT Valid Output data in Frame following the Commanded Master Reset (interrupted Integration)
    - Valid Output data in subsequent Frames
- **Rising Edge of FSYNC**
  - Rising Edge of FSYNC Resets the Readout and Integration Control Sequencing Logic Into Known State
  - Allows Graceful Interruption Of Frame Readout
    - If used to interrupt the Integration Cycle for this frame – Output data is not valid
    - The Frame following the FSYNC interrupt of Integration will be valid Output data
  - Does Not Affect Control Register Bit States

ISC0404
Standard 1k x 1k, 16 Output ROIC

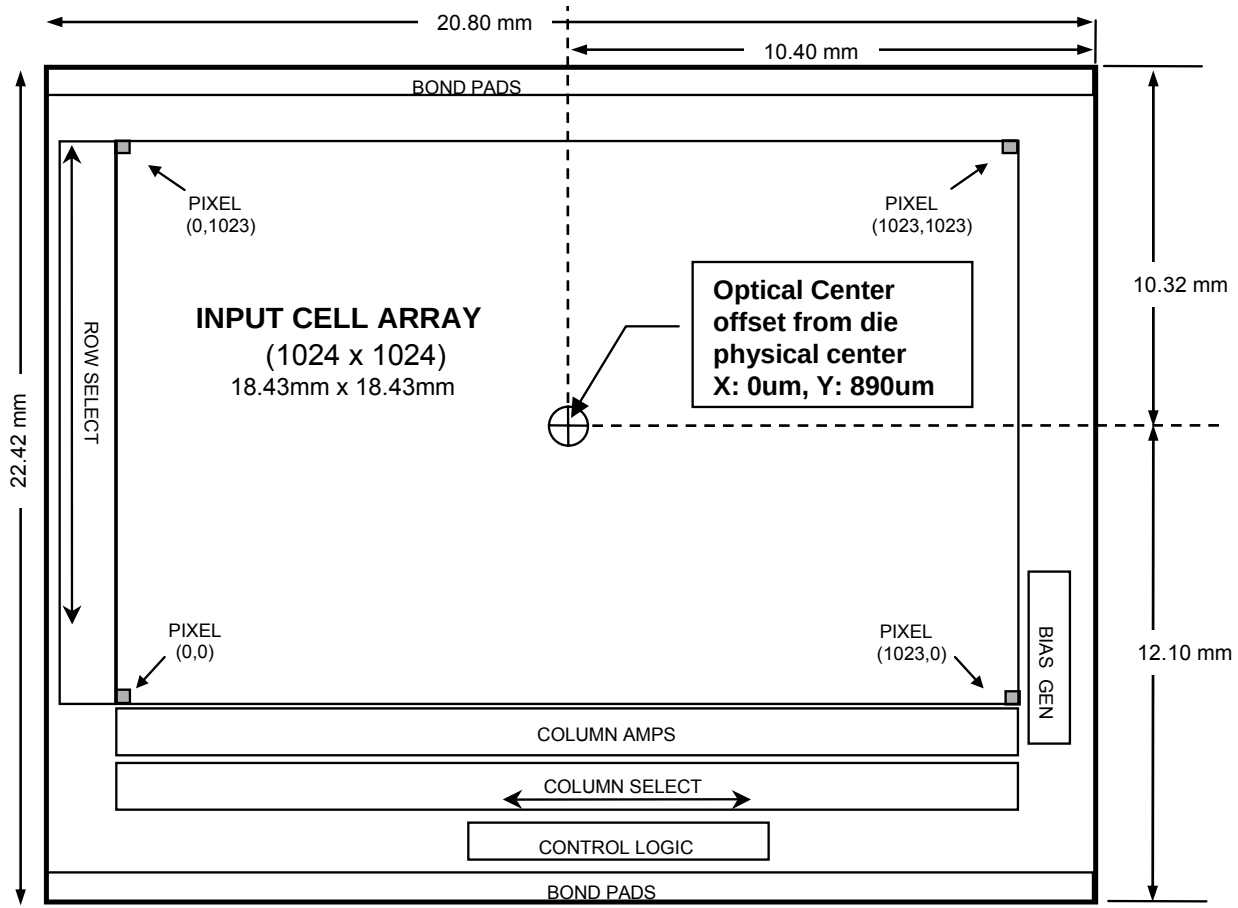
Physical Design

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404
Layout Overview

- **AMI Standard 0.35um process (AMI350)**
- **Die Size = 20.80mm x 22.42mm**
  - Die Size As Measured to Edge of Scribe Lane
- **200mm (8") Wafers**
  - Estimate 48 Die / Wafer
  - 180um Horizontal Scribe Lane (Die Y dimension)
  - 180um Vertical Scribe Lane (Die X Dimension)
  - Input Cell Pad Opening:
    - 6.0um x 6.0um

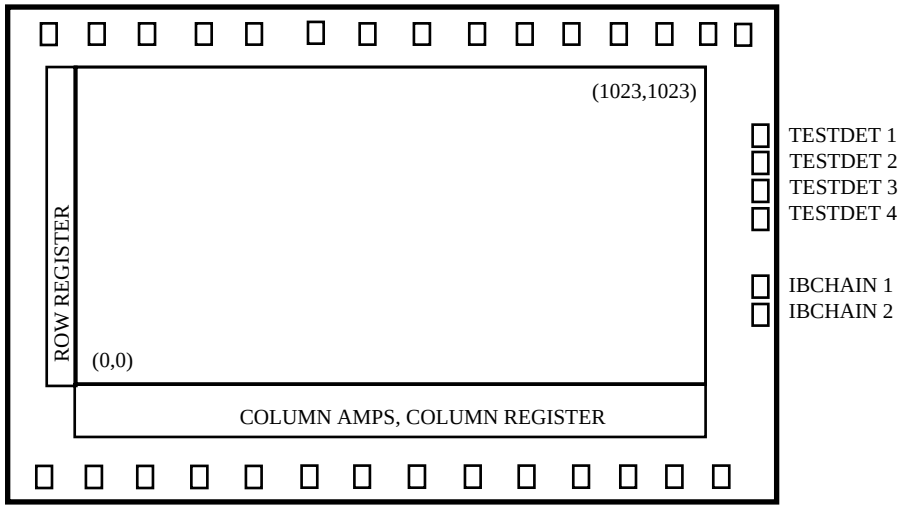
ISC0404 ROIC Layout



ISC0404
Detector Interface (1 of 3)

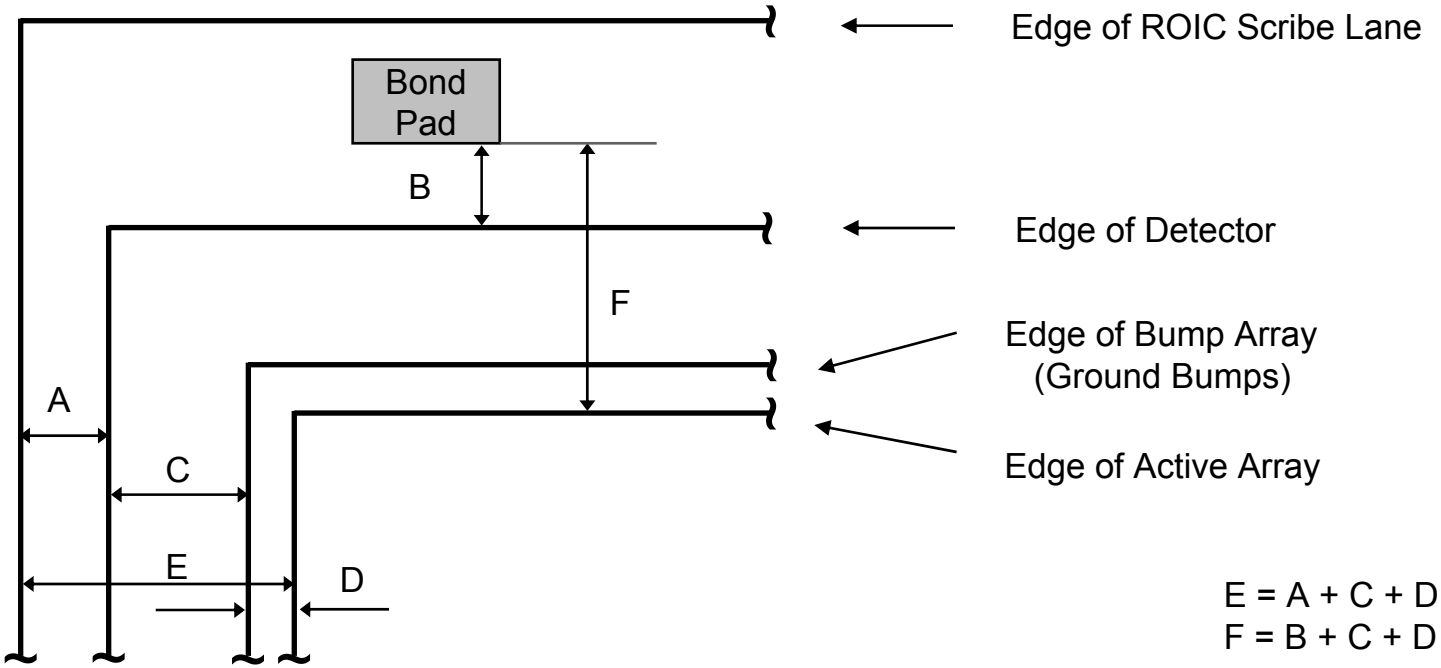
- **1024 x 1024 active detectors**
  - 18um x 18um pixel size
  - 6.0um x 6.0um pad opening, centered in pixel
- **Ring of 6 detector common pixels around array**
  - Total array = 1036 x 1036 pixels
  - Not compatible with ISC0107 detectors
- **Hybridization alignment targets**
  - 4 targets (crosses), 1 near each array corner (symmetric)
  - 90° rotational symmetry
- **Required detector clearances**
  - > 1150um (45mil) from edge of detector to edge of scribe lane
    - (3x die thickness, die thinned to 15mil)
  - > 750um from edge of detector to edge of bond pad

ISC0404
Detector Interface (2 of 3)



- **4 test diodes**
  - Direct access from test pads
- **Indium bump chain**
  - 100 element / 50 indium bumps

ISC0404
Detector Interface (3 of 3)

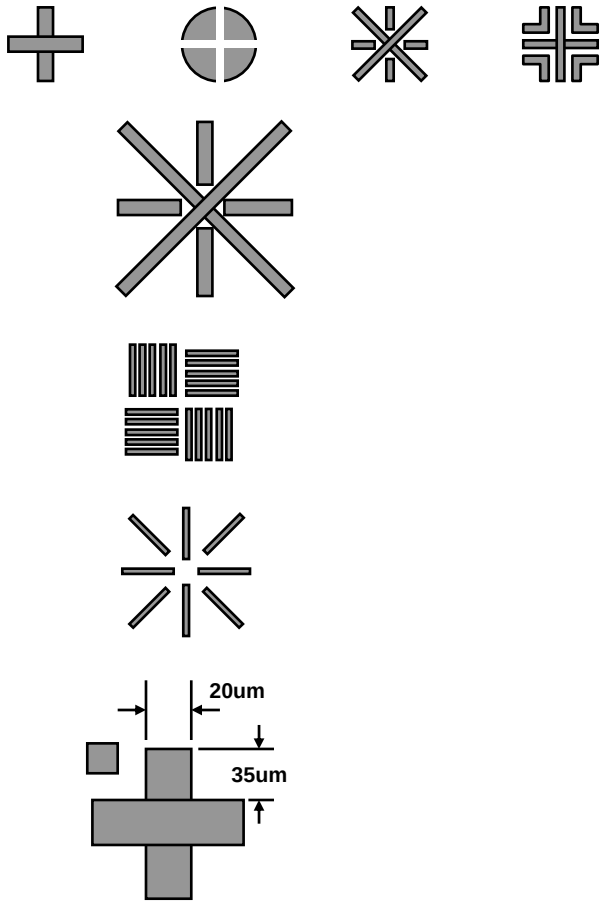


E = A + C + D
F = B + C + D

	Required	Actual (min)
A = Edge of detector to edge of ROIC scribe lane	A ≥ 1150um	976um
B = Edge of detector to bond pad opening	B ≥ 750um	703um
C = Extension of detector beyond ground ring	**C = 100um**	
D = Width of detector ground ring (6 pixels)	**D = 108um**	
E = Active pixel to ROIC scribe lane	**E ≥ 1358um**	**1184um**
F = Active pixel to bond pad opening	**F ≥ 958um**	**911um**

ISC0404 Alignment / Processing Structures (1 of 3)

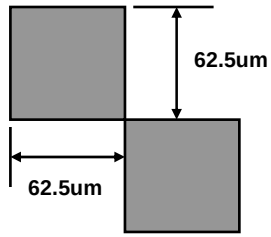
- **All features drawn in Metal5 layer unless otherwise specified**
- **MVS targets for Ultratech stepper**
  - 1 set per die
- **MVS off-axis target for Ultratech stepper**
  - 1 300um type X target per die
- **Local targets for GCA stepper**
  - 1 set per die
- **Global targets for GCA stepper**
  - 1 set per die
  - Spaced on die to meet wafer spacing requirement of 63.5mm
- **Hybridization targets**
  - 1 cross at each corner of detector array
  - 90° rotational symmetry



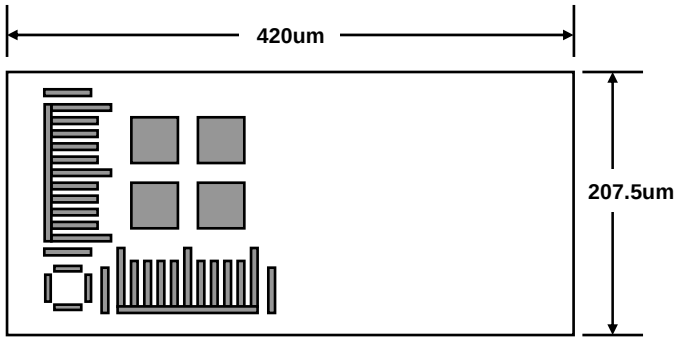
ISC0404 Alignment / Processing Structures (2 of 3)

- **Automated wire bonding targets**
  - 450um x 450um clear area on readout
  - Implemented in Contact metal (Indigo post processing)
  - Located near upper right and lower left corners of die

- **Manual wire bonding / packaging fiducial targets**
  - 1 butterfly target per edge (on detector centerline)
  - Located on detector centerline



- **Contact metal targets / verniers**
  - 1 set per die
  - Includes clear area for verniers to be placed in Contact metal
    - Locate > 200um from bond pad opening

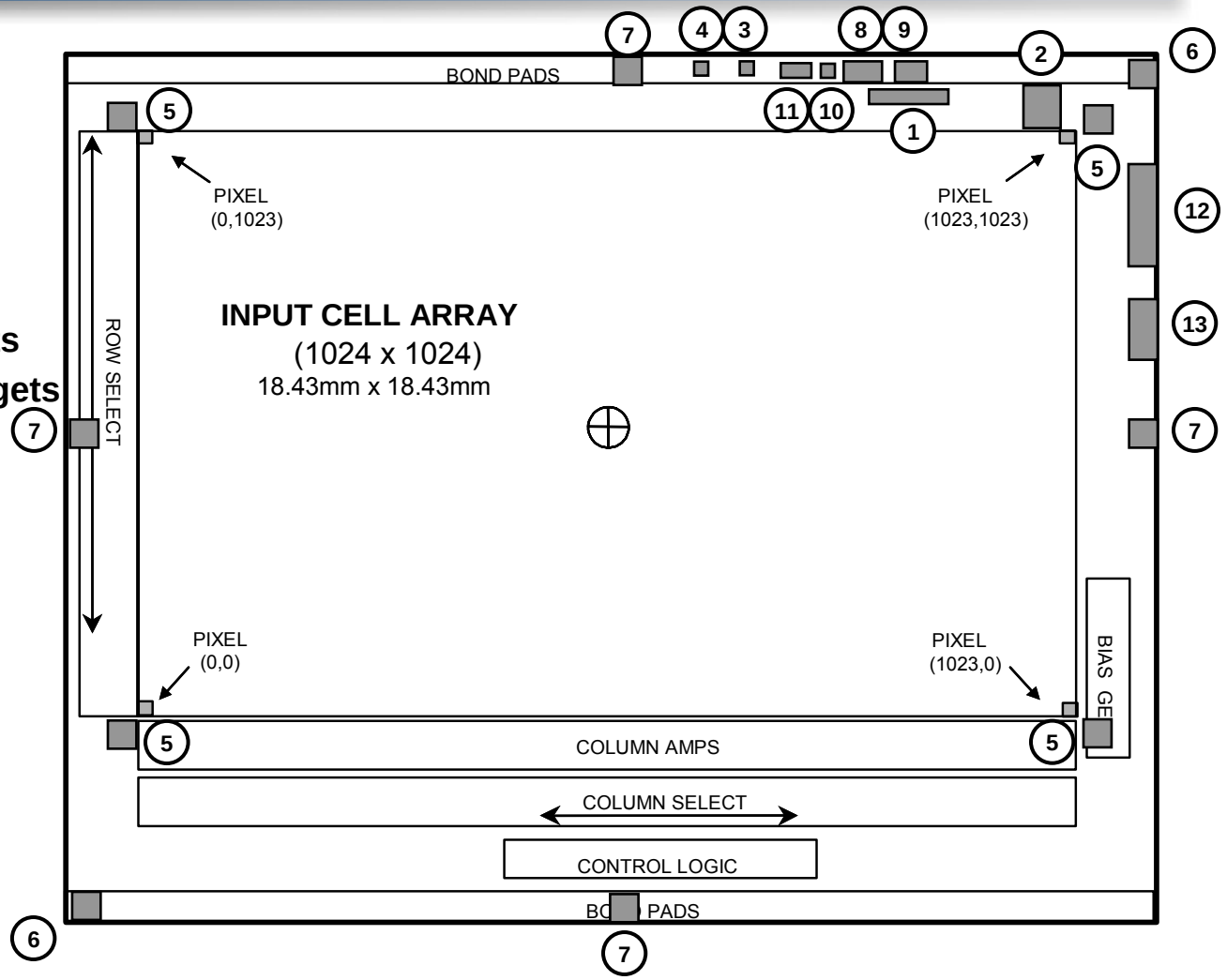


ISC0404 Alignment / Processing Structures (3 of 3)

- **Leave clear areas for**
  - Rev block for hybridization metal layers
    - 300um x 250um
  - Contact metal die ID (row / column location on wafer)
    - 350um x 80um

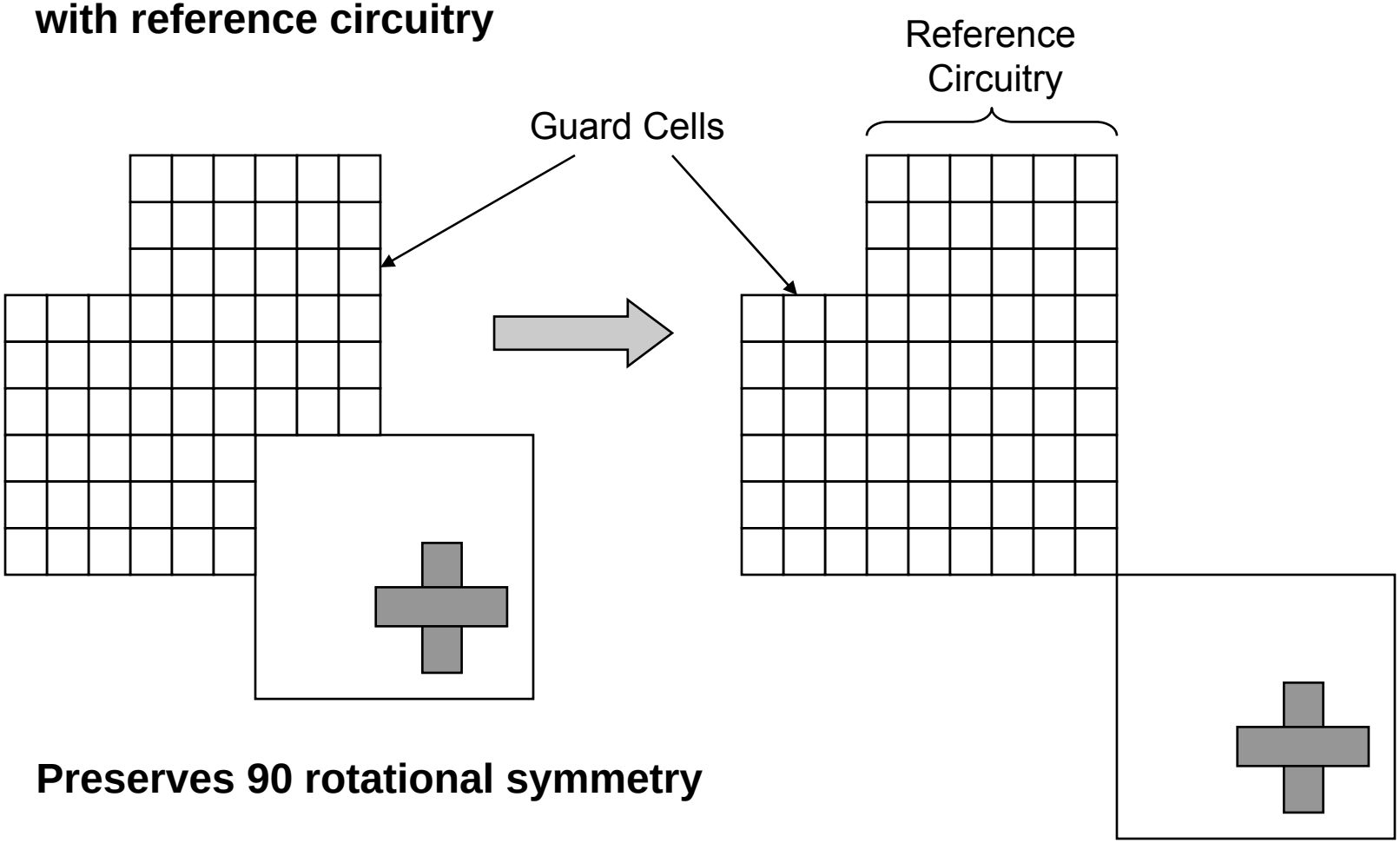
ISC0404 Alignment / Processing Structure Locations

1. MVS Targets
2. MVS Off-Axis Target
3. Local GCA Targets
4. Global GCA Targets
5. Hybridization Targets
6. Auto Wire Bonding Targets
7. Manual Wire Bonding Targets
8. Contact Metal Verniers
9. Hybridization Rev Block
10. Die ID (ROIC)
11. Die ID (Contact Metal)
12. Test Detectors
13. IB Chain



ISC0404 Hybridization Target Location

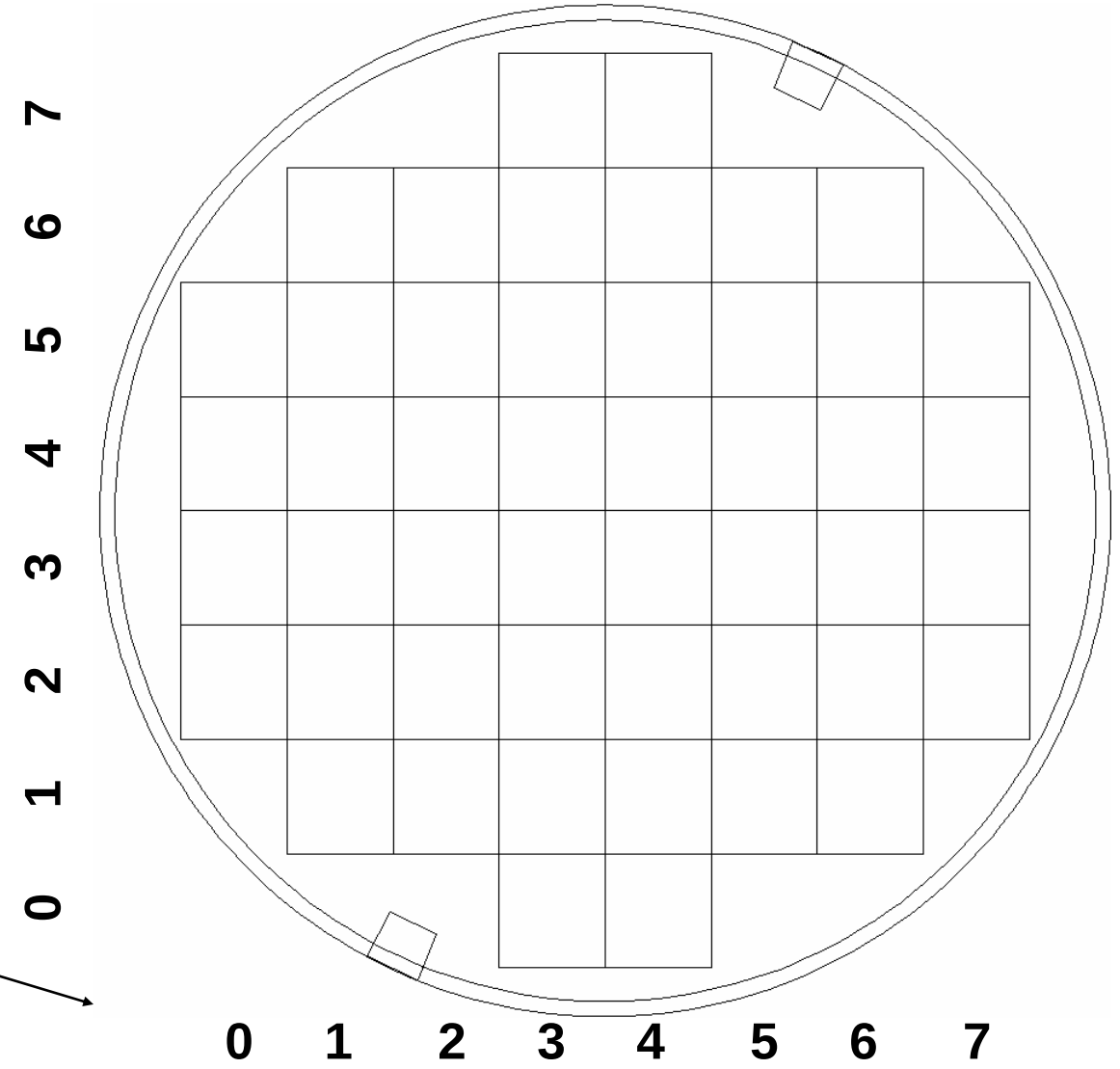
- **Hybridization targets pulled away from guard cells to avoid conflict with reference circuitry**



- **Preserves 90 rotational symmetry**

ISC0404
Preliminary Wafer Diagram

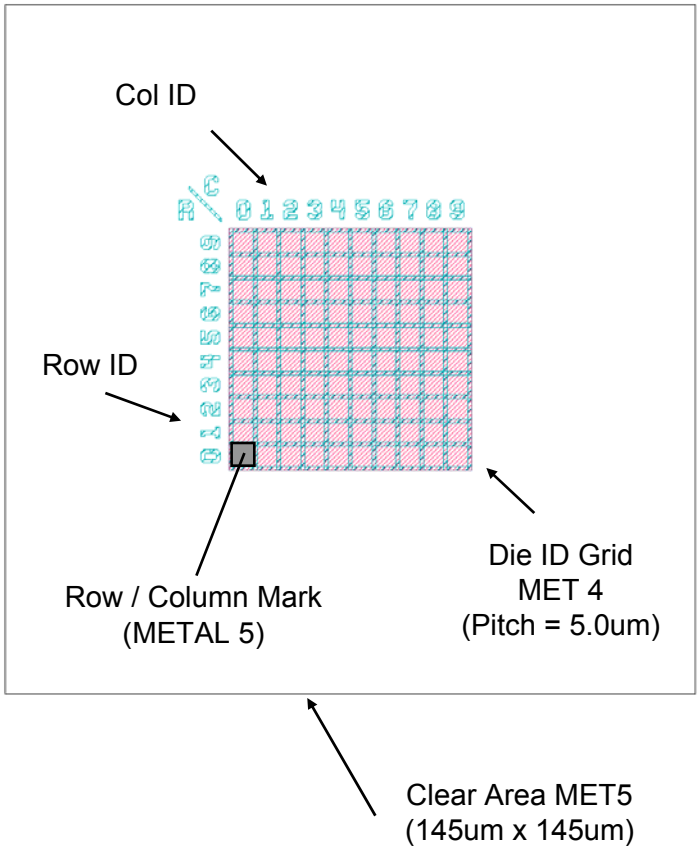
- **Estimate 48 ISC0404 die per 8" wafer**
- **Assumes 180um Scribe Lanes**
- **Stepping Centers**
  - 20.98mm in X
  - 22.60mm in Y



Row / Column Locations
For Die ID

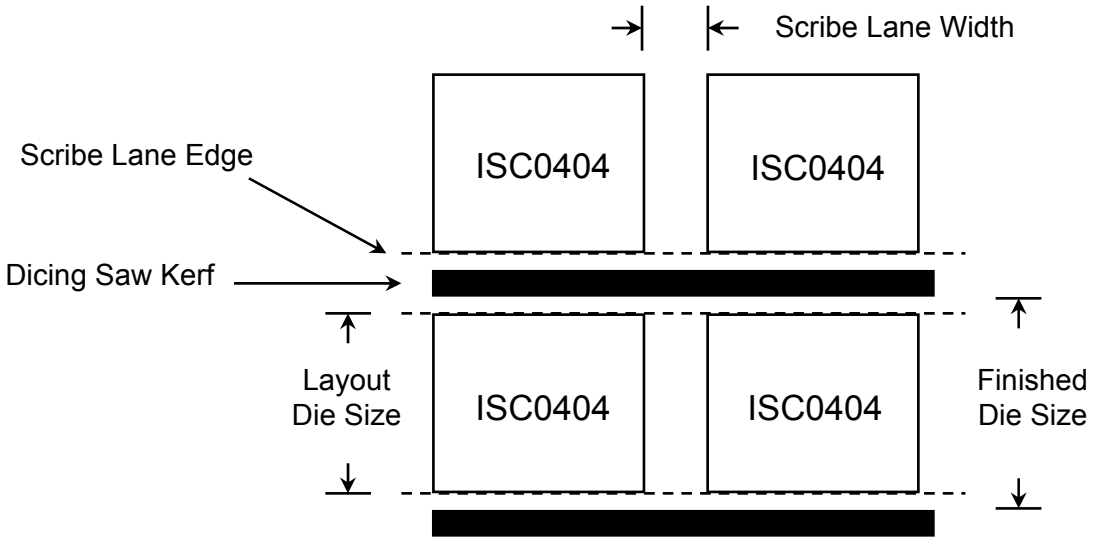
ISC0404 Die ID

- **Die ID Structure Implemented To Provide Unique ID For Each Die Location On The Wafer**
- **Die ID Grid Is Drawn In METAL 4 Layer**
  - 5.0um Pitch
  - Row / Column ID Values Correspond To Wafer Diagram
  - Place Center Of (0,0) Location On 10um Grid (Die Database Coords) In X and Y
- **Row / Column Mark Is Drawn In METAL 5**
- **Patterning Row / Column Mark Requires 2 Pass Exposure Of METAL 5 Layer**
  - Resulting Exposure Leaves Row / Column Mark Over Appropriate Grid Location For Each Die



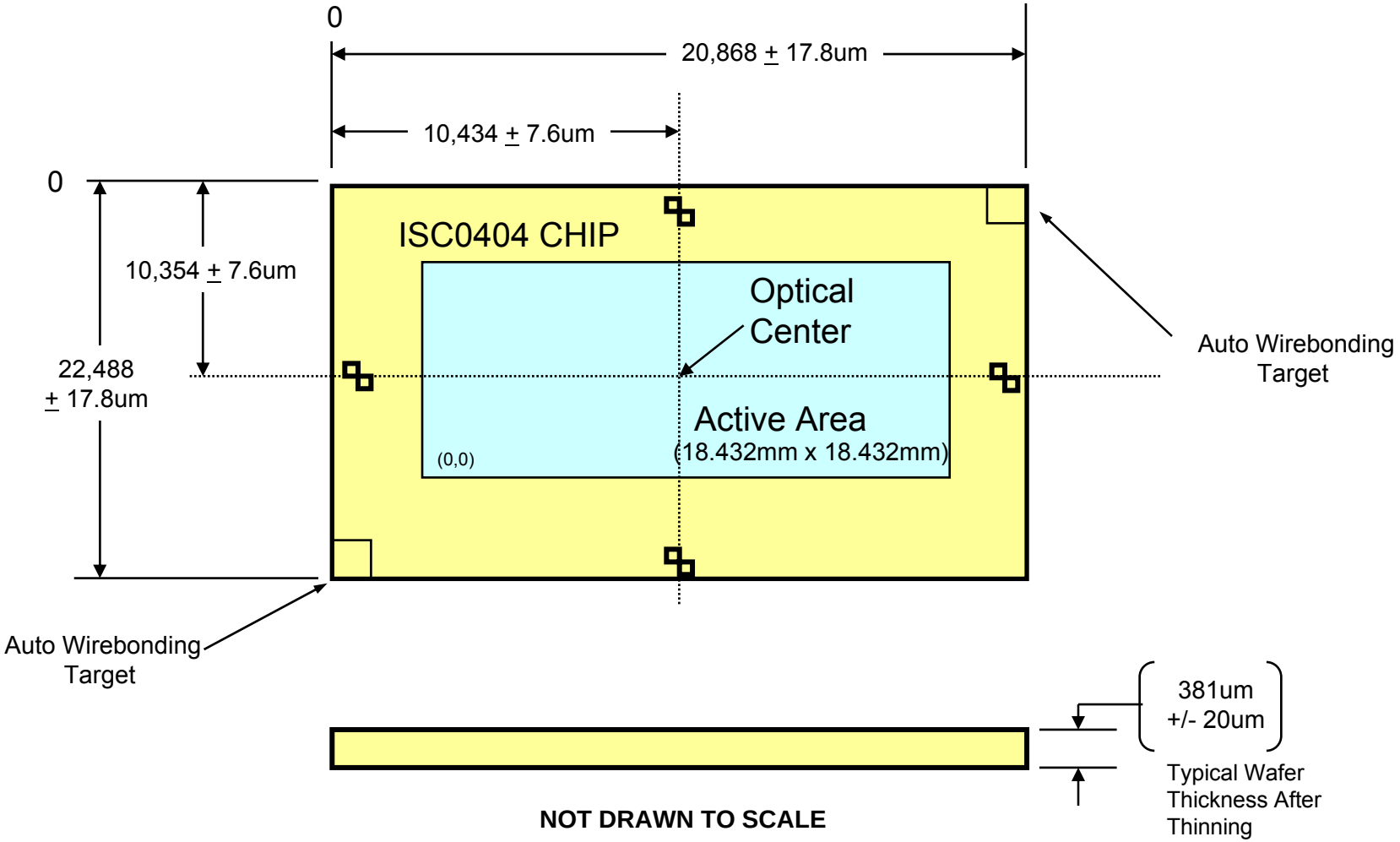
ISC0404
Finished Die Size

- **Layout die size is to scribe lane edge**
- **Finished die size is a function of wafer layout and dicing**



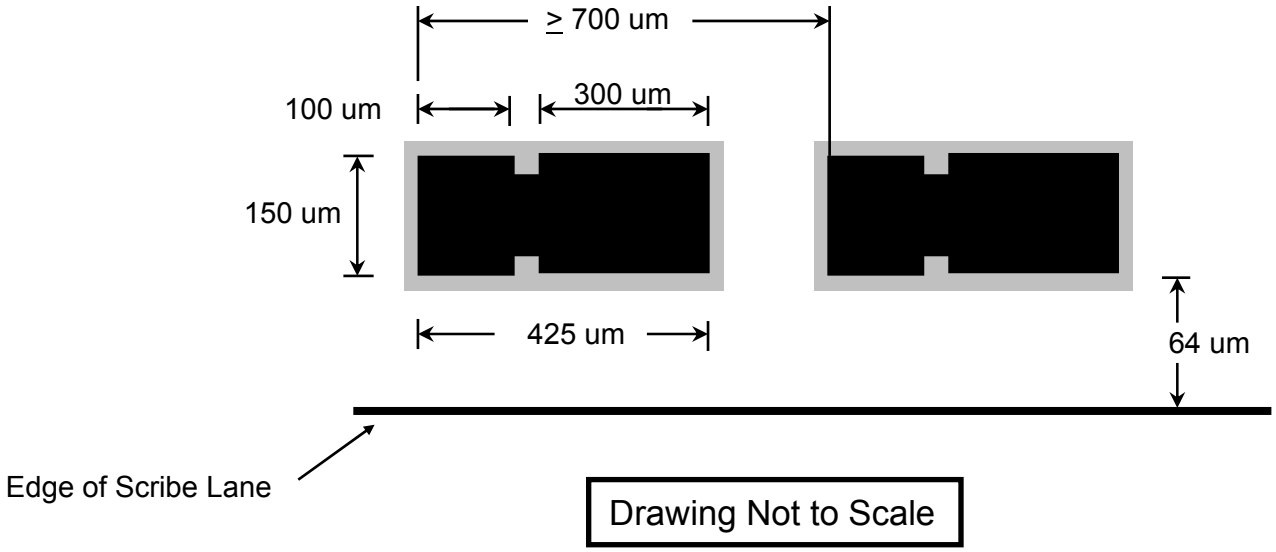
- **Post-Dicing Die Size = Layout Die Size + Scribe Lane Width - Saw Kerf**
  - Scribe Lane Width = 180um in X and 180um in Y Directions
  - Saw Kerf = 112um +/- 17.8um
  - Estimated Final Die Size = (20,868 +/- 17.8um, 22,488 +/- 17.8um)

ISC0404 Preliminary Mechanical Drawing



ISC0404
Bond Pad Layout

- **Passivation Openings:**
  - **Test Opening : 100 x 150 Microns**
  - **Flight Opening: 300 x 150 Microns**
- **Pad Pitch: ≥ 700 Microns**
- **Distances Measured from Overglass Openings**

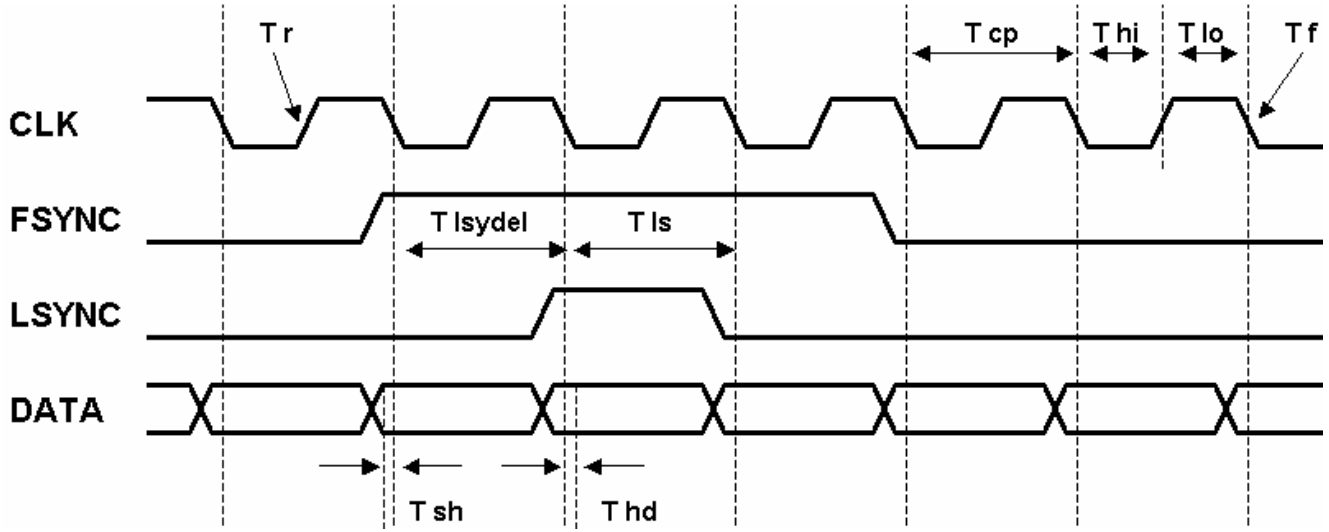


ISC0404
Standard 1k x 1k, 16 Output ROIC

Interface

INDIGO OPERATIONS DOCUMENT # 400-0404-10 VERSION 1.00

ISC0404
Clock Timing Requirements



PARAMETER	Min	Typ	Max	Comments
T r	--	--	10ns	10% - 90% (All Signals)
T f	--	--	10ns	10% - 90% (All Signals)
T sh	10ns	0.5 * T cp	T cp - 10ns	Setup Time: All Signals to Falling CLK Edge
T hd	10ns	0.5 * T cp	T cp - 10ns	Hold Time: All Signals to Falling CLK Edge
T cp	160ns	200ns	--	Typ - 5.0MHz CLK Rate = 10.0MHz Pixel Rate
T hi , T lo	0.45 * T cp	0.5 * T cp	0.55 * T cp	Typ - CLK Duty Cycle = 50%
T ls	--	1 * T cp	--	LSYNC Width = 1 CLK Cycle
T lsydel	640 * T cp	--	--	FSYNC to LSYNC Delay defined in Integration Timing

ISC0404 Interface Definition

BIAS	VOLTAGE	CURRENT	PK CURRENT	GAIN TO OUTPUT	Function
VPOS	3.6V	< 60mA	< 250mA	< 1	Positive Analog Supply
VNEG	0V	< 60mA	< 250mA	< 1	Negative Analog Supply / Chip Substrate
VPOSOUT	3.6V	< 40mA	< 100mA	< 0.2	Output Driver Positive Supply
VNEGOUT	0V	< 40mA	< 100mA	< 0.2	Output Driver Negative Supply
VPD	3.6V	< 5mA	< 50mA	< 0.1	Positive Logic Supply, Must Track VPOSOUT voltage
VND	0V	< 5mA	< 50mA	< 0.1	Negative Logic Supply
VDET_ADJ	0V – 3.6V	< 1mA	< 1mA	< 0.6	Detector Bias Resistive Divider
VOUTREF	1.0V nominal	< 1mA	< 50mA	< 1	Analog Output Reference Level / Dead Time Reference

Note: 0V and 3.6V Supplies May be Combined After Capacitive Bypass

CLOCKS	LEVELS	LOAD	RISE / FALL	Function
CLK	0V – VPD	< 20pF	< 10ns	Master Clock – Output on Half Clock Cycle
FSYNC	0V – VPD	< 10pF	< 10ns	Frame Sync – Controls Frame Start & Integration Time
LSYNC	0V – VPD	< 10pF	< 10ns	Line Sync – Controls Line Readout Timing
DATA	0V – VPD	< 10pF	< 10ns	Data Word Input – Programs Chip Function Registers
RESET_B	0V – VPD	< 10pF	< 10ns	Master Reset, Pulled Up If Not Connected

OUTPUTS	LEVELS	LOAD	SETTLE	Function
OUTA-OUTP	1.0V to 3.2V	18pF // 100k	< 55ns to 0.1%	16 Outputs, 0.1% at 77K, 0.8% at 300K
REFOUT	1.0V	18pF // 100k		Reference for Common Mode Output

MISC	VOLTAGE	Function
IMSTR_ADJ	0V to VPOS	Power Override
TEMP	0V to VPOS	Temp Monitor
TESTOUT	0V – VPD	VET Output
VTESTINE	0V to VPOS	Test Row Input Signal For Even Channels
VTESTINO	0V to VPOS	Test Row Input Signal For Odd Channels
TESTDET[1-4]	0V to VPOS	Test Detector Access
IBCHAIN[1-2]	0V to VPOS	Indium Bump Test Chain

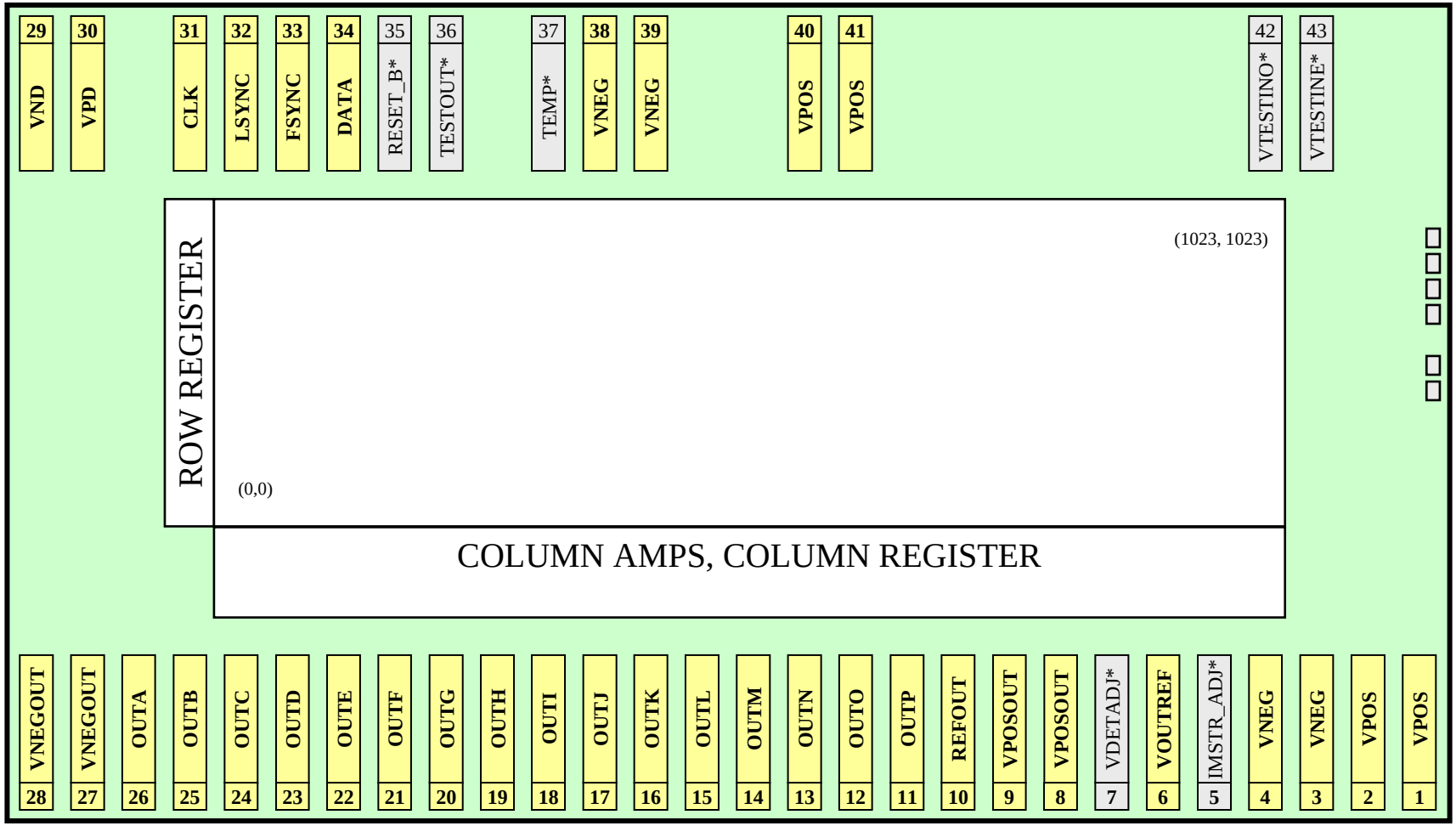
ISC0404
Suggested I/O Interface

PAD #	PAD	I/O RESISTANCE (Ohms)	I/O INDUCTANCE (nH)	I/O CAPACITANCE (F)
1-2, 40-41	VPOS	≤ 0.5	≤ 20	≥ 20u (2)
3-4, 38-39	VNEG	≤ 0.5	≤ 20	NA
5	IMSTR_ADJ	N.C.	N.C.	N.C.
6	VOUTREF	≤ 5	≤ 20	≥ 5u (2)
7	VDET_ADJ	N.C.	N.C.	N.C.
8-9	VPOSOUT	≤ 1	≤ 20	≥ 5u (3)
10	REFOUT	≤ 5	≤ 50	≤ 18p
11-26	OUTP - OUTA	≤ 5	≤ 50	≤ 18p
27-28	VNEGOUT	≤ 1	≤ 20	NA
29	VND	≤ 10	≤ 50	NA
30	VPD	≤ 10	≤ 50	≥ 5u (1)
31	CLK	≤ 25	≤ 50	NA
32	LSYNC	≤ 25	≤ 50	NA
33	FSYNC	≤ 25	≤ 50	NA
34	DATA	≤ 25	≤ 50	NA
35	RESET_B	≤ 25	≤ 50	NA
36	TESTOUT	N.C.	N.C.	N.C.
37	TEMP	≤ 50	≤ 50	≤ 100p
42	VTESTINO	N.C.	N.C.	N.C.
43	VTESTINE	N.C.	N.C.	N.C.

Values for Worst case 6.25MHz CLK

NOTES:
(1) Bypass To VND
(2) Bypass To VNEG
(3) Bypass To VNEG_OUT

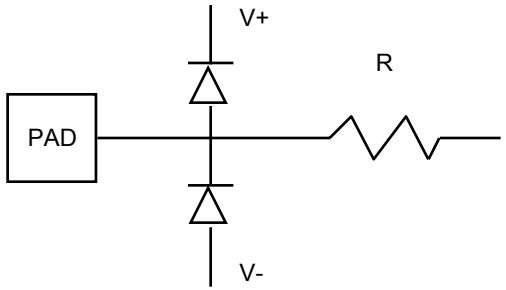
ISC0404 Pad Placement



* Pads in grey are optional

ISC0404 Pad Protection

- **ISC0404 Uses Resistor / Parallel Diode ESD Structure:**
  - Parallel Diode Network
  - Series Resistor (N+ or NWELL)
  - AMI Design Rule Compliant
  - Indigo Standard



Pad	Signal	Resistance (1)	V+ / V-
1-2	VPOS	0	-- / VNEG
3-4	VNEG	0	-- / --
5	IMSTR_ADJ	LOW	VPOS / VNEG
6	VOUTREF	0	VPOS / VNEG
7	VDET_ADJ	LOW	VPOS / VNEG
8-9	VPOSOUT	0	-- / VNEG
10	REFOUT	0	VPOSOUT / VNEG
11-26	OUTP - OUTA	0	VPOSOUT / VNEG
27-28	VNEGOUT	0	-- / VNEG
29	VND	0	-- / VNEG
30	VPD	0	-- / VNEG
31	CLK	LOW	VPD / VNEG
32	LSYNC	HIGH	VPD / VNEG
33	FSYNC	HIGH	VPD / VNEG
34	DATA	HIGH	VPD / VNEG
35	RESET_B (2)	HIGH	VPD / VNEG
36	TESTOUT	LOW	VPD / VNEG
37	TEMP	LOW	VPOS / VNEG
38-39	VNEG	0	-- / --
40-41	VPOS	0	-- / VNEG
42	VTESTINO	0	VPOS / VNEG
43	VTESTINE	0	VPOS / VNEG
--	TESTDET[1-4]	0	-- / VNEG
--	IBCHAIN[1-2]	--	-- / --

Notes:
(1) LOW = 50 ohm,
HIGH = 500 ohm
(2) w/ Pull-up

ISC0404 Recommended Power On / Off Sequence

- **All negative supplies connected (ground)**
- **Turn ON biases in the following order:**
  - VPOS
  - VPOSOUT
  - VPD
  - VOUTREF
- **Turn ON the clocks**
- **Turn OFF biases and clocks in reverse order as above**