Analisi e sviluppo di un run-time per il power management per HPC basato su DDS

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Research Topic: ? HPC ?

1 Introduction

In recent years, the rapid growth of supercomputing systems has led to an increased demand for efficient power management strategies. As these systems continue to evolve, optimizing power consumption has become a critical challenge to address. Effective power management not only contributes to reducing energy costs but also has a positive impact on the environment by minimizing the carbon footprint associated with data centers and large-scale computing infrastructures. Furthermore, the development of open-source power managers allows for greater flexibility and adaptability to the specific needs of different HPC environments.

In a power management system, there are several types of actors (node-manager, job-manager, monitor, etc.) each of which must interact with hundreds of entities (nodes, cores). All this generates a significant amount of data traffic that must be managed in real-time in an efficient and secure manner. The area of interest of this project is to implement a DDS service among the many available within an open-source power management stack for HPC.

1.1 DDS & RTPS

DDS (Data Distribution Service) and RTPS (Real-Time Publish-Subscribe) constitute two pivotal technologies in the realm of distributed and real-time communications. These technologies play a critical role in enabling efficient and reliable data transmission among interconnected devices and applications, holding particular significance in intricate scenarios such as embedded systems, the Internet of Things (IoT), and high-performance applications like High-Performance Computing (HPC).

Specifically, DDS serves as a distributed communication framework that facilitates data exchange among software components distributed across heterogeneous networks. Built upon a publish-subscribe model, DDS establishes a mechanism for efficient data sharing. On the other hand, RTPS serves as the underlying protocol employed by DDS to realize the publish-subscribe paradigm within real-time networks. RTPS focuses on the dependable delivery of real-time messages, ensuring that data reaches the appropriate recipients in the most efficient manner. This protocol manages critical aspects such as data flow control, node synchronization, and quality of service management.

1.2 Components

2 State of the Art

To the best of my knowledge, the current landscape of power management solutions for power management strategies are often characterized by proprietary hardware and software implementations.

To the best of my knowledge, la maggior parte del panorama del power management, per le applicazioni di HPC, è affrontata tramite soluzioni hardware e software proprietarie, principalmente sviluppate in modo ad hoc dai diversi centri di calcolo. Le alternative più complete e open-source che coprono l'ambito trattato sono GEOPM [1] e REGALE [2]. Inoltre, uno studio approfondito sull'implementazione e sull'utilizzo di DDS è rappresentato dal middleware implementato in ROS2 chiamato *rmw_rtps*.

2.1 GEOPM

2.2 REGALE

2.3 Middleware

3 Project's Description

The primary objective of this research is to analyze, design, and develop a runtime system for power management that exploits and leverage the capabilities of the DDS protocol considering all entities that are included and all their interactions in the system. By dynamically adjusting the power consumption of individual components based on their current workloads and communication patterns, the proposed system aims to achieve substantial energy savings without compromising system performance. A second point of the project is to explore the potential of utilizing DDS as a basis for runtime power management. By leveraging the advantages of DDS, we intend to develop an open-source power management solution that offers transparency, adaptability, and scalability. Si proverà anche a fornire un middleware per poter scegliere a piacere una implementazione diversa di DDS

4 Expected Results

This project is expected to achieve three main contributions:

- the analysis of several advanced control structures aimed at answering the new upcoming requirements and constraints originated from the increasing complexity of processors in the edge and high-performance computing domains;
- The exploration of more compute-intensive control paradigm (model predictive control, deep reinforcement learning), and HW architectures to execute them efficiently.

- the development of a simulation framework for the co-design of all the parts of the control system (HW, run-time/RTOS, control policy, interfaces with processors and sensors);
- the development of an open-source power controller firmware based on open-source hardware, aimed at being implemented in a broad range of chips.

5 Proposed project timeline

- Year 1:
  - Literature overview on advanced control designs and on the State of the Art control algorithms applicable to the power and thermal control of a processor.
  - Creation of a simulation framework. Development of system and controller models.
  - Initial Firmware architecture design.
- Year 2:
  - Analysis and comparison of the identified control structure designs.
  - Intermediate version of the controller Firmware targeting an identified open-source hardware design.
- Year 3:
  - SECURITY?
  - Adapt the project to a broad range of scenarios and possible implementations.

6 Outline of the proposed findings assessment criteria

The criteria to asses the proposed findings will be:

- an open-source publication on GitHub of an operational firmware for a processor power controller, associated with an open-source RTL component regarding the controller hardware.
- the possibility to consider the implementation of the open-source controller project in a real processor design.
- an exhaustive analysis of the control structures relevant to the power and thermal control of a processor, publishable on a paper.
- the development of a simulation framework able to provide reliable results.

References

[1] INTEL. *GEOPM*. 2017. URL: `https://geopm.github.io/index.html`.
[2] CINECA. *Open Architecture for Future Supercomputers*. 2021. URL: `https://regale-project.eu/` (visited on 05/07/2023).