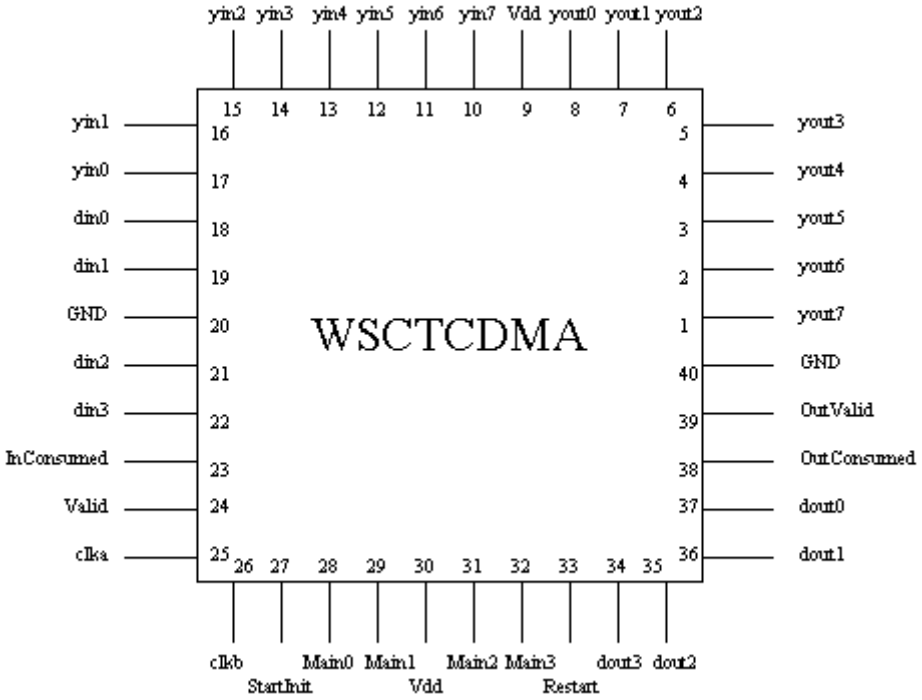
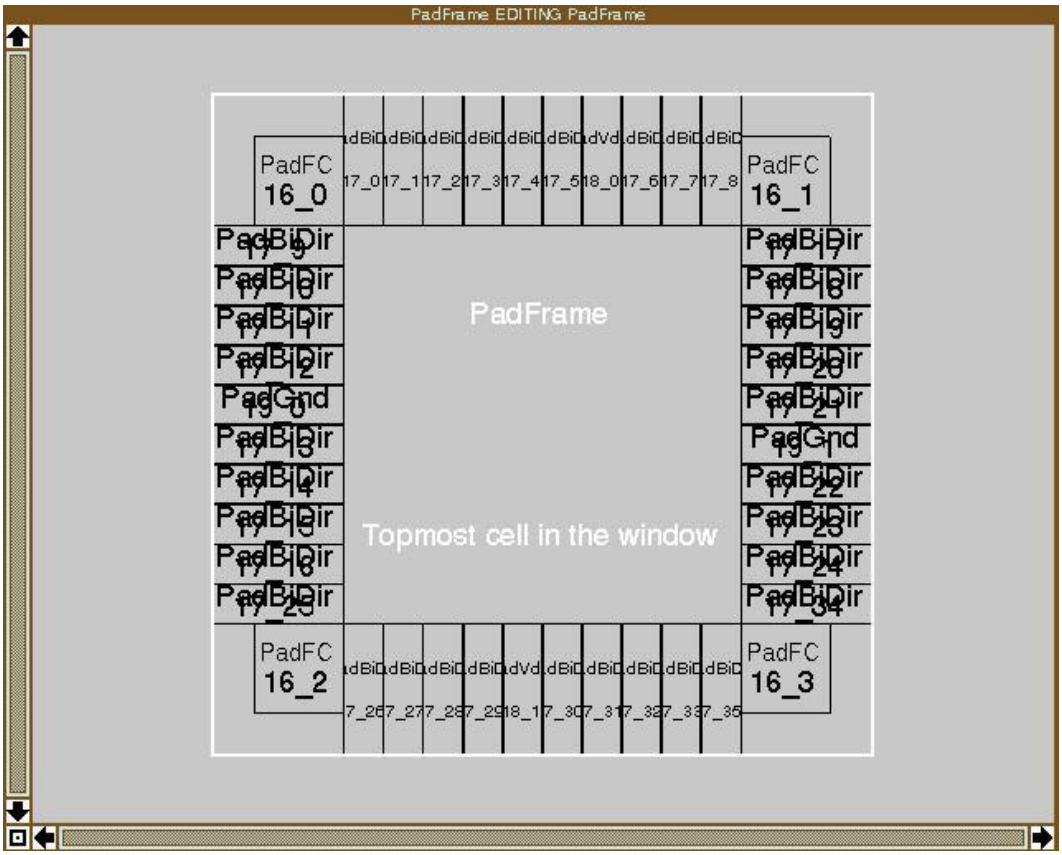
Elec 422 / 527 VLSI Systems Design
Rice University
MOSIS 0.5u Pad Frames



Sample Pin Numbering of MOSIS AMI 0.5 TinyChip Padframe at Rice University with corresponding *Magic* Padframe below. Please note the location of Pin 1 on the right hand side of the padframe. Recall that the inside core dimensions are 3000 by 3000 lambda. The outside dimension is 5000 by 5000 lambda. This padframe is on the CLEAR cluster at: /clear/courses/elec422/2016_spring/pad_06



PadFrame.mag is the main file, and uses PadVdd.mag, PadGnd.mag, PadFC.mag, and PadBiDir.mag. The file PadBiDir.mag is the bidirectional I/O pad where the enable signals are connected.

Below is a sample Pad Frame for double size MOSIS TinyChip I/O padframe. This frame uses the same pad cells, but is organized into a larger frame. The outside dimension is 5000 by 8600 lambda. The inside core dimensions are 3000 by 6600 lambda. There are four Vdd and four GND pads in this padframe. This is an example of scaling the padframe and is not used for new MOSIS projects.