MADHAVA KRISHNAN RAMANATHAN

540-988-6619 ♦ madhavakrishnan@vt.edu ♦ LinkedIn ♦ GitHub ♦ Website

EDUCATION

PhD, Computer Engineering (May 2018 - Present)
Virginia Polytechnic Institute and State University (CGPA: 3.85/4.0)
Master of Science, Computer Engineering (Graduated, May 2017)
University of Texas at San Antonio (CGPA: 3.9/4.0)
Bachelor of Engineering, Electronics & Communication (Graduated, May 2015)
Anna University, Chennai, India (CGPA: 3.74/4.0)

Technologies:
♦ C, C++ ♦ Kernel Programming
♦ Concurrent Programming
Tools:
♦ M-sim ♦ Git ♦ Linux ♦ Pthreads
♦ gdb ♦ perf ♦ GNU Make ♦ ctags

CAREER DEVELOPMENTS

May 2020 – August 2020: Nvidia, DGX SW Team-- Software Engineer Intern, Filesystems.
Worked in the DGX SW team, extended the XFS filesystem to support GPU direct storage. Developed IO benchmarks using CUDA to evaluate GPU direct storage.
June 2019 – August 2019: AT&T Labs, Advanced Wireless and Systems Group – Research Intern
Designed and implemented a novel key value store architecture for the emerging persistent memory and tested it with the Redis key value store. The proposed architecture archives high performance (~1.9x) and scalability.
May 2018 - Present: COSMOSS Lab @ Virginia Tech - Graduate Research Assistant
My current research focuses on understanding and analyzing the impact of the emerging persistent memory technologies and its programming models at the various levels of hardware and software stack.
Research Interest: Scalable Operating Systems, Storage & Filesystems, and Computer Architecture.

RESEARCH PROJECTS AND PUBLICATIONS

- W. Kim, **M.K. Ramanathan**, S. Kashyap, C. Min, "PACTree: A High-Performance Persistent Range Index Using PAC Guidelines, In Proceedings of SOSP, October 2021
- **M.K. Ramanathan**, W. Kim, H. Lee, M. Jang, S. Monga, A. Mathew, C. Min, "TIPS: Making Volatile Index Persistent Using DRAM-NVMM Tiering, In Proceedings of the USENIX ATC, July 2021.
- **M.K. Ramanathan**, J. Kim, A. Mathew, X. Fu, A. Demeri, C. Min, and S. Kannan, "Durable Transactional Memory Can Scale with Timestone", In Proceedings of the ASPLOS, Lausanne, Switzerland, March 2020.
- **M.K. Ramanathan**, J. Kim, A. Mathew, X. Fu, A. Demeri, C. Min, and S. Kannan, "Durable Transactional Memory Can Scale with Timestone", 11th Annual Non-Volatile Memories Workshop (NVMW). San Diego, CA, March 2020.
- **M.K. Ramanathan** and W.-M. Lin, "A Controlled Fetching Technique for Effective Management of Shared Resources in SMT Processors." Microprocessors and Microsystems 57C (2018).

NOTABLE ACADEMIC PROJECTS

- **Design IO Benchmarks for Characterizing Emerging Byte-addressable Persistent Memory**
  Designed an IO benchmark framework from scratch and uses it to study and evaluate the performance and multi-core scalability aspects of byte-addressable persistent memory.
- **Design and Evaluation of Concurrent Data Structures**
  Implemented linked list and hash table using three different concurrency models—Mutex, Lock-free and transactions and evaluated the performance and multi-core scalability on 64-core Intel server.
- **Design and Implementation of Smart Pointer Interface for Multi-Version Transactions**
  Implemented smart pointer interface using C++ for transactional programming and data structure design
- **Design and Implementation of Simple Virtual File System in Linux Kernel**
  Implemented a procfs like module in the Linux kernel v4.18, the implemented VFS displays the key attributes of process for the given Process Id.
- **Design and Implementation of Simple Distributed Shared Memory**
  Utilized C to implement page-granule MSI protocol among different machines using userfaultfd and the communication between the machines is established using socket programming.