R. MADHAVA KRISHNAN

540-988-6619 ⋄ madhavakrishnan@vt.edu ⋄ LinkedIn ⋄ Website ⋄ GitHub ⋄ Google Scholar

EDUCATION

05/2018 – 05/2023 Ph.D. in Computer Engineering, Virginia Tech
Research Area: Storage Systems, Operating Systems, Concurrency, and Multi-core Scalability.
Advisor: Dr. Changwoo Min; CGPA: 3.85/4.0

08/2015 – 05/2017 M.S. in Computer Engineering, University of Texas, San Antonio
Thesis: "A Statistical Fetching Approach for Effective Physical Register File Management in SMT processors."; Advisor: Dr. Wei-Ming Lin; CGPA: 3.9/4.0

08/2011 – 04/2015 B.E. in Electronics and Communication, Anna University
Final Project: "Design of Autonomous 6 DOF Robotic Arm and Gesture Controlled Hand."
CGPA: 8.0/10 **(First Class Honors)**

WORK EXPERIENCE

05/2023 – Current: Senior Member of Technical Staff-- Oracle
I am working on Oracle's hybrid columnar database storage engine. My work involves designing and implementing in-memory data formats on disk to efficiently access on-disk data and enable performance-efficient data tiering across Oracle's Exadata storage layers.

05/2022 – 08/2022: System Architect Intern-- Memory Solutions Lab, Samsung Semiconductor
Designed a novel cross-layered key-value store architecture for computational storage drives. Proposed novel techniques to improve SSD performance, endurance, and reliability. Filed three patents as a primary contributor for the aforementioned ideas.

05/2020 – 08/2020: Software Engineer Intern-- Filesystems, Nvidia.
Worked in the DGX SW team and extended the XFS filesystem to support GPU direct storage. Developed IO benchmarks using CUDA to evaluate GPU direct storage. Worked on integrating Swift object storage to use GPU direct storage.

06/2019 – 08/2019: Research Intern-- Advanced Wireless and Systems Group, AT&T Labs.
Designed and implemented a key-value store framework for emerging persistent memory. Ported the Redis key-value store using the framework developed.

RESEARCH PUBLICATIONS

M.K. Ramanathan, B. Sanjana, S. Jain, W. Kim, H. Hadian, V. Maram, C.Min "**Retina:** Scaling Deep Learning Training Using Computational Storage", **MASCOTS** 2023.

M.K. Ramanathan, D. Zhou, W. Kim, S. Kashyap, S. Kannan, C.Min "**TENET:** Memory Safe and Fault-tolerant Persistent Transactional Memory", In Proceedings of **USENIX FAST**, February 2023.

W. Kim, **M.K. Ramanathan**, S. Kashyap, C. Min, "PACTree: A High-Performance Persistent Range Index Using PAC Guidelines, In Proceedings of SOSP, October 2021.

M.K.Ramanathan, W.Kim, H.Lee, M.Jang, S.Monga, A.Mathew, C.Min, "**TIPS:** Making Volatile Index Persistent Using DRAM-NVMM Tiering, In Proceedings of the **USENIX ATC**, July 2021.

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Anthony Demeri, Wookhee Kim, **M.K.Ramanathan**, Jaeho Kim, Mohannad Ismail, Changwoo Min." **Poseidon:** Safe, Fast and Scalable Persistent Memory Allocator", In Proceedings of the 21st Middleware Conference **(Middleware '20**), December 2020.

M.K.Ramanathan, J.Kim, A. Mathew, X.Fu, C.Min, and S.Kannan, "Durable Transactional Memory Can Scale with **Timestone**", In Proceedings of the **ASPLOS**, March 2020.

M.K.Ramanathan, J.Kim, A. Mathew, X.Fu, A.Demeri, C.Min, and S.Kannan, "Durable Transactional Memory Can Scale with Timestone", 11th Annual Non-Volatile Memories Workshop (**NVMW**), March 2020.

J.kim, A.Mathew, S.kashyap, **M.K.Ramanathan**, and C.W.Min, "MV-RLU: Scaling Read-Log-Update with Multi Versioning", In Proceedings of the **ASPLOS**, RI, April 2019.

M.K. Ramanathan and W.M. Lin, "A Controlled Fetching Technique for Effective Management of Shared Resources in SMT Processors." **Microprocessors and Microsystems** 57C (2018).

NOTABLE ACADEMIC PROJECTS

Designing Optimistic Concurrency Control (OCC) Protocol Using Version Locks
Designed OCC locking protocol using version locks, implemented in C++. Evaluated Version lock against Readers-writer lock, Lock-free, and mutex-enabled hash table. Version lock shows high scalability, and performance and exhibits better sensitivity towards hotspots and NUMA.
Design IO Benchmarks for Characterizing Emerging byte-addressable Persistent Memory
Designed an IO benchmark framework to study and evaluate the performance and multi-core scalability aspects of byte-addressable persistent memory**.**
Design and Evaluation of Concurrent Data Structures
Implemented linked list and hash table using three different concurrency models—Mutex, Lock-free, and transactions and evaluated the performance and multi-core scalability on a 64-core Intel server.
Design and Implementation of Smart Pointer Interface for Multi-Version Transactions
Implemented smart pointer interface using C++ for transactional programming. Smart pointer interface hides the complexities of multi-versioning under the hood and enables applications to develop and design data structures like a typical C++ 11 program.
Design and Implementation of Simple Distributed Shared Memory
Utilized C to implement page-granule MSI protocol among different machines using userfaultfd and the communication between the machines is established using socket programming.

HONORS and AWARDS

Travel Grant for FAST 2023 ASPLOS 2019, ASPLOS 2020, NVMW 2020.
OCI Scholarship awarded by The Open Cloud Institute. University of Texas, San Antonio
Valero Research Scholarship awarded by Valero Energy Corporation in Spring 2016.
ECE Pioneer Scholarship awarded by The Department of ECE, University of Texas, San Antonio.

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RESEARCH INTERESTS

Scalable Storage and Operating Systems Design, Parallel and Concurrent Programming, Distributed Storage, Computer Architecture, and Systems for Machine Learning.

REFERENCES

Dr. Changwoo Min (Advisor),
Igali (previously at Virginia Tech)
multics65@gmail.com
Dr. Sudarsun Kannan,
Asst Professor at Rutgers University,
sudarsun@rutgers.edu
Dr. Ali R. Butt,
Professor at Virginia Tech,
butta@cs.vt.edu
Dr. Sanidhya Kashyap,
Asst Professor at EPFL,
sanidhya@epfl.edu