ESE 555 Final Project

8 BIT CARRY SELECT ADDER

Madhu Sudhanan | 115294248 | 17th Dec, 2023

Abstract

This project aims to design and verify a pipelined synchronous 8-bit carry select adder using a 45nm CMOS technology. The primary objective is to minimize the power consumption and ensure that it can run at 4GHz while also keeping minimal area.

A 1-bit mirror adder, 2-to-1-mux and d-flip-flop were designed and then used to for an 8-bit carry select adder. Layout of the same was also designed. Schematic level and post-layout simulation were performed to verify the design.

Area of layout – 1246.46 μm^2

Speed of schematic simulation – 5.8GHz

Speed of post-layout simulation – 4GHz

Average power in schematics – 736 µW

Average power post-layout – 1.106 mW

Introduction

Adders are digital circuits that perform the basic arithmetic operations of additions and subtractions that most other operations are dependent on a computer system, such as address calculation, branch target address calculation or any data calculations.

In mulit-bit adders, the carry path is usually the critical path and hence we try to concentrate on reducing it as much as possible. Various adder topologies and designs have been proposed in the past to alleviate this issue, trading power and area and delay of carry generation path.

Carry select adder is a popular architecture that exploits this tradeoff. The carry-out is computed for both values of the carry-in before the actual carry-in is generated. Once the
correct carry-in is generated, the corresponding carry-out is chosen utilizing a multiplexor.

1) RIPPLE CARRY ADDER

The ripple carry adder is notable for establishing the quickest carry path possible, despite its simplicity and energy efficiency. Nevertheless, it still experiences a noticeable amount of delay. In this design, the carry-in of the next most significant full adder replaces the carry-out of each preceding full adder. This characteristic gives the term "ripple carry adder" its name, as each carry bit ripples into the subsequent step.

In a ripple carry adder, the correctness of the sum and carry-out bits for each half adder stage relies on the presence of the carry-in for that specific stage. This dependence arises from propagation delays within the logic circuitry, where propagation delay represents the duration between the application of an input and the corresponding output.

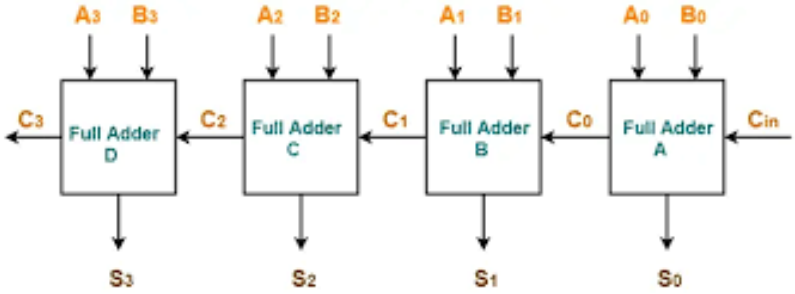


Figure 1: 4-bit ripple carry adder.

2) CARRY LOOK AHEAD ADDER

The Carry Look-Ahead Adder is an improved version of the ripple carry adder, offering simultaneous and rapid generation of the carry-in for each full adder with a time complexity of (log n). In parallel adders, the carry output from each full adder serves as the carry input for the subsequent higher-order state. This ensures that adders cannot produce carry and sum outputs for any state without a specific carry input for that state. Consequently, the circuit must wait for the carry bit to propagate to all states before computation can take place, resulting in a carry propagation delay.

While effectively reducing propagation latency, it's essential to highlight that only the first carry bit from the initial stage influences the carry output at any given step. This characteristic allows for the calculation of intermediate results. Currently, the Carry Look-Ahead Adder stands as the fastest adder utilized in computing.

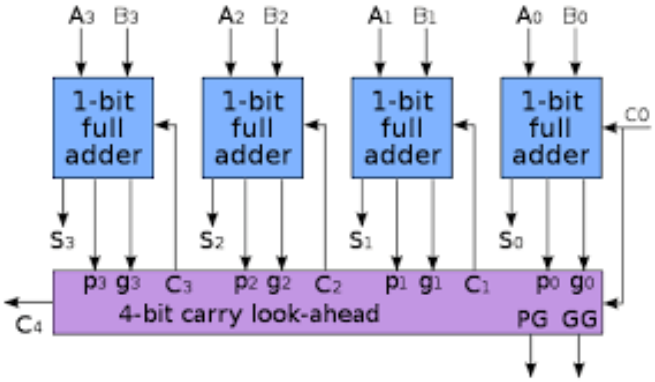


Figure 2: Carry look ahead adder.

3) CARRY SKIP ADDER

Incorporating dynamic principles into Carry Look-Ahead (CLA) methods is a key factor in achieving high performance, and one example of this integration in CMOS circuitry is the Manchester Carry Chain (MCC). In MCC, the PMOS transistor undergoes pre-charging when the clock (Clk) is low, resulting in a

zero output. Conversely, the NMOS evaluation transistor activates when the Clk is high, and the circuit's output is determined by logic. When Pi is equal to 1, ci+1 equals ci.

Due to technical limitations, the Manchester carry chain is restricted to a length of four links. The transistor-level circuit schematic of a basic 4-bit MCC using footless domino logic is illustrated in Fig. 3.

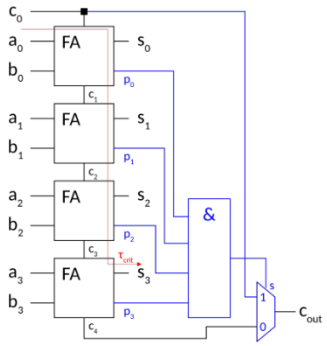


Figure 3: Carry skip adder.

Implementing the MCC with footless domino logic enhances speed, and there is also a reduction in the total transistor count and system clock load capacitance because of this implementation.

Carry Select Adder Design

1) BLOCK LEVEL ARCHITECHTURE

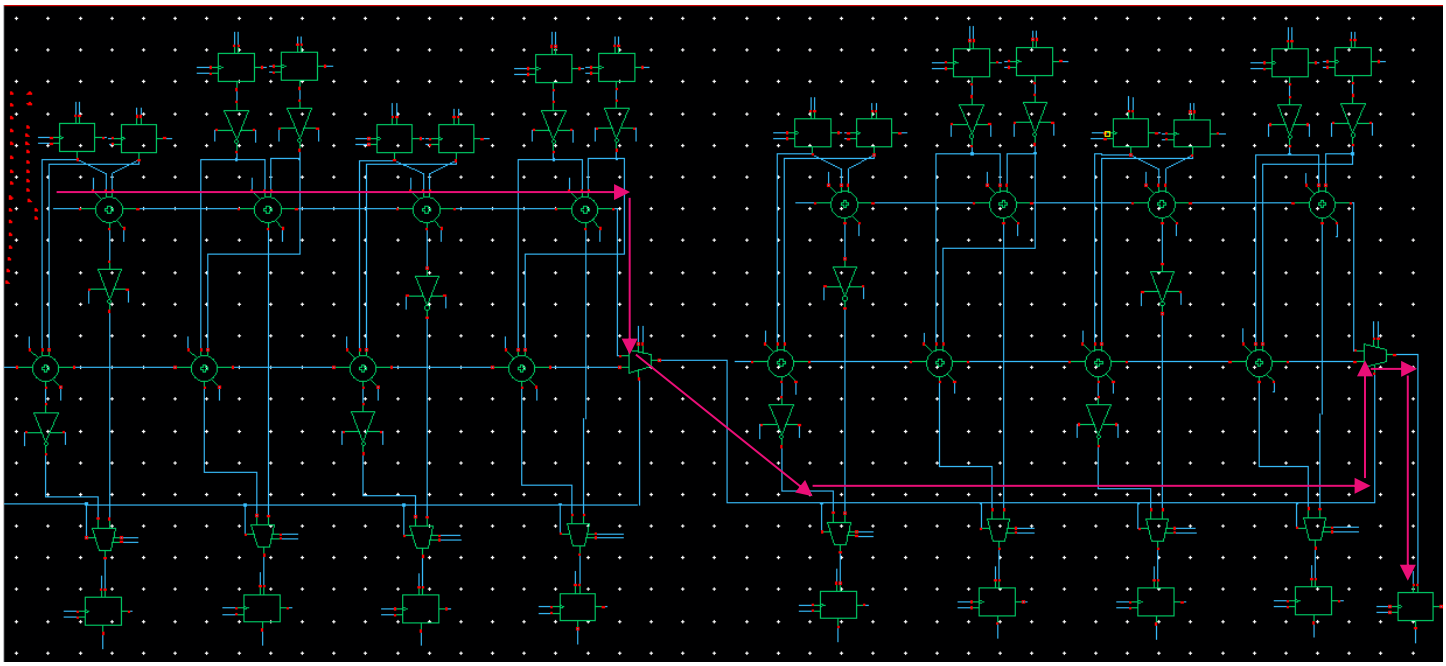


Figure 4: 8-bit CSL adder top level schematic.

- Here we can see the top-level architecture of the 8-bit carry select adder. Inputs Ao – A7 and Bo – B7 go through a register (d-flip-flop).

- The 8 bits are divided into 4-bit blocks each with ripple carry adders.
- Within each 4-bit block we have two ripple carry adders whose Cin is set to '0' and '1'. At the end of the 4^{th} bit, each of the carry is sent to a multiplexer whose select signals is the previous block's carry.
- The final block's Cout would be the overall carry signal.
- In this this case the first block's Cin is always '0' and although carry select architecture in the first block is not required, it is included for modular design purposes so that this can be instantiated directly in larger bit adders.
- This architecture uses 'Inversion' technique to reduce critical path by eliminating inverters at Cout (since Cout logic is inverting). Then when we send ~Cout to the next adder, we also need to invert the inputs to give non-inverted outputs, since this addition operation is a symmetric function. Although, this adds inverter delay to sum, it does not affect overall performance since carry path is the critical path.
- Similarly, for the above reasons, output sums from adders are inverted alternatively.
- The sums from each adder go to a multiplexer to select the valid sum based on previous block's carry.
- These outputs of the muxes are connected to registers for synchronizations.
- The flip-flops have clk, reset, D and Q.
- No intermediate pipelining was done. Flip-flops are used only at the primary inputs and primary outputs.
- The highlighted path in pink is the critical path that determines the clock period.

2) D-FLIP-FLOP

- The D flip-flop is implemented by employing CMOS inverters, transmission gates, NAND gates, tri-state NANDs, and tri-state inverters. Together, these components contribute to the flip-flop's functionality, enabling precise control and synchronization within the design. The integration of flip-flops and the associated CMOS components is crucial for optimizing the performance and frequency characteristics of the adder.
- It has 3 inputs for clock, reset and data, and one output for data. The reset is asynchronous.

Schematic of D-Flip-Flop

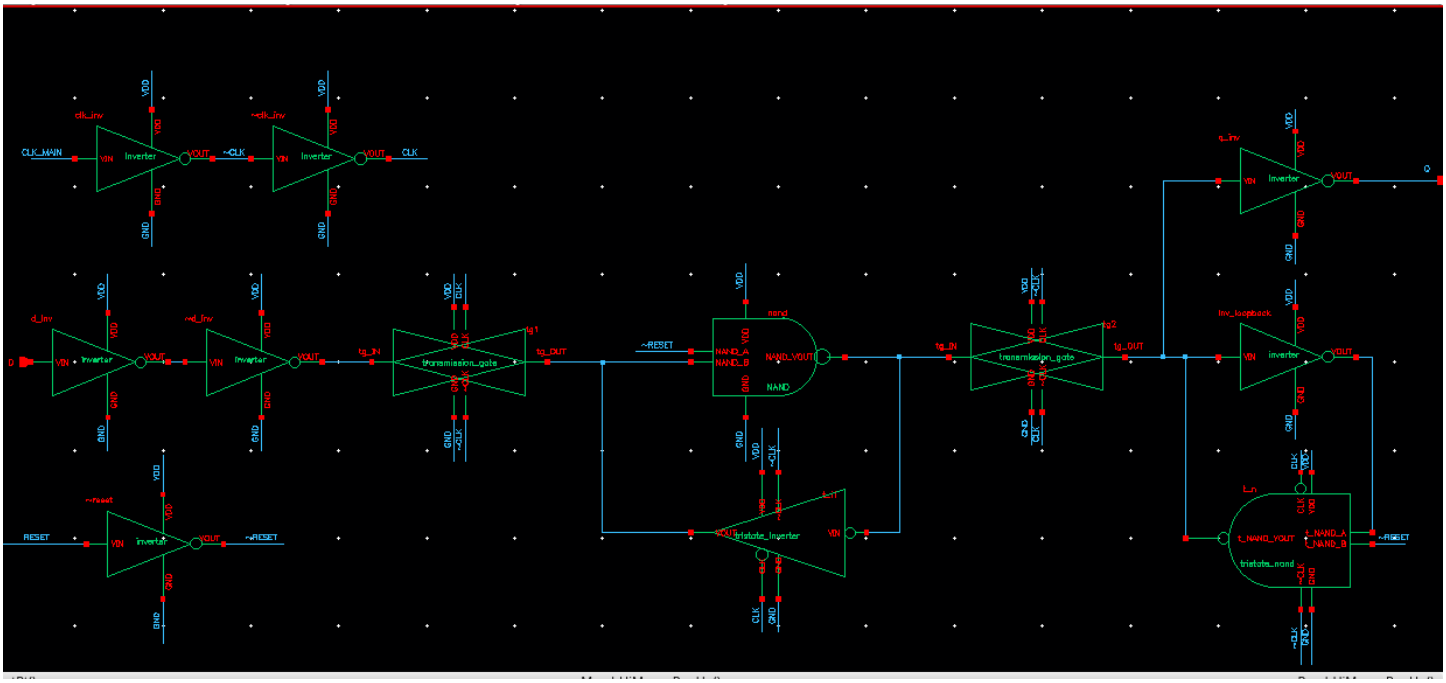


Figure 5: D-Flip_Flop schematics.

Layout of D-Flip-Flop

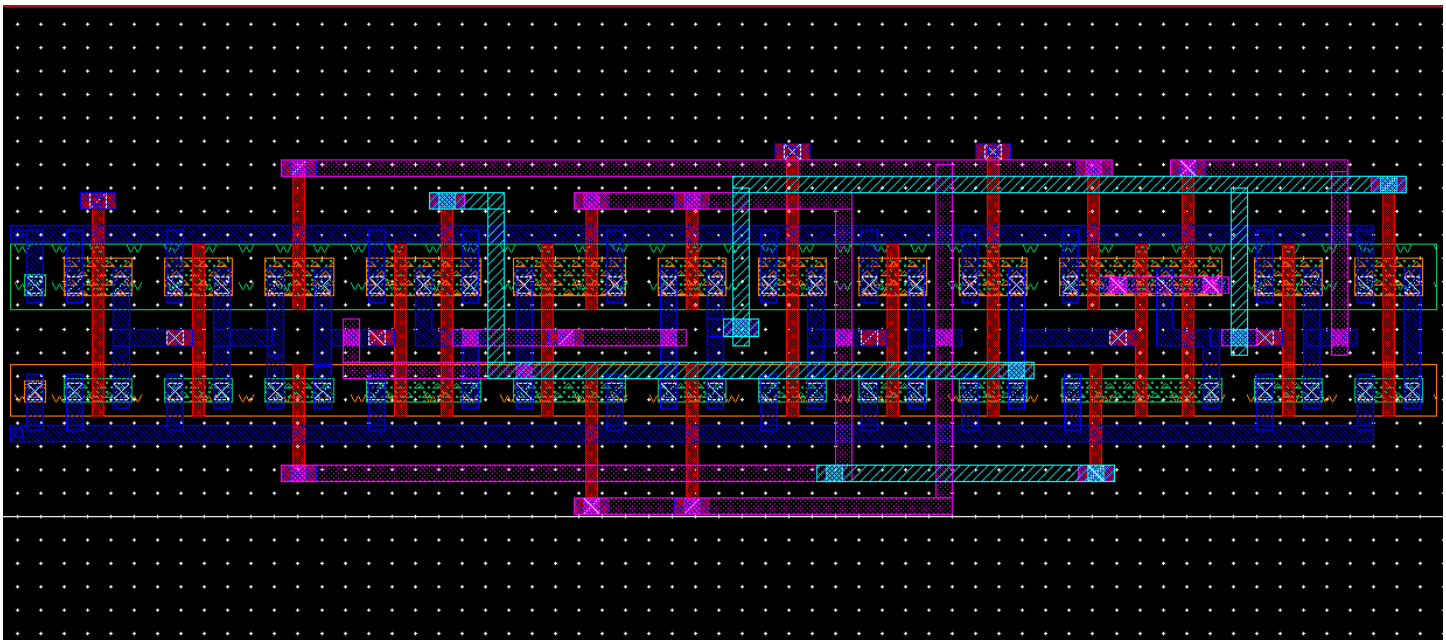


Figure 6: D-Flip_Flop layout.

3) 1-BIT ADDER

- The 1-bit adder implements the following logic:
  - Cout = AB + (A+B)Cin
  - Sum = ABCin + ~Cou(A + B + Cin)
- The topology chosen is a mirror adder which has 24 total transistors (output inverters excluded to implement 'inversion' technique in top level module).
- The driver transistors that drive ~Cout net is increased in size to produce more powerful pull-up and pull-down network to reduce delay.
- The transistors directly connected to ~Cout net has been reduce in size to reduce gate capacitance on net because the sum logic is not the critical path.

Schematic of 1-Bit Adder

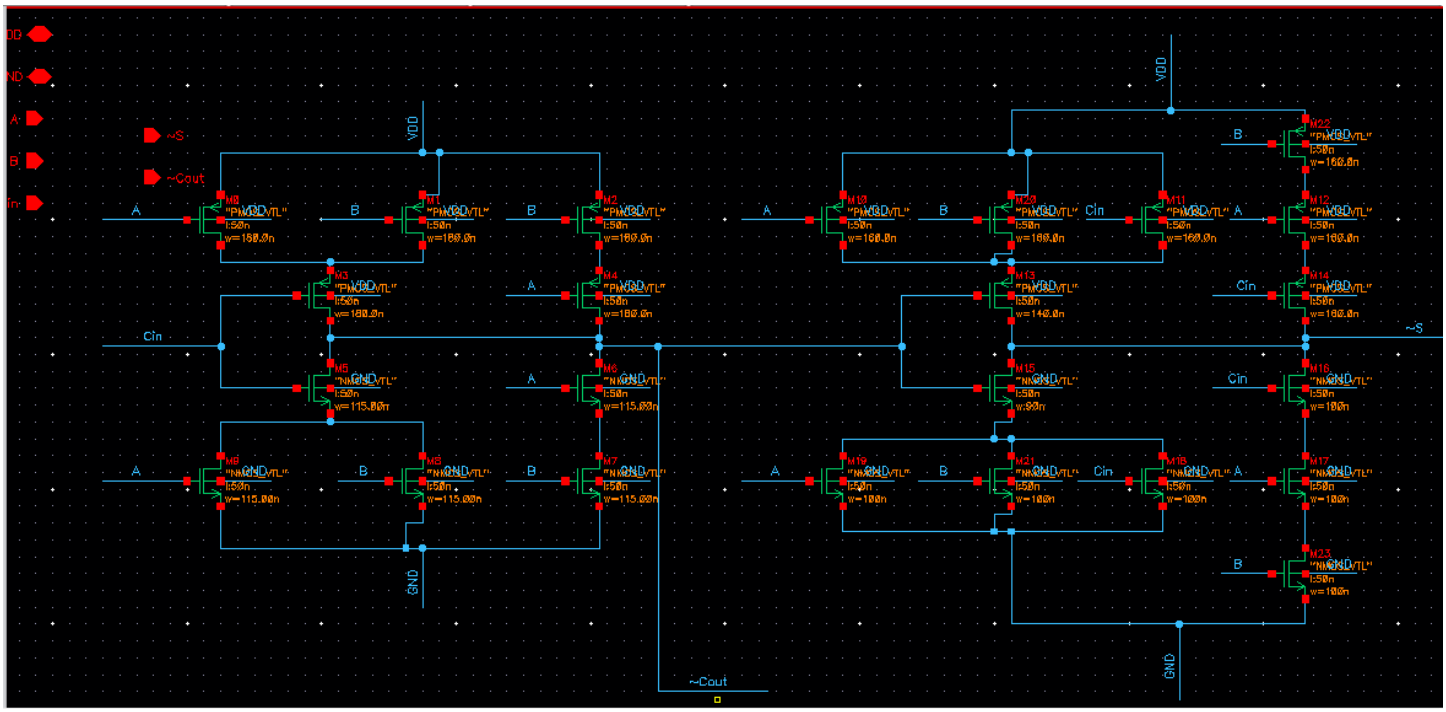


Figure 7: 1-bit mirror adder schematics.

Layout of 1-Bit Adder

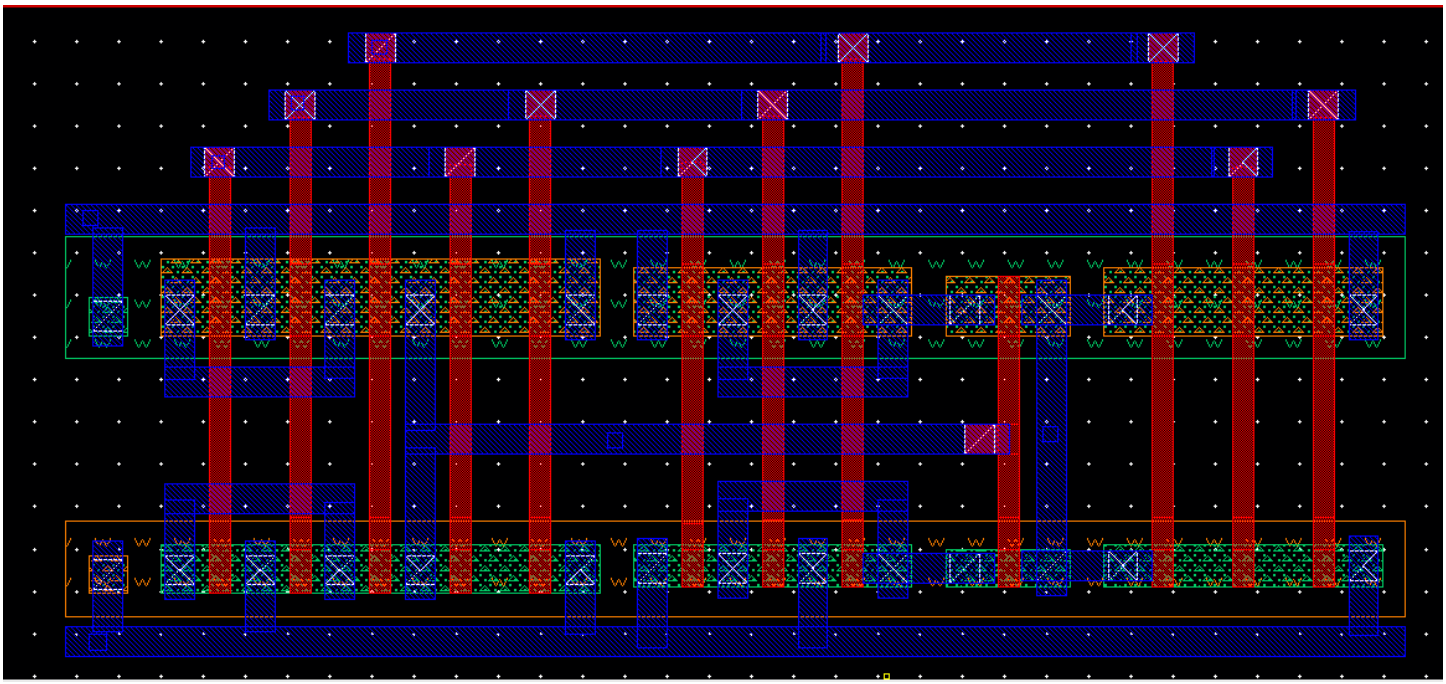


Figure 8: 1-bit mirror adder layout.

4) 2-TO-1-MUX

- The mux uses a select signal to select between two input lines. It uses transmission gate for this purpose.
- The input select signal is inverted using an inverter.
- If the select is '0', it outputs input 1 and input 2 otherwise.

Schematic of 2-to-1-mux

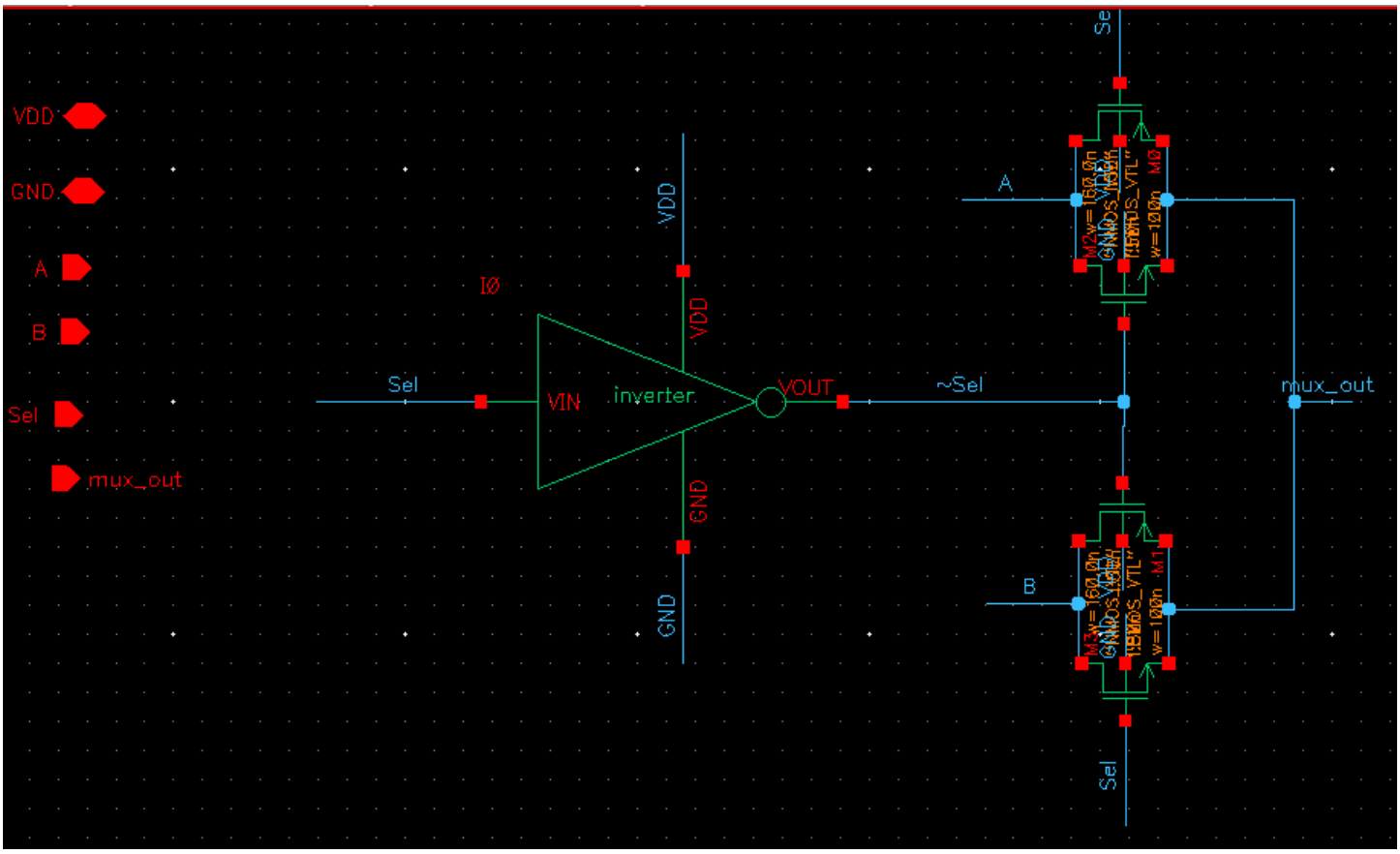


Figure 9: 2-to-1-mux schematics.

Layout of 2-to-1-mux

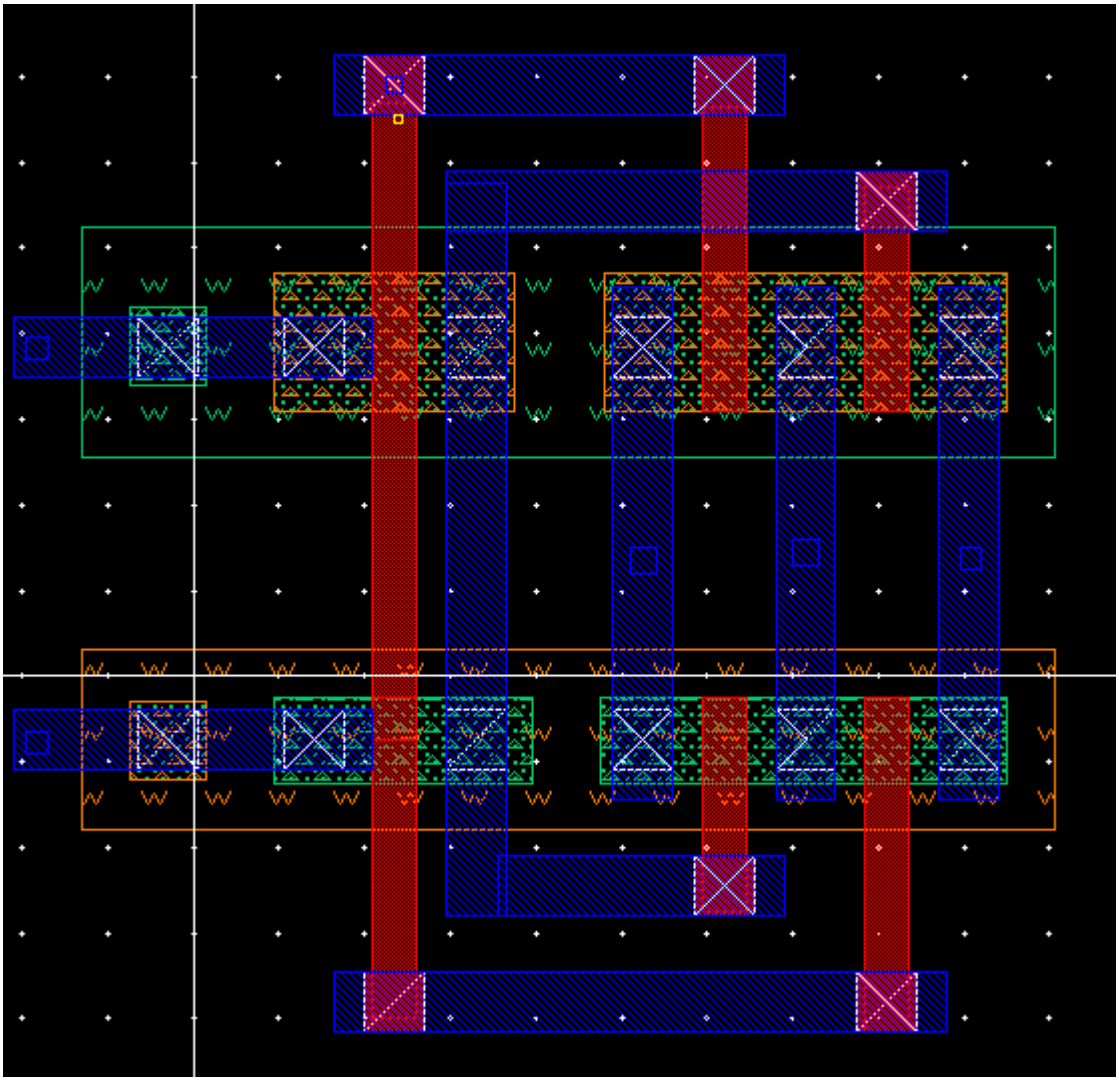
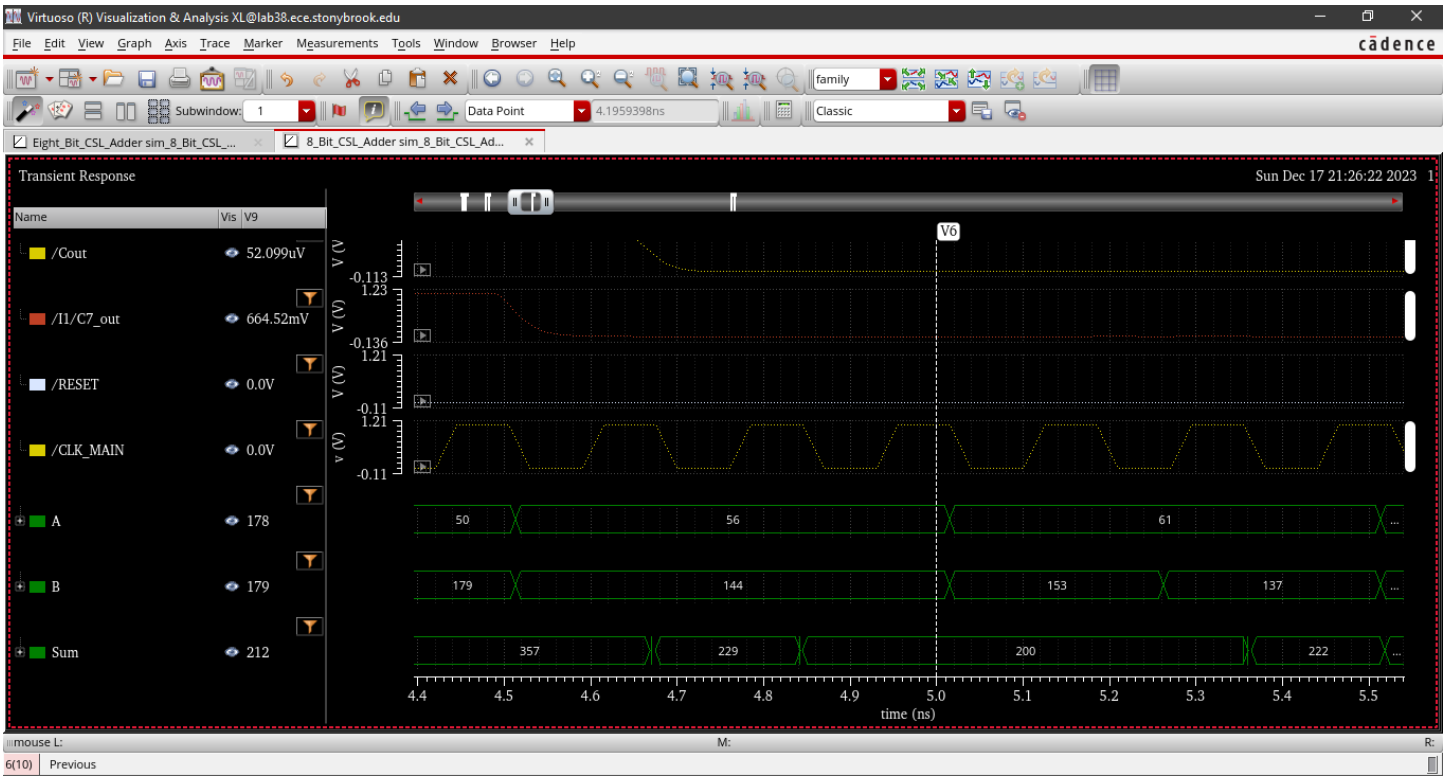


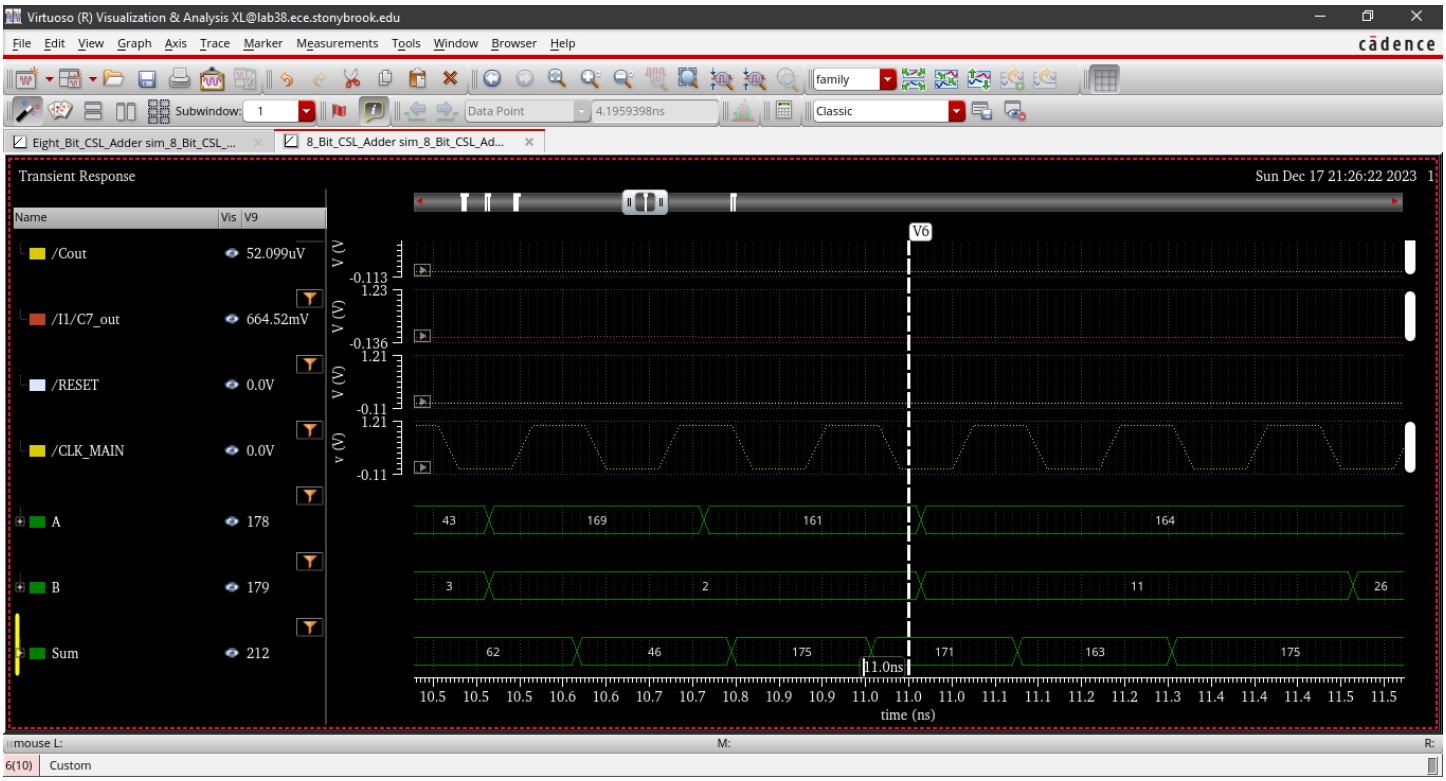
Figure 10: 2-to-1-mux layout.

Schematic Simulation results

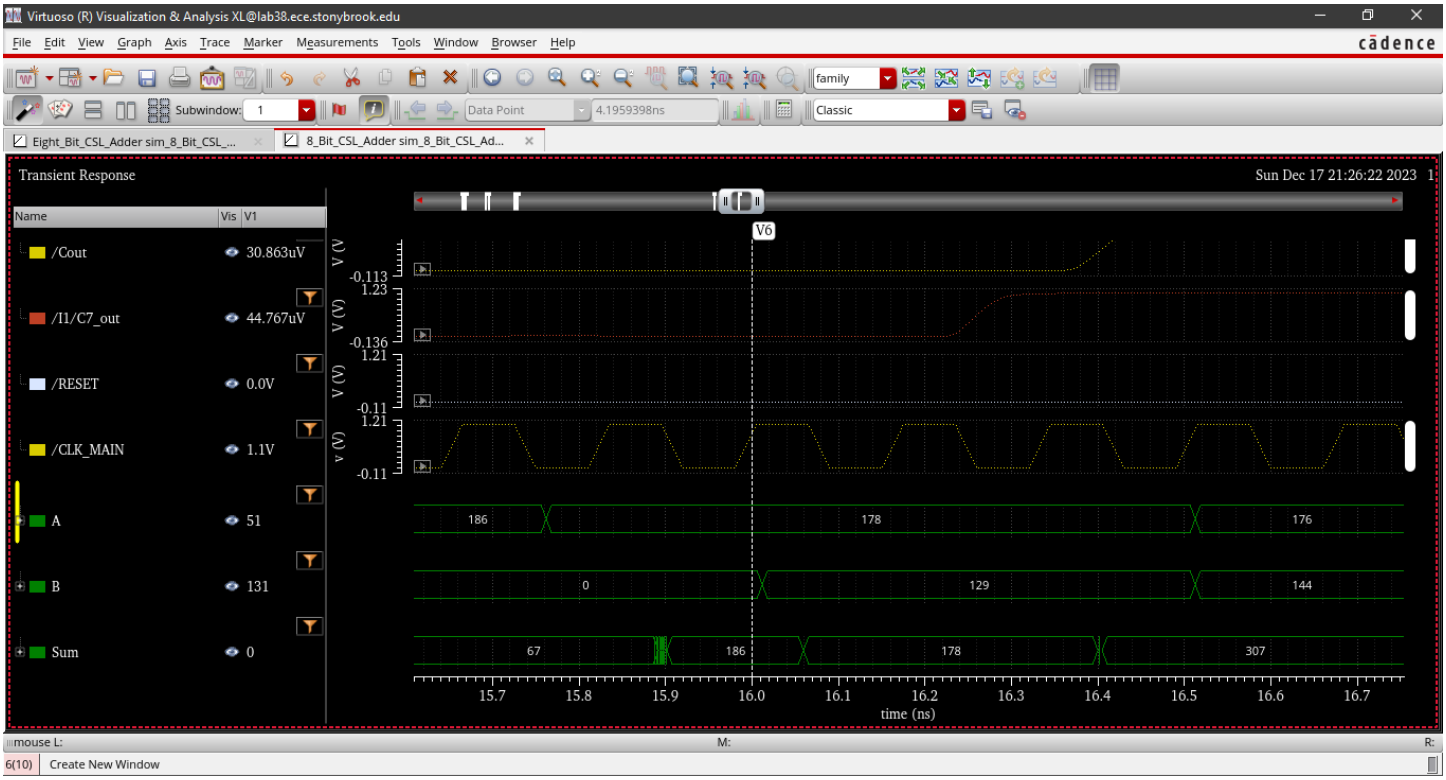
5ns



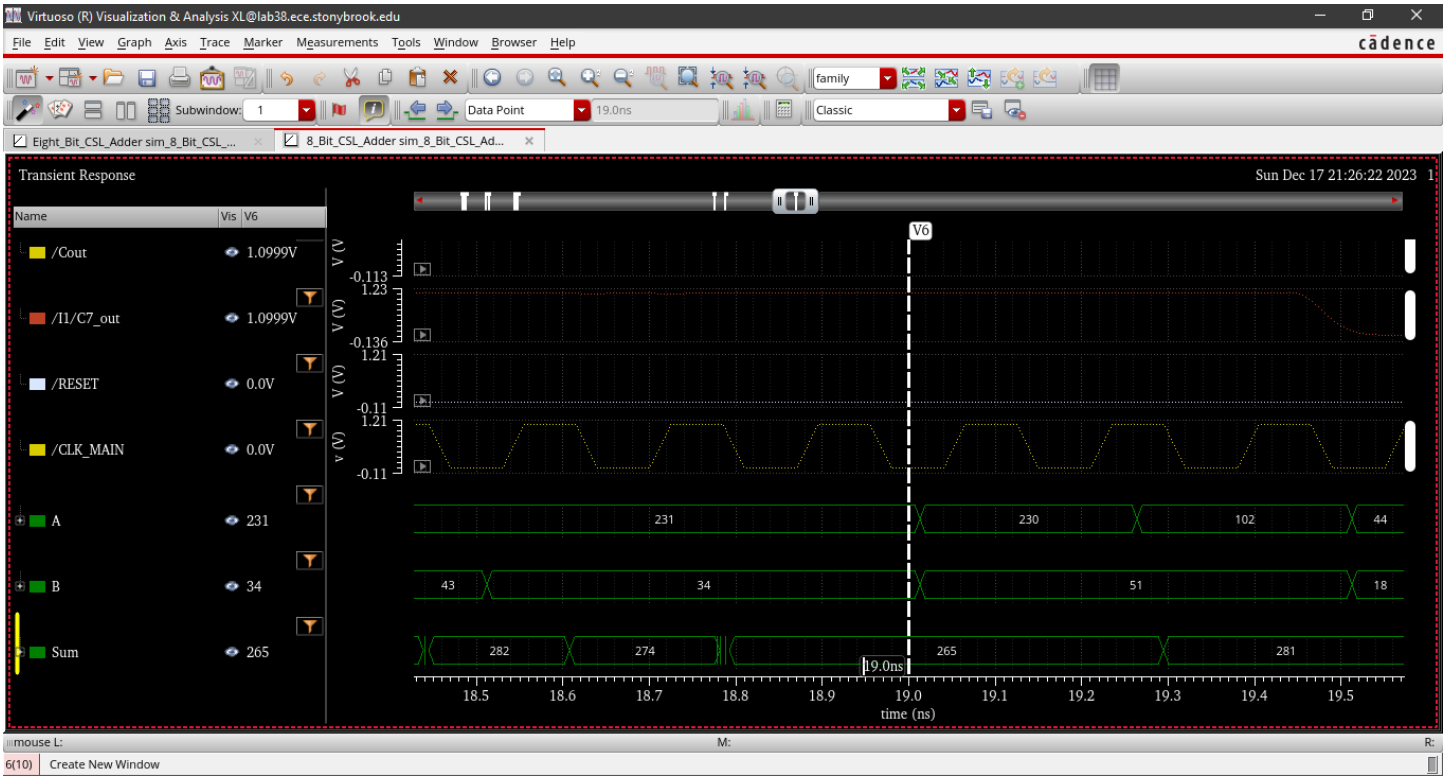
11ns



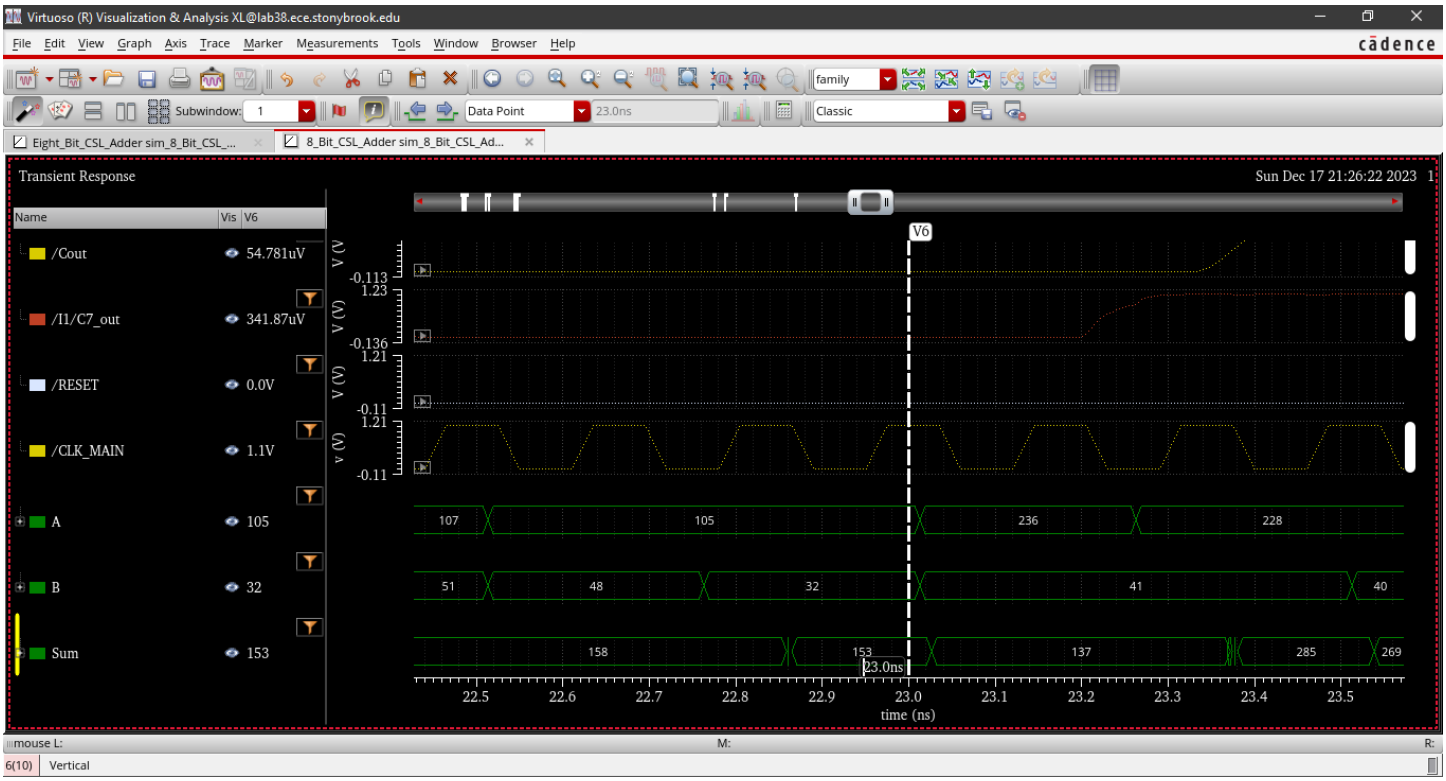
16ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V1
/Cout 30.863uV
/I1/C7_out 44.767uV
/RESET 0.0V
/CLK_MAIN 1.1V
A 51
B 131
Sum 0
V6
186 178 176
0 129 144
67 186 178 307
15.7 15.8 15.9 16.0 16.1 16.2 16.3 16.4 16.5 16.6 16.7
time (ns)

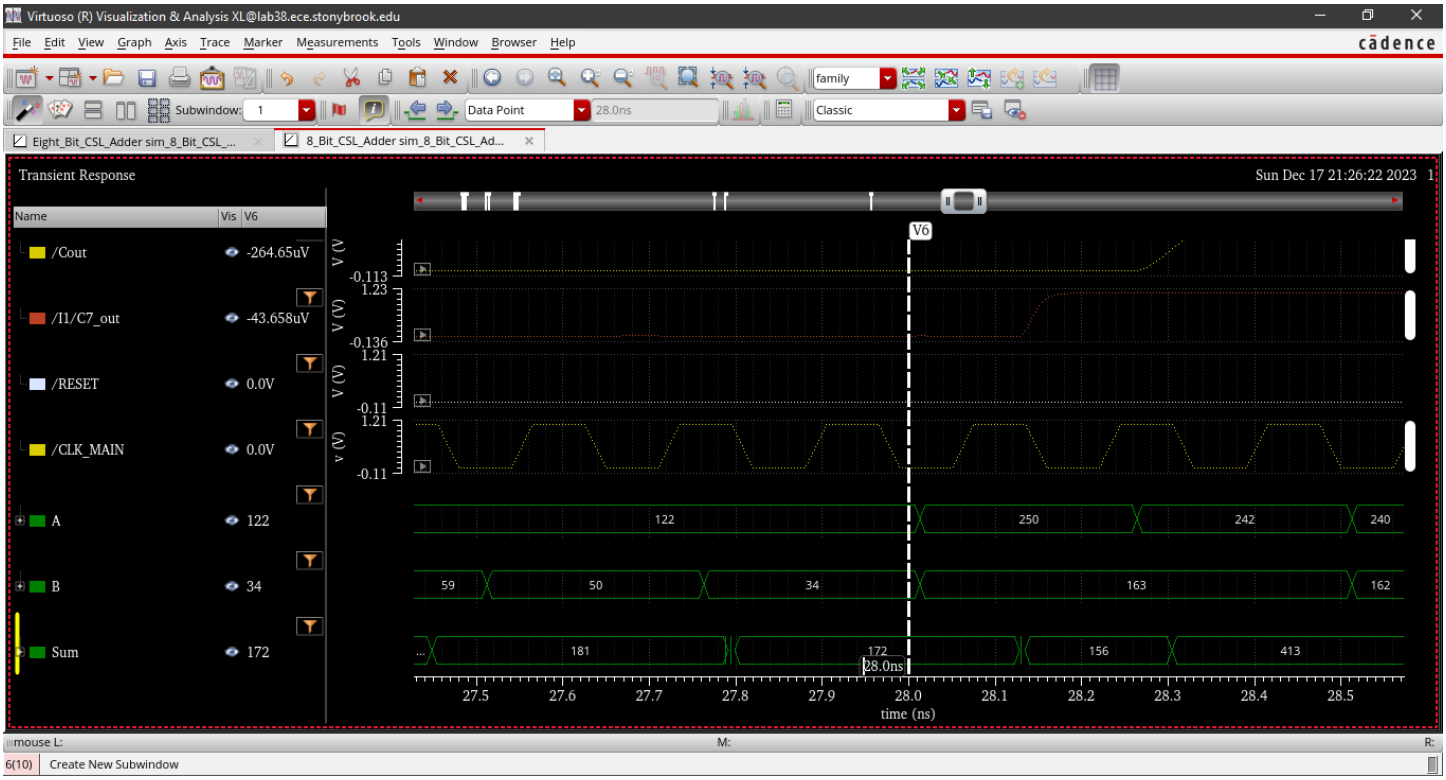
19ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V6
/Cout 1.0999V
/I1/C7_out 1.0999V
/RESET 0.0V
/CLK_MAIN 0.0V
A 231
B 34
Sum 265
V6
231 230 102 44
43 34 51 18
282 274 265 281
19.0ns
18.5 18.6 18.7 18.8 18.9 19.0 19.1 19.2 19.3 19.4 19.5
time (ns)

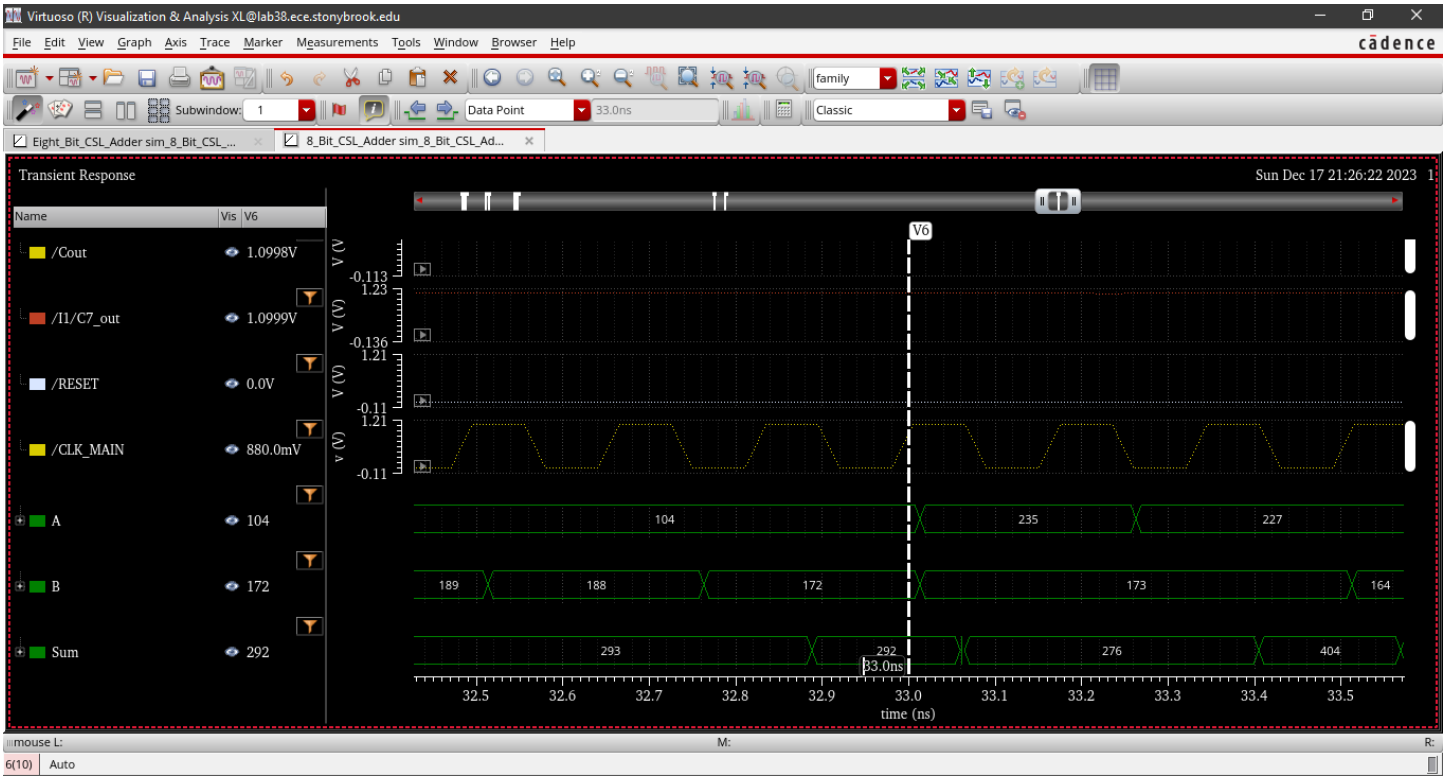
23ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V6
/Cout 54.781uV
/I1/C7_out 341.87uV
/RESET 0.0V
/CLK_MAIN 1.1V
A 105
B 32
Sum 153
V6
23.0ns
time (ns)
mouse L:
M:
R:
6(10) Vertical

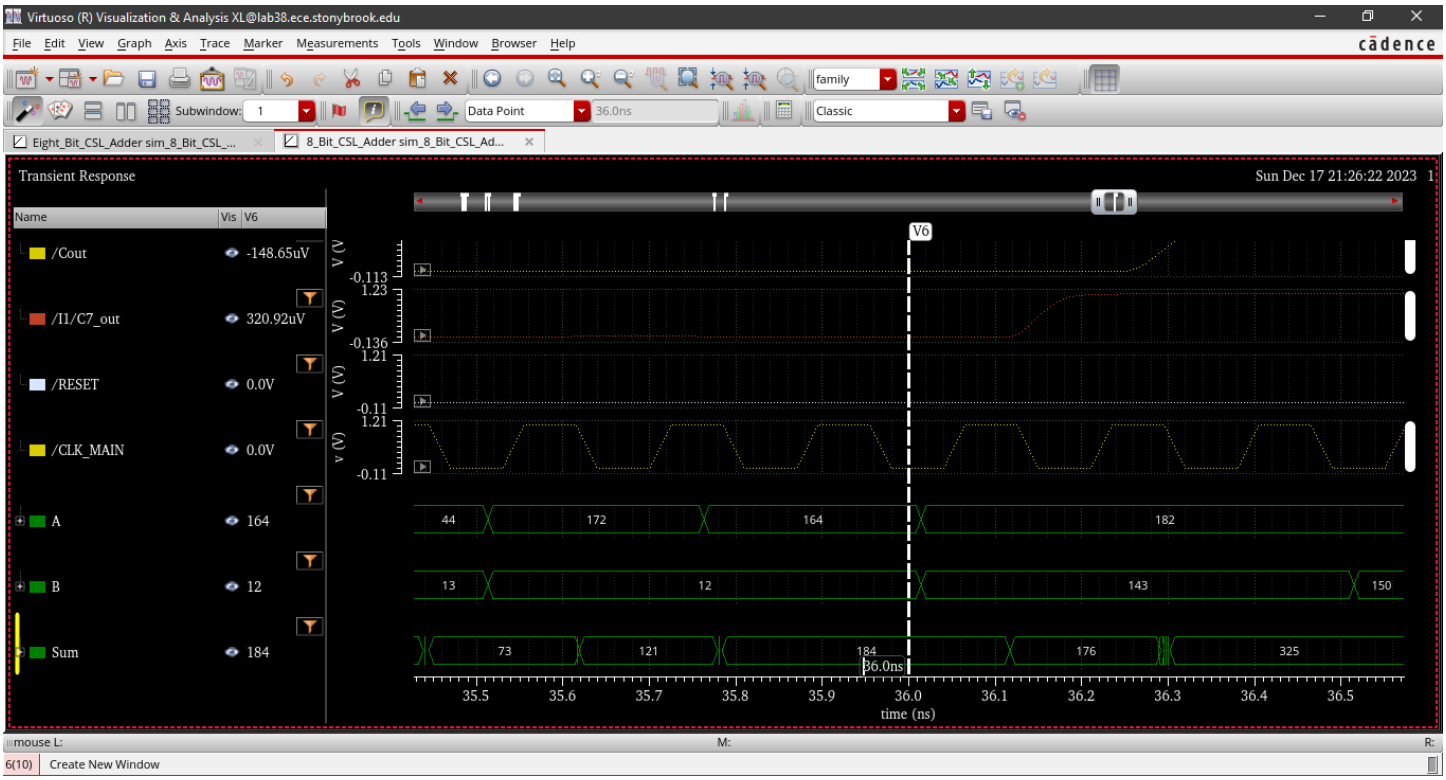
28ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V6
/Cout -264.65uV
/I1/C7_out -43.658uV
/RESET 0.0V
/CLK_MAIN 0.0V
A 122
B 34
Sum 172
V6
28.0ns
time (ns)
mouse L:
M:
R:
6(10) Create New Subwindow

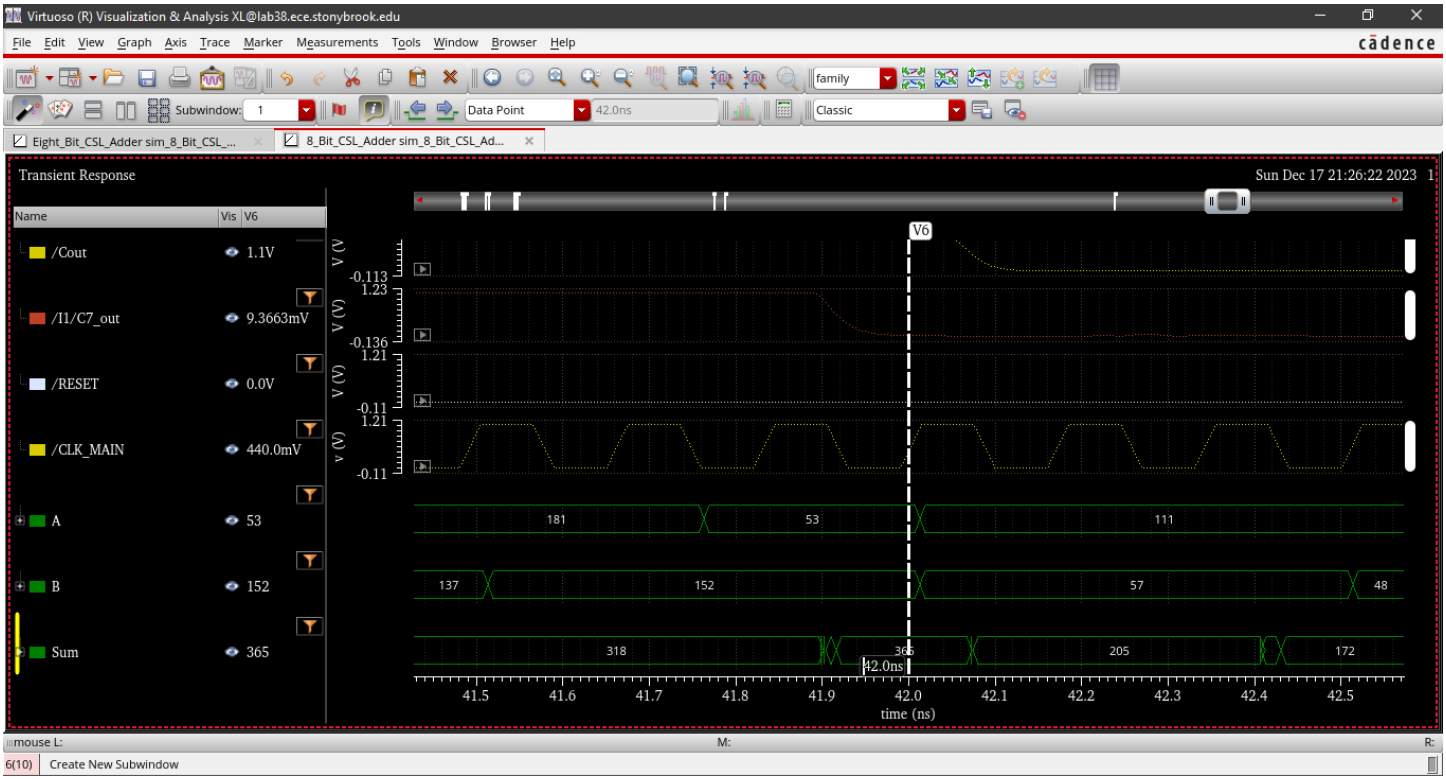
33ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V6
/Cout 1.0998V
/I1/C7_out 1.0999V
/RESET 0.0V
/CLK_MAIN 880.0mV
A 104
B 172
Sum 292
V6
104 235 227
189 188 172 173 164
293 292 276 404
33.0ns
32.5 32.6 32.7 32.8 32.9 33.0 33.1 33.2 33.3 33.4 33.5
time (ns)

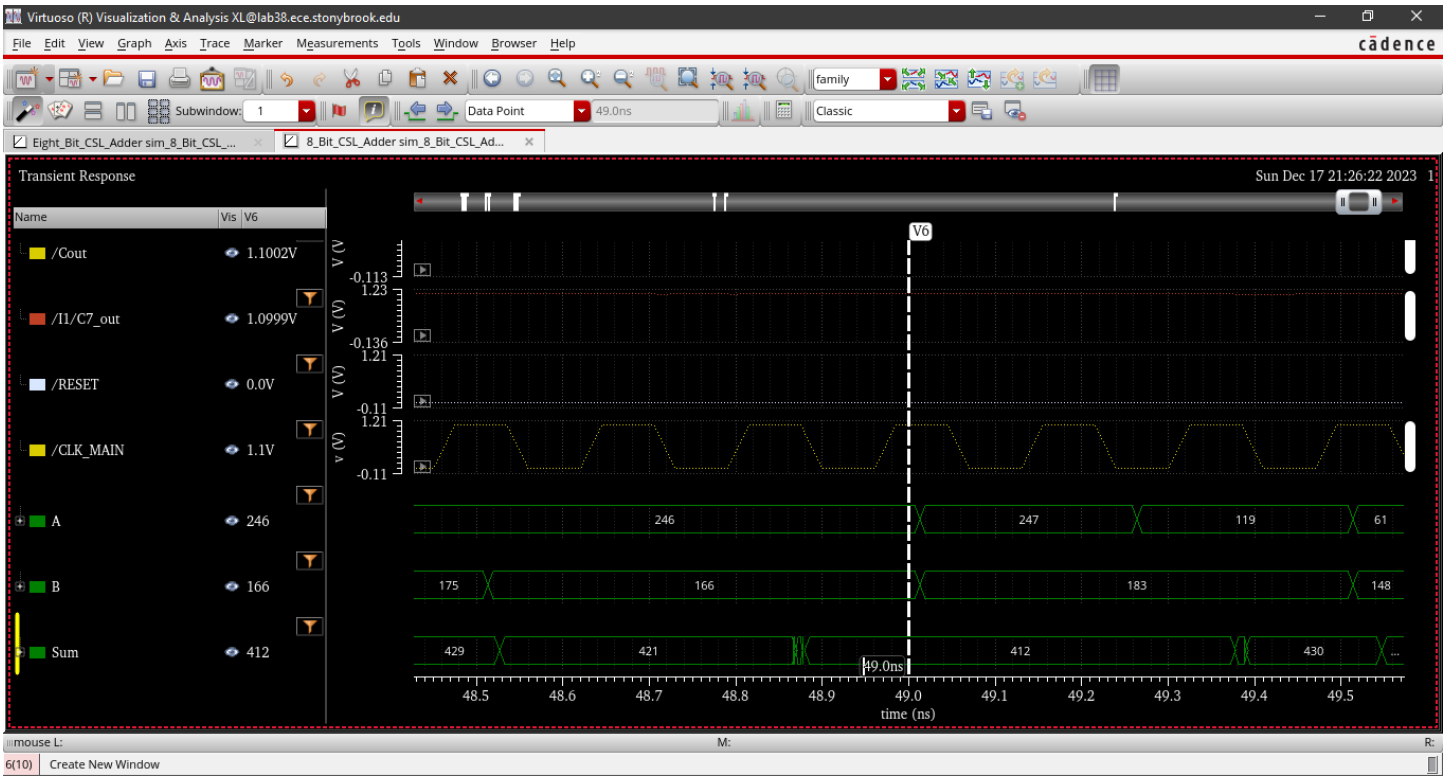
36ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 17 21:26:22 2023
Name Vis V6
/Cout -148.65uV
/I1/C7_out 320.92uV
/RESET 0.0V
/CLK_MAIN 0.0V
A 164
B 12
Sum 184
V6
44 172 164 182
13 12 143 150
73 121 184 176 325
36.0ns
35.5 35.6 35.7 35.8 35.9 36.0 36.1 36.2 36.3 36.4 36.5
time (ns)

42ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
Data Point
42.0ns
Classic
Eight_Bit_CSL_Adder sim_8_Bit_CSL_...
8_Bit_CSL_Adder sim_8_Bit_CSL_Ad...
Transient Response
Sun Dec 17 21:26:22 2023
Name
Vis
V6
/Cout
1.1V
/I1/C7_out
9.3663mV
/RESET
0.0V
/CLK_MAIN
440.0mV
A
53
B
152
Sum
365
V6
181
53
111
137
152
57
48
318
365
205
172
42.0ns
41.5
41.6
41.7
41.8
41.9
42.0
42.1
42.2
42.3
42.4
42.5
time (ns)
mouse L:
M:
R:
6(10)
Create New Subwindow

49ns


Virtuoso (R) Visualization & Analysis XL@lab38.ece.stonybrook.edu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
Data Point
49.0ns
Classic
Eight_Bit_CSL_Adder sim_8_Bit_CSL_...
8_Bit_CSL_Adder sim_8_Bit_CSL_Ad...
Transient Response
Sun Dec 17 21:26:22 2023
Name
Vis
V6
/Cout
1.1002V
/I1/C7_out
1.0999V
/RESET
0.0V
/CLK_MAIN
1.1V
A
246
B
166
Sum
412
V6
246
247
119
61
175
166
183
148
429
421
412
430
49.0ns
48.5
48.6
48.7
48.8
48.9
49.0
49.1
49.2
49.3
49.4
49.5
time (ns)
mouse L:
M:
R:
6(10)
Create New Window

Layout of 8-Bit Carry Select Adder

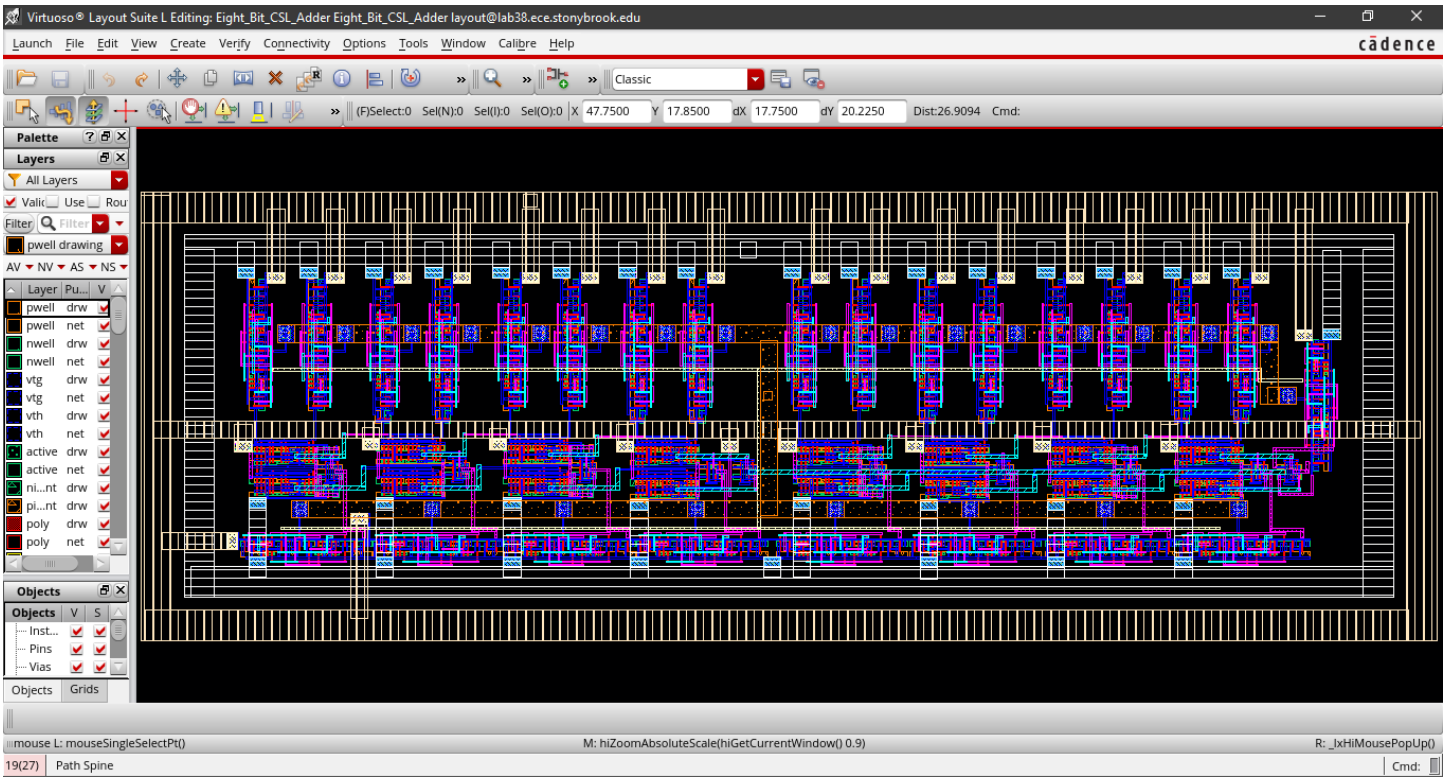
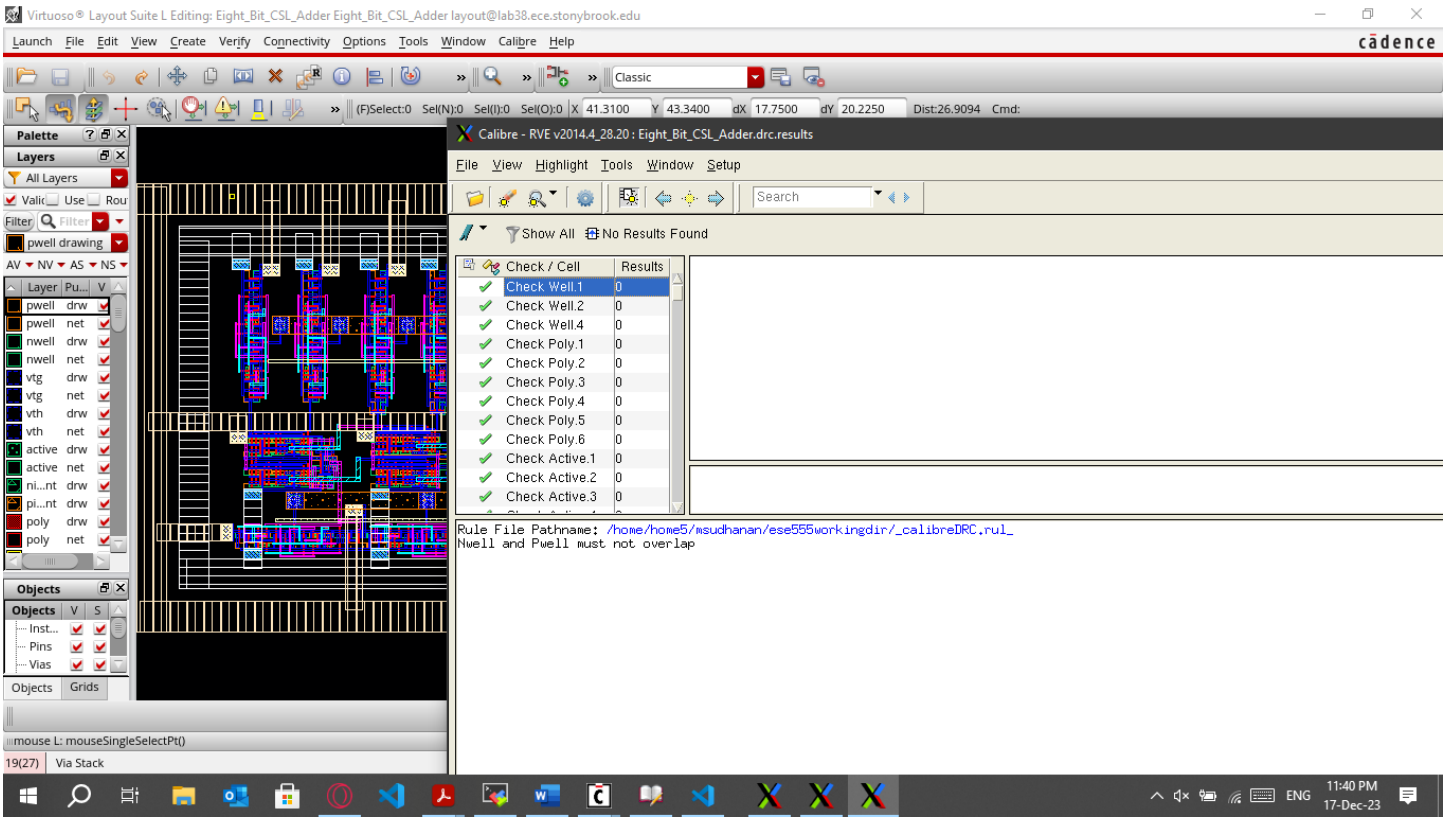
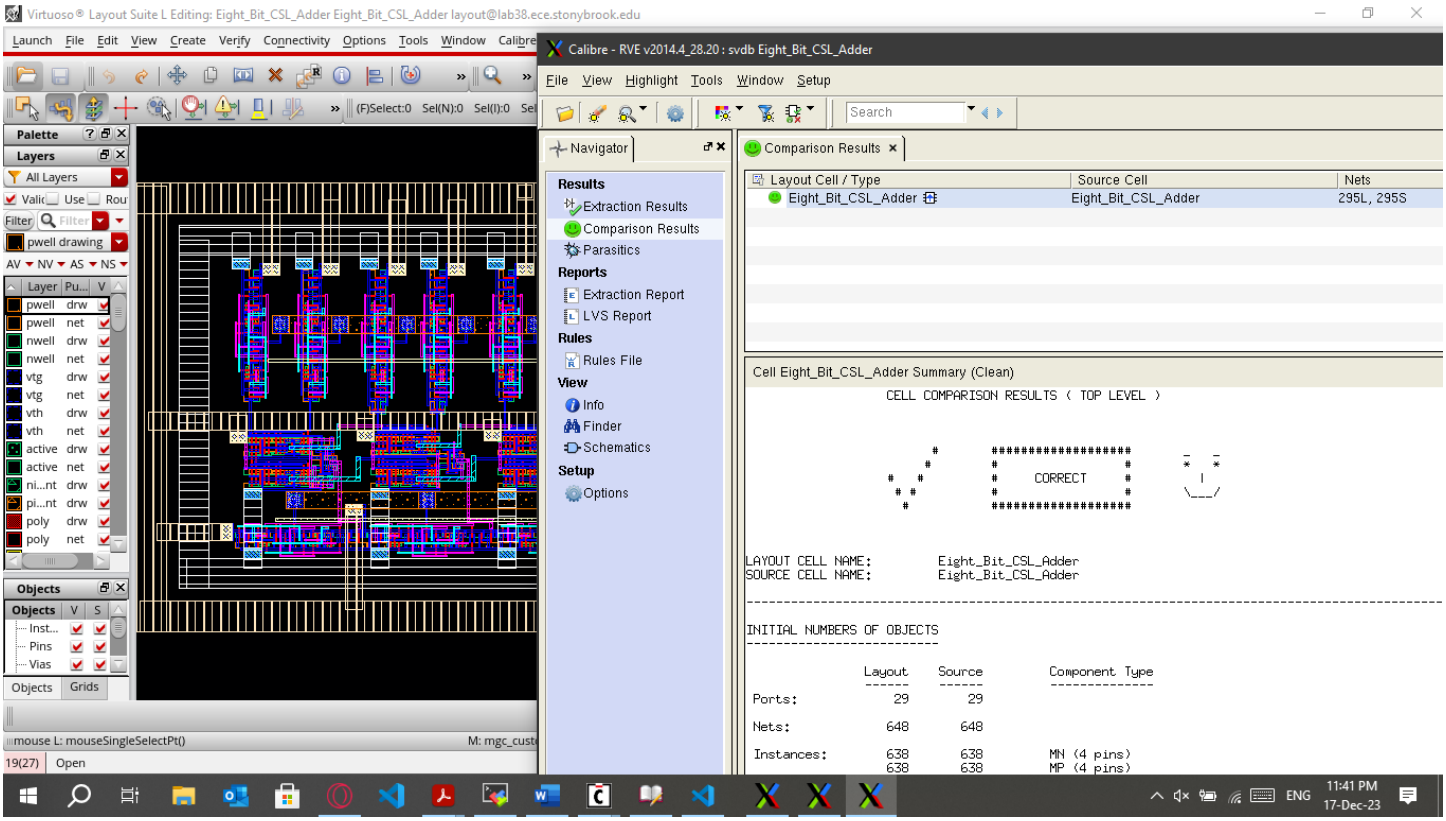


Figure 11: Layout of 8-bit CSL adder.

DRC

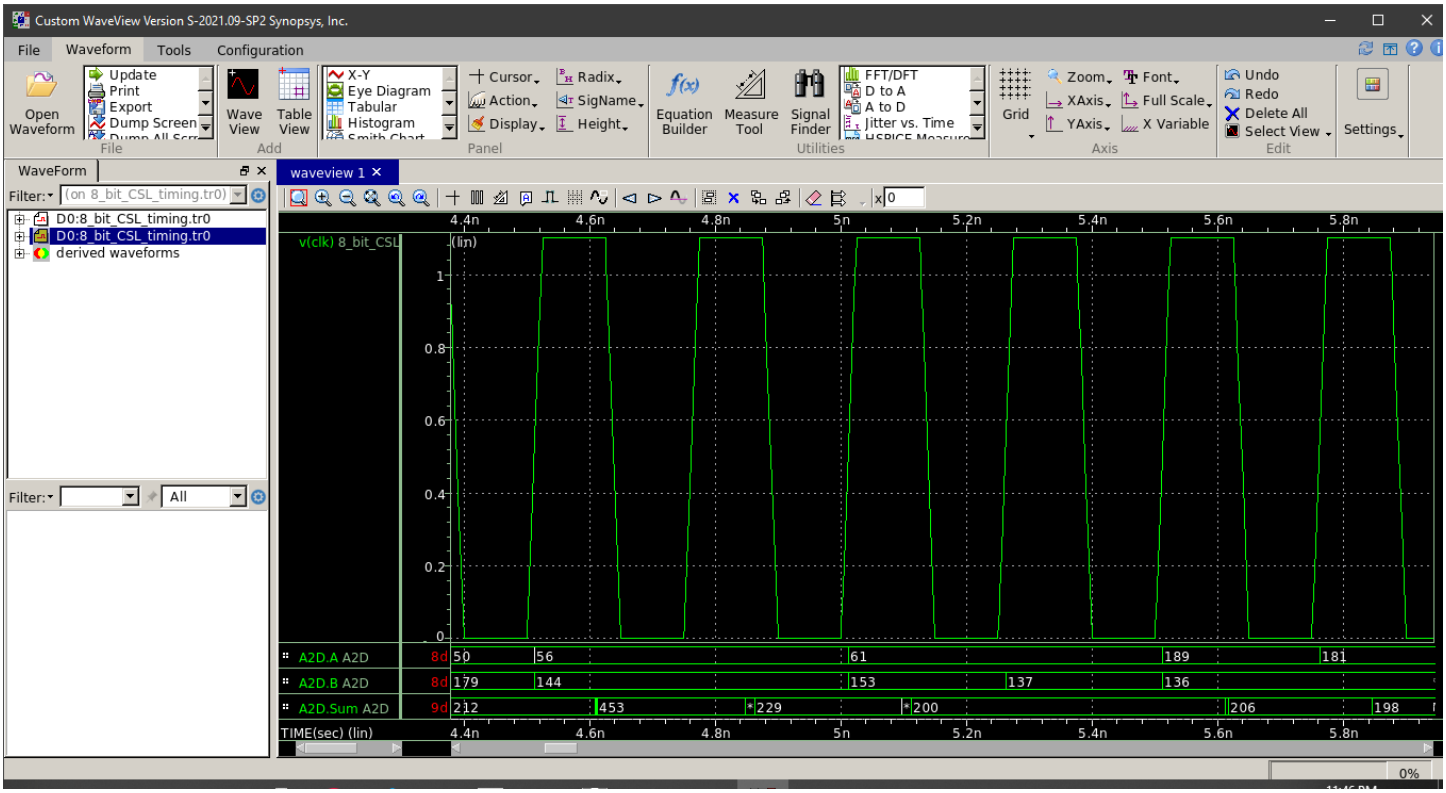


LVS

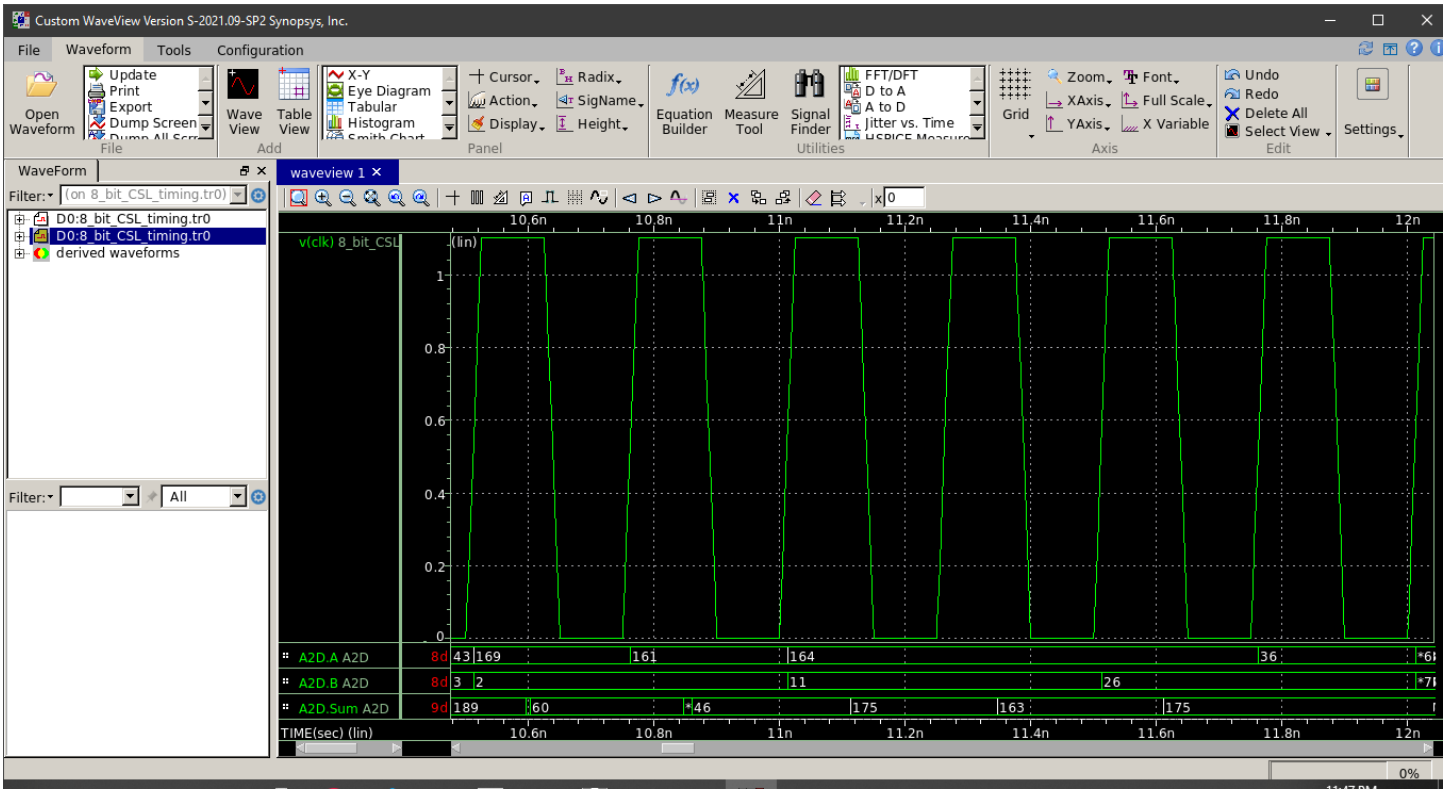


POST-LAYOUT SIMULATION RESULTS

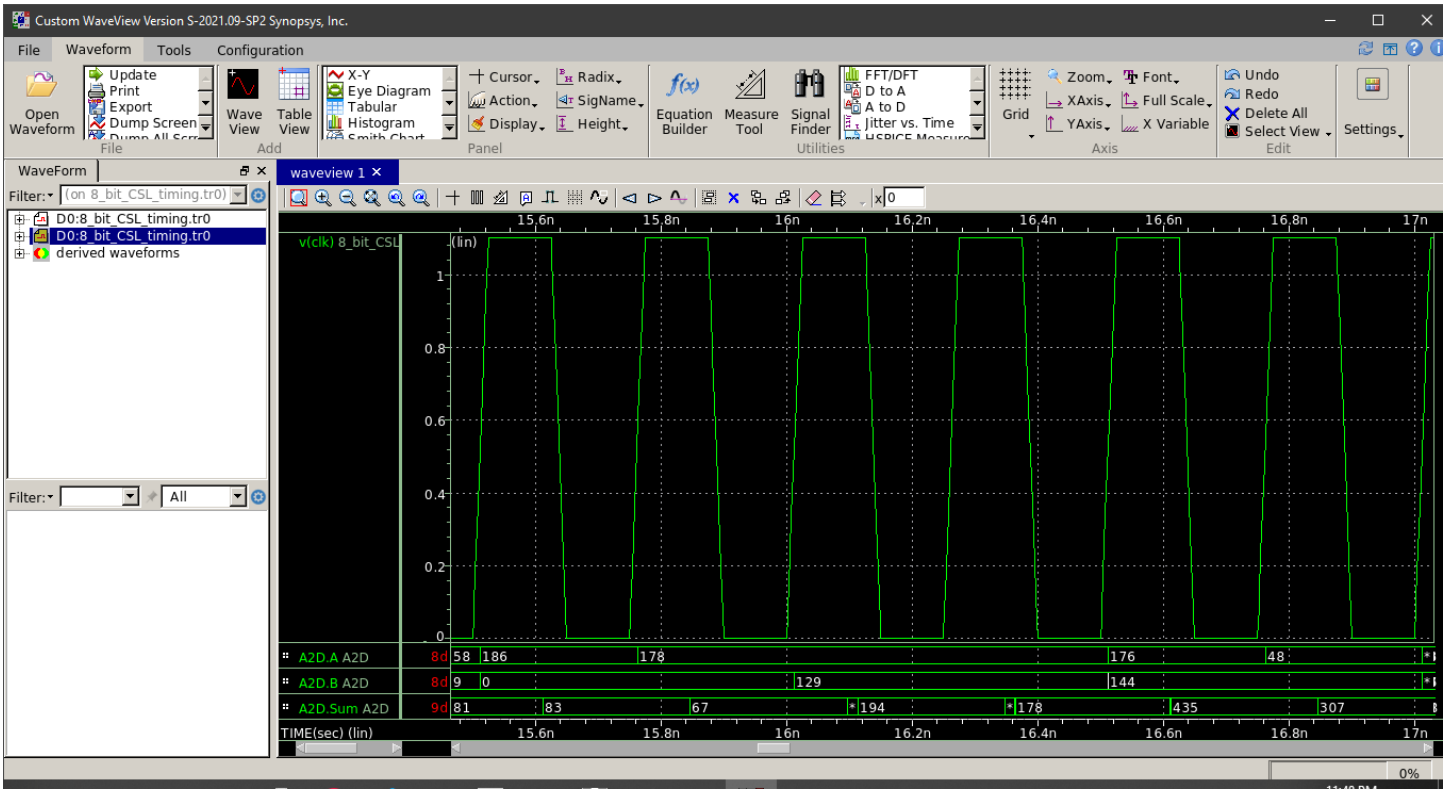
5ns



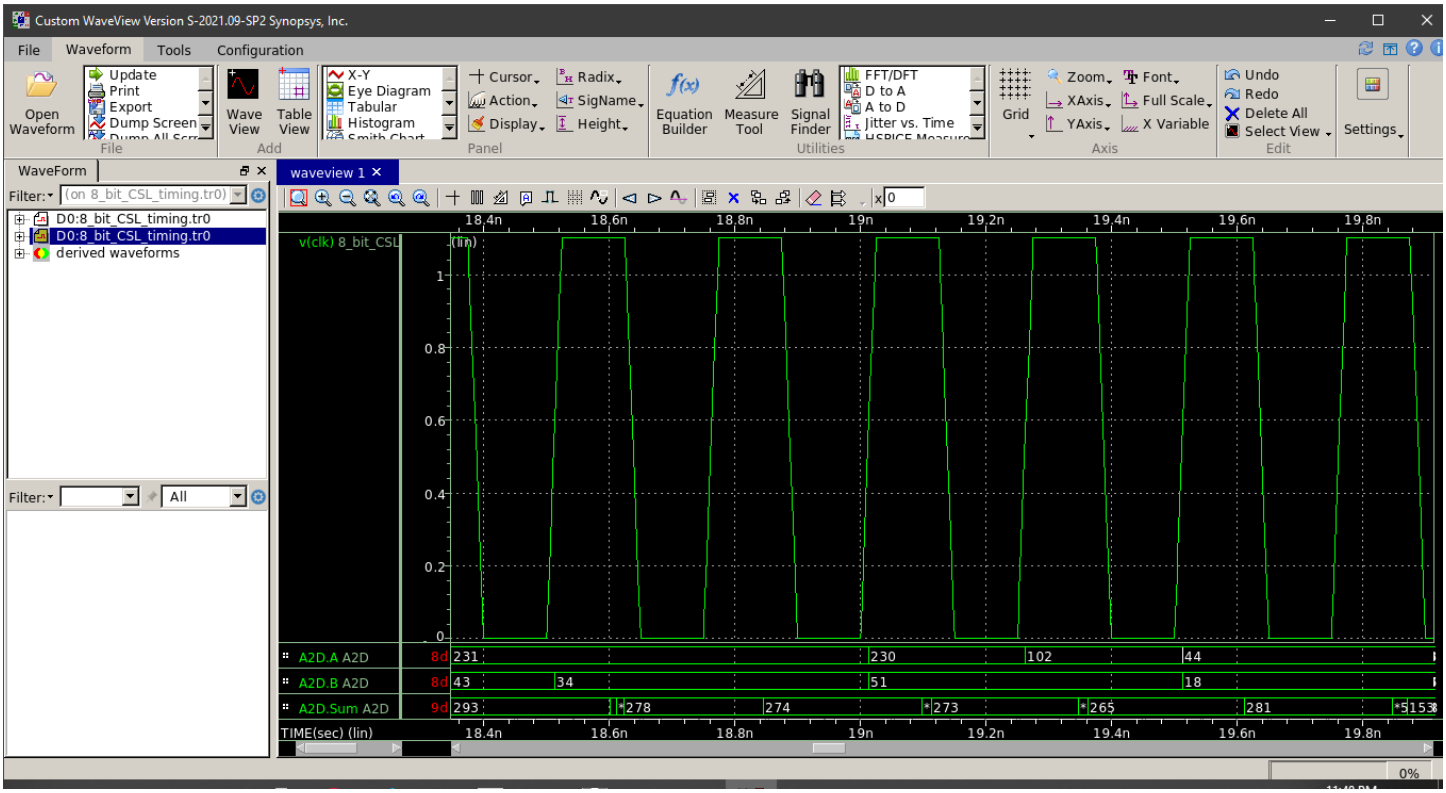
11ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Jitter vs. Time
Grid
Zoom
XAxis
YAxis
Font
Full Scale
X Variable
Undo
Redo
Delete All
Select View
Settings
WaveForm
Filter:
(on 8_bit_CSL_timing.tr0)
D0:8_bit_CSL_timing.tr0
D0:8_bit_CSL_timing.tr0
derived waveforms
All
waveview 1
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
10.6n
10.8n
11n
11.2n
11.4n
11.6n
11.8n
12n
0%

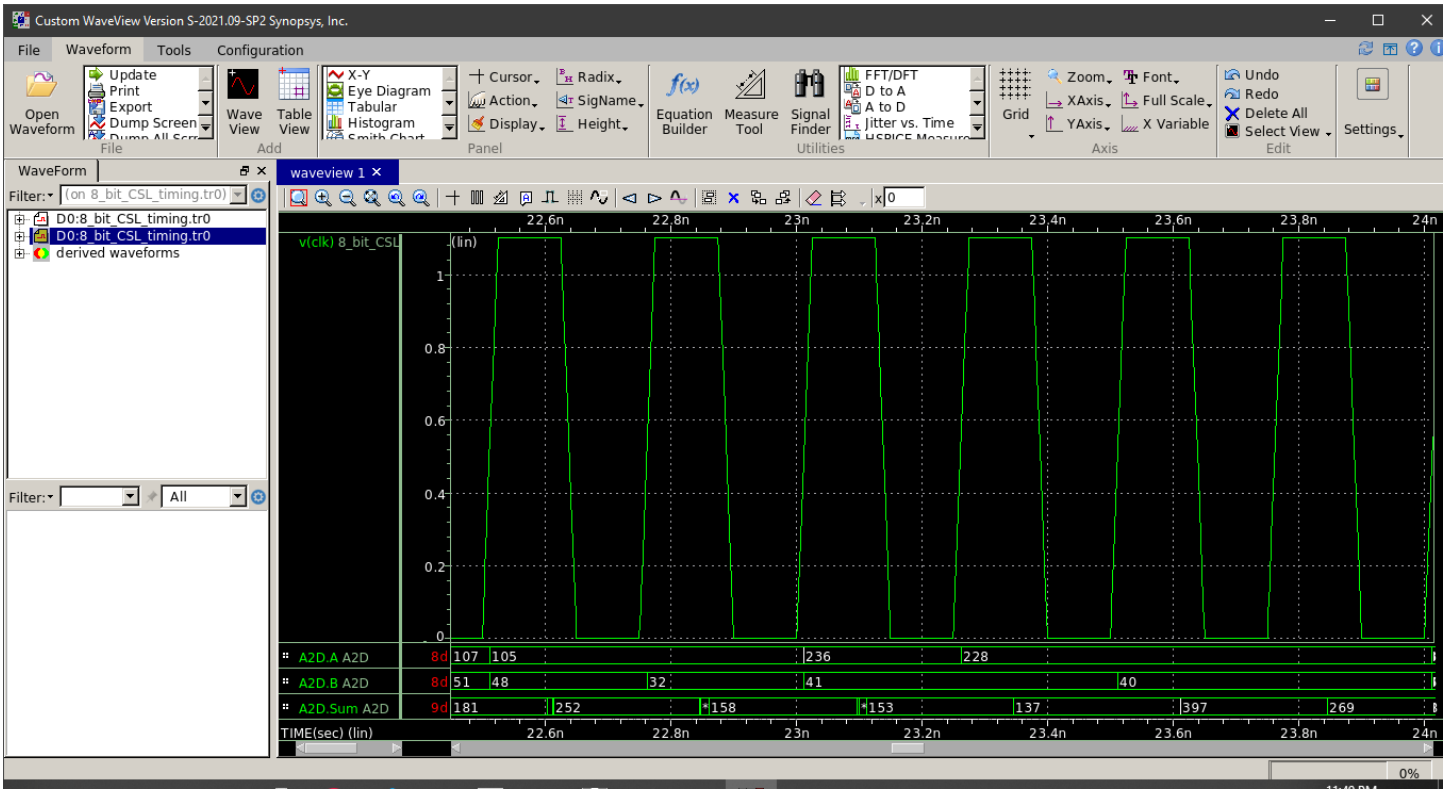
16ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Jitter vs. Time
Grid
Zoom
XAxis
YAxis
Font
Full Scale
X Variable
Undo
Redo
Delete All
Select View
Settings
WaveForm
Filter:
(on 8_bit_CSL_timing.tr0)
D0:8_bit_CSL_timing.tr0
D0:8_bit_CSL_timing.tr0
derived waveforms
All
waveview 1
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
15.6n
15.8n
16n
16.2n
16.4n
16.6n
16.8n
17n
0%

19ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
Tools
Configuration
Open Waveform
Update
Print
Export
Dump Screen
Wave View
Table View
X-Y
Eye Diagram
Tabular
Histogram
Cursor
Action
Display
Radix
SigName
Height
Equation Builder
Measure Tool
Signal Finder
FFT/DFT
D to A
A to D
Jitter vs. Time
Grid
Zoom
XAxis
YAxis
Font
Full Scale
X Variable
Undo
Redo
Delete All
Select View
Settings
WaveForm
waveview 1
D0:8_bit_CSL_timing.tr0
derived waveforms
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)

23ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
Tools
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Open Waveform
Update
Print
Export
Dump Screen
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X Variable
Undo
Redo
Delete All
Select View
Settings
WaveForm
waveview 1
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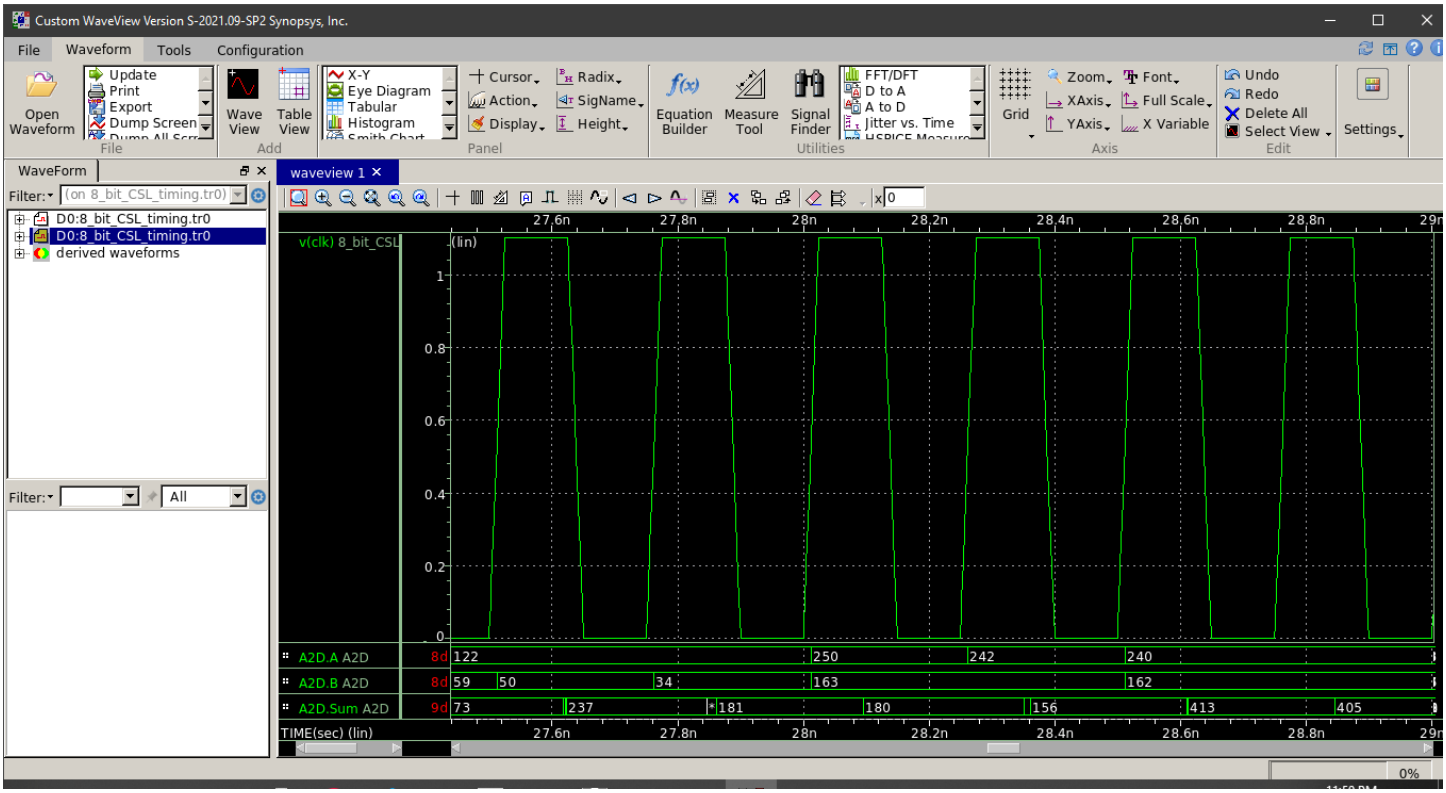
derived waveforms
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)

28ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
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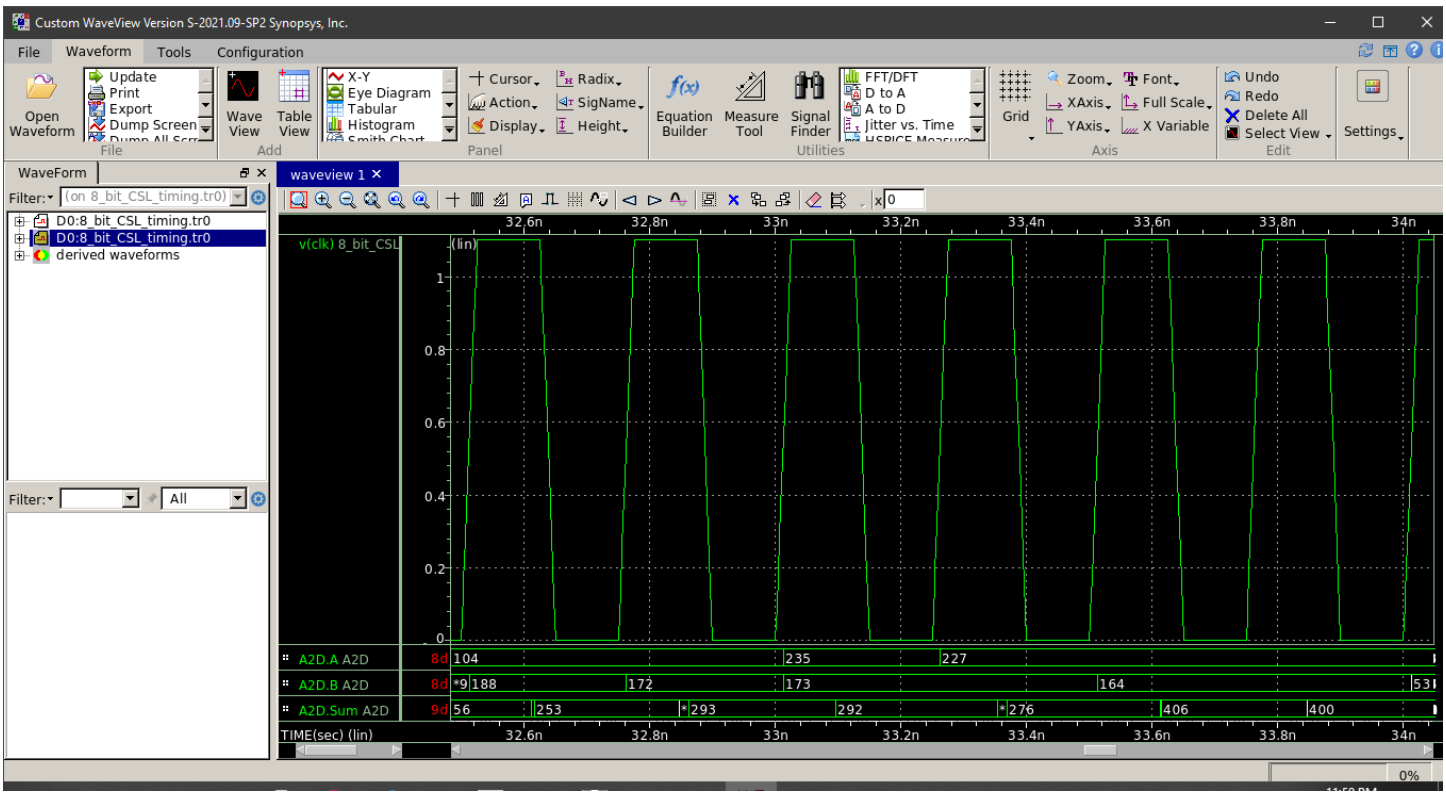
D0:8_bit_CSL_timing.tr0
derived waveforms
All
waveview 1
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
27.6n
27.8n
28n
28.2n
28.4n
28.6n
28.8n
122
250
242
240
59
50
34
163
162
73
237
181
180
156
413
405

33ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
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Dump Screen
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Jitter vs. Time
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XAxis
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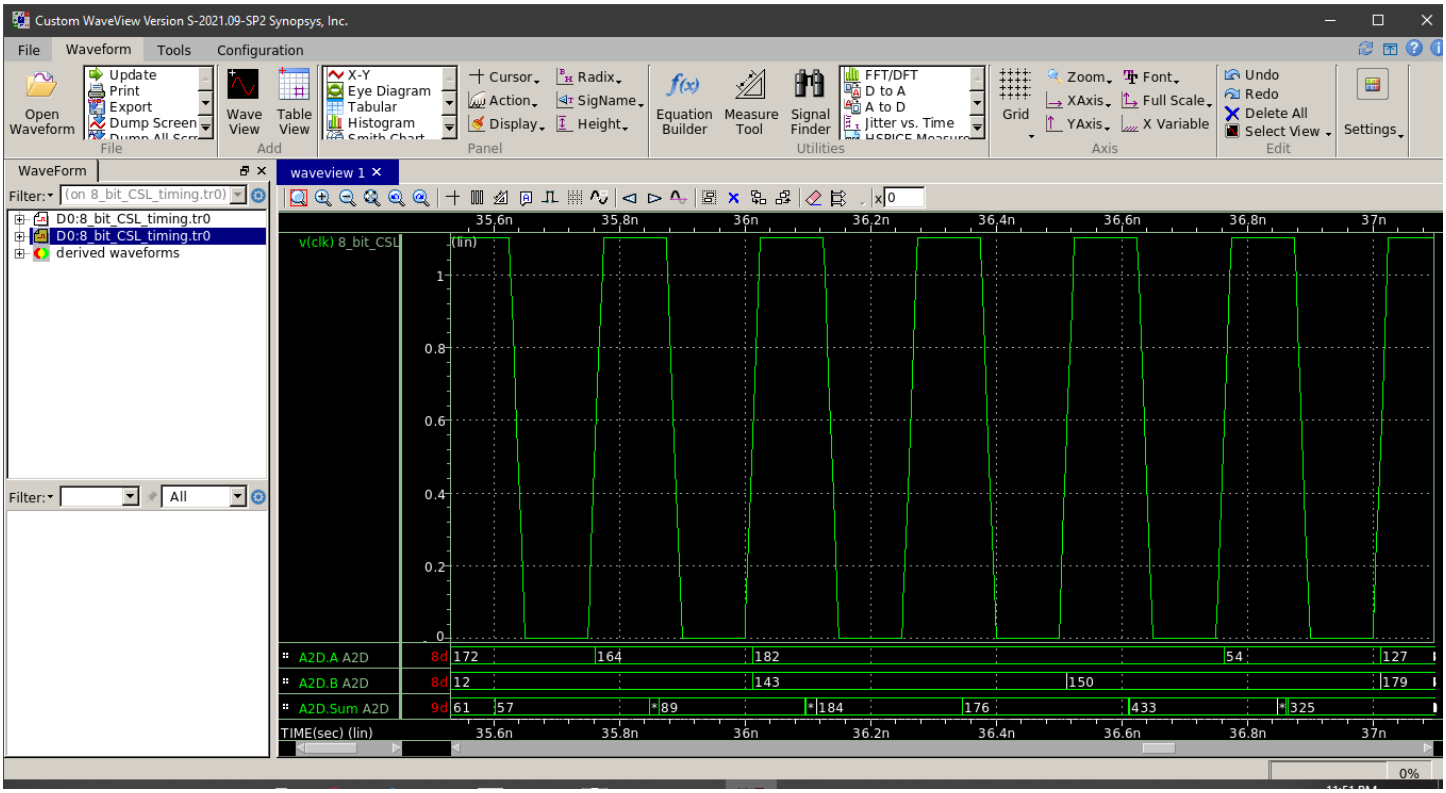
D0:8_bit_CSL_timing.tr0
D0:8_bit_CSL_timing.tr0
derived waveforms
All
waveview 1
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
32.6n
32.8n
33n
33.2n
33.4n
33.6n
33.8n
34n
104
235
227
188
172
173
164
56
253
293
292
276
406
400

36ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
Waveform
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Grid
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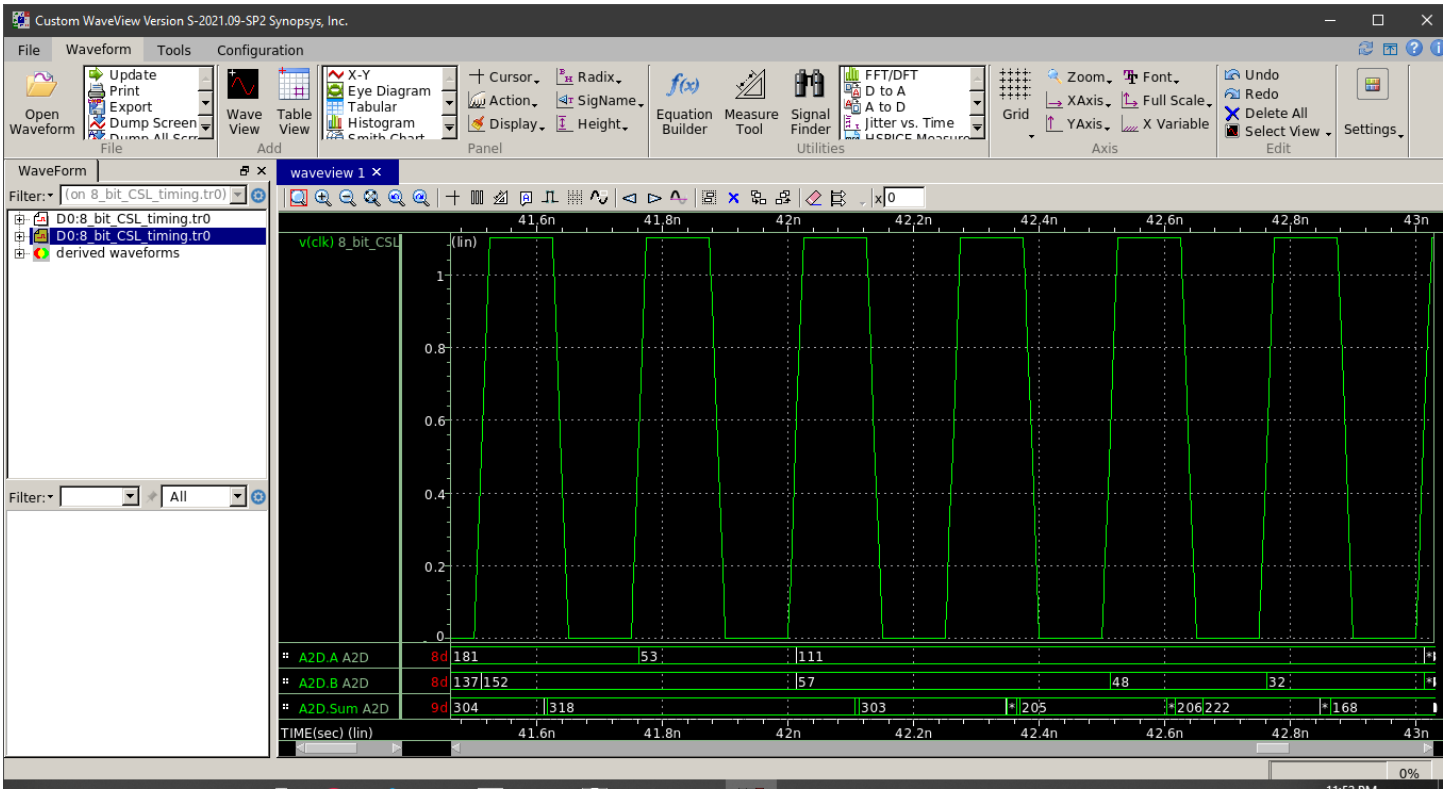
Font
Full Scale
X Variable
Undo
Redo
Delete All
Select View
Settings
WaveForm
waveview 1
Filter:
(on 8_bit_CSL_timing.tr0)
D0:8_bit_CSL_timing.tr0
D0:8_bit_CSL_timing.tr0
derived waveforms
All
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
35.6n
35.8n
36n
36.2n
36.4n
36.6n
36.8n
37n
0%

42ns


Custom WaveView Version S-2021.09-SP2 Synopsys, Inc.
File
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Font
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X Variable
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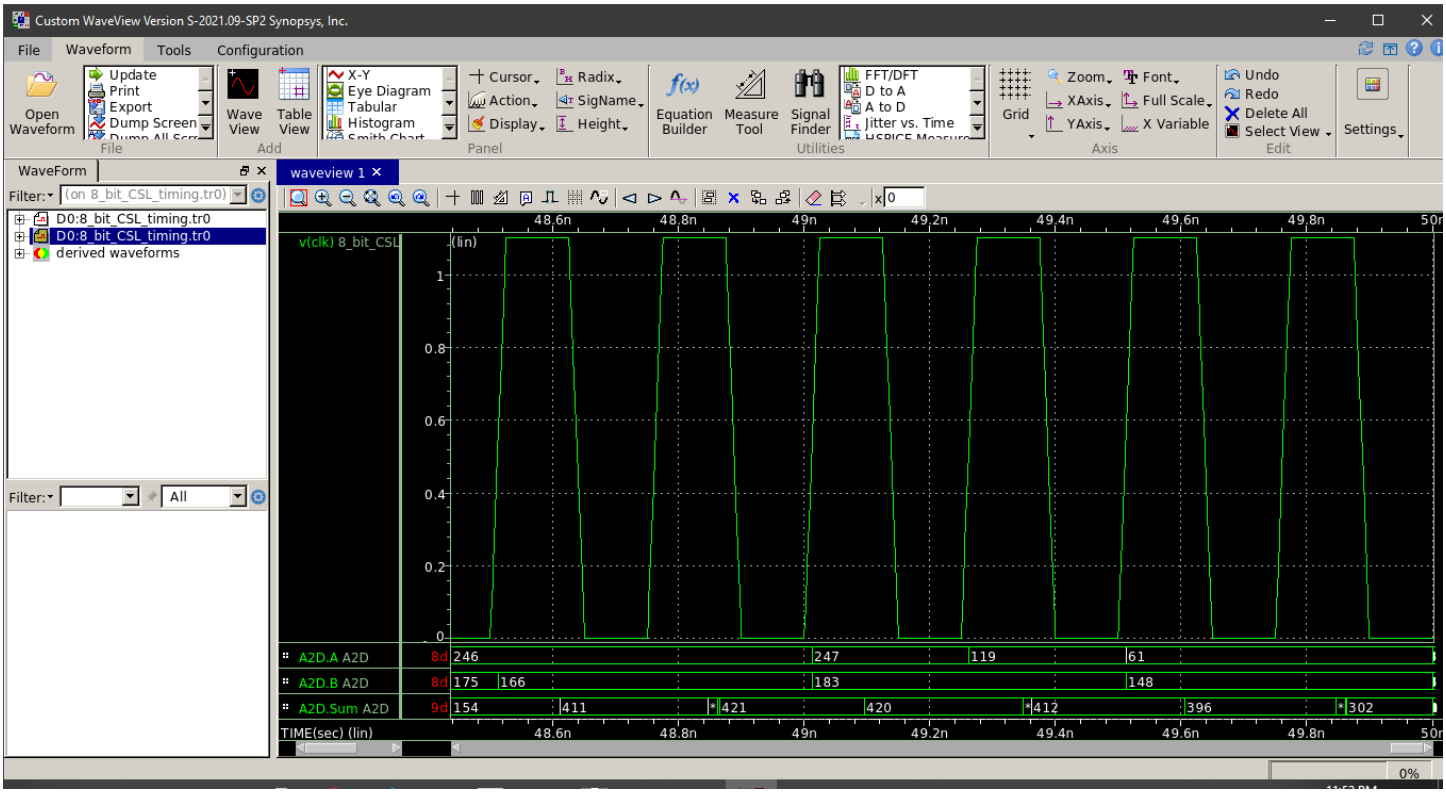
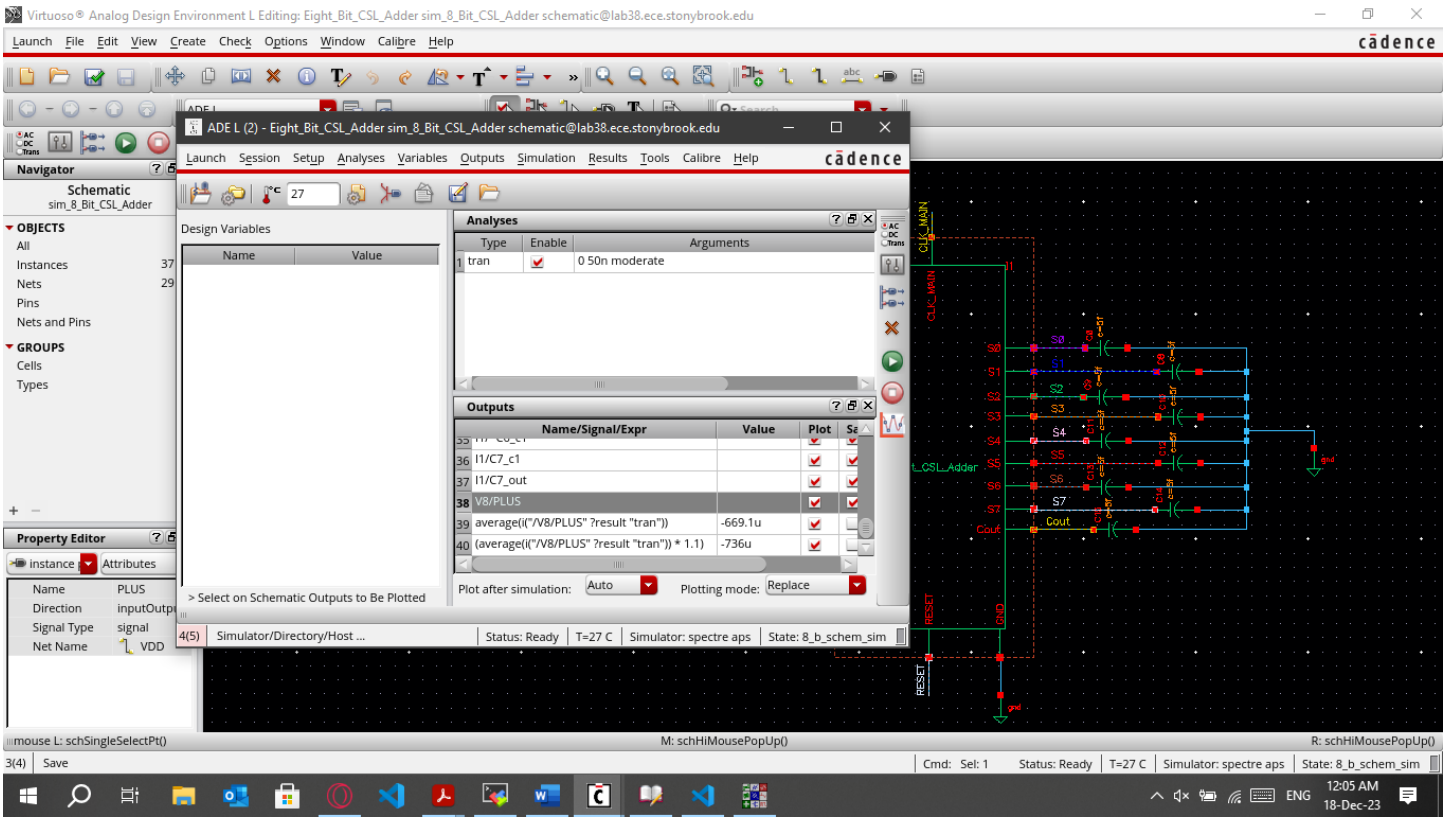
(on 8_bit_CSL_timing.tr0)
D0:8_bit_CSL_timing.tr0
D0:8_bit_CSL_timing.tr0
derived waveforms
All
v(clk) 8_bit_CSL
(lin)
A2D.A A2D
A2D.B A2D
A2D.Sum A2D
TIME(sec) (lin)
41.6n
41.8n
42n
42.2n
42.4n
42.6n
42.8n
43n
0%

49ns

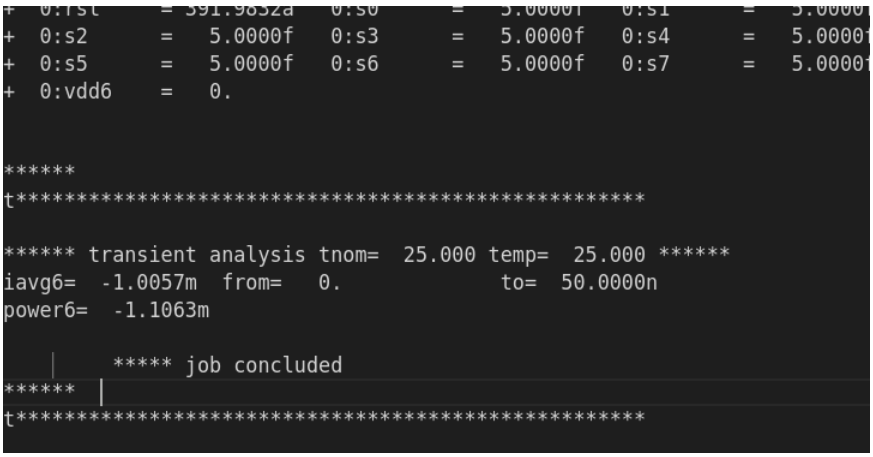


Average Power

Schematics Average power consumption of 736 µW



Post-layout average power consumption of 1.106 mW



Discussion

- While performing layout, I encountered a new DRC error called Check.Anntenna.Metal10. The apparently means that the ratio of total metal and via areas to the ratio of gate is more than 300:1 which would cause plasma induces gate oxide damage. That is, while fabricating higher metal layers, a specific step involves the induction of high energy plasma. And after the fabrication the plasma ions try to discharge through these etched gates. When the gate is is less, these huge volume of plasma ions discharge through it eroding the gate oxide and permanently damaging the transistor. I fixed it by removing direct connection from vias to gates and distancing the connection between gate's polys and metal layers.
- Designing this project gave me an understanding of how industry grade VLSI front end and back end would be carried out.
- I learnt new power/ground routing techniques, especially grid structure.

Conclusion

In conclusion, an 8-bit CSL adder was designed in schematics and layout and was verified to mee frequency and power constraints. The schematics design gave a maximum frequency of operation of 5.8GHz which is a good over-designing so that the final layout and post-fabrication circuit can tolerate a reduction in few MHz due to net capacitances and process variations. The final layout successfully ran at 4GHz consuming power of 1.106 mW.

Possible improvements:

- The first block could have been made into a standard ripple carry adder to reduce power consumption because the adder with Cin as '1' is just wastefully computing results. It also adds unnecessary muxes.