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A Project Report on

8:1 MULTIPLEXER USING LOGIC GATES & DYNAMIC CMOS LOGIC

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AIM:

Designing and implementation 8:1 mux using logic gates and dynamic cmos logic using cadence virtuoso.

Abstraction :

An 8:1 multiplexer is a digital circuit that selects one of eight input signals and forwards it to a single output line. The selection of the input signal to be transmitted is controlled by a set of three binary control inputs (often labeled A, B, and C). These control inputs determine which input signal is passed through to the output.

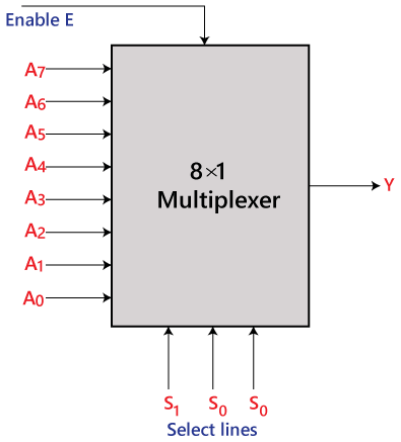
The 8:1 multiplexer has eight input lines and one output line. When a particular combination of the three control inputs is applied to the multiplexer, the corresponding input signal is transmitted to the output line. For example, if the control inputs are set to "000", the input signal on the first input line will be transmitted to the output line. If the control inputs are set to "001", the input signal on the second input line will be transmitted to the output line, and so on.

The 8:1 multiplexer is a basic building block in digital circuit design and is commonly used in a wide range of applications, including data transmission, memory addressing, and signal routing.

IMPLEMENTATION: 8 to 1 Multiplexer

In the 8 to 1 multiplexer, there are total eight inputs, i.e., A0, A1, A2, A3, A4, A5, A6, and A7, 3 selection lines, i.e., S0, S1and S2 and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines S0, S1, and S2, one of these 8 inputs are connected to the output. The block diagram and the truth table of the 8×1 multiplexer are given below.

Block Diagram:



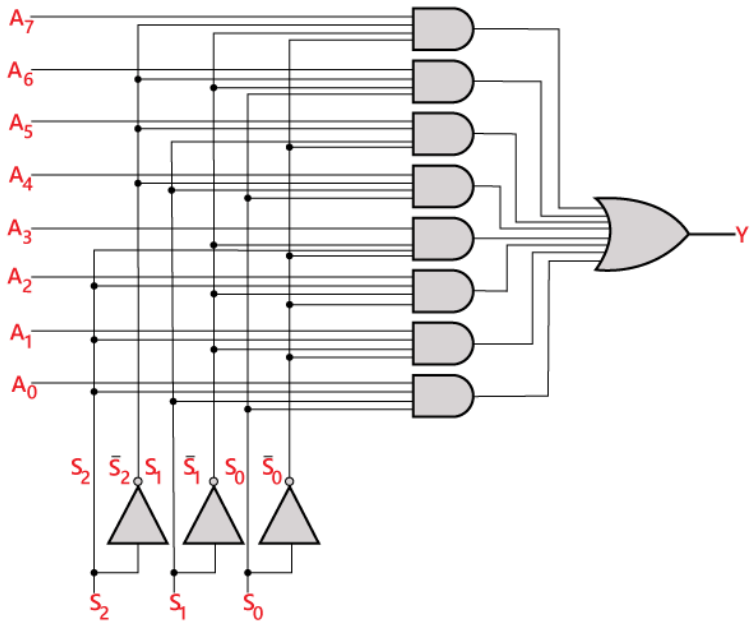
Truth Table:

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

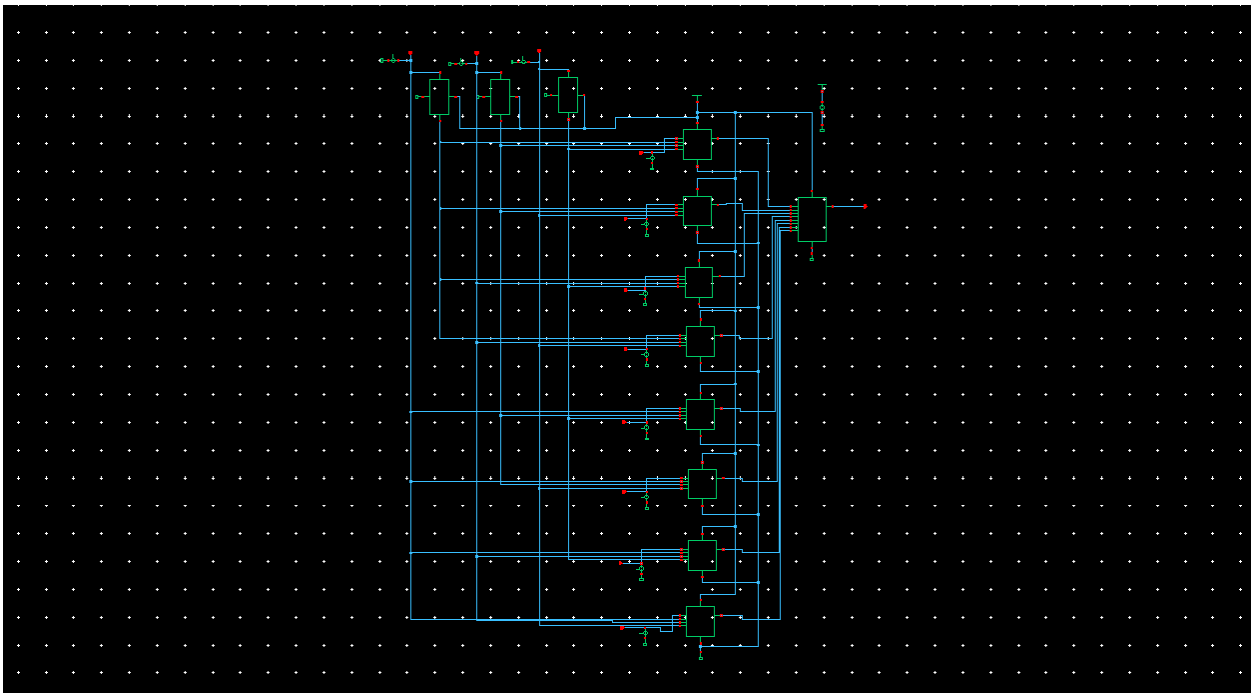
The logical expression of the term Y is as follows:

Y=S0'.S1'.S2'.A0+S0.S1'.S2'.A1+S0'.S1.S2'.A2+S0.S1.S2'.A3+S0'.S1'.S2 A4+S0.S1'.S2 A5+S0'.S1.S2 .A6+S0.S1.S3.A7

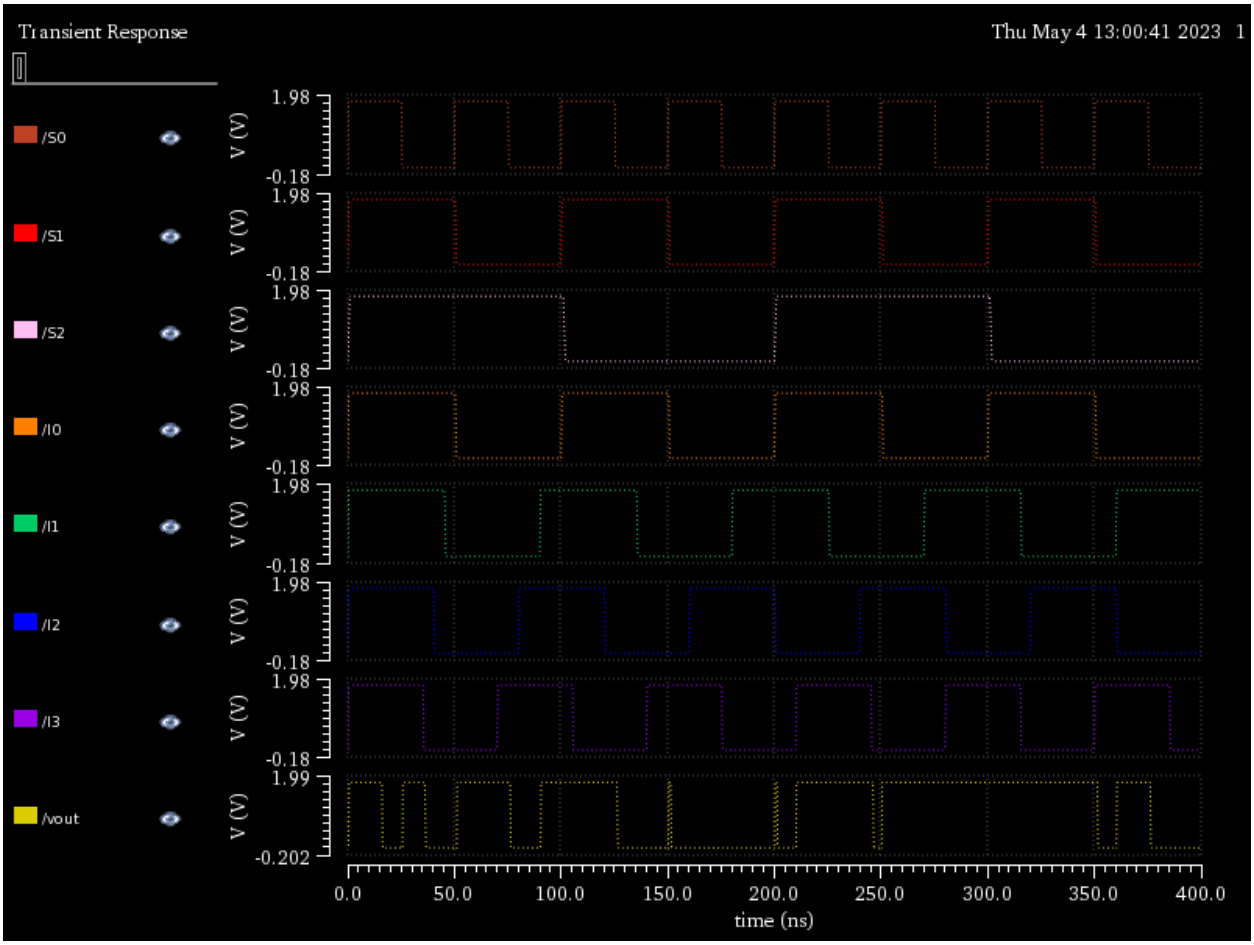
Logical circuit of the above expression is given below:



CIRCUITE DIAGRAM : 8:1 mux using logic gates.



TIMING DIAGRAM:



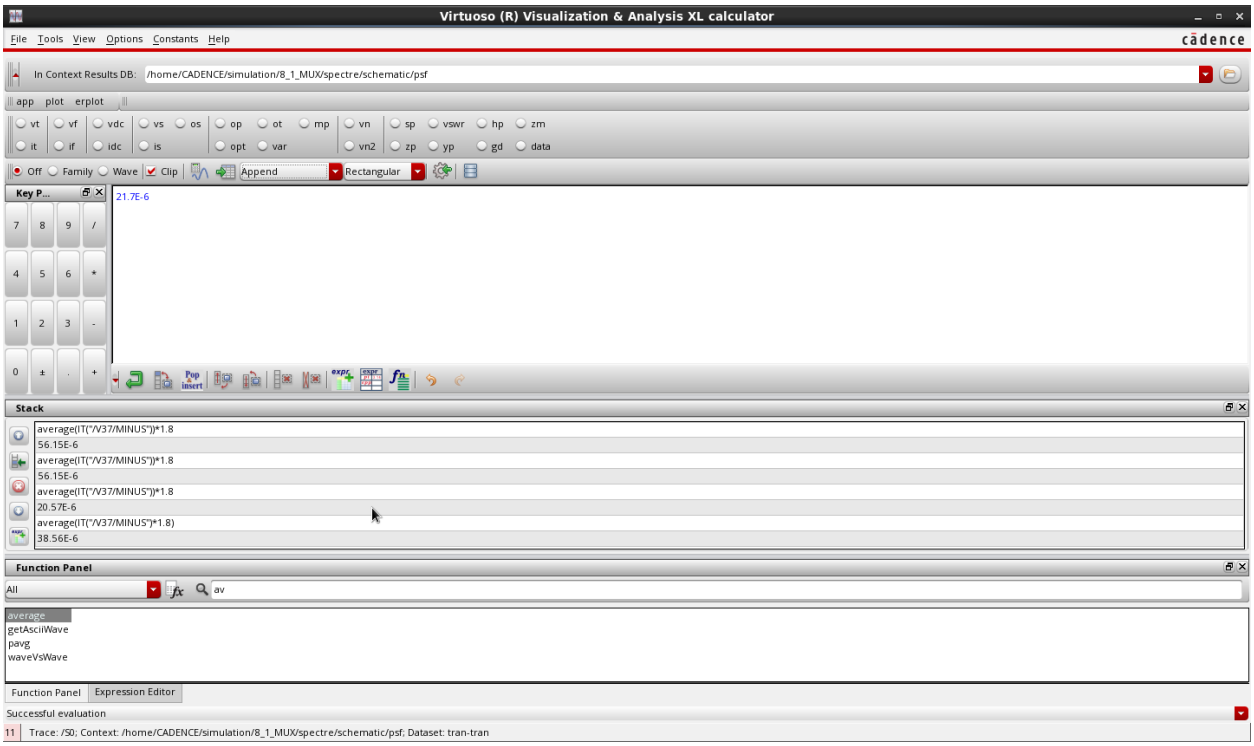
Whenever the test cases are :

S0	S1	S2	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

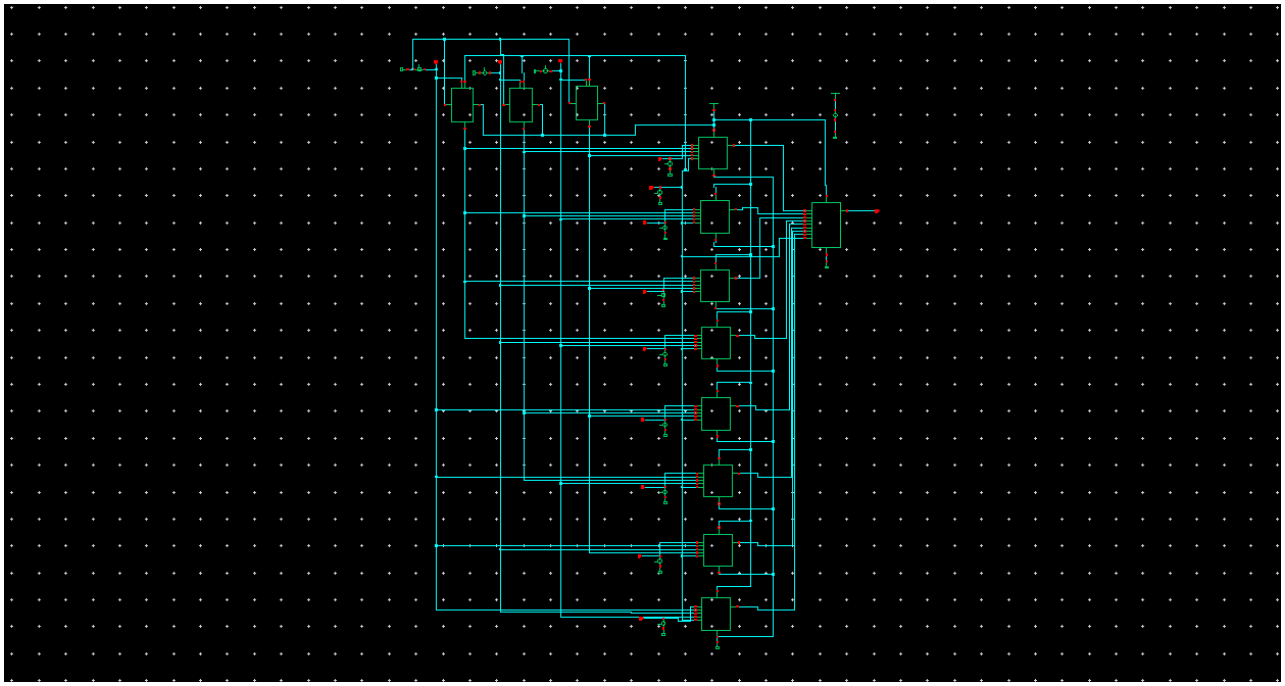
Input power :

Input power = voltage * current

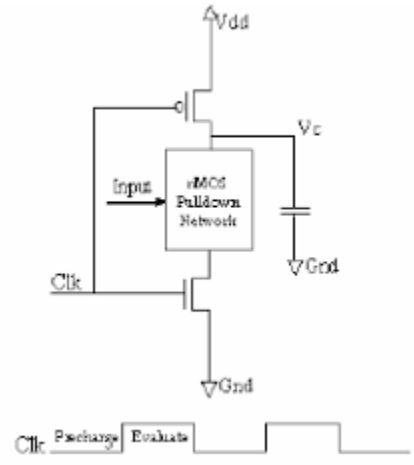
= 21.7E-6 W



IMPLEMENTATION OF 8:1 MUX USING DYNAMIC COMOS LOGIC:



DYNAMIC CMOS(PULL DOWN) logic:



dynamic logic is less low-power consuming and have high speed than static logic. In particular, dynamic CMOS gates are supposed to be more

advantageous than static ones mainly because of a total absence of output glitching and a reduced parasitic capacitance.

Observation :

Compare to static cmos logic dynamic cmos logic is better in terms of Area and power and also delay.

Number of transistors in static cmos logic : 2ip-not_gate =3*2=6

4ip_AND_gate=8*8=64

8in_OR_gate= 16*1=16

Total = 86 transistors

Number of transistors in dynamic cmos logic : 2ip-not_gate =3*3=6

4ip_AND_gate=8*6=48

8in_OR_gate= 16*1=10

Total = 64 transistors