

1 Introduction

1.1 Referenced documents

- [1] J. E. Volder, "The CORDIC Trigonometric Computing Technique," in *IRE Transactions on Electronic Computers*, vol. EC-8, no. 3, pp. 330-334, Sept. 1959, doi: 0.1109/TEC.1959.5222693.
- [2] E. O. Garcia, R. Cumplido and M. Arias, "Pipelined CORDIC Design on FPGA for a Digital Sine and Cosine Waves Generator," *2006 3rd International Conference on Electrical and Electronics Engineering, Veracruz, Mexico, 2006*, pp. 1-4, doi: 10.1109/ICEEE.2006.251917.
- [3] Sharat, Kavya, B. V. Uma, and D. M. Sagar. "Calculation of Sine and Cosine of an Angle using the CORDIC Algorithm." *International Journal of Innovative Technology and Research (IJITR)*.– February–March (2014): 891-895.
- [4] Kim, Young-Man. "Error Analysis of CORDIC Processor with FPGA Implementation." *arXiv preprint arXiv:2308.01025* (2023).

1.2 Design library name

Path: /afs/iitd.ac.in/user/j/jv/jvl232241/umc65/PD_flow/Cordic

1.3 People involved in the block

Mudit Bajaj	JVL232239
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Madhur Aswani	JVL232241
Hasti Kasundra	JVY237559

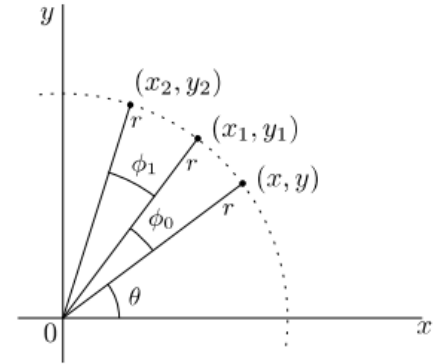
2 Function

2.1 Brief overview

- **CORDIC: COordinate Rotation DIgital Computer.**
- It is an iterative algorithm used for various trigonometric and other mathematical computations, particularly for calculating sine, cosine, and vector rotation.
- It operates by performing a series of rotations to gradually transform an initial value to the desired result.
- All iterations are performed in parallel, using a pipelined structure. This generally produces 1 additional bit of accuracy for each iteration.
- It is a hardware efficient algorithm as it uses only shift-add arithmetic.
- It contains the arctan table (LUT) for each iteration and the logic needed to manipulate the x, y and z values.

Basic Principle:

- Rotate (1,0) by Φ degrees to get (x,y): $x = \cos\Phi$ and $y = \sin\Phi$.
- Rotation of any (x,y) vector:
$$x' = x.\cos\Phi - y.\sin\Phi$$
$$y' = y.\cos\Phi + x.\sin\Phi$$
- Rearranging, we get:
$$x' = \cos\Phi.[x - y.\tan\Phi]$$
$$y' = \cos\Phi.[y + x.\tan\Phi]$$
- Can compute rotation of Φ in steps where each step size is of:
$$\tan\Phi = \pm 2^{-i}$$
- Gain: $K = \pi.\cos\Phi$ depends on rotation angle $\Phi_1, \Phi_2, \Phi_3, \dots, \Phi_n$.
- Since same angles are rotated always, K is a constant which is pre-computed ($K = 1.64676$)



Iterative Rotations:

$$x_{i+1} = K_i (x_i - (y_i d_i 2^{-i}))$$

$$y_{i+1} = K_i (y_i + (x_i d_i 2^{-i}))$$

where, d_i : decision (rotation mode)

z_i is introduced to keep track of angle that has been rotated ($z_0 = \Phi$)

$$z_{i+1} = z_i - d_i \tan^{-1}(2^{-i})$$

$$d_i = -1 \text{ if } z_i < 0$$

$$1 \text{ otherwise}$$

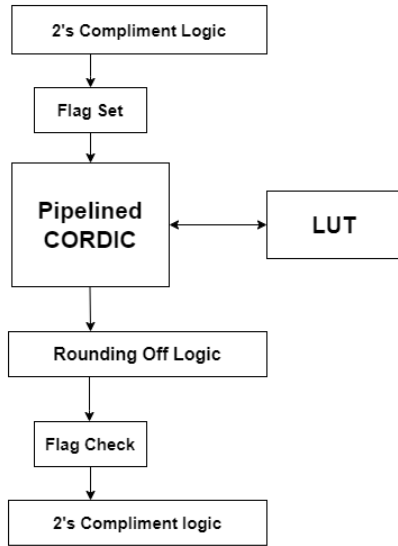
The purpose of this design is to do a RTL to GDS flow for a 8-bit dedicated processor for calculating sine and cosine of an angle using the CORDIC algorithm. The specifications are mentioned below:

Specifications	
Maximum Frequency	100MHz
Input	8-bit Angle input (in radians)
Output	8-bit Sine & Cosine
Error (%)	1%
Technology	umc65

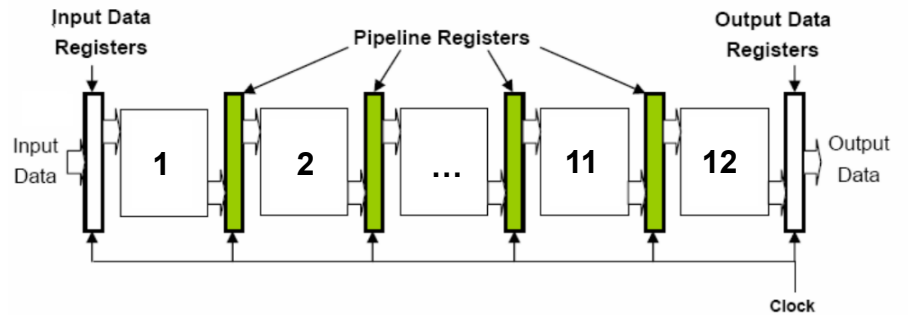
2.2 Interfaces

Signal name	I/O	Description	Logical grouping
clk	input	Clock input	-
rst	input	Reset input	-
[7:0] in	input	Signed 8-bit Angle in Radians	-
[7:0] sine	output	Signed 8-bit Sine of the given angle	-
[7:0] cosine	output	Signed 8-bit Cosine of the given angle	-

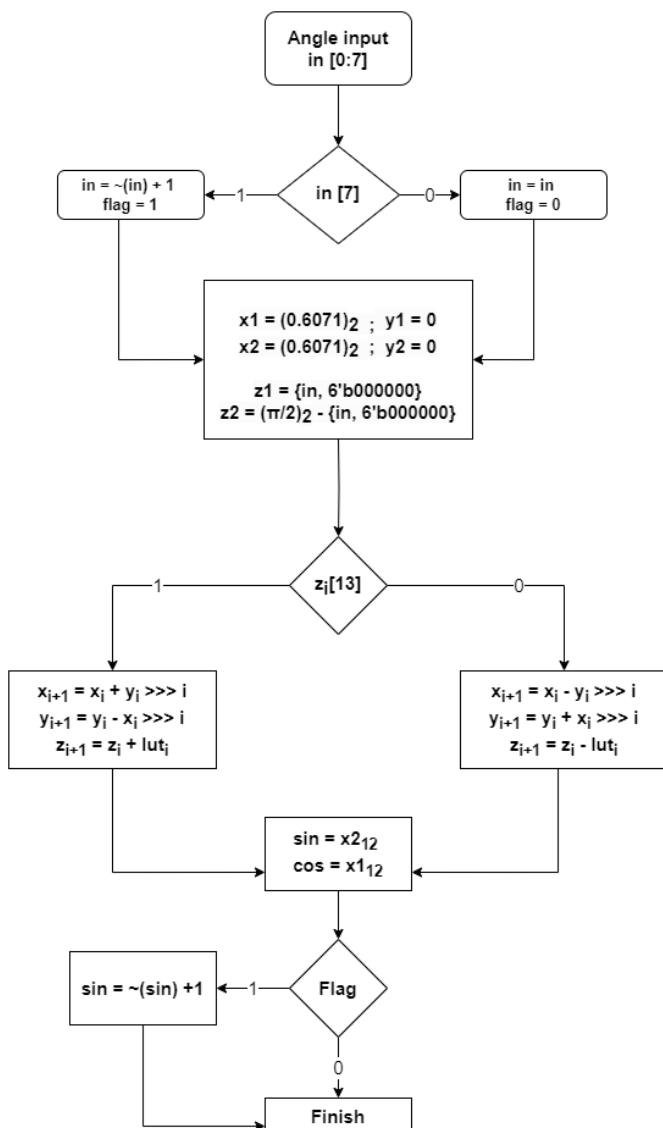
2.3 Architecture



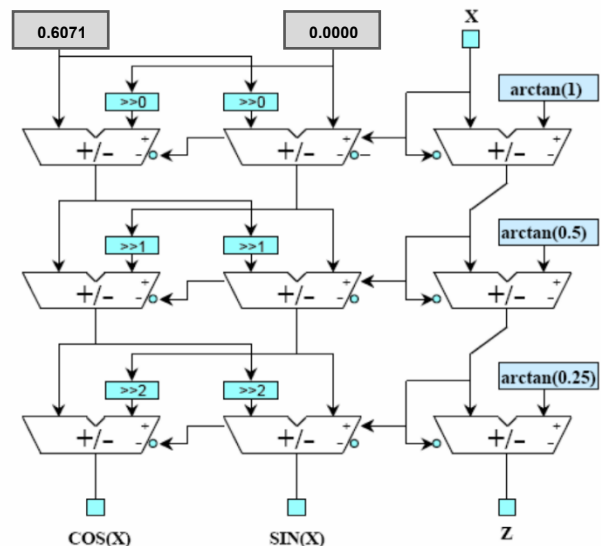
Pipelined CORDIC



2.4 Detailed functional description



- Input signal: 8-bit angle in the range: $-\pi/2$ to $+\pi/2$ radians.
- First bit of angle input is the sign bit. If sign bit = 1, i.e. if the angle is in 4th quadrant ($-\pi/2$ to 0), we take 2's complement.
- Input vectors x & y and phase angle z are initialized.
- Performs iterations for 12 pipelined stages where in each iteration, the algorithm aims to rotate the vector (x,y) towards the positive x-axis and the current angle is either added or subtracted from the phase angle z.
- Here, we consider Φ to compute cosine and $(\pi/2 - \Phi)$ to compute sine of the given angle Φ , in order to achieve higher accuracy.
- The rotation angles are precomputed and stored in a lookup table (LUT) which contains arctan values of
- As the iterations progress, the vector (x,y) converges towards a point that corresponds to the given phase angle z.
- The final stage input vectors represent the cosine and sine components of the input angle.
- The computed 14-bit sine and cosine are rounded off to 8 bits to get the final output.



3 Design parameters

3.1 Performance Requirements

- 8-bit dedicated Cordic processor
- Maximum Frequency: 100MHz
- Output: 8-bit Sine and Cosine for the given angle in radians
- Error(%) = 1%

3.2 Clock Distribution

- Clock period: 10ns
- Rise & Fall time: 0.1ns (1% of clock period)
- Source Latency: 0.1ns
- Clock uncertainty: 0.1ns
- Max Capacitance: 4pF
- Max Fanout: 150

3.3 Reset

- Reset is asynchronous and active low.

3.4 Timing Description

- Clock period = 10ns
- Pipeline stages = 12
- Latency = 15 clock cycles
- Post genus synthesis, maximum slack of 7.511ns is observed.
- The preCTS timing and postCTS timing is reported.

4 Verification Strategy

4.1 Objectives

- The objective is to validate the Verilog sine and cosine outputs corresponding to a specified angle in radians. This involves comparing the Verilog results with the true sine and cosine values and computing the percentage error.

4.2 Tools and Version

- Verilog (Modelsim- Intel FPGA Edition vsim 2020.1)
- Cadence Genus & Innovus

4.3 Checking mechanisms

- **Self-checking mechanism:** A testbench is developed in verilog that instantiates the CORDIC module and feeds it various input angles. This verilog generated output is subsequently compared with the actual sine and cosine values, and the error percentage is computed.

5 Functional Checklist

The basic functionality of this design is to compute sine & cosine values for the given angle input. To check this, we need to verify the following:

- If the module correctly handles positive & negative input angles in the range $-\pi/2$ to $+\pi/2$.
- LUT is correctly implemented is appropriately sized to balance accuracy and resource utilization.
- Proper scaling and rounding that is applied to convert internal representations to the final output format of 8-bits.
- The algorithm meets the required performance requirements.
- Verify the final verilog sine and cosine output and compare with the true values to find the error %.

5 Testbench

5.1 Overview

- 2 testbenches are designed to test the functionality of CORDIC algorithm which monitors the sine and cosine outputs of the CORDIC module
 - The initial testbench focuses on functional verification of the CORDIC algorithm at critical angles such as 0 , $\pm\pi/4$, $\pm\pi/2$, aiming to quantify the error percentage at these critical points. This testbench also verifies the congruence of input and output frequencies by observing the output of the pipelined stage at each cycle with a latency of 15 clock cycles.
 - A separate testbench has been designed to analyze the error percentage across the complete range of angles, spanning from $-\pi/2$ to $+\pi/2$.

5.2 Architecture

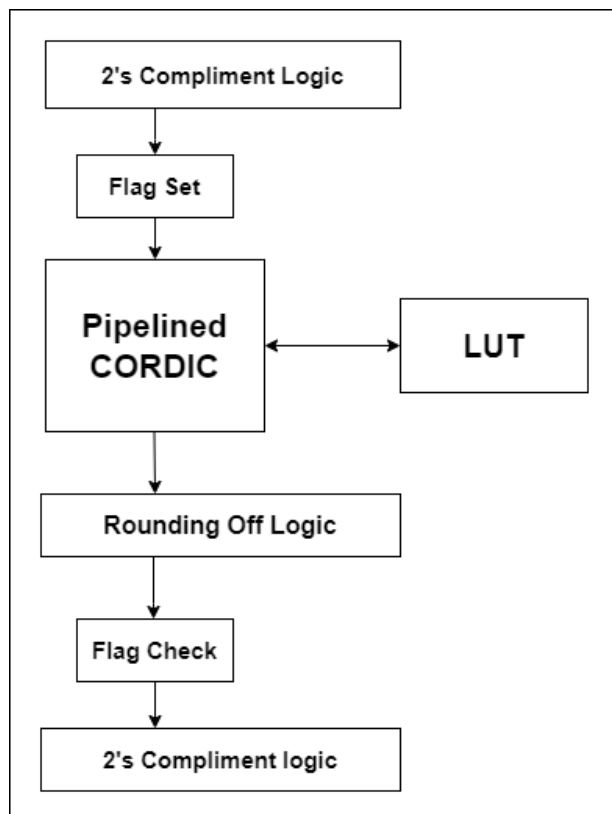
- Clock and other signals are initialized. Time period is set to 10ns.
- Sizing factor for input angle and for generating true sine & cosine values of that angle is $sf = 2^{-6}$.
- Sizing factor for output is $o_sf = 2^{-7}$.
- Information regarding cycle information, cosine, sine, input angle, and actual sine and cosine values is displayed.

6 Tests Specification

- Angle input: Testbenches are designed to check the CORDIC functionality at critical angles including 0 , $\pm\pi/4$, and $\pm\pi/2$ and the entire spectrum of input angles ranging from $-\pi/2$ to $+\pi/2$.
- Input clock with period of 10ns and rise & fall time of 0.1ns (1% of Clock period) provided.
- The test cases and corresponding output results have been reported in section: 10.3.

7 Design Microarchitecture

7.1 Top Level Interface



7.2 Sub-Block Description

- **2's Complement Logic:** When the sign bit is set to 1, we invert the input and pass the resulting value to BEC-1 (Binary Excess Code-1) logic. This approach allows the synthesizer to generate more efficient logic for incrementing the least significant bit (LSB) by 1 compared to employing a ripple carry adder. Conversely, when the sign bit is 0, the input value remains unaltered and is directly passed to the output.
- **Flag Set:** When the sign-bit is 1, we set the flag=1 to indicate that the angle is negative ($-\pi/2$ to 0). The flag is set to 0 in other case.
- **Pipelined CORDIC:** The CORDIC computation is divided into 12 pipelined stages, where the output of one stage feeds directly into the next stage. The input angle is fed into the pipeline. Initial values for x, y, and z are set. Each stage rotates the vector (x,y) by a precomputed angle. The rotation angle is determined based on the iteration and is part of a lookup table. The rotated values are passed to the next stage. Registers are introduced between stages to store intermediate results. The rotated angle is accumulated in z. The final values of input vectors represent the cosine and sine of the original input angle, respectively
- **LUT:** It is used to store pre-computed values of rotation angles which is looked-up and used for performing shift and add operation of Cordic algorithm. The LUT of this design stores 14-bit values for $\tan^{-1}(1)$, $\tan^{-1}(1/2)$,... upto $\tan^{-1}(1/2048)$. These binary values have been computed using python.
- **Rounding Off Logic:** Our 8-bit output comprises of 1 sign bit and 7 fractional bits. When approaching values close to 1, introducing an additional one, as done during rounding up, becomes impractical as it will change the sign of the output. The rounding process selectively applies only to values that retain their signs post-rounding. Here, the 13th bit of our 12-bit x register is used as a case to check whether to round of the output or not.
- **Flag Check:** This stage verifies whether the flag was set to 1 or 0. If the flag was set to 1, it indicates that the input angle falls within the range of $-\pi/2$ to 0. Consequently, sine values for this angle are negative. Therefore, in this scenario, the 2's complement of the sine is computed.

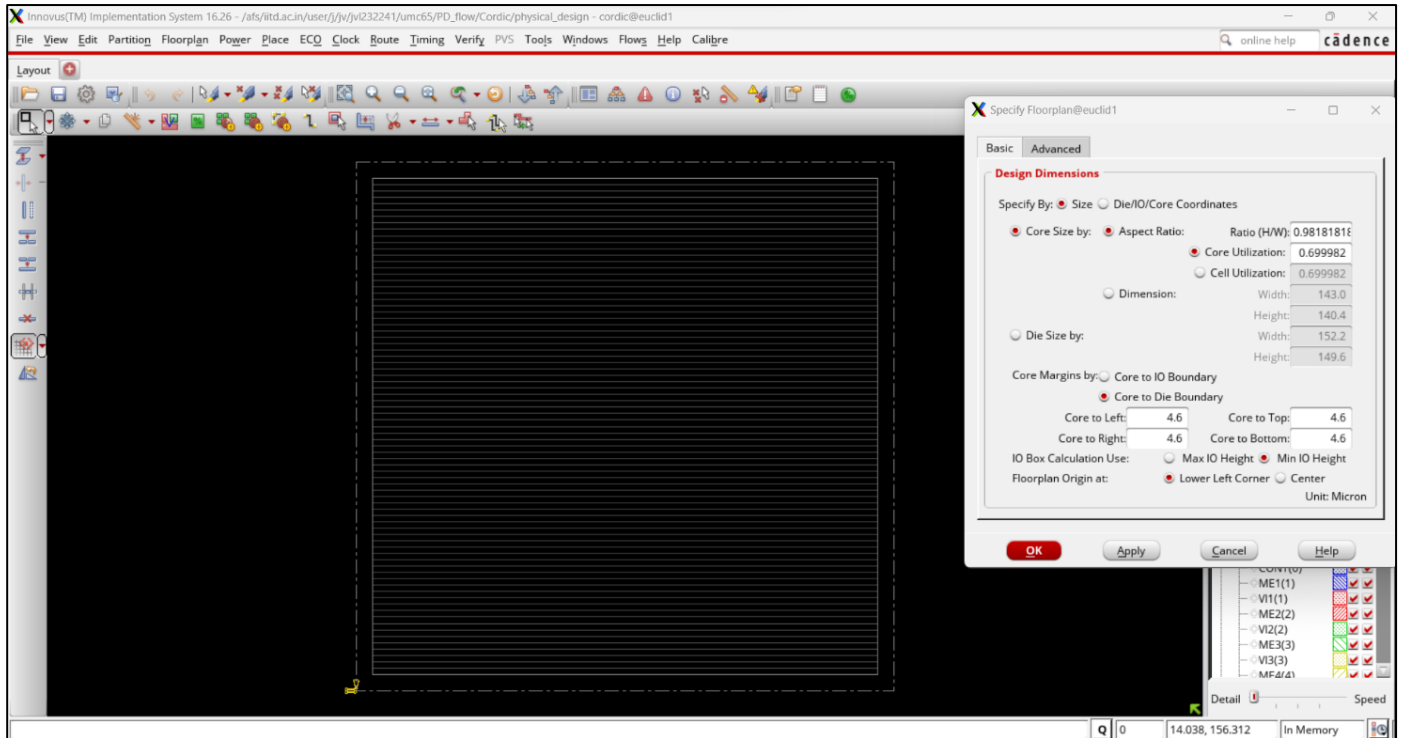
7.3 Structural Mapping Process

Cadence Genus is primarily used for synthesis, while Innovus is employed for place and route along with other physical design steps. This flow ensures a comprehensive transformation from high-level RTL description to a layout ready for manufacturing, addressing considerations such as timing, power, and physical design rules. Following steps are involved in Structural Mapping Process:

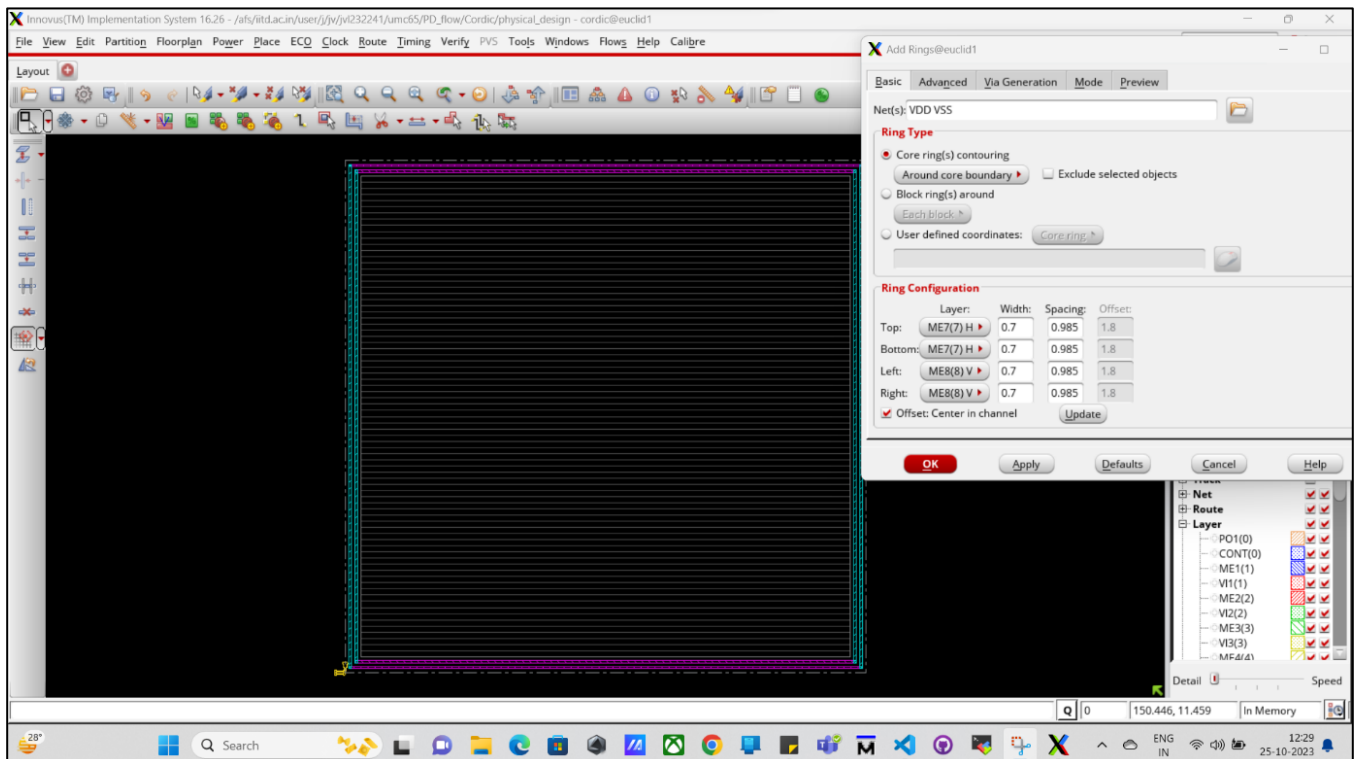
- RTL Synthesis (Genus): Translating the RTL code (Verilog) into a gate-level netlist
- Floorplanning (Innovus)
- Place and Route (Innovus)
- Clock Tree Synthesis (Innovus)
- Static Timing Analysis (Innovus)
- Physical Verification (Innovus)

8 Physical hierarchy

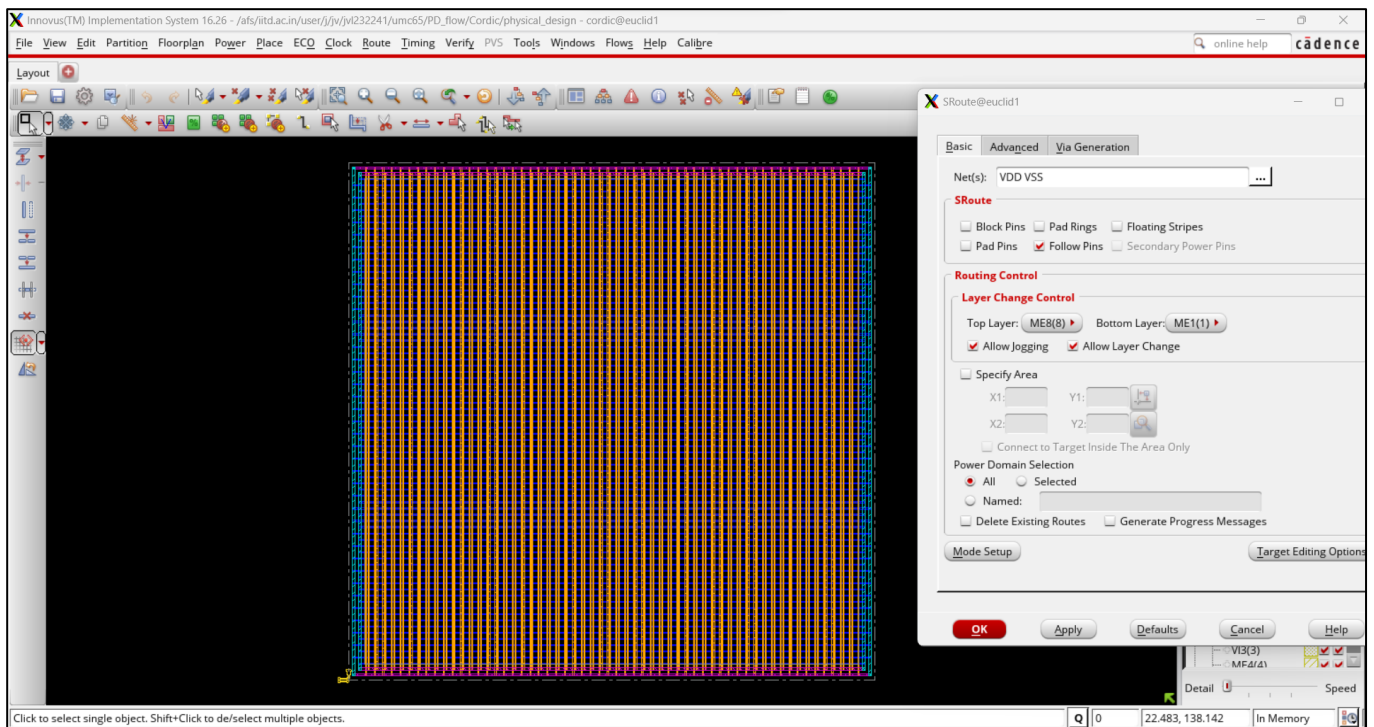
8.1 Floorplanning



Initial Floor Plan



Power Rings Added



Power Planning

8.2 Clock-tree insertion

```
set sdc_version 1.7

set_units -capacitance 1000.0fF
set_units -time 1ns

# Set the current design
current_design cordic

create_clock -name "clk" -add -period 10 -waveform {0 5} [get_ports "clk"]

set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_latency -source 0.1 [get_clocks "clk"]

set_max_capacitance 4 [all_inputs]

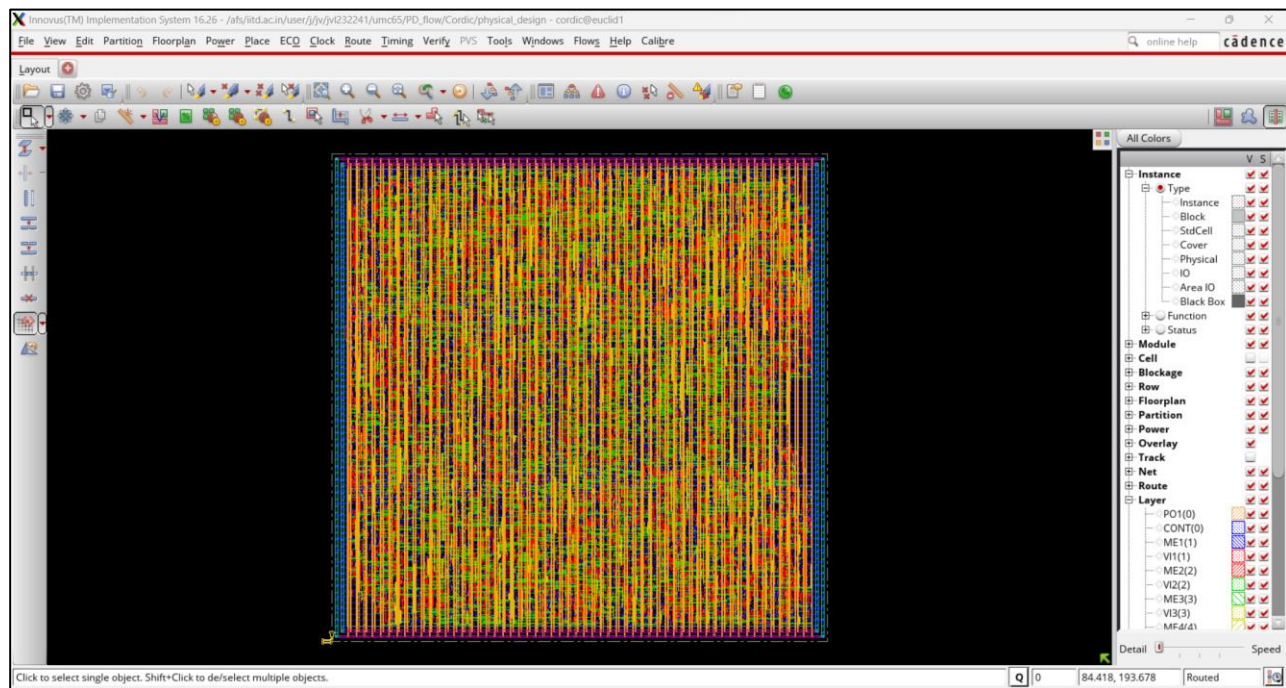
set_max_fanout 150 [all_inputs]

set_clock_uncertainty 0.1 [get_clocks "clk"]

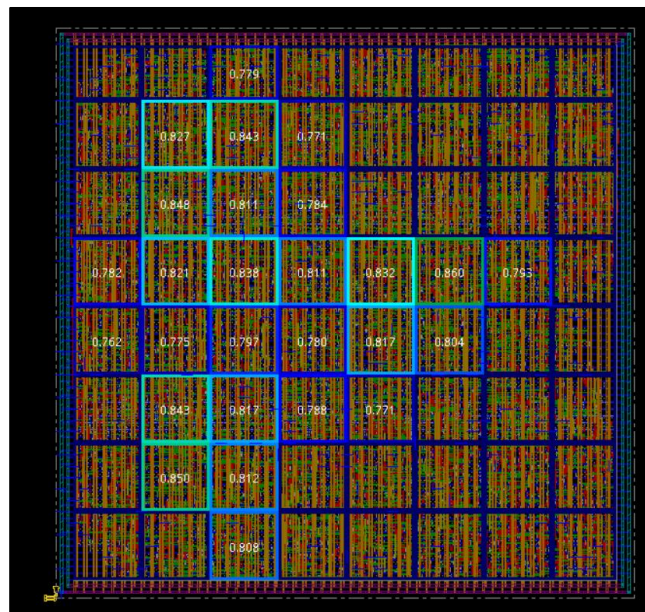
set_input_delay -clock [get_clocks "clk"] -add_delay 0.05 [get_ports "rst"]

set_wire_load_mode "top"
```


8.3 Layout Strategy



Final Layout



Hotspot Congestion

9 Results

9.1 Area

- Area = 14363.28 μm^2
- Gate Count = 13299

```
innovus 1> report_area
Depth  Name    #Inst  Area (um^2)
-----
0      cordic    3251   14363.28
1
```

```
Gate area 1.0800 um^2
[0] cordic Gates=13299 Cells=3251 Area=14363.3 um^2
*** Statistics for net list cordic ***
Number of cells      = 3251
Number of nets       = 4006
Number of tri-nets    = 0
Number of degen nets = 0
Number of pins       = 12288
Number of i/os       = 26
```

Power:

Total Power					

Total Internal Power:	0.62984682		69.7898%		
Total Switching Power:	0.26986422		29.9021%		
Total Leakage Power:	0.00278076		0.3081%		
Total Power:	0.90249179				

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)

Sequential	0.4509	0.03604	0.001137	0.4881	54.08
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.1373	0.1414	0.00152	0.2803	31.06
Clock (Combinational)	0.04162	0.09238	0.0001237	0.1341	14.86
Clock (Sequential)	0	0	0	0	0

Total	0.6298	0.2699	0.002781	0.9025	100

10.2 Timing

Post synthesis slack = 7.511ns

Timing	Worst Negative Slack			Total Negative Slack		
	All	Reg2Reg	Default	All	Reg2Reg	Default
Pre-CTS Setup	4.600 ns	4.600 ns	8.215 ns	0	0	0
Pre-CTS Hold	-0.099 ns	0.076 ns	-0.099 ns	-0.288 ns	0	-0.288 ns
Post-CTS Setup	5.123 ns	5.123 ns	7.547 ns	0	0	0
Post-CTS Hold	-0.126 ns	0.073 ns	-0.126 ns	-0.368 ns	0	-0.368 ns

Terminal window showing a Verilog simulation. The terminal title is 'jv232241@eucld1.vlsi.ee.uitd.ac.in'. The left sidebar shows a file explorer with 'afslitld.ac.in/user/jv/jv232241/u' selected, containing a file 'cordic.sdc'. The main terminal area displays a Verilog simulation log for a 'CORDIC' module. The log includes a list of operations (ADD, TC, CI) with their corresponding values and a final 'Cost Group' summary. The bottom of the terminal shows the command 'legacy_genus:/>'.

```

g44176/A
g44176/Z
ADD_TC_CI_OP782_g345/CI      MXB2M1RA      1  2.7  146  +188  780 F
ADD_TC_CI_OP782_g345/CO      ADFM2RA      1  2.7  50  +156  936 F
ADD_TC_CI_OP782_g344/CI      ADFM2RA      1  2.7  50  +120  1055 F
ADD_TC_CI_OP782_g344/CO      ADFM2RA      1  2.7  50  +119  1174 F
ADD_TC_CI_OP782_g343/CI      ADFM2RA      1  2.7  50  +119  1174 F
ADD_TC_CI_OP782_g342/CO      ADFM2RA      1  2.7  50  +119  1294 F
ADD_TC_CI_OP782_g341/CI      ADFM2RA      1  2.7  50  +119  1413 F
ADD_TC_CI_OP782_g340/CI      ADFM2RA      1  2.7  50  +119  1532 F
ADD_TC_CI_OP782_g339/CI      ADFM2RA      1  2.7  50  +119  1651 F
ADD_TC_CI_OP782_g338/CI      ADFM2RA      1  2.7  50  +119  1770 F
ADD_TC_CI_OP782_g337/CI      ADFM2RA      1  2.7  50  +119  1890 F
ADD_TC_CI_OP782_g336/CI      ADFM2RA      1  2.7  50  +119  2009 F
ADD_TC_CI_OP782_g335/CI      ADFM2RA      1  2.7  50  +119  2128 F
ADD_TC_CI_OP782_g334/CI      ADFM2RA      1  2.7  50  +119  2247 F
ADD_TC_CI_OP782_g333/CI      ADFM2RA      1  1.4  41  +111  2358 F
g44331/A
g44331/Z
XOR3M2RA      1  1.3  37  +226  2584 R
DFQM2RA      100  +5  2584 R
y4b_reg[13]/D
y4b_reg[13]/CK
-----
(clock clk)      capture      10000 R
latency      +100  10100 R
-----
Cost Group : 'clk' (path_group 'clk')
Timing slack : 751ps
Start-point : diff_cosine3_reg[13]/CK
End-point : y4b_reg[13]/D
legacy_genus:/>

```

Post Synthesis Slack

Terminal Sessions View X server Tools Games Settings Macros Help

Quick connect...

fs/aiid.ac.in/user/jy232241/u

Design Name: cordic
Design Mode: 90nm
Analysis Mode: MMCM Non-OCV
Parasitics Mode: No SPEF/RCDB
Signoff Settings: SI Off

AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...

***WARNING: (IMPESI-3014): The RC network is incomplete for net in[7]. As a result, a lumped model is used. This may affect timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.

AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2009.71 CPU=0:00:00.9 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:01.2 real=0:00:01.0 totSessionCpu=0:02:56 mem=2009.7M)

timeDesign Summary

Setup views included:
worst_case

Setup mode	all	reg2reg	default
WNS (ns):	4.600	4.600	8.251
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	1285	1266	19

DRVs	Real		Total	
	Nr nets (terms)	Worst Vio	Nr nets (terms)	
max_cap	47 (47)	-0.023	47 (47)	
max_tran	47 (1156)	-0.493	47 (1156)	

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Timing Analysis@euclid1

Basic Advanced

Use Existing Extraction and Timing Data

Design Stage

Pre-Place Pre-CTS Post-CTS Post-Route Sign-Off

Analysis Type

Setup Hold

Include SI

Reporting Options

Number of Paths: 50
Report file(s) Prefix: cordic_preCTS
Output Directory: timingReports

OK Apply Cancel Help

Pre-CTS Setup Time

Terminal Sessions View X server Tools Games Settings Macros Help

Quick connect...

fs/aiid.ac.in/user/jy232241/u

Design Name: cordic
Design Mode: 90nm
Analysis Mode: MMCM Non-OCV
Parasitics Mode: No SPEF/RCDB
Signoff Settings: SI Off

AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...

***WARNING: (IMPESI-3014): The RC network is incomplete for net clk. As a result, a lumped model is used. This may affect timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.

AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2430.95 CPU=0:00:00.8 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:01.1 real=0:00:01.0 totSessionCpu=0:07:00 mem=2431.0M)

timeDesign Summary

Hold views included:
best_case

Hold mode	all	reg2reg	default
WNS (ns):	-0.099	0.076	-0.099
TNS (ns):	-0.288	0.000	-0.288
Violating Paths:	3	0	3
All Paths:	1285	1266	19

Density: 71.540%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 1.41 sec
Total Real time: 1.0 sec
Total Memory Usage: 2353.570312 Mbytes
innovus 11>

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Timing Analysis@euclid1

Basic Advanced

Use Existing Extraction and Timing Data

Design Stage

Pre-Place Pre-CTS Post-CTS Post-Route Sign-Off

Analysis Type

Setup Hold

Include SI

Reporting Options

Number of Paths: 50
Report file(s) Prefix: cordic_preCTS
Output Directory: timingReports

OK Apply Cancel Help

Pre-CTS Hold Time

Terminal window showing the results of a timing analysis for a design named "cortic". The analysis is for a 90nm technology node, using a Non-OCV analysis mode. The results show a setup time violation for net in[7].

***WARN: (IMPESI-3014): The RC network is incomplete for net in[7]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.

Total number of fetched objects 3852
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2428.95 CPU=0:00:00.8 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:01.1 real=0:00:01.0 totSessionCpu=0:07:06 mem=2429.0M)

timeDesign Summary

Setup views included:
worst_case

Setup mode	all	reg2reg	default
WNS (ns):	5.123	5.123	7.547
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	1285	1266	19

DRVs	Real	Total
Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0 (0)
max_ttran	0 (0)	0 (0)
max_fanout	0 (0)	0 (0)
max_length	0 (0)	0 (0)

Density: 71.540%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 1.74 sec
Total Real time: 2.0 sec
Total Memory Usage: 2371.71875 Mbytes
innovus 11>

Timing Analysis@euclid1

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☒ Setup ☐ Hold

☐ Include SI

Reporting Options

Number of Paths: 50
Report file(s) Prefix: cortic_postCTS
Output Directory: timingReports

OK Apply Cancel Help

Post-CTS Setup Time

Terminal window showing the results of a timing analysis for a design named "cortic". The analysis is for a 90nm technology node, using a Non-OCV analysis mode. The results show a hold time violation for net in[7].

Design Name: cortic
Design Mode: 90nm
Analysis Mode: Non-OCV
Parasitics Mode: No SPEF/RCDB
Signoff Settings: SI Off

AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcMc mode...
*** Calculating scaling factor for min timing library libraries using the default operating cond

***WARN: (IMPESI-3014): The RC network is incomplete for net clk. As a result, a lumped model w
g accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
***WARN: (IMPESI-3014): The RC network is incomplete for net in[7]. As a result, a lumped model
ing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
Total number of fetched objects 3852
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2430.95 CPU=0:00:00.8 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:01.1 real=0:00:01.0 totSessionCpu=0:07:14 mem=2431.0M)

timeDesign Summary

Hold views included:
best_case

Hold mode	all	reg2reg	default
WNS (ns):	-0.126	0.073	-0.126
TNS (ns):	-0.368	0.000	-0.368
Violating Paths:	3	0	3
All Paths:	1285	1266	19

Density: 71.540%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 1.58 sec
Total Real time: 1.0 sec
Total Memory Usage: 2353.570312 Mbytes
innovus 11>

Timing Analysis@euclid1

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

☐ Include SI

Reporting Options

Number of Paths: 50
Report file(s) Prefix: cortic_postCTS
Output Directory: timingReports

OK Apply Cancel Help

Post-CTS Hold Time

10.3 Testability analysis

The pipelined CORDIC has been tested with various input scenarios to validate its performance. The following table shows the outcomes of a testbench incorporating specific angle inputs, including crucial angles like 0, $\pm\pi/4$, and $\pm\pi/2$. It is observed that the output frequency matches the input frequency, as that the output is generated after each cycle, with a latency of 15 clock cycles.

Input	Sine			Cosine		
Angle (Radians)	Output	Actual	Error %	Output	Actual	Error %
0.218750	0.218750	0.217010	0.80%	0.968750	0.976169	0.76%
-1.531250	-0.992188	-0.999218	0.70%	0.039063	0.039536	1.19%
1.531250	0.992188	0.999218	0.70%	0.039063	0.039536	1.19%
0.000000	-0.007813	0.000000	-	0.992188	1.000000	0.78%
0.781250	0.703125	0.704168	0.14%	0.703125	0.710034	0.97%
-0.781250	-0.703125	0.704168	0.14%	0.703125	0.710034	0.97%

```

# Cycle:      0  Cosine: -0.000000  Sine: -0.000000  angle: -0.000000  actual_sine: -0.000000  actual_cosine: 1.000000
# Cycle:      0  Cosine: -0.000000  Sine: -0.000000  angle: 0.218750  actual_sine: 0.217010  actual_cosine: 0.976169
# Cycle:      1  Cosine: -0.000000  Sine: -0.000000  angle: -1.531250  actual_sine: -0.999218  actual_cosine: 0.039536
# Cycle:      2  Cosine: -0.000000  Sine: -0.000000  angle: 1.531250  actual_sine: 0.999218  actual_cosine: 0.039536
# Cycle:      3  Cosine: -0.000000  Sine: -0.000000  angle: 0.000000  actual_sine: 0.000000  actual_cosine: 1.000000
# Cycle:      4  Cosine: -0.000000  Sine: -0.000000  angle: 0.781250  actual_sine: 0.704168  actual_cosine: 0.710034
# Cycle:      5  Cosine: -0.000000  Sine: -0.000000  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     15  Cosine: 0.968750  Sine: 0.218750  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     16  Cosine: 0.039063  Sine: -0.992188  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     17  Cosine: 0.039063  Sine: 0.992188  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     18  Cosine: 0.992188  Sine: -0.007813  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     19  Cosine: 0.703125  Sine: 0.703125  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034
# Cycle:     20  Cosine: 0.703125  Sine: -0.703125  angle: -0.781250  actual_sine: -0.704168  actual_cosine: 0.710034

```

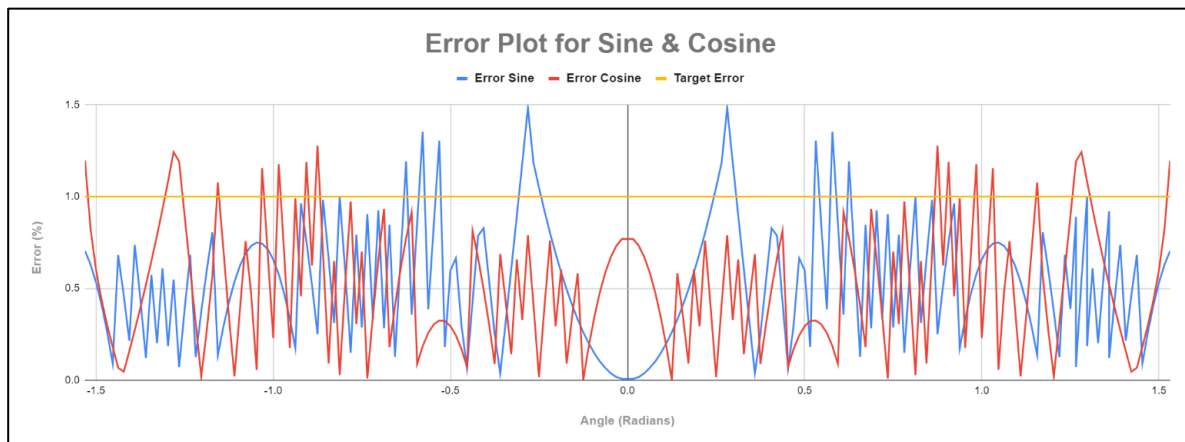
Testbench Output

Error Calculation is done using following formula:

$$\% \text{ Error (Sine)} = \left| \frac{\text{Sine Output} - \text{Actual Sine}}{\text{Actual Sine}} \right| * 100\%$$

$$\% \text{ Error (Cosine)} = \left| \frac{\text{Cosine Output} - \text{Actual Cosine}}{\text{Actual Cosine}} \right| * 100\%$$

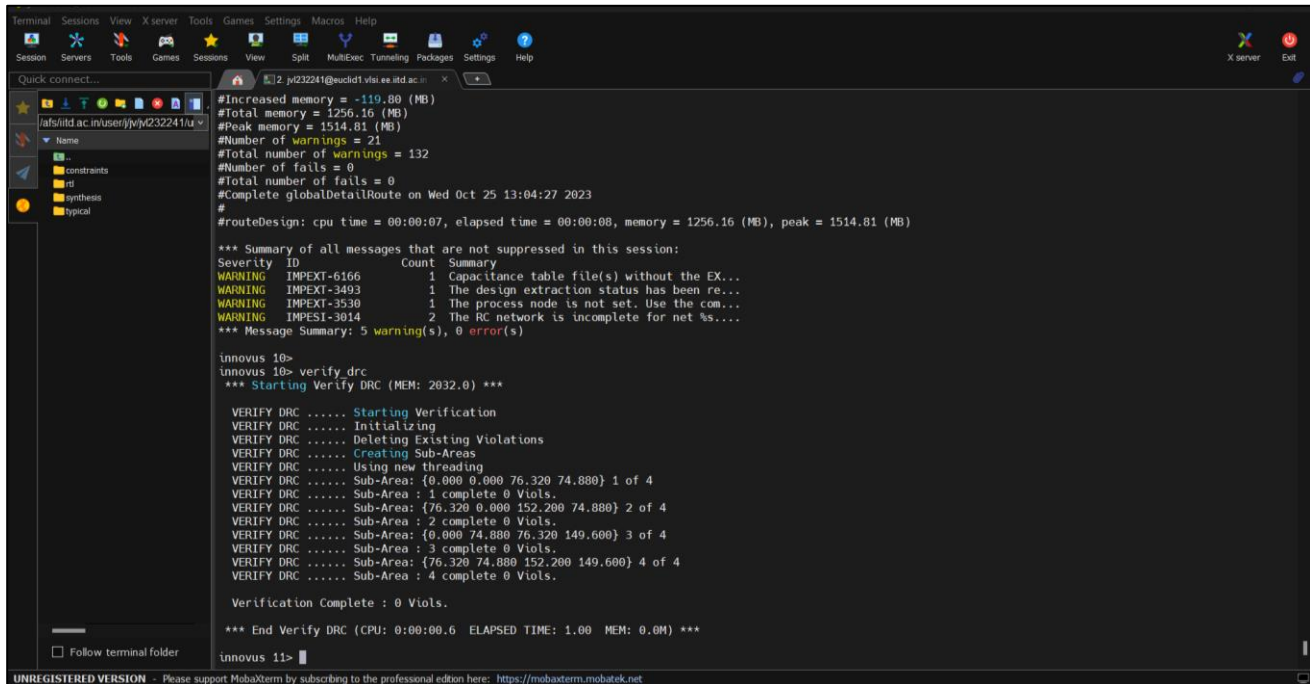
Another testbench has been developed to check the error across the complete spectrum of angle inputs, ranging from -1.53125 to +1.53125 radians. Following plot illustrates the % error between the computed sine and cosine outputs and their actual values across input angles ranging from $-\pi/2$ to $+\pi/2$.



Average Sine Error = 0.54%

Average Cosine Error% = 0.51%

10.4 DRC rule violations



```
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
j232241@eucld1.vlsi.ee.illd.ac.th

#Increased memory = -119.80 (MB)
#Total memory = 1256.16 (MB)
#Peak memory = 1514.81 (MB)
#Number of warnings = 21
#Total number of warnings = 132
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Wed Oct 25 13:04:27 2023
#
#routeDesign: cpu time = 00:00:07, elapsed time = 00:00:08, memory = 1256.16 (MB), peak = 1514.81 (MB)

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPEXT-6166 1 Capacitance table file(s) without the EX...
WARNING IMPEXT-3493 1 The design extraction status has been re...
WARNING IMPEXT-3539 1 The process node is not set. Use the com...
WARNING IMPEST-3814 2 The RC network is incomplete for net %s....
*** Message Summary: 5 warning(s), 0 error(s)

innovus 10>
innovus 10> verify_drc
*** Starting Verify DRC (MEM: 2032.0) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 76.320 74.880} 1 of 4
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {76.320 0.000 152.200 74.880} 2 of 4
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 74.880 76.320 149.600} 3 of 4
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {76.320 74.880 152.200 149.600} 4 of 4
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.6 ELAPSED TIME: 1.00 MEM: 0.0M) ***

innovus 11>
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
```

DRC cleared

11 Bugs known at submission date

None.