

1

Number Systems & Binary Codes

LEVEL - 1 Questions

1. The octal equivalent of the HEX number AB.CD is (GATE-EE-2007)
 (a) 253.314 (b) 253.632
 (c) 526.314 (d) 526.632
2. The binary equivalent of hexadecimal number 4 F 2 D is (IES-EE-2002)
 (a) 0101 1111 0010 1100
 (b) 0100 1111 0010 1100
 (c) 0100 1110 0010 1101
 (d) 0100 1111 0010 1101
3. Decimal 43 in Hexadecimal and BCD number system is respectively.
 (GATE-EC-2005)
 (a) B2, 0100 0011 (b) 2B, 0100 0011
 (c) 2B, 0011 0100 (d) B2, 0100 0100
4. $(1217)_8$ is equivalent to (IES-EC-2008)
 (a) $(1217)_{16}$ (b) $(028F)_{16}$
 (c) $(2297)_{10}$ (d) $(0B17)_{16}$
5. The hexadecimal representation of 657_8 is: (IES-EC-2010)
 (a) 1 AF H (b) D 78 H
 (c) D 71 H (d) 32 F H
6. Match List - I with List - II and select the correct answer by using the codes given below the lists: (IES-EE-1992)

List - I	List - II
(Octal)	(Binary)
A. 75	1. 010110
B. 65	2. 110101
C. 37	3. 111101
D. 26	4. 011111

Codes:

	A	B	C	D
(a)	3	1	4	2
(b)	3	2	4	1
(c)	1	2	3	4
(d)	4	1	2	3

7. Given $(135)_x + (144)_x = (323)_x$ What is the value of base x? (IES-EC-2005)
 (a) 5 (b) 3 (c) 12 (d) 6
8. Which one of the following is a non-valid BCD code? (IES-EE-1998)
 (a) 0111 1001 (b) 0101 1011
 (c) 0100 1000 (d) 0100 1001
9. What is the addition of $(-64)_{10}$ and $(80)_{16}$? (IES-EC-2007)
 (a) $(-16)_{10}$ (b) $(16)_{16}$
 (c) $(11000000)_2$ (d) $(01000000)_2$
10. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number? (GATE-EC-2004)
 (a) 25, 9 and 57 respectively
 (b) -6, -6 and -6 respectively
 (c) -7, -7 and -7 respectively
 (d) -25, -9 and -57 respectively
11. Zero has two representations in:
 (GATE-CSIT-1999)
 (a) Sign magnitude
 (b) 1's complement
 (c) 2's complement
 (d) None of the above
12. The number 43 in 2's complement representation is (GATE-CSIT-2000)
 (a) 01010101 (b) 11010101
 (c) 00101011 (d) 10101011

13. The decimal number -15 is represented in 8-bit signed 2's complement form as **(GATE-IN-1994)**
 (a) 11010001 (b) 11100111
 (c) 11110001 (d) 10001111
14. $(24)_8$ is expressed in Gray code as which one of the following? **(IES-EC-2008)**
 (a) 11000 (b) 10100
 (c) 11110 (d) 11111
15. Which of the following binary is equal to octal number 66.3 **(ISRO)**
 (a) 101101.100 (b) 1101111.111
 (c) 111111.1111 (d) 110110.011
16. The greatest negative number which can be stored in a computer that has 8-bit word length and uses 2's complement arithmetic is **(ISRO)**
 (a) -256 (b) -255
 (c) -128 (d) -127

LEVEL – 2 Questions

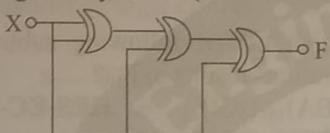
01. The minimum decimal equivalent of the number $11C_x$ is **(IES-EC-2000)**
 (a) 183 (b) 194 (c) 268 (d) 269
02. The number of 1's in 8-bits representation of -127 in 2's complement form is m and that in 1's complement form is n. What is the value of m:n? **(IES-EC-2005)**
 (a) 2:1 (b) 1:2 (c) 3:1 (d) 1:3
03. A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should **(GATE-EC-1997)**
 (a) Copy the original byte to the less significant byte of the word and fill
- the more significant byte with zeros.
 (b) Copy the original byte to the more significant byte of the word and fill the less significant byte with zeros.
 (c) Copy the original byte to the less significant byte of the word and make each bit of the more significant byte equal to the most significant bit of the original byte.
 (d) Copy the original byte to the less significant byte as well as the more significant byte of the word.
04. Assuming all numbers are in 2's complement representation, which of the following numbers is divisible by 11111011? **(GATE-CSIT-2003)**
 (a) 11100111 (b) 11100100
 (c) 11010111 (d) 11011011
05. Two's complement of a given 3 or more bit binary number of non – zero magnitude is the same as the original number if all bits except the
 (a) MSB are zeros **(IES-EC-1995)**
 (b) LSB are zeros
 (c) MSB are ones
 (d) LSB are ones
06. If $(2.3)_4 + (1.2)_4 = (y)_4$; What is the value of y? **(IES-EC-2005)**
 (a) 10.1 (b) 10.01
 (c) 10.2 (d) 1.02
07. A number in 4- bit two's complement representation is $X_3 X_2 X_1 X_0$. This number when stored using 8 – bits will be **(GATE-INS-1999)**
 (a) 0000 $X_3 X_2 X_1 X_0$.
 (b) 1111 $X_3 X_2 X_1 X_0$.
 (c) $X_3 X_3 X_3 X_3 X_2 X_1 X_0$
 (d) $\overline{X}_3 \overline{X}_3 \overline{X}_3 \overline{X}_3 X_3 X_2 X_1 X_0$

2

Logic Gates, Boolean Algebra & K - Maps

LEVEL - 1 Questions

01. For the circuit shown below the output F is given by **(GATE-EC-1988)**



- (a) $F = 1$ (b) $F = 0$
 (c) $F = X$ (d) $F = \bar{X}$

02. Minimum number of 2-input NAND gates required to implement the function, $F = (\bar{X} + \bar{Y})(Z+W)$ is **(GATE-EC-1988)**

- (a) 3 (b) 4 (c) 5 (d) 6

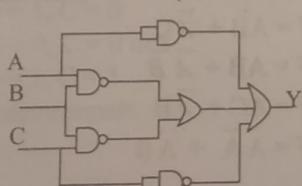
03. What is the minimum number of gates required to implement the Boolean function $(AB + C)$ if we have to use only 2-input NOR gates? **(GATE-CSIT-2009)**

- (a) 2 (b) 3 (c) 4 (d) 5

04. The minimum number of NAND gates required to implement the Boolean function $A+A\bar{B}+A\bar{B}C$ is equal to **(IES-EC -2003)**

- (a) Zero (b) 1 (c) 4 (d) 7.

05. For the logic circuit shown in Figure, the output is equal to **(GATE-EC-1993)**



(a) $\overline{A}\overline{B}\overline{C}$

(b) $\overline{A}+\overline{B}+\overline{C}$

(c) $\overline{AB}+\overline{BC}+\overline{A}+\overline{C}$

(d) $\overline{AB}+\overline{BC}$

06. Karnaugh map is used to **(IES-EC-2000)**

- (a) Minimize the number of flip-flops in a digital circuit.
 (b) Minimize the number of gates only in a digital circuit.
 (c) Minimize the number of gates and fan in of a digital circuit.
 (d) Design gates.

07. The Boolean expression $\overline{XYZ} + \overline{X}\overline{YZ} + XY\overline{Z} + X\overline{YZ} + XYZ$

can be simplified to **(GATE-EE-2003)**

(a) $X\overline{Z} + \overline{X}Z + YZ$

(b) $XZ + \overline{Y}Z + Y\overline{Z}$

(c) $\overline{XY} + YZ + XZ$

(d) $\overline{XY} + Y\overline{Z} + X\overline{Z}$

08. The simplified form of the Boolean expression **(GATE-EE-2004)**

$Y = (\overline{ABC} + D)(\overline{A}D + \overline{B}\overline{C})$ can be written as

(a) $\overline{A}D + \overline{B}\overline{C}D$

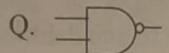
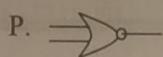
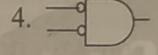
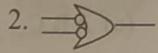
(b) $AD + B\overline{C}D$

(c) $(\overline{A} + D)(\overline{B}C + \overline{D})$

(d) $\overline{AD} + BCD$

09. Match the logic gates in **column A** with their equivalents in **column B**.

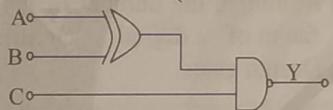
(GATE-EC-2010)

Column A**Column B**

- (a) P-2, Q-4, R-1, S-3
 (b) P-4, Q-2, R-1, S-3
 (c) P-2, Q-4, R-3, S-1
 (d) P-4, Q-2, R-3, S-1

10. The Boolean expression for the output of the logic circuit shown in figure is

(GATE-EE-1996)



- (a) $Y = \overline{A} \overline{B} + AB + \overline{C}$
 (b) $Y = \overline{A} B + AB + \overline{C}$
 (c) $Y = \overline{A} B + \overline{A} B + C$
 (d) $Y = \overline{A} B + \overline{A} \overline{B} + \overline{C}$

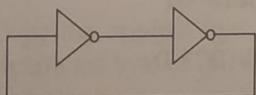
11. The min terms expansion of $f(P, Q, R) = PQ + QR + PR$ is

(GATE-CSIT-2010)

- (a) $m_2 + m_4 + m_6 + m_7$
 (b) $m_0 + m_1 + m_3 + m_5$
 (c) $m_0 + m_1 + m_6 + m_7$
 (d) $m_2 + m_3 + m_4 + m_5$

12. The digital circuit using two inverters shown in Fig. will act as

(GATE-EE-2004)



- (a) A bistable multi-vibrator
 (b) An astable multi-vibrator
 (c) A Monostable multi-vibrator
 (d) An oscillator

13. The minimum Boolean for the following circuit is

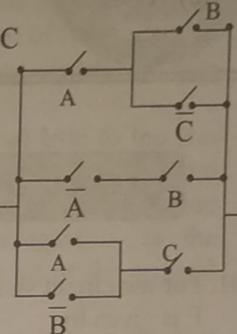
(IES-EC-1993)

- (a) $AB + AC + BC$

- (b) $A + BC$

- (c) $A + B$

- (d) $A + B + C$



14. Which of the following subtraction operations results in F_{16} ?

1. $(BA)_{16} - (AB)_{16}$

(IES-EC-2006)

2. $(BC)_{16} - (CB)_{16}$

3. $(CB)_{16} - (BC)_{16}$

Select the correct answer using the code given below:

- (a) Only 1 and 2 (b) Only 1 and 3
 (c) Only 2 and 3 (d) 1, 2 and 3

15. What is the simplified form of the given Boolean expression

$$T = (X + Y)(X + \bar{Y})(\bar{X} + Y)?$$

(IES-EE-2008)

- (a) $\bar{X} \bar{Y}$

- (b) $\bar{X} Y$

- (c) XY

- (d) $X \bar{Y}$

16. The Boolean expression

$$\bar{Y} \bar{Z} + \bar{X} \bar{Z} + \bar{X} \bar{Y}$$

is logically equivalent to

(IES-EE-2005)

- (a) $YZ + \bar{X}$

- (b) $YZX + \bar{X} \bar{Y} \bar{Z}$

- (c) $YZ + XZ + XY$

- (d) $X \bar{Y} \bar{Z} + \bar{X} \bar{Y} \bar{Z} + \bar{X} Y \bar{Z} + \bar{X} \bar{Y} Z$

17. In Boolean algebra, if

$$F = (A + B)(\bar{A} + C),$$

(IES-EE-2001)

- (a) $F = AB + \bar{A} C$

- (b) $F = AB + \bar{A} \bar{B}$

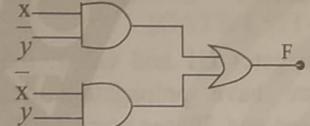
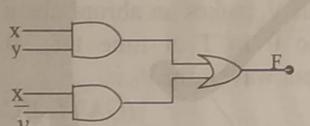
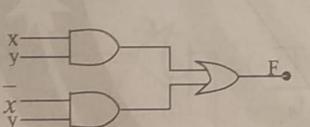
- (c) $F = AC + \bar{A} B$

- (d) $F = A \bar{A} + \bar{A} B$

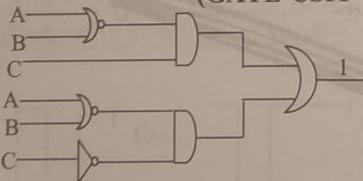
18. According to De Morgan's second theorem
(IES-EE-1992)

- (a) A NAND gate is always complimentary to an AND gate
- (b) A NAND gate equivalent to a bubbled NAND gate
- (c) A NAND gate is equivalent to a bubbled AND gate
- (d) A NAND gate is equivalent to a bubbled OR gate.

19. Which of the following is a coincidence logic circuit:
(IES-EC-1992)

- (a) 
- (b) 
- (c) 
- (d) 

20. In the digital circuit shown below, the output f is found to be logic 1 when A is logic '0'. The values of B and C are
(GATE-CSIT-1992)



- (a) B = 1, C = 0
- (b) B = 0, C = 0 or 1
- (c) B = 1, C = 1
- (d) indeterminate

21. The Boolean expression $\overline{A + B + C}$ is equal to
(GATE-CSIT-1994)

- (a) $\overline{A} + \overline{B} + \overline{C}$
- (b) $\overline{A} \cdot \overline{B} \cdot \overline{C}$
- (c) $A + B + C$
- (d) $A \cdot (B + C)$.

22. A combinational circuit has inputs A, B and C and its Karnaugh map is given in below Fig .The output of the circuit is
(GATE-CSIT-1995)

	AB	00	01	11	10
C	0		1		1
1	1	1		1	

- (a) $(\overline{A}B + A\overline{B})C$
- (b) $(\overline{A}\overline{B} + A\overline{B})\overline{C}$
- (c) $A \oplus B \oplus C$
- (d) $\overline{A} \overline{B} \overline{C}$

23. In the logic equation
 $A(A + \overline{B}\overline{C} + C) + \overline{B}(\overline{C} + \overline{A}) + BC = 1$,
if $C = \overline{A}$ then
(DRDO)

- (a) $A + B = 1$
- (b) $\overline{A} + B = 1$
- (c) $A + \overline{B} = 1$
- (d) $A = 1$

24. A Boolean function can be expressed
(JTO)

- (a) as sum of max terms or product of min terms
- (b) as product of max terms or sum of min terms
- (c) partly as product of max terms and partly as sum of min terms
- (d) partly as sum of max terms and partly as product of min terms

LEVEL - 2 Questions

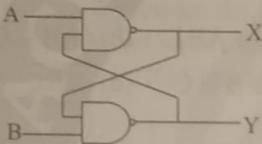
01. Two 2's complement numbers having sign bits x and y are added and the sign bit of the result is z . Then, the occurrence of overflow is indicated by the Boolean function.

(GATE-ECE-1998)

- (a) xyz
- (b) $\bar{x}\bar{y}\bar{z}$
- (c) $\bar{x}\bar{y}z + x\bar{y}\bar{z}$
- (d) $xy + yz + zx$

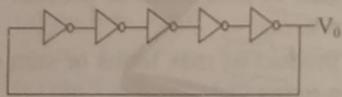
02. In below fig., $A = 1$ and $B = 1$. The input B is now replaced by a sequence $101010 \dots$, the outputs X and Y will be

(GATE-EC-1998)



- (a) Fixed at 0 and 1, respectively
- (b) $X = 1010 \dots$ while $Y = 0101 \dots$
- (c) $X = 1010 \dots$ and $Y = 1010 \dots$
- (d) fixed at 1 and 0, respectively

03. For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 Pico sec. What is the fundamental frequency of the oscillator output? (GATE-EC-2001)

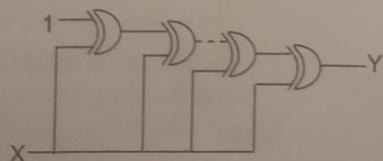


- (a) 10MHz
- (b) 100MHz
- (c) 1GHz
- (d) 2GHz.

04. If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is X then the output Y is equal to

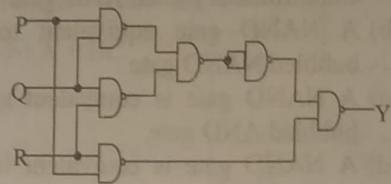
(GATE-EC-2002)

- (a) 0
- (b) 1
- (c) \bar{X}
- (d) X



05. The output Y in the circuit below is always "1" when

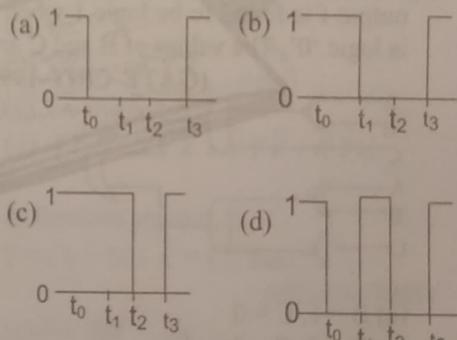
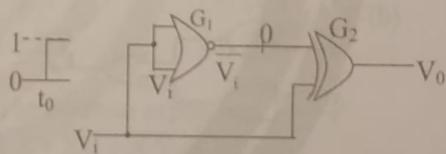
(GATE-EC-2011)



- (a) two or more of the inputs P, Q, R are "0"
- (b) two or more of the inputs P, Q, R are "1"
- (c) any odd number of the inputs P, Q, R is "0"
- (d) any odd number of the inputs P, Q, R is "1"

06. The gates G_1 and G_2 in the below figure have propagation delays of 10nsec and 20nsec respectively. If the input V_i makes an abrupt change from logic 0 to 1 at time $t=t_0$, then the output waveform V_0 is

(GATE-EC-2002)

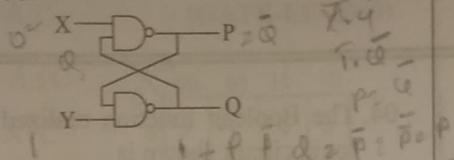


07. The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

(GATE-EC-2007)

$X=0, Y=1$; $X=0, Y=0$; $X=1, Y=1$.

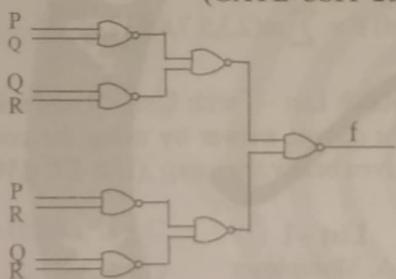
The corresponding stable P,Q outputs will be



- (a) $P=1, Q=0; P=1, Q=0; P=1, Q=0$ or $P=0, Q=1$
- (b) $P=1, Q=0; P=0, Q=1$; or $P=0, Q=1; P=1, Q=0$
- (c) $P=1, Q=0; P=1, Q=1; P=1, Q=0$ or $P=0, Q=1$
- (d) $P=1, Q=0; P=1, Q=1; P=1, Q=1$

08. What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below?

(GATE-CSIT-2010)



- (a) $\overline{Q+R}$
- (b) $\overline{P+Q}$
- (c) $\overline{P+R}$
- (d) $\overline{P+Q+R}$

09. How many min terms (excluding redundant terms) does the minimal switching function

$$f(v, w, x, y, z) = x + \bar{y}z$$

Originally have? (IES-EC-1998)

- (a) 16
- (b) 20
- (c) 24
- (d) 32

10. Match List-I(Boolean Logic Function) with List-II(Inverse of Function) and select the correct answer using the code given below the lists:

List-I (IES-EC-2007)

- A. $ab+bc+ca+abc$
- B. $a\bar{b}+\bar{a}\bar{b}+\bar{c}$
- C. $a+bc$
- D. $(\bar{a}+\bar{b}+\bar{c})(a+\bar{b}+\bar{c})(\bar{a}+\bar{b}+c)$

List-II

- 1. $\bar{a}(\bar{b}+\bar{c})$
- 2. $\bar{a}\bar{b}+\bar{b}\bar{c}+\bar{c}\bar{a}$
- 3. $(a \oplus b)c$
- 4. $abc+\bar{a}\bar{b}c+a\bar{b}\bar{c}$

Codes:

	A	B	C	D
(a)	3	2	1	4
(b)	2	3	1	4
(c)	3	2	4	1
(d)	2	3	4	1

11. An odd function involving three Boolean variables is (DRDO-CSE)

- (a) $\Sigma(1, 3, 5, 7)$
- (b) $\Sigma(0, 2, 4, 6)$
- (c) $\Sigma(1, 2, 4, 7)$
- (d) $\Sigma(0, 3, 5, 6)$

3

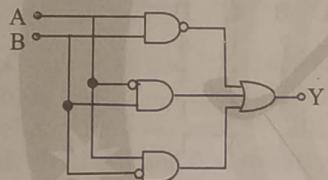
Combinational Circuits

LEVEL - 1 Questions

01. The Boolean expression $X(P, Q, R) = \pi(0, 5)$ is to be realized using only two 2-input gates. Which are these gates? (IES-EC-2006)

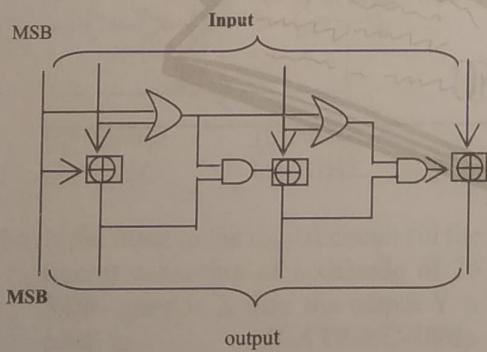
- (a) AND and OR
- (b) NAND and OR
- (c) AND and XOR
- (d) OR and XOR

02. In the given circuit, the output Y equals which one of the following? (IES-EE-2008)



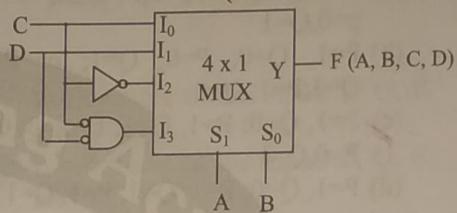
- (a) $A + B$
- (b) $\overline{AB} + A\overline{B}$
- (c) AB
- (d) $\overline{A} + \overline{B}$

03. The circuit shown in the figure converts (GATE-EC-2003)



- (a) BCD to Binary code
- (b) Binary to excess-3 code
- (c) Excess-3 to Gray code
- (d) Gray to Binary code.

04. The Boolean function realized by the logic circuit shown is (GATE-EC-2010)



- (a) $F = \sum m(0, 1, 3, 5, 9, 10, 14)$
- (b) $F = \sum m(2, 3, 5, 7, 8, 12, 13)$
- (c) $F = \sum m(1, 2, 4, 5, 11, \dots, 5)$
- (d) $F = \sum m(2, 3, 5, 7, 8, 9, 12)$

05. Match List - I with List - II and select the correct answer by using the codes given below the lists: (IES-EC-1992)

List - I

- A. Multiplexer
- B. Shift - Register
- C. Encoder

List - II

- 1. Sequential memory
- 2. Converts decimal number to binary
- 3. Data selector

A	B	C
(a) 1	2	3
(b) 2	3	1
(c) 3	1	2
(d) 1	2	2

06. The logic function $f = (\overline{x}\cdot\overline{y}) + (\overline{x}\cdot y)$ is the same as (GATE-EE-1999)

- (a) $f = (x+y)(\overline{x} + \overline{y})$
- (b) $f = (\overline{x} + \overline{y}) + (x+y)$
- (c) $f = (\overline{x}\cdot y)(x\cdot\overline{y})$
- (d) none of (A), (B), (C)

07. The minimal product-of-sums function described by the K-map given in Fig.

(a) $\overline{A} \overline{C}$ (GATE-EE-2000)

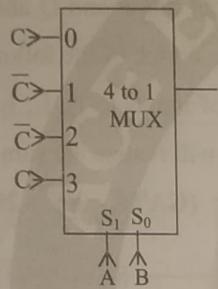
(b) $\overline{A} + \overline{C}$

	AB	00	01	11	10
C	0	1	1	ϕ	0
0	1				
1	0	0	ϕ	0	

(c) $A+C$

(d) AC

08. Consider the circuit in Fig. f implements (GATE-CSIT-1996)



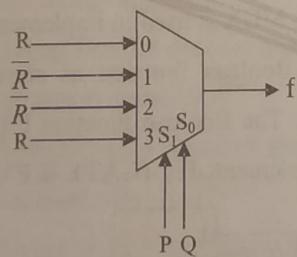
(a) $\overline{A} \overline{B} C + \overline{A} B \overline{C} + ABC$

(b) $A + B + C$

(c) $A \oplus B \oplus C$

(d) $AB + BC + CA$

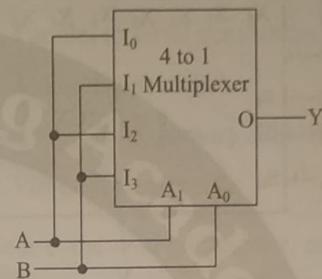
09. The Boolean expression for the output f of the multiplexer shown below is (GATE-CSIT-2010)



(a) $\overline{P \oplus Q \oplus R}$ (b) $P \oplus Q \oplus R$

(c) $P+Q+R$ (d) $\overline{P+Q+R}$

10. A gate having two inputs (A, B) and one output (Y) is implemented using a 4-to-1 multiplexer as shown in Fig. A_1 (MSB) and A_0 are the control bits and $I_0 - I_3$ are the inputs to the multiplexer. The gate is (DRDO)



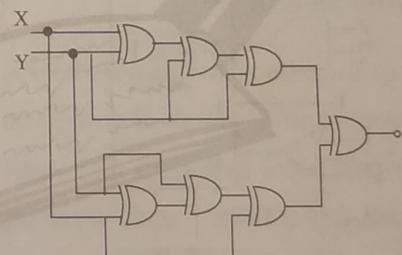
(a) NAND (b) NOR

(c) XOR (d) OR

LEVEL - 2 Questions

01. The circuit shown in the figure below generates the function of (IES-EE-2010)

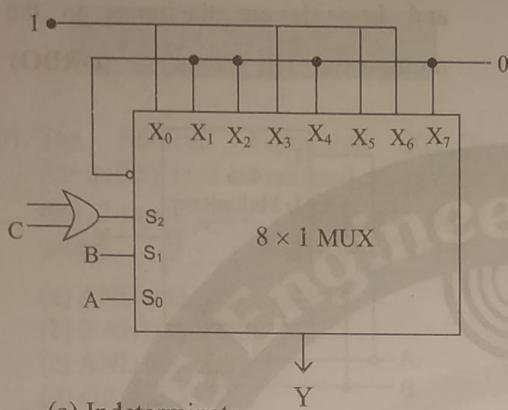
(IES-EE-2010)



(a) $x \oplus y$ (b) 0

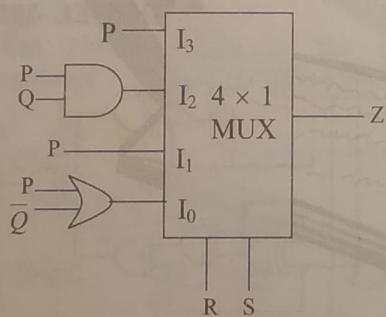
(c) $x\bar{y} + yx + \bar{y}x$ (d) $x \cdot \bar{y}$

02. In the TTL circuit in the figure, S_2 to S_0 are select lines and X_7 to X_0 are input lines. S_0 and X_0 are LSB's. The output Y is (GATE-EC-2001)



- (a) Indeterminate
 (b) $A \oplus B$
 (c) $\overline{A \oplus B}$
 (d) $\overline{C}(\overline{A \oplus B}) + C(A \oplus B)$

03. For the circuit shown in the following I_0 – I_3 are inputs to the 4:1 multiplexer. R (MSB) and S are control bits (GATE-EC-2008)



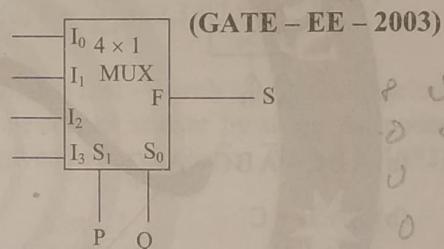
The output Z can be represented by

- (a) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$
 (b) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
 (c) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
 (d) $PQ\bar{R} + PQRS + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$

04. What are the minimum number of 2-to-1 multiplexers required to generate a 2-input AND gate and a 2-input EX-OR gate?

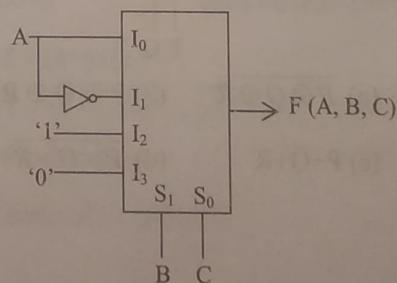
- (GATE-EC-2009)
 (a) 1 and 2 (b) 1 and 3
 (c) 1 and 1 (d) 2 and 2

05. Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in} . Which of the following combinations of inputs to I_0 , I_1 , I_2 and I_3 of the MUX will realize the sum S?



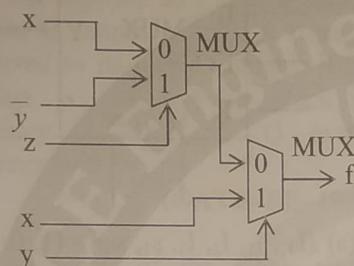
- (GATE - EE - 2003)
 (a) $I_0 = I_1 = C_{in}; I_2 = I_3 = \bar{C}_{in}$
 (b) $I_0 = I_1 = \bar{C}_{in}; I_2 = I_3 = C_{in}$
 (c) $I_0 = I_3 = C_{in}; I_1 = I_2 = \bar{C}_{in}$
 (d) $I_0 = I_3 = \bar{C}_{in}; I_1 = I_2 = C_{in}$

06. A 4x1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function F (A, B, C) implemented is (GATE-EE-2006)



- (a) $F(A, B, C) = \sum(1, 2, 4, 6)$
 (b) $F(A, B, C) = \sum(1, 2, 6)$
 (c) $F(A, B, C) = \sum(2, 4, 5, 6)$
 (d) $F(A, B, C) = \sum(1, 5, 6)$

07. Consider the circuit above. Which one of the following options correctly represents $f(x, y, z)$? (GATE-CSIT-06)



- (a) $xz + xy + \bar{y}z$ (b) $x\bar{z} + xy + \bar{y}z$
 (c) $xz + xy + \bar{y}\bar{z}$ (d) $xz + x\bar{y} + \bar{y}z$

08. How many 3 to 8 decoders with an enable input are needed to construct 6 to 64 line decoder without using any other logic gates (GATE-CSIT-2007)

- (a) 7 (b) 8 (c) 9 (d) 10

09. Consider the following statements:

A 4: 16 decoder can be constructed (with enable input) by:

1. Using four 2:4 decoder (each with an enable input) only.
2. Using five 2:4 decoders (each with an enable input) only
3. Using two 3:8 decoders (each with an enable input) only
4. Using two 3:8 decoders (each with an enable input) and an inverter.

Which of the statements given above is/are correct (IES-EC-2005)

- (a) 2 & 3 (b) 1 only
 (c) 2 and 4 (d) None of the above.

10. A digital multiplexer can be used for which of the following?

1. Parallel to serial conversion
2. Many-to-one switch
3. To generate memory chip select.
4. For code conversion.

Select the correct answer using the code given below: (IES-EC-2008)

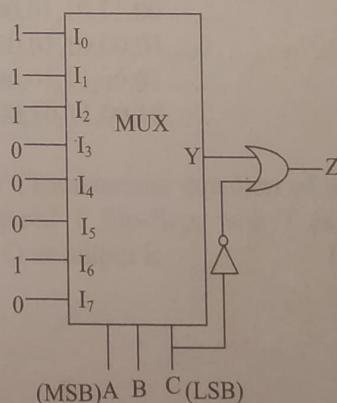
- (a) 1, 3 and 4 (b) 2, 3 and 4
 (c) 1 and 2 only (d) 2 and 3 only

11. Assertion(A): A de-multiplexer cannot be used as a decoder.

Reason (R): A de-multiplexer selects one of many outputs, whereas a decoder selects an output corresponding to the coded input.

(IES-EC-2011)

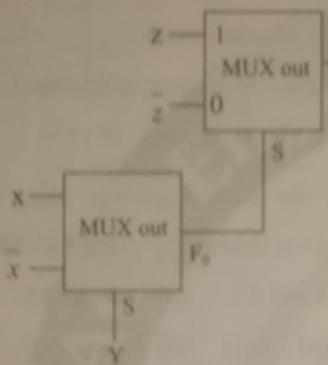
12. A combinational circuit using a 8-to -1 multiplexer is shown in the following figure. The minimized expression for the output (Z) is (GATE-INS-2006)



- (a) $C(\bar{A} + \bar{B})$ (b) $C(A + B)$
 (c) $\bar{C}(\bar{A}B)$ (d) $\bar{C} + AB$

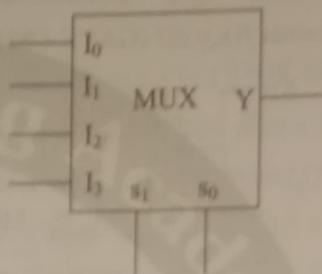
13. A MUX circuit shown in the figure below implements a logic function F_1 . The correct expression for F_1 is

(GATE-INS-2007)



- (a) $(\bar{X} \oplus \bar{Y}) \oplus Z$ (b) $(X \oplus Y) \oplus Z$
 (c) $(X \oplus Y) \oplus \bar{Z}$ (d) $(X \oplus Y) + Z$
 (e) $(X \oplus Y) \oplus Z$

14. The Boolean function $F(A, B, C) = \prod(0, 2, 4, 7)$ is to be implemented using a 4×1 multiplexer shown in figure. Which one of the following choices of inputs to multiplexer will realize the Boolean function? (JTO)



- (a) $(I_0, I_1, I_2, I_3, s_1, s_0) = (1, 0, \bar{A}, A, C, B)$
 (b) $(I_0, I_1, I_2, I_3, s_1, s_0) = (1, 0, \bar{A}, A, B, C)$
 (c) $(I_0, I_1, I_2, I_3, s_1, s_0) = (0, 1, \bar{A}, A, C, B)$
 (d) $(I_0, I_1, I_2, I_3, s_1, s_0) = (0, 1, A, \bar{A}, B, C)$

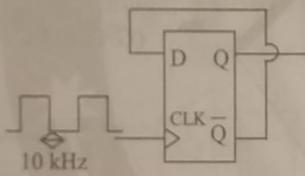
4

Sequential Circuits

LEVEL - I Questions

01. For a J-K flip-flop its J input is tied to its own Q output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency will be _____.
(GATE-EE-1995)

02. The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in Fig. is 10 kHz. The frequency of the signal available at Q is _____
(GATE-EE-2002)



- (a) 10 kHz (b) 2.5 kHz
(c) 20 kHz (d) 5 kHz

03. Choose the correct one from among the alternatives A, B, C, and D after matching an item from Group1 with the most appropriate item in Group2.

Group1 (GATE-EC-2004)

P. shift register

Q. Counter

R. Decoder

Group2

1. Frequency division
 2. Addressing in memory chips
 3. Serial to parallel data conversion
- (a) P-3, Q-2, R-1
(b) P-3, Q-1, R-2
(c) P-2, Q-1, R-3
(d) P-1, Q-3, R-2

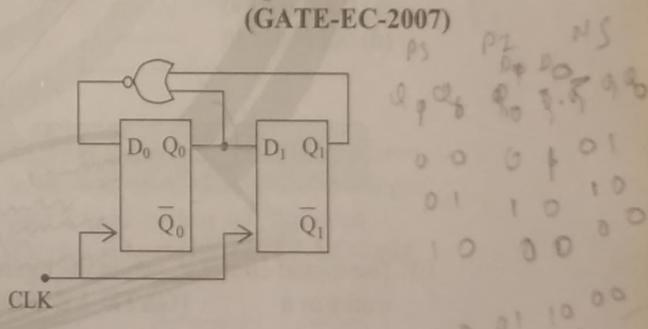
04. The present output Q_n of an edge triggered JK flip flop is logic 0. If $J=1$, then Q_{n+1} = _____
(GATE-EC-2005)

- (a) Cannot be determined
(b) Will be logic 0
(c) Will be logic 1
(d) Will race around

05. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then
(GATE-EC-2003)

- (a) R= 10ns, S= 40ns
(b) R=40ns, S=10ns
(c) R=10ns, S=30ns
(d) R=30ns, S=10ns

06. For the circuit shown, the counter state $(Q_1 Q_0)$ follows the sequence
(GATE-EC-2007)

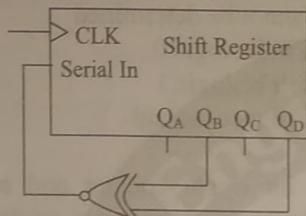


- (a) 00,01,10,11,00.....
(b) 00,01,10,00,01.....
(c) 00,01,11,00,01.....
(d) 00,10,11,00,10.....

07. The Characteristic equation of a level triggered T flip-flop, with T as input and Q as output is
(JTO)

- (a) $Q(n+1) = T\bar{Q} + \bar{T}Q$
 (b) $Q(n+1) = \bar{T}$
 (c) $Q(n+1) = Q$
 (d) $Q(n+1) = TQ + \bar{T}\bar{Q}$

08. A 4-bit serial-in-parallel-out shift register is used with a feedback as shown in Fig. The shifting sequence is $Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$. (DRDO)



If the output is 0000 initially, the output repeats after

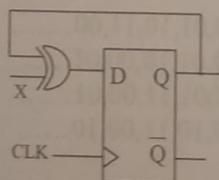
- (a) 4 clock cycles
 (b) 6 clock cycles
 (c) 15 clock cycles
 (d) 16 clock cycles

09. If a counter having 10 FLIP-FLOP's is initially at 0, what count will it hold after 2060 pulses? (ISRO)

- (a) 0000001100
 (b) 0000011100
 (c) 0000011000
 (d) 0000001110

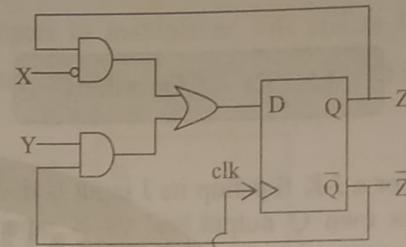
LEVEL - 2 Questions

01. The digital circuit shown in the figure works as a (GATE-EE-2005)



- (a) JK flip-flop
 (b) Clocked RS flip-flop
 (c) T-flip-flop
 (d) Ring counter

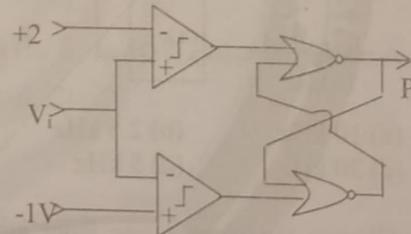
02. A sequential circuit using D Flip Flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is (GATE-EC-2000)



- (a) S-R Flip Flop with inputs $X=R$ and $Y=S$
 (b) S-R Flip Flop with inputs $X=S$ and $Y=R$
 (c) J-K Flip Flop with inputs $X=J$ and $Y=K$
 (d) J-K Flip Flop with inputs $X=K$ and $Y=J$

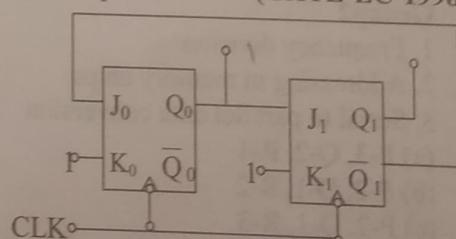
03. Choose the correct statements relating to the circuit of figure

(GATE-EC-1987)



- (a) For $V_i = -2V$, $P=0$
 (b) For $V_i = +3V$, $P=0$
 (c) For $V_i = 0V$, $P = 0$ always
 (d) For $V_i = 0V$, P can be either 0 or 1.

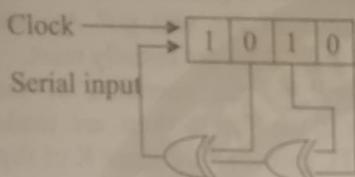
04. Figure shows a mod-K counter. Here K is equal to (GATE-EC-1998)



- (a) 1 (b) 2 (c) 3 (d) 4

05. The shift register shown in fig. is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?

(GATE-EE-2003)

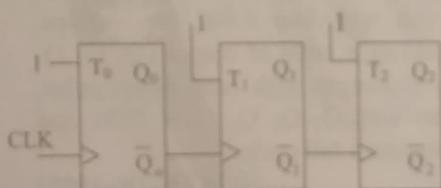


(a) 3
(c) 11

(b) 7
(d) 15

06. The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2Q_1Q_0=011$, then its next state ($Q_2Q_1Q_0$) will be

(GATE-EC-2005)

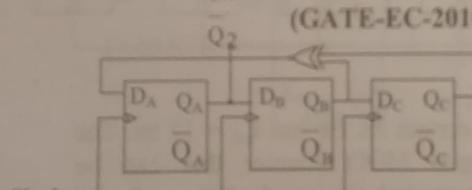


(a) 010
(c) 111

(b) 100
(d) 101

07. Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is

(GATE-EC-2010)

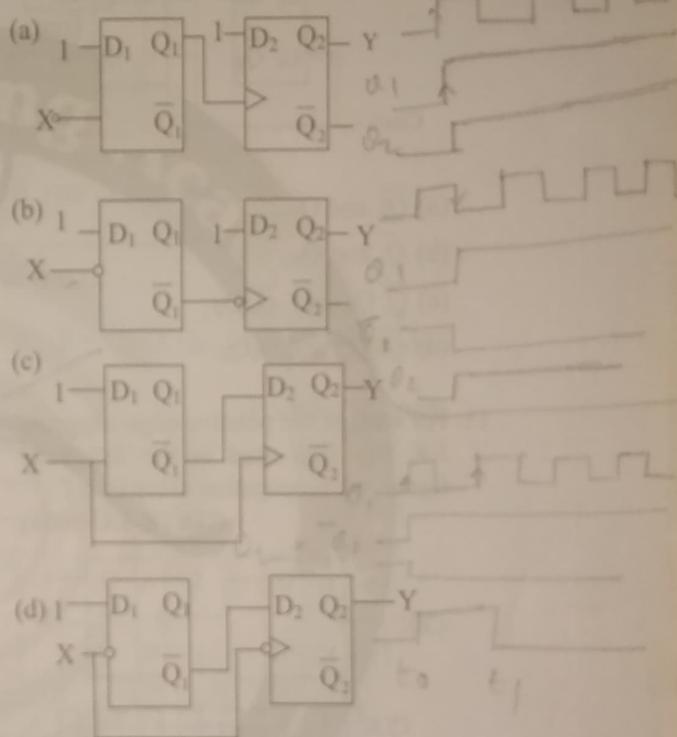
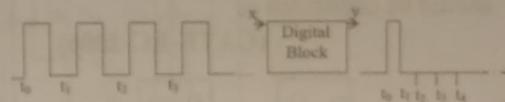


(a) 0010111...
(c) 0101111...

(b) 0001011...
(d) 0110100...

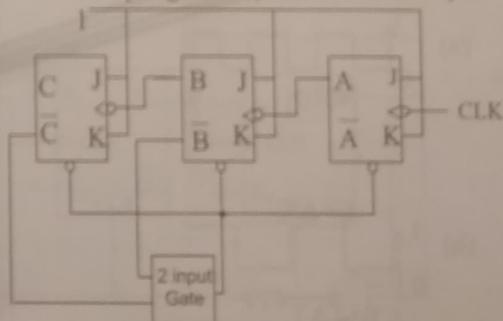
08. The digital block in the figure is realized using two positive edge triggered D flip-flops. Assume that for $t < t_0$, $Q_1 = Q_2 = 0$. The circuit in the digital block is given by

(GATE-EC-2001)



09. In the modulo-6 ripple counter shown in the figure, the output of the 2-input gate is used to clear J-K flip-flops.

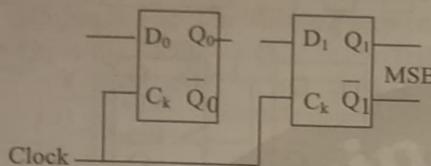
The 2-input gate is (GATE-EC-2004)



(a) a NAND gate
(c) an OR gate

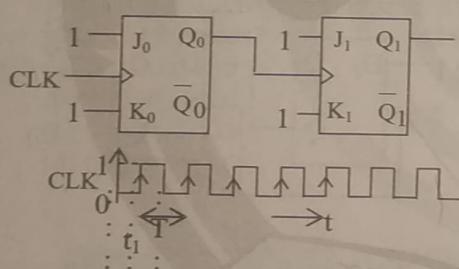
(b) a NOR gate
(d) an AND gate

10. Two D-flip flops, as shown below, are to be connected as a synchronous counter that goes through the following $Q_1 Q_0$ sequence $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$. The inputs D_0 and D_1 respectively should be connected as
(GATE-EC-2006)

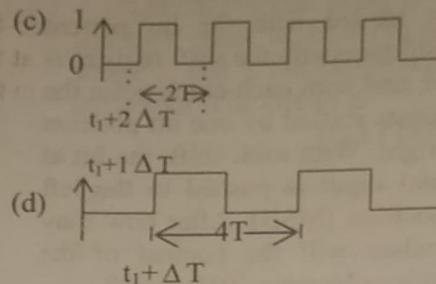
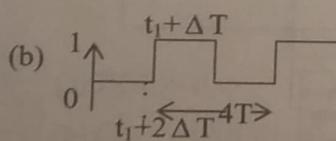
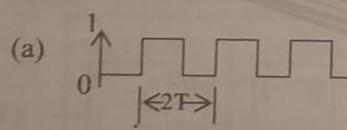


- (a) $\overline{Q_1}$ and Q_0
- (b) $\overline{Q_0}$ and Q_1
- (c) $\overline{Q_1} Q_0$ and $\overline{Q_1} Q_0$
- (d) $\overline{Q_1} \overline{Q_0}$ and $Q_1 Q_0$

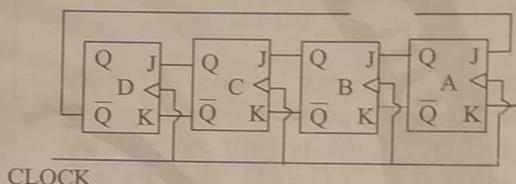
11. For each of the positive edge-triggered J-K flip flop used in the following figure, the propagation delay is ΔT
(GATE-EC-2008)



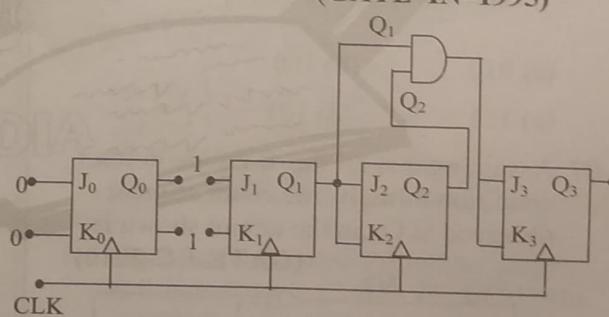
Which of the following waveforms correctly represents the output at Q_1 ?



12. Through what sequence of states does the counter of Fig will go? Assume that all flip-flops are initially reset. What will be the operation of the counter if the flip-flops are made from TTL gates and the input K of flip-flop A is kept open?
(GATE-IN-1992)



13. The below fig shows a sequential circuit with four J-K flip-flops. Generate a table of output ($Q_3 Q_2 Q_1 Q_0$) changes with each clock pulse. Start with $Q_3 Q_2 Q_1 Q_0 = 0001$ and complete a full cycle.
(GATE-IN-1995)

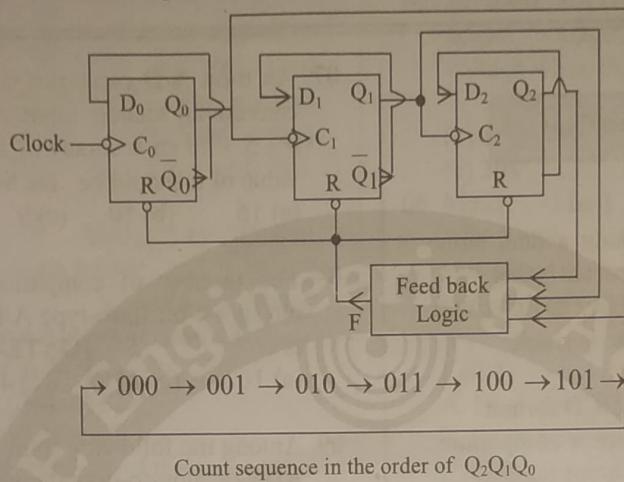


14. A certain JK FF has $t_{pd} = 12$ ns. The largest MOD counter that can be constructed from such FF's and still operate up to 10 MHz is
(ISRO)

- (a) 16
- (b) 256
- (c) 8
- (d) 128

15. A ripple counter using negative edge-triggered D-flip flops is shown in below Fig the flip flops are cleared to '0' by a '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same figure. The correct feedback logic is:

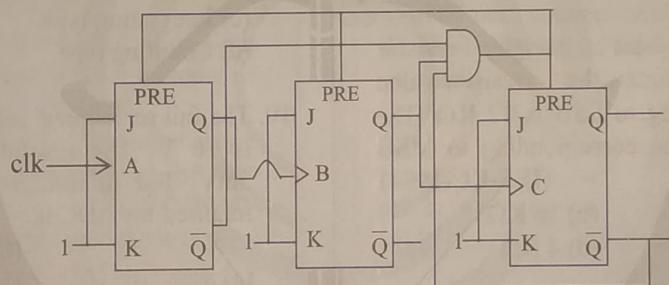
(GATE-EC- 1987)



(a) $F = \overline{Q_2} \overline{Q_1} \overline{Q_0}$ (b) $F = Q_2 \overline{Q}_1 \overline{Q}_0$ (c) $F = \overline{Q}_2 \overline{Q}_1 Q_0$ (d) $F = \overline{Q}_2 \overline{Q}_1 \overline{Q}_0$

16. The ripple counter shown in the figure works as a

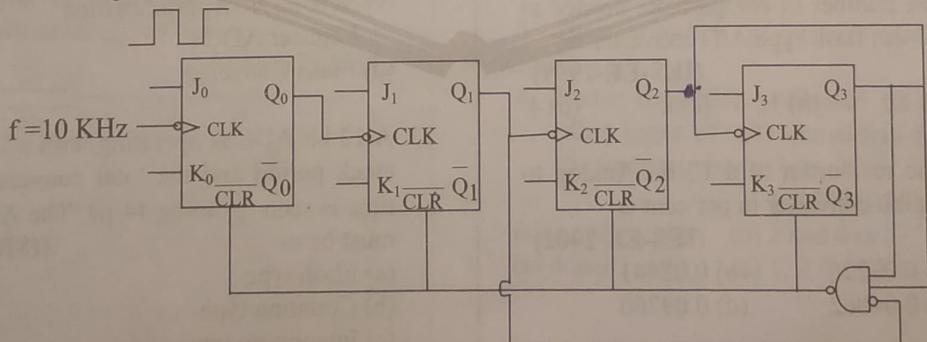
(GATE-EC-1999)



- (a) Mod-3 up counter (b) Mod-5 up counter
 (c) Mod-3 down counter (d) Mod-5 down counter

17. In the figure, the J and K inputs of all the four flip flops are made high. The frequency of the signal at output Y is

(GATE-EC-2000)



- (a) 0.833 KHz (b) 1.0 KHz (c) 0.91 KHz (d) 0.77 KHz

5

A/D & D/A Converters

LEVEL – 1 Questions

01. The advantage of using a dual slope ADC in a digital voltmeter is that
(GATE-EC-1998)
(a) Its conversion time is small
(b) Its accuracy is high
(c) It gives output in BCD format
(d) It does not require a comparator.
02. The minimum number of comparators required to build an 8 bit flash ADC is
(GATE-EC-2000)
(a) 8 (b) 63 (c) 255 (d) 256
03. In a 4-bit weighted-resistor D / A converter, the resistor value corresponding to LSB is $32\text{ K}\Omega$. The resistor value corresponding to MSB will be
(IES-EC-1994)
(a) $32\text{ K}\Omega$ (b) $16\text{ K}\Omega$
(c) $8\text{ K}\Omega$ (d) $4\text{ K}\Omega$
04. Number of comparators required to build a 5-bit Analog to Digital Converter (ADC) is **(IES-EE-1994)**
(a) 5 (b) 11
(c) 21 (d) 31
05. The number of comparators needed in a 4-bit flash-type A/D converter is
(IES-EE-1999)
(a) 32 (b) 15 (c) 8 (d) 4
06. The resolution of a 12 bit Analog to Digital converter in per cent is
(IES-EE-2002)
(a) 0.01220 (b) 0.02441
(c) 0.04882 (d) 0.09760

07. An n-bit A/D converter is required to convert an analog input in the range $0 - 5\text{ V}$ to an accuracy of 10 mV . The value of n should be **(IES-EE-2003)**
(a) 16 (b) 10 (c) 9 (d) 8
08. The number of comparisons carried out in a 4-bit flash-type A/D converter is
(GATE-EE-1994)
(a) 16 (b) 15 (c) 4 (d) 3
09. Among the following four, the slowest ADC (analog-to-digital converter) is
(GATE-EE-2001)
(a) Parallel-comparator (i.e., flash) type
(b) Successive approximation type
(c) Integrating type
(d) Counting type
10. The full scale input voltage to an ADC is 10 V . The resolution required is 5 mV . The minimum number of bits required for ADC is
(GATE-IN-1998)
(a) 8 (b) 10 (c) 11 (d) 12
11. Which of the following ADCs uses over sampling in its operation
(ISRO)
(a) Sigma-delta ADC
(b) Counter ramp converter
(c) Successive Approximation Register ADC
(d) Flash Converter
12. A 12 bit ADC is operating with a $1\text{ }\mu\text{s}$ clock period and the total conversion time is seen to be $14\text{ }\mu\text{s}$. The ADC must be of
(ISRO)
(a) Flash type
(b) Counting type
(c) Integrating type
(d) Successive Approximation type

LEVEL - 2 Questions

01. For a D/A converter, the resolution required is 50 mV and the total maximum input is 10V. The number of bits required is (IES-EC-1991)
 (a) 7 (b) 8 (c) 9 (d) 200

02. Consider the Analog to Digital converters given below:

(IES-EC-1996)

1. Successive Approximation ADC
2. Dual Ramp ADC
3. Counter method ADC
4. Simultaneous ADC

The correct sequence of the ascending order in terms of conversion times of these ADC'S is

- (a) 3,2,4,1 (b) 2,3,4,1
 (c) 2,3,1,4 (d) 3,2,1,4

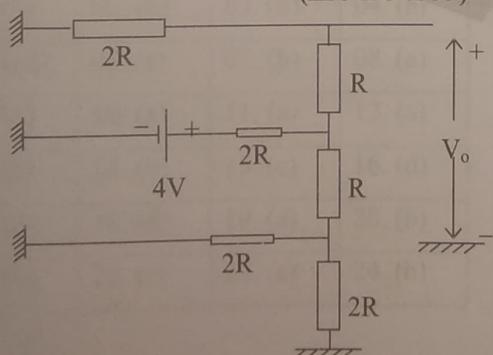
03. **Assertion (A):** The output of an 8-bit A to D converter is 80H for an input of 2.5V.

Reason (R): ADC has an output range of 00 to FFH for an input range of -5V to +5V. (IES-EC-1999)

- (a) Both A and R are true and R is the correct explanation of A.
 (b) Both A & R are true but R is NOT the correct explanation of A
 (c) A is true but R is false
 (d) A is false but R is true.

04. The output voltage V_o with respect to ground of the R-2R ladder network shown in the given figure is

(IES-EC-1999)



- | | |
|--------|--------|
| (a) 1V | (b) 2V |
| (c) 3V | (d) 4V |

05. An 8-bit D/A converter has a full scale output voltage of 20V. The output voltage when the input is 1011011, is
 (IES-EC-2001)

- | | |
|-----------|----------|
| (a) 160mV | (b) 78mV |
| (c) 20V | (d) 17V |

06. Match List-I (Type of N-bit ADC) with List-II (Characteristics) and select the correct answer using the codes given below the lists:

(IES-EC-2004&2009)

List-I

- A. Flash converter
- B. Successive approximation
- C. Counter ramp
- D. Dual slope

List-II

1. Integrating type
2. Fastest converter
3. Maximum conversion time=N bits
4. Uses a DAC in its feedback path

Codes:

A	B	C	D
(a) 1	4	3	2
(b) 1	3	4	2
(c) 2	4	3	1
(d) 2	3	4	1

07. Dual-slope integration type Analog-to-Digital converters provide:

1. Higher speeds compared to all other types of A/D converters
2. Very good accuracy without putting extreme requirements on component stability.
3. Good rejection of power supply hum.
4. Better resolution compared to all other types of A/D converters for the same number of bits.

(IES-EC-2011)

- | | |
|------------------|-------------------|
| (a) 2 and 3 only | (b) 3 and 4 only |
| (c) 4 and 1 only | (d) 1, 2, 3 and 4 |

08. A 10 bit A/D converter is used to digitize an analog signal in the 0 to 5 v range. The maximum peak to peak ripple voltage that can be allowed in the D.C. supply voltage is

(GATE-EE-1993)

- (a) Nearly 100mV
- (b) Nearly 50mV
- (c) Nearly 25mV
- (d) Nearly 5.0mV

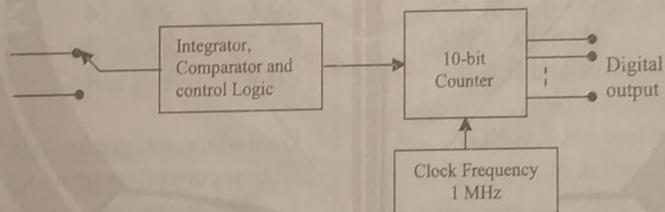
09. For a dual ADC type 3 ½ digit DVM, the reference voltage is 100 mV and the first integration time is set to 300 ms. For some input voltage, the "de integration" period is 370.2ms. The DVM will indicate. (GATE-EE-1999)

- (a) 123.4
- (b) 199.9
- (c) 100.0
- (d) 1.414

12. The simplified block diagram of a 10-bit A/D converter of dual slope integrator type is shown in the Fig. The 10-bit counter at the output is clocked by a 1 MHz clock. Assuming negligible timing overhead for the control logic, the maximum frequency of the analog signal that can be converted using this A/D converter is approximately.

(GATE-EE-2003)

- (a) 2 kHz
- (b) 1 kHz
- (c) 500 Hz
- (d) 250 Hz



Digital Electronics Key Sheet

Chapter – 1 Number systems and Binary codes

LEVEL – 1

01. (b)	02. (d)	03. (b)	04. (b)
05. (a)	06. (b)	07. (d)	08. (b)
09. (d)	10. (c)	11. a&b	12. (c)
13. (c)	14. (c)	15. (d)	16. (c)

LEVEL – 2

01. (b)	02. (a)	03. (c)	04. (a)
05. (a)	06. (a)	07. (c)	

Chapter – 2 Logic Gates, Boolean Algebra & K Maps

LEVEL – 1

01. (b)	02. (b)	03. (b)	04. (a)
05. (all)	06. (c)	07. (b)	08. (a)
09. (d)	10. (a)	11. (a)	12. (a)
13. (d)	14. (b)	15. (c)	16. (d)
17. (c)	18. (d)	19. (a)	20. (b)
21. (b)	22. (c)	23. (c)	24. (b)

LEVEL – 2

01. (c)	02. (a)	03. (c)	04. (b)
05. (b)	06. (c)	07. (c)	08. (a)
09. (b)	10. (b)	11. (c)	

Chapter – 3 Combinational Circuits

LEVEL – 1

01. (d)	02. (d)	03. (d)	04. (d)
05. (c)	06. (d)	07. (a)	08. (c)
09. (b)	10. (d)		

LEVEL – 2

01. (a)	02. (b)	03. (a)	04. (a)
05. (c)	06. (a)	07. (a)	08. (c)
09. (c)	10. (c)	11. (d)	12. (c)
13. (e)	14. (d)		

Chapter - 4

Sequential Circuits

LEVEL - 1

01. 0.5 M Hz	02. (d)	03. (b)	04. (c)
05. (b)	06. (b)	07. (a)	08. (b)
09. (a)			

LEVEL - 2

01. (c)	02. (d)	03. (b)	04. (c)
05. (b)	06. (b)	07. (d)	08. (c)
09. (c)	10. (a)	11. (b)	12. *
13. *	14. (b)	15. (a)	16. (d)
17. (a)			

* Conventional Question

Chapter - 5

A/D & D/A Converters

LEVEL - 1

01. (b)	02. (c)	03. (b)	04. (c)
05. (d)	06. (d)	07. (a)	08. (d)
09. (a)	10. (d)	11. (d)	12. (c)

LEVEL - 2

01. (b)	02. (c)	03. (d)	04. (d)
05. (b)	06. (b)	07. (c)	08. (b)
09. (c)	10. (c)	11. (a)	12. (d)

(a) 10	(b) 50	(c) 50	(d) 10
(a) 80	(b) 50	(c) 50	(d) 20
(a) 50	(b) 10	(c) 10	(d) 50
(a) 50	(b) 20	(c) 20	(d) 10
(a) 00	(b) 00	(c) 00	(d) 00