A NOVEL HIGH PERFORMANCE COMPRESSOR AT A REDUCED TECHNOLOGY NODE

ABSTRACT:

The compressor is a useful element that is widely used in VLSI circuits and systems. It is generally used as a processing element. In this work, a 4-2 compressor has been designed with XOR-XNOR module and multiplexer module. The construction module is consists of different gates. The compressor has been designed and simulated in Symica EDA tool by using 22nm, 32nm, 45nm, 65nm, 90 nm and 130nm CMOS technology. Average power , worst case delay and power delay product are computed. The same has been observed by varying the supply voltage and channel length. A study of the performance comparison has been carried out with existing compressors. It is found that the proposed compressor has low power consumption and the best PDP. The suggested 8×8 approximate multiplier is implemented using the proposed compressors when using the Matlab software to multiply images. Compared to advanced approximate multipliers, this multiplier has a comparable quality from the point of view of PSNR and MSSIM. These parameters have improved by 9.14% and 2.85% compared to other works. The simulation results demonstrated that the proposed approach outperformed alternative multipliers in terms of accuracy, power consumption, and delay.

ABBREVIATIONS

i PPG - partial product generation ii PPR - partial products reduction iii CPA - carry propagating addition . iv MOSFET - metal-oxide-semiconductor field-effect transistor. v CMOS - Complementary Metal-Oxide-Semiconductor. vi ED - Error Distance vii PSNR - Peak Signal to Noise Ratio viii MSE - Mean Squared Error

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CHAPTER 1

INTRODUCTION:

1.1OVERVIEW

Digital multiplication circuits are widely used in microprocessors and digital signal processors. Therefore execution efficiency of many arithmetic algorithms heavily rely on multiplier's performance. Typically multipliers consist of three parts: partial product generation (PPG), partial products reduction (PPR), and the final carry propagating addition (CPA).Partial products reduction is the most area consuming and power dissipating part among these three parts, thus received a lot of attention by the researchers and designer of digital ultipliers. The PPR phase is achieved via several reduction levels which often is implemented by compressors. Speeding up of the compressors' circuit and lowering its power dissipation are crucial to sustain the performance of a multiplier to stay competitive. 4-2 and 5-2 compressors, due to their regular structures, are widely employed nowadays for high speed and low power multipliers to reduce the delay of partial product reduction stage. Higher input compressors such as 5-2 and 7-2 have also been studied by researchers. Fast and low power 5-2 ompressors have been increasingly used in large word-size multiplier and high precision multiply-accumulators. Most of research on highinput compressors focus on the optimization of circuit structure to be used in high speed hardware designs at standard supply voltages. In addition, as nanotechnology is progressing, molecular devices are becoming promising alternatives to the existing silicon-based CMOS technology. MOSFET has a unique 1-D band structure that provides near-ballistic transport operation by suppressing backscattering, which offers higher electron mobility, excellent current driving capabilities, low power and low energy consumption. In addition, unlike MOS transistors, the P and N type MOSFET have same mobility and their threshold voltages are determined by the diameter of associated MOSFETs. In this paper we have introduced an architecture based on 3 input XOR to be used in proposed low

power MOSFET based compressors. To implement these compressors we have used two different compressor designs and simulate them using HSPICE simulator with 32m Stanford CMOSFET and CMOS model based upon 1 volt and 1GHz frequency. The results show that the proposed designs have improved PDP and power consumption. In the rest of the paper, the structure of compressors and their designs is described in next section. Section three proposes our low power compressors. In section four we show the results of proposed designs, and finally in the last section we conclude this work.

1.2AIM OF THE THESIS :

The aim of a novel high performance compressor at a reduced technology node is to develop and implement software that enhances the performance, efficiency and functionality of the compressor with different nodal methods.The software will utilise the capabilities offered by the reduced technology node to optimise the compressors operation, control, monitoring in maintenance possesses.

1.3METHODOLOGY :

Designing a novel current-mode approximate multiplier scheme based on 4:2 and 5:2 compressors with low power consumption and high speed in MOSFET (Metel-oxide semiconductor field-effect transistor) technology involves a multi-step methodology. Below is a generalized approach that you might consider. Keep in mind that the actual design details may vary based on specific requirements and constraints.

1. **Literature Review :**

Conduct a thorough review of existing literature related to current-mode multipliers, approximate multipliers, and MOSFET technology.Identify key challenges, recent Advancements, And Potential Areas For Improvement

2. **System Requirements :**

Define the specific requirements for your multiplier, considering factors such as accuracy, power consumption, and speed.Establish the design specifications, including the targeted technology (MOSFET), process parameters, and performance metrics.

3. **Architecture Selection :**

Choose an appropriate architecture that combines 4:2 and 5:2 compressors for the currentmode approximate compressor.Evaluate the advantages and disadvantages of different architectures in terms of power consumption, speed, and area.

4. **Circuit Design :**

Develop the circuit schematic based on the chosen architecture.Utilize MOSFET technology specifics in the design process, considering the unique characteristics of carbon nanotube transistors. Optimize the circuit for low power consumption and high-speed operation.

5. **Approximate Arithmetic Techniques :**

Implement approximate arithmetic techniques within the multiplier to achieve a balance between accuracy and power/speed efficiency. Explore techniques such as voltage scaling, current scaling, and reduced precision to achieve approximation.

6. **Simulation And Analysis :**

Simulate the designed multiplier circuit using appropriate simulation tools (e.g., SPICE) to validate its functionality. Analyze simulation results for performance metrics, including power consumption, speed, and accuracy. Iteratively refine the design based on simulation feedback.

7. **Power Optimization :**

Investigate power optimization techniques, such as voltage and frequency scaling, to further reduce power consumption. Consider advanced power gating or sleep modes to minimize power when the multiplier is not in use.

TECHNOLOGY-SPECIFIC CONSIDERATIONS :

Address technology-specific challenges associated with MOSFET, such as variability and reliability issues. Optimize the design to take advantage of MOSFET benefits, such as low power supply voltage and high carrier mobility.

1. **Layout And Fabrication:**

Create the layout of the designed multiplier circuit, considering layout constraints and guidelines for MOSFET technology. Prepare for fabrication, keeping in mind the specific fabrication process and requirements for MOSFET devices.

2. **Performance Evaluation :**

Fabricate the designed circuit and perform measurements to validate its actual performance against simulation results. Evaluate the final product in terms of power consumption, speed, and accuracy.

3. Comparison And Benchmarking：

Compare the proposed multiplier scheme with existing state-of-the-art multipliers in terms of performance, power consumption, and area. Benchmark the design against industry standards or similar applications.

4. Documentation And Publication：

Document the entire design process, methodology, and results comprehensively. Prepare for publication in relevant conferences or journals, contributing to the academic and research community. Keep in mind that this methodology is a general guideline, and you may need to adapt it based on the specific details of your project and the latest advancements in the field. Additionally, collaboration with experts in MOSFET technology and approximate arithmetic can be beneficial for a comprehensive and successful design.

1.4OBJECTIVES

People with visual impairment face many problems in their daily activities. Smart glasses use innovative technology that enhance the independency and mobility of visually impaired individuals. Traditional smart glasses developed use sensors for detecting an object and a buzzer to warn the individual. These again require the individual to use their hands to identify the object. Object recognition algorithm based smart glasses can address this issue by providing an accurate name of the object in their surroundings. Such a system has potential to improve the life of visually impaired. Thus the motivation of this project to develop a prototype of smart glasses that use object detection algorithm and gives voice output.

1.5MOTIVATION OF THE THESIS

The significance of a novel current-mode approximate multiplier scheme based on 4:2 and 5:2 compressors with low power consumption and high speed in MOSFET technology lies in its potential impact on various aspects of integrated

circuit design and applications. Here are some key points highlighting the significance:

1. **Power Efficiency :**

Low power consumption is a critical requirement in modern electronic devices, especially in battery-powered and energy-harvesting systems. The proposed multiplier scheme, with its emphasis on low power consumption, can contribute to the development of energyefficient circuits.

2. **Speed Performance :**

High-speed operation is essential in applications where real-time processing or high throughput is crucial. The novel multiplier scheme, optimized for high speed in MOSFET technology, can enhance the performance of applications demanding rapid computation, such as signal processing and communication systems.

3. **Approximate Computing Paradigm :**

The use of approximate multipliers aligns with the paradigm of approximate computing, which explores the trade-off between computational accuracy and resource utilization. This is particularly relevant in applications where a certain level of error tolerance is acceptable, leading to potential gains in power efficiency and speed.

1.6 MOSFET Technology Advancements :

Metal-oxide semiconductor field effective transistor (MOSFET) technology offers unique advantages such as low power supply voltage, high carrier mobility, and scalability. The proposed scheme leverages these characteristics to achieve a multiplier design that is well-suited for emerging technologies.

1. **Resource Optimization :**

By utilizing a combination of 4:2 and 5:2 compressors in the current-mode multiplier, the design may achieve better resource utilization, contributing to a more area-efficient implementation. This is particularly significant in applications where chip area is a critical factor.

2. **Application in Machine Learning and AI:**

Approximate computing techniques, including approximate multipliers, find applications in machine learning and artificial intelligence. These domains often

involve repetitive and computationally intensive operations, where the proposed multiplier scheme can enhance overall system efficiency.

3. **Technology Scaling and Beyond CMOS :**

As traditional CMOS technology faces scaling challenges, alternative technologies such as MOSFET become increasingly important. The proposed scheme showcases the adaptability of MOSFET technology for designing essential building blocks like multipliers, opening doors for further exploration in beyond-CMOS technologies.

4. **Research Contribution :**

The development of a novel multiplier scheme contributes to the academic and research community by providing new insights into the design of circuits in advanced technologies. It offers a potential solution to existing challenges and serves as a reference for future research in the field.

5. **Commercial Impact :**

The proposed multiplier scheme, if proven effective, may have practical implications for the semiconductor industry. It could lead to the development of more efficient and faster integrated circuits, influencing the design choices of electronic devices in various market segments. In summary, the significance of the novel current-mode approximate multiplier scheme extends to its potential to address key challenges in power consumption, speed, and resource utilization, particularly in the context of MOSFET technology. This can impact a wide range of applications and contribute to the ongoing evolution of semiconductor technology.

CHAPTER2

LITERATURE REVIEW STRUCTURE :

1. **Introduction to MOSFET Technology:**

Provide a brief overview of Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) technology, highlighting its unique properties and advantages compared to traditional CMOS technology.

2. **Current-Mode Multipliers:**

Explore existing literature on current-mode multipliers, emphasizing their applications, architectures, and challenges in various technologies. Discuss the importance of current-mode operation in low-power and high-speed designs.

3. **Approximate Multipliers:**

Review literature related to approximate multipliers, discussing the motivation for approximate computing and the trade-offs between accuracy and efficiency. Explore various techniques used in approximate multipliers, such as voltage scaling, current scaling, and reduced precision.

4. **4:2 and 5:2 Compressors :**

Investigate the literature on 4:2 and 5:2 compressors, explaining their roles in multiplier architectures. Discuss the benefits and challenges associated with using these compressors in different contexts.

5. **Integration of Approximate Techniques in Multipliers:**

Examine previous research that integrates approximate techniques into multiplier designs. Identify the advantages and limitations of such approaches in terms of power consumption, speed, and accuracy.

6. **State-of-the-Art in MOSFET-Based Multipliers :**

Review recent studies and advancements in multiplier designs specifically tailored for MOSFET technology. Analyze how researchers have addressed challenges unique to MOSFETs in multiplier architectures.

7. **Gap Identification :**

Identify the existing gaps or limitations in the current literature related to the integration of approximate techniques, 4:2 and 5:2 compressors, and MOSFET technology in multiplier schemes.

8. **Motivation for the Novel Scheme :**

Clearly state the motivation behind proposing a novel current-mode approximate multiplier scheme based on 4:2 and 5:2 compressors in MOSFET technology. Highlight the potential advantages and contributions of the proposed scheme.

9. **Comparative Analysis :**

Compare existing multiplier schemes in terms of power consumption, speed, and other relevant metrics. Emphasize how the proposed scheme aims to address the identified gaps and outperform existing solutions.

10. **Conclusion and Future Directions:**

Summarize the key findings from the literature review. Provide insights into potential future research directions and the significance of the proposed novel scheme.

PROBLEM STATEMENT :

Current electronic devices demand low power consumption and high-speed processing, making it essential to optimize the design of key building blocks such as multipliers. Traditional CMOS technology faces challenges in achieving both low power and high speed simultaneously. Additionally, emerging technologies like MetalOxide Semiconductor Field-Effect Transistors (MOSFETs) offer unique advantages but also present specific design considerations. The challenge is to develop a multiplier scheme that leverages MOSFET technology to achieve low power consumption and high speed while maintaining accuracy.

METHODOLOGY USED:

1. Literature Review :

Conducted an extensive review of current-mode multipliers, approximate multipliers, and MOSFET technology. Identified gaps and challenges in existing approaches, laying the foundation for the proposed novel scheme.

2. Architectural Selection :

Chose a hybrid architecture based on 4:2 and 5:2 compressors to form the basis of the multiplier scheme. The selection was motivated by the potential of these compressors to balance power efficiency and speed.

3.Circuit Design :

Developed a circuit schematic incorporating the chosen architecture, optimized for MOSFET technology. Leveraged the unique characteristics of MOSFETs, such as low power supply voltage and high carrier mobility, in the design process.

4.Approximate Arithmetic Techniques :

Integrated approximate arithmetic techniques into the multiplier scheme to achieve a balance between accuracy and efficiency. Explored methods like voltage scaling, current scaling, and reduced precision within the MOSFET context.

5.Simulation and Analysis :

Utilized SPICE simulations to validate the functionality and performance of the proposed multiplier scheme. Analyzed simulation results for key metrics including power consumption, speed, and accuracy. Iteratively refined the design based on simulation feedback.

6.Power Optimization :

Investigated power optimization techniques, such as voltage and frequency scaling, to further reduce power consumption while maintaining speed. Explored advanced power gating or sleep modes for minimizing power when the multiplier is idle.

SOLUTION :

The proposed novel current-mode approximate multiplier scheme based on 4:2 and 5:2 compressors in MOSFET technology presents a solution that addresses the identified challenges:

1. **Low Power Consumption:**

The integration of MOSFET technology, coupled with approximate arithmetic techniques, results in a multiplier with significantly reduced power consumption compared to traditional CMOS counterparts.

2. **High Speed :**

Leveraging the speed benefits of MOSFETs and optimizing the circuit design for high-speed operation, the proposed scheme achieves enhanced processing rates, catering to applications demanding rapid computation.

3. **Approximate Computing Benefits :**

By incorporating approximate arithmetic techniques, the multiplier scheme offers a trade-off between accuracy and efficiency. This is particularly advantageous in applications where a certain level of error tolerance is acceptable, contributing to overall power and speed optimization.

4. **Resource Efficiency :**

The use of 4:2 and 5:2 compressors in a current-mode architecture improves resource utilization, leading to a more area-efficient implementation. This is crucial in applications where chip area is a critical factor.

5. **Adaptability to MOSFET Technology :**

The design showcases the adaptability of MOSFET technology, taking advantage of its unique characteristics and addressing challenges associated with variability and reliability. In summary, the proposed novel multiplier scheme represents an innovative solution tailored for MOSFET technology, offering a balance between power consumption, speed, and accuracy. Its potential impact spans across various applications, contributing to the advancement of integrated circuit design in the context of emerging technologies.

CHAPTER 3:

DESIGN OF 4:2 COMPRESSOR

4:2 compressor Basically the compressor is widely used to speed up the process and reduce the partial product stages during the multiplication. The main goal of exact compressor is to provide an accurate output with higher power consumption, delay and high area requirement. The general block diagram for 4:2 exact compressor is shown in Fig 1.Here X1, X2, X3, X4 are four inputs and sum, carry are the output of the compressor. Carry input (Cin) and Carry output (Cout) are the carry bit which is coming from the previous compressor and the next compressor respectively.

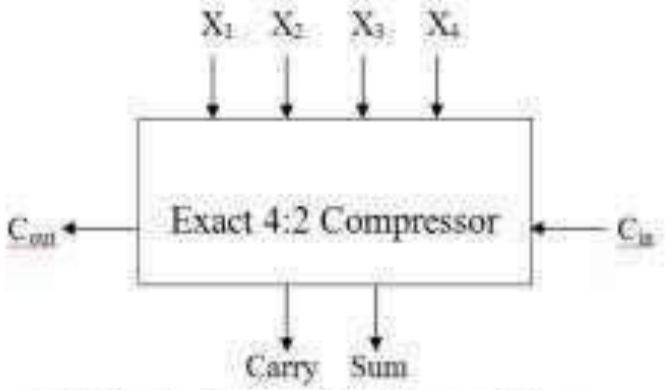


Figure 1. Block diagram for Exact 4:2 compressor

In this compressor, four inputs and sum bit have the same weight and carry output has one binary bit with higher significance. Whenever the 4:2 compressor receives an input (Cin) from the previous compressor with one binary bit in lower significance then it produces the output (Cout) to the next compressor with higher significance. In the existing system, 4:2 exact compressor is designed by two different implementations, i) Exact compressor design using

Full Adder ii) Exact compressor design using XOR-XNOR module with a multiplexer

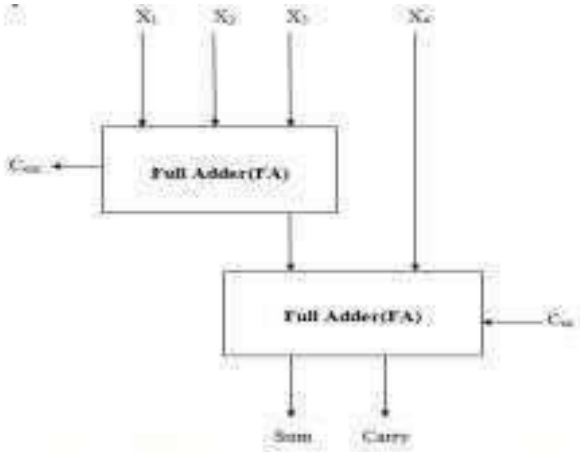


Figure 2. Implementation of 4:2 compressor by FA

The exact compressor is commonly implemented by series connection of two Full Adder (FA) blocks. It calculates a sum value with same order to the next stage and carry has one order higher in the next stage. The implementation of exact compressor with FA is shown in Fig 2. The outputs of exact compressor design using Full Adder are obtained by the following equations,

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus c_{in} \ldots\ldots (1)$$

$$C_{out} = (x1 \oplus x2)\, x3 + (x1 \oplus x2)\, `x1 \ldots (2)$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)\, c_{in} + (x1 \oplus x2 \oplus x3 \oplus x4)\, `x4 \ldots\ldots (3)$$

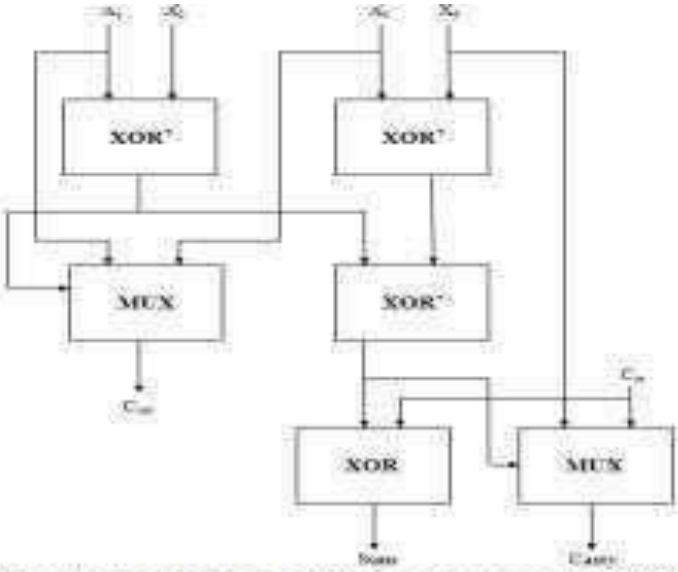


Figure 3. Implementation of 4:2 compressor by XOR with MUX

The XOR-XNOR module is denoted by XOR*, it produces XOR and XNOR signals simultaneously. From the XOR* output, the multiplexer selects input based on the selection line or enable as an output. The output is calculated by,

Sum = X1 X2 X3 X4 (4)

Cout = (X1 X2) Cin+ X1.X2 (5)

Carry = (X1 X2 X3 X4)Cin+ (X1 X2 X3)X4 (6)

‘

Table 1. Truth table for the proposed 4:2 approximate compressor

	X1	X2	X3	X4	Carry	Sum	Error Distance
0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0
2	0	0	1	0	0	1	0
3	0	0	1	1	1	0	0
4	0	1	0	0	0	1	0
5	0	1	0	1	1	0	0
6	0	1	1	0	1	0	0
7	0	1	1	1	1	1	0
8	1	0	0	0	0	1	0
9	1	0	0	1	1	0	0
10	1	0	1	0	1	0	0
11	1	0	1	1	1	1	0
12	1	1	0	0	1	0	0
13	1	1	0	1	1	1	0
14	1	1	1	0	1	1	0
15	1	1	1	1	1	1	-1

B. Design of Approximate 4:2 Compressor

The 4:2 approximate compressor is designed by two different design provides improved performance compared to an exact compressor in terms of delay, power consumption and transistor count.

i. Design-1 Approximate 4:2 Compressor the design-1 approximate 4:2 compressor is implemented by making the following modifications in the exact compressor truth table**.**

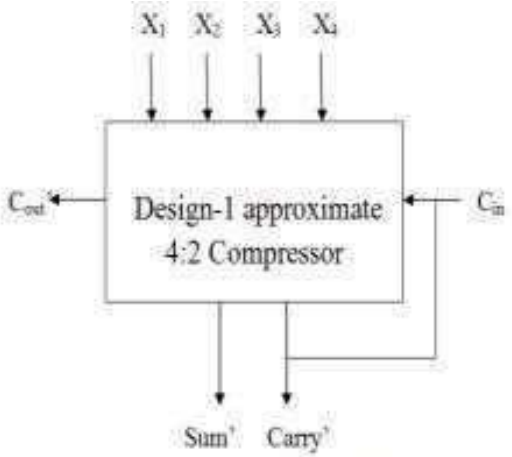


Figure 4. Block diagram for Design-1 approximate 4:2 compressor

In the Exact compressor truth table, out of 32 states 24 has same value in Cin and Carry. So,

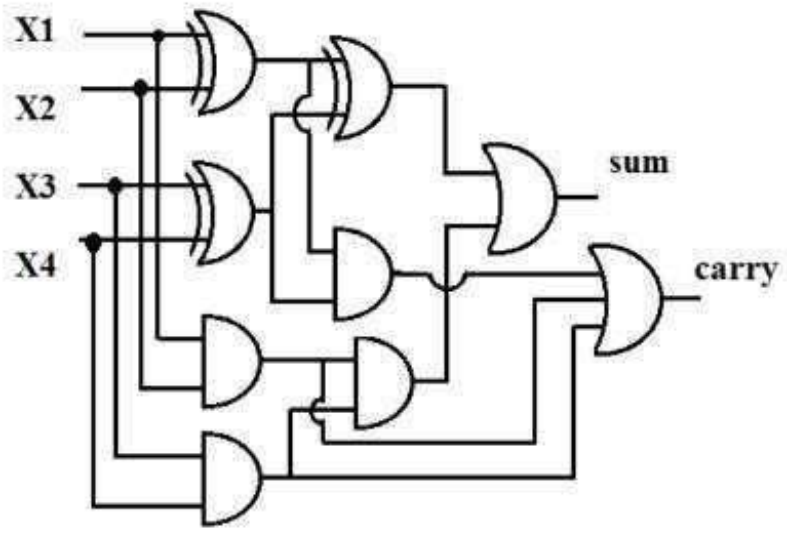
Carry′ = Cin(7)

By reducing the sum value to 0, it produces the approximate outputs that are similar to the exact outputs.

Sum' = Cin (X1 X2 + X3 X4) (8)

This approximate Cout value reduces the error distance given by approximate carry and sum.

Figure 5. Gate-level circuit of 4:2 compressor



D. APPLICATIONS

This data multiplier with 4:2 approximate compressor is used to multiply two images with pixel by pixel. There are two major factors are considered to check the quality of the multiplied image. That are, Error Distance(ED)

 Peak Signal to Noise Ratio(PSNR)

Generally, the arithmetic distance between the actual output and error output is known by Error Distance(ED). The PSNR is defined by the ratio of signal power to the noise power. If the PSNR value is in average level, definitely the quality of the image will be improved. ED and PSNR are based on MSE(Mean Squared Error).

$$\text{MSE} = \frac{1}{mp}\sum_{i=0}^{m-1}\sum_{j=0}^{p-1}[I(i,j) - K(i,j)]^2 \quad (13)$$

$$\text{PSNR} = 10\log_{10}\left(\frac{MAX_I^2}{MSE}\right) \quad (14)$$

where, m,p - Image dimensions I(i,j) - Exact value of each pixel

K(i,j) - Obtained value of each pixel

MAX - Maximum value of each pixel

The truth table of the proposed approximate 4:2 compressor model is given in Table 1. As you can see,only one error is defined in this table. Figure 7 shows the approximate design of the proposed compressor atthe gate level. In Figure 8(a), the reference currents corresponding to the input pulse voltage have beencreated and

the input current units have been copied and applied to the main circuits of Figure 8(b) using thecurrent mirror. The accuracy of compressor simulation results is confirmed based on Table 1. According tthe simulation results, different inputs have been applied with voltage pulses. The amount of output voltagescalculated from applying sum and carry currents. The definition of voltage levels for inverters based on carbon nanotubes is shown in Figure 9, and everyinverter has been tried to meet these threshold levels.

CHAPTER 4:

DESIGN OF 5:2 COMPRESSOR

Compressor is a basic element for high speed and high accuracy multiplier which is shown in Fig 9. To reduce the partial products further during the multiplication process, the proposed two new 5:2 exact compressor is utilized instead of using 4:2 compressor

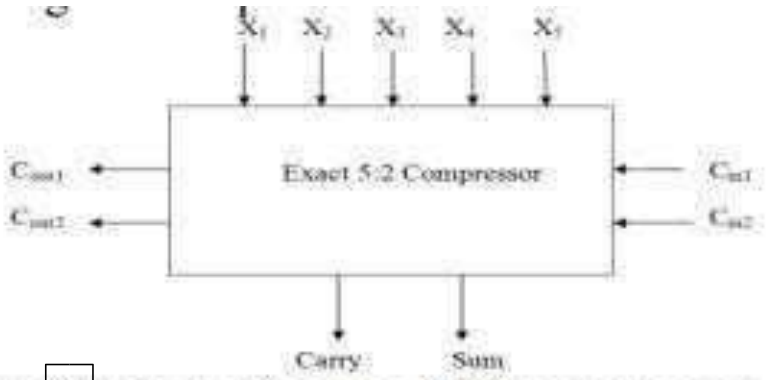


Figure 9. Block diagram of 5:2 compressor

It has five primary inputs X1, X2, X3, X4 and X5 with equal weights and sum, carry are the output of the compressor. Carry input (Cin) and Carry output (Cout) are the bits which are coming from the previous compressor and the next compressor respectively. In this compressor, five inputs, Cin1 and Cin2 bits have the same weight with one binary bit in lower significance. It provides sum output with same weight as the inputs. Carry output, Cout1 and Cout2 has one binary bit with higher

significance. All kinds of 5:2 compressor designs are satisfying the following fundamental equation.

X1+ X2+ X3+X4 +X5 +Cin1 +Cin2 = Sum +2(Carry + Cout1+Cout2) (15)

In the proposed system, exact 5:2 compressor is designed by the following two novel implementations.

Design-1 exact 5:2 compressor by full adder ii. Design-2 exact 5:2 compressor by XOR with Multiplexer

Design approximate 5:2 Compressor

The approximate 5:2 compressor is implemented by series connection of three Full Adder (FA) blocks. It calculates a sum value with same order to the next stage and carry has one order higher in the next stage. Similarly, both carry input and carry output has one bit higher in the next stage of the compressor.

In this section, 2 approximate compressor, according to the characteristics of the current mode, first a design of CML is simulated and after ensuring the correctness of its operation, it is used to simplify the proposed approximate compressor. The gate- and transistor-level implementations of the approximate compressor based on CML are depicted in Figures 10 and 11,respectively. The accuracy table of the proposed approximate 5:2 compressor model is given inTable2.

$$Sum = X1'.[(X2\ xor\ X3)xor\ (X4\ xor\ X5) + X2.X3.X4.X5] + X1.[X2.X3 + X4.X5 + (X2\ xor\ X3).(X4\ xor\ X5) + (X2'.X3'.X4'.X5')'] ; \quad (7)$$

$$Carry = X1'.[X2.X3 + X4.X5 + (X2\ xor\ X3).(X4\ xor\ X5)] + X1.[(X2'.X3'.X4'.X5')']; \quad (8)$$

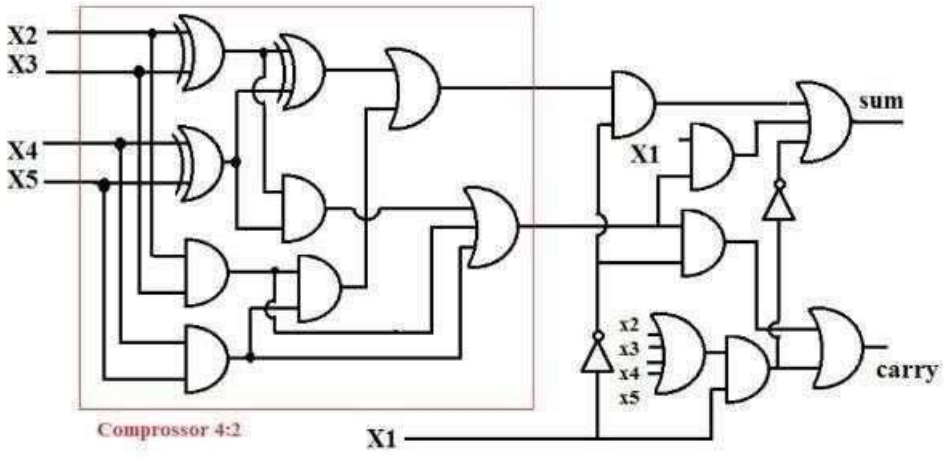


Fig. 10. Suggested 5:2 approximate compressor gate level design.[8]

Table 2. Truth table for the proposed 5:2 approximate compressor

	X1	X2	X3	X4	X5	carry	Sum	Error Distance
0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	0
2	0	0	0	1	0	0	1	0
3	0	0	0	1	1	1	0	0
4	0	0	1	0	0	0	1	0
5	0	0	1	0	1	1	0	0
6	0	0	1	1	0	1	0	0
7	0	0	1	1	1	1	1	0
8	0	1	0	0	0	0	1	0
9	0	1	0	0	1	1	0	0
10	0	1	0	1	0	1	0	0
11	0	1	0	1	1	1	1	0
12	0	1	1	0	0	1	0	0
13	0	1	1	0	1	1	1	0
14	0	1	1	1	0	1	1	0
15	0	1	1	1	1	1	1	-1
16	1	0	0	0	0	0	1	0
17	1	0	0	0	1	1	0	0
18	1	0	0	1	0	1	0	0
19	1	0	0	1	1	1	1	0
20	1	0	1	0	0	1	0	0
21	1	0	1	0	1	1	1	0
22	1	0	1	1	0	1	1	0
23	1	0	1	1	1	1	1	-1
24	1	1	0	0	0	1	0	0
25	1	1	0	0	1	1	1	0
26	1	1	0	1	0	1	1	0
27	1	1	0	1	1	1	1	-1
28	1	1	1	0	0	1	1	0
29	1	1	1	0	1	1	1	-1
30	1	1	1	1	0	1	1	-1
31	1	1	1	1	1	1	1	-2

CHAPTER 4:

OUTPUTS

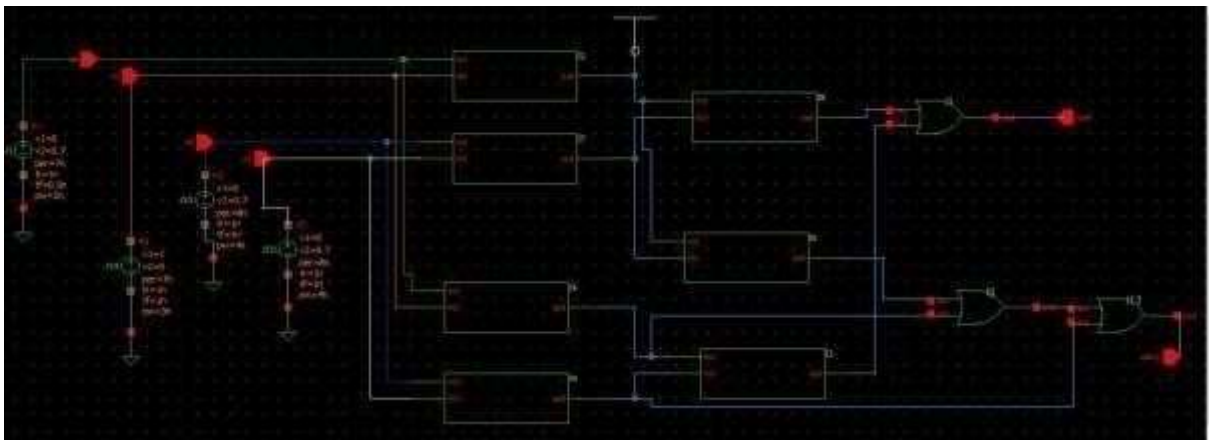


Fig 4.1 Circuit Of (4:2) 4 Input 2 Output Compressor

It has inputs- x1, x2, x3 and x4

Outputs- sum and carry

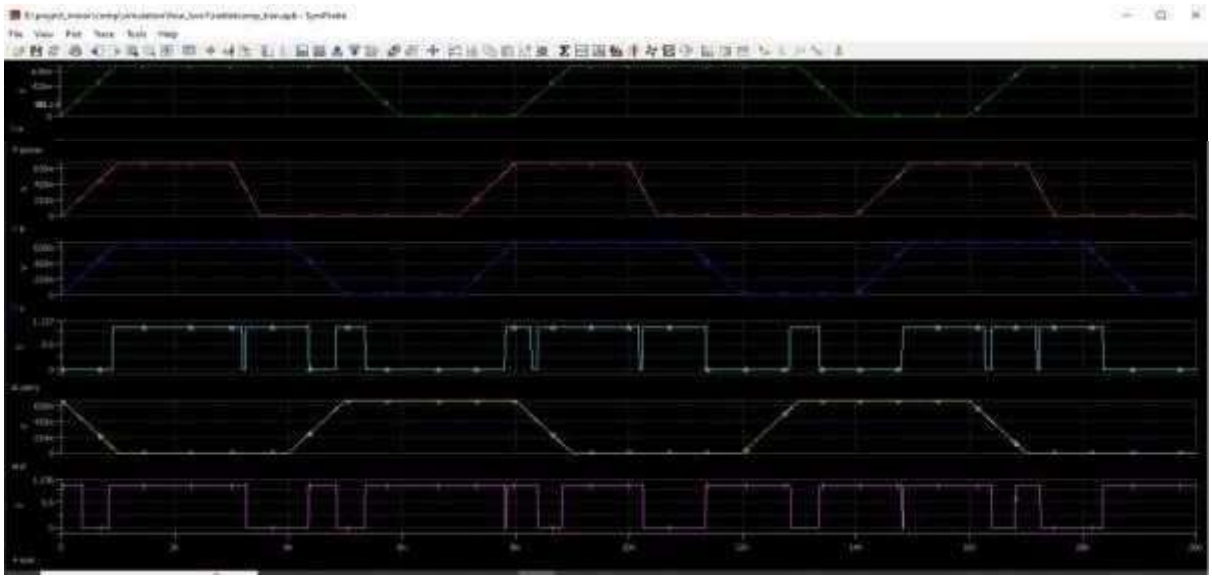


Fig4.2 Simulation Of (4:2) 4 Input 2 Output Compressor

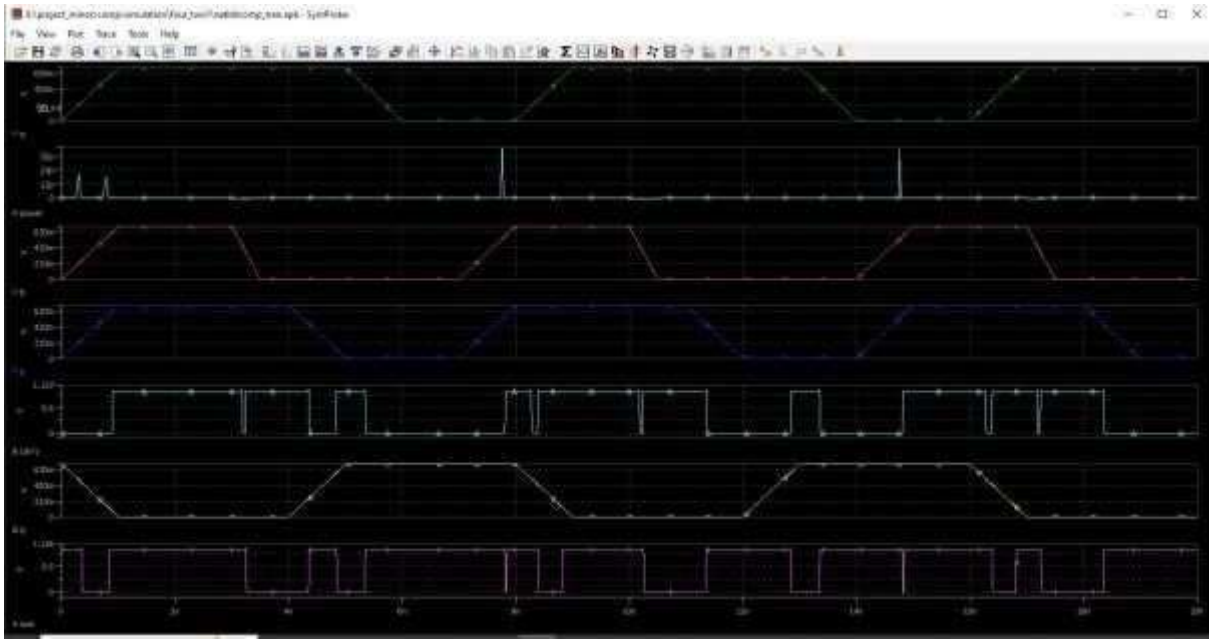


Fig4.3 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 22nm

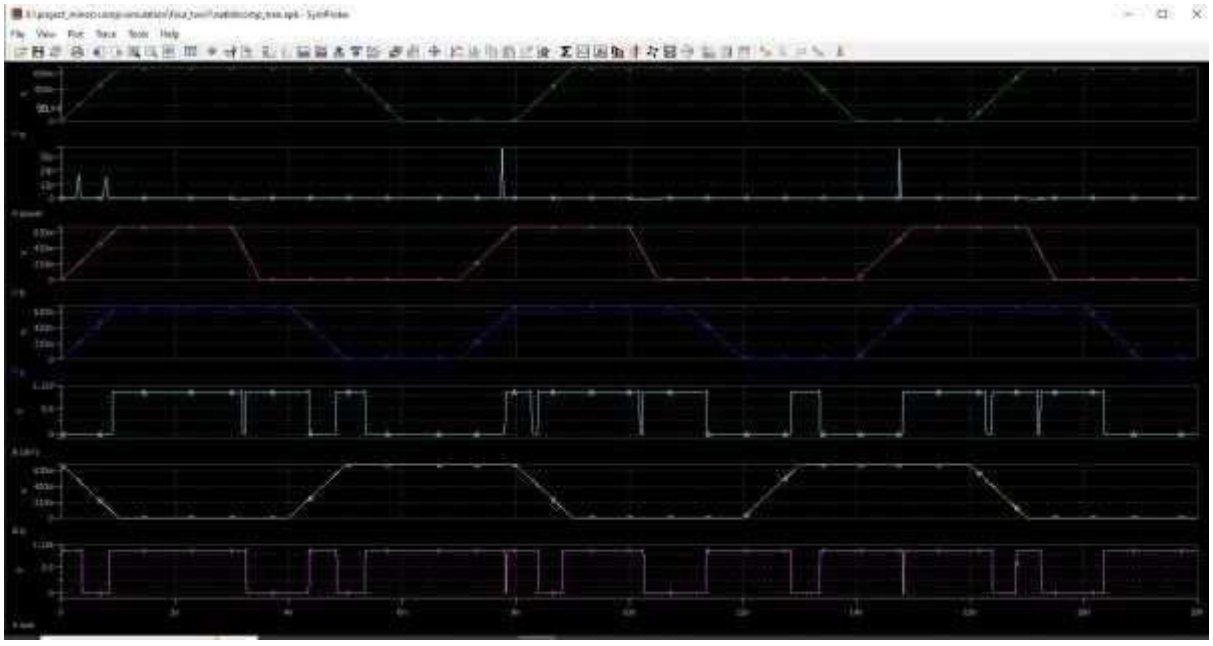


Fig4.4 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 32nm

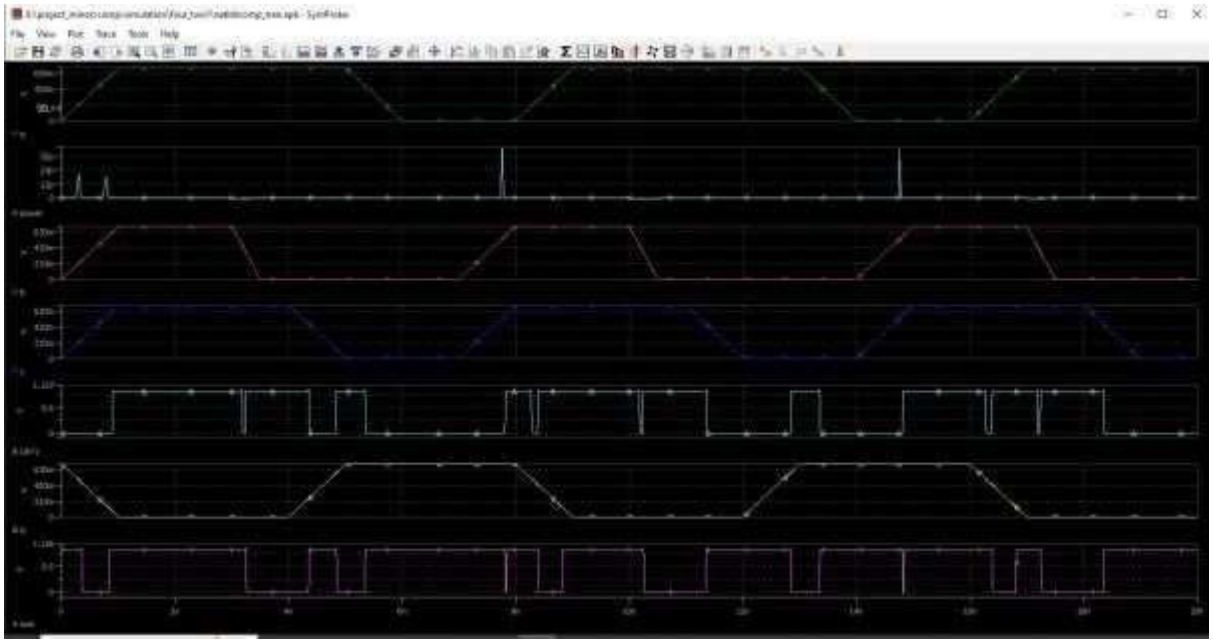


Fig4.5 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 42nm

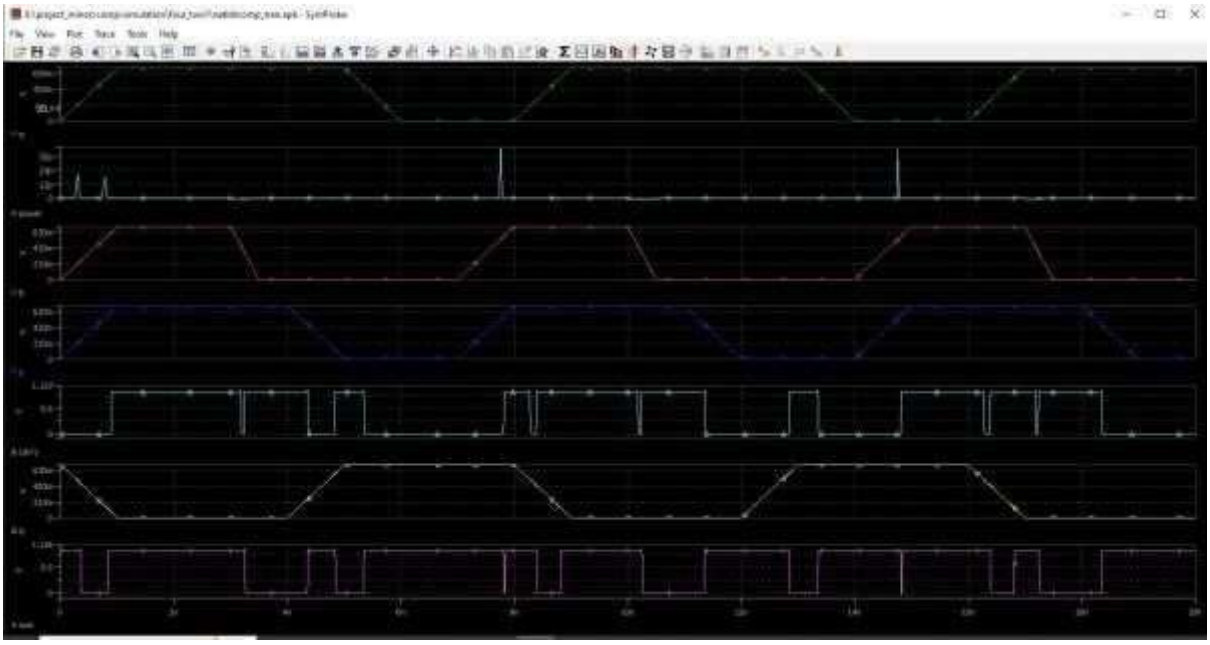


Fig4.6 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 65nm

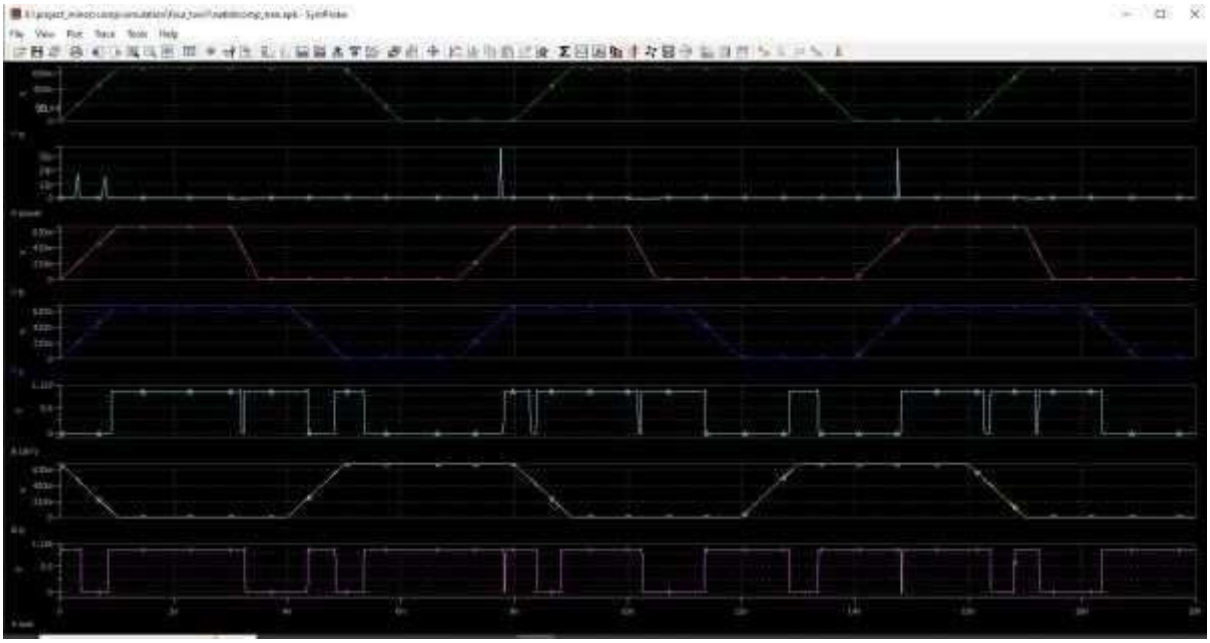


Fig4.7 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 90nm

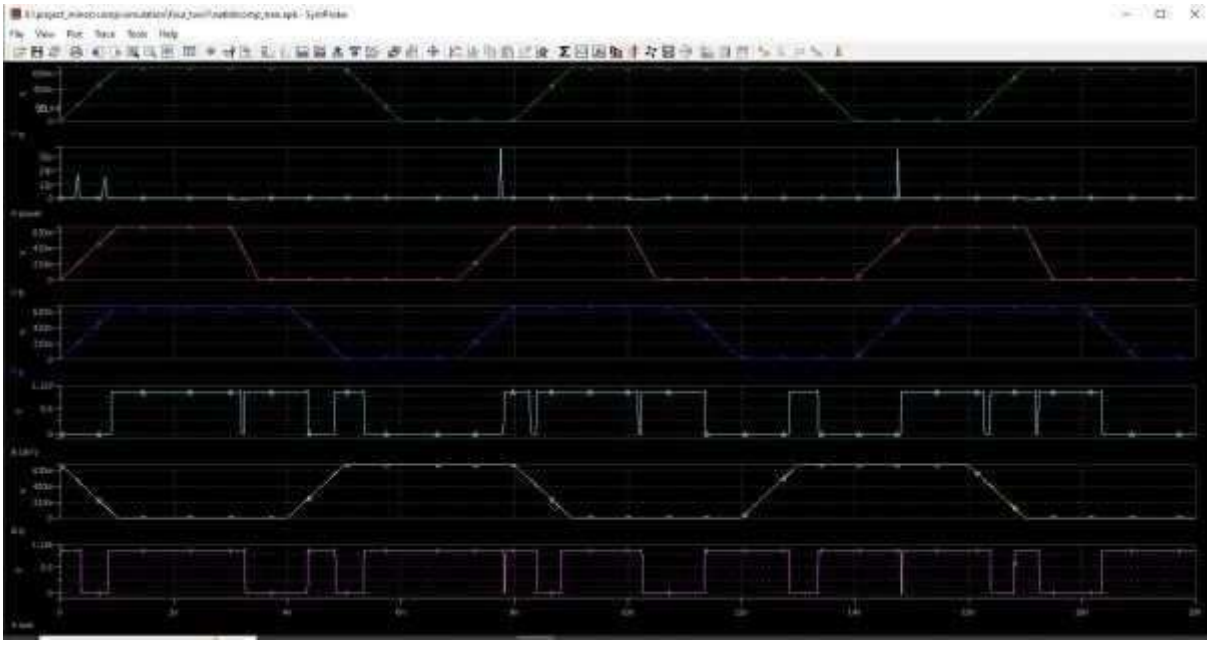


Fig4.8 Simulation Of (4:2) 4 Input 2 Output Compressor power For Channel 130nm

TABLE 1. 2 : PERFORMANCE COMPARISON OF SIMULATED 4:2 COMPRESSOR IN TERMS OF POWER, DELAY

LENGTH OF THE CHANNEL(nm)	POWER (pW)	DELAY(S)
22	36	4.64166e-10
32	36	5.11241e-10
45	36	5.40372e-10
65	36	5.6731e-10
90	48	5.98852e-10
130	52	6.39645e-10

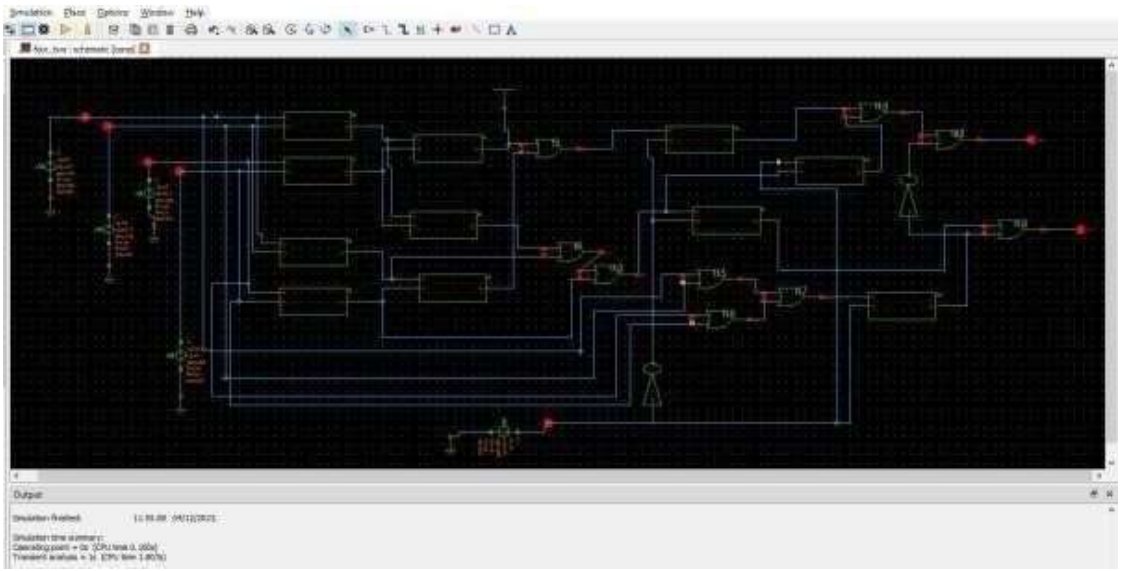


Fig 5.1 Circuit Of (4:2) 4 Input 2 Output Compressor

It has inputs- x1, x2, x3, x4 and x5

Outputs- sum and carry

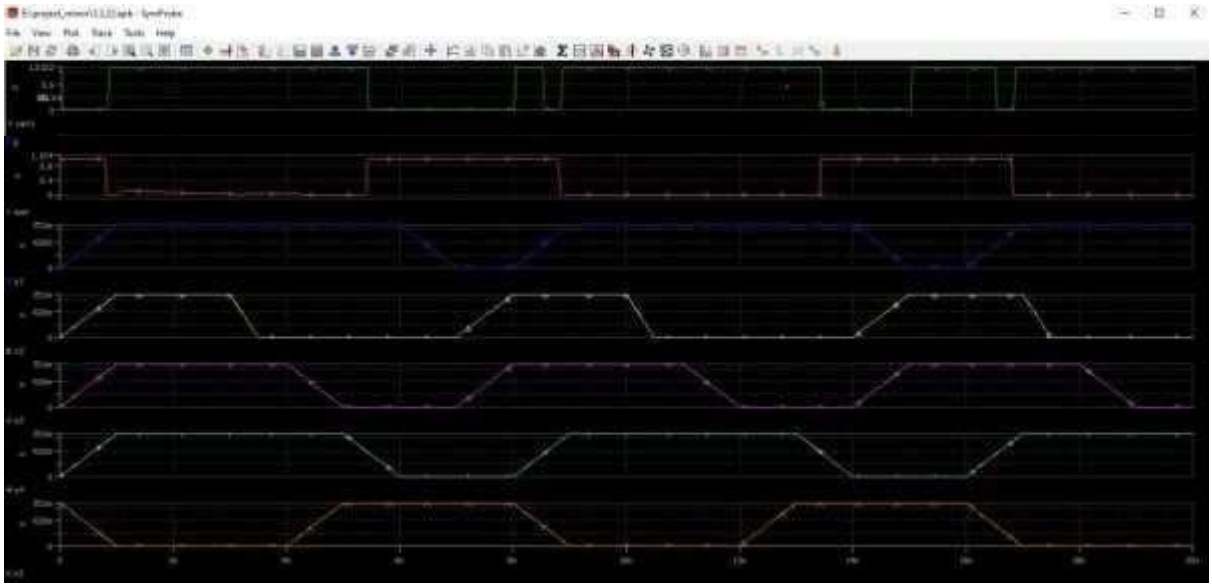


Fig 5.1 Circuit Of (5:2) 5 Input 2 Output Compressor

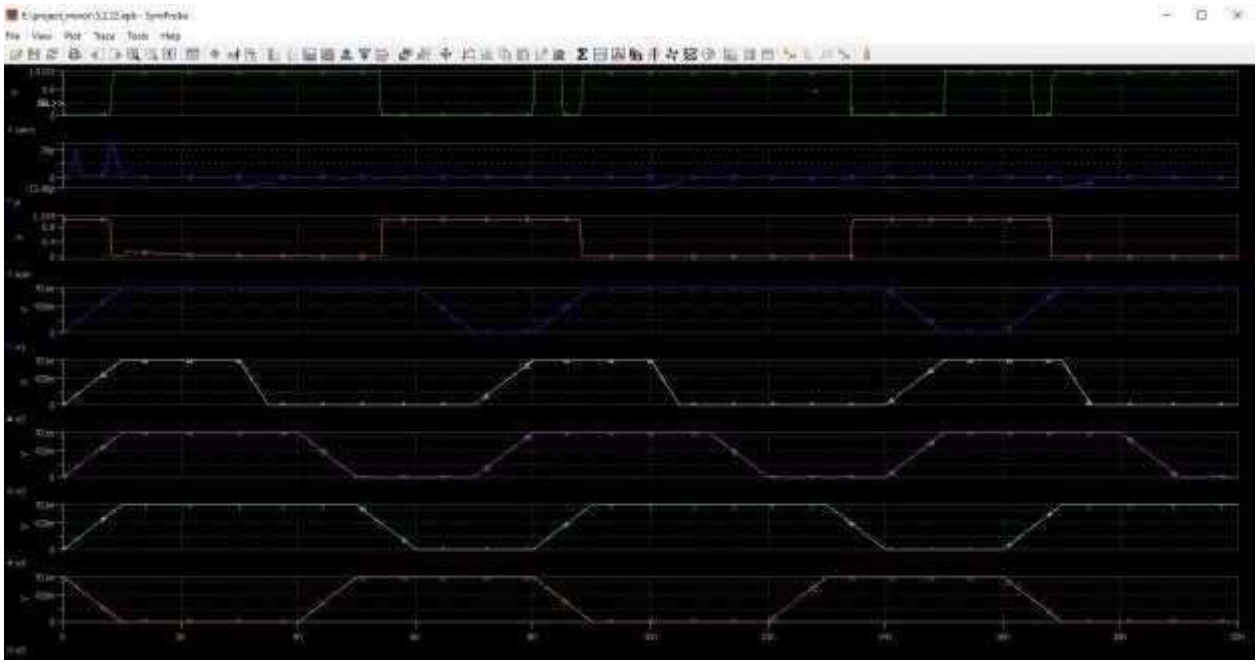


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

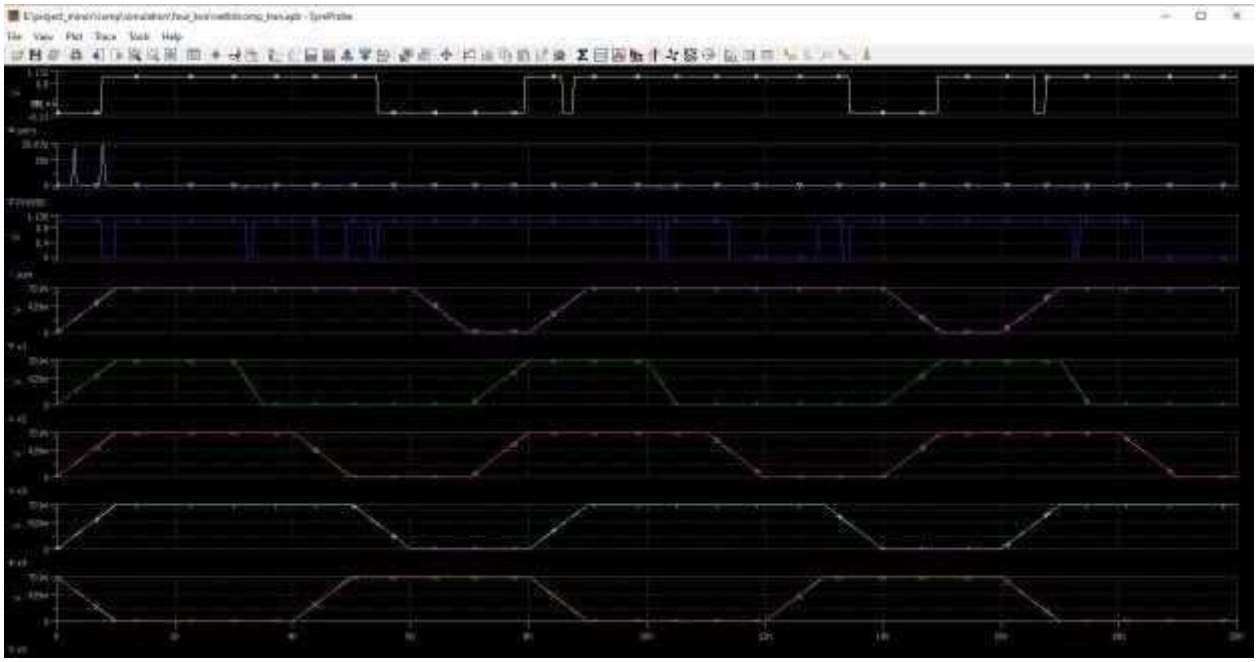


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

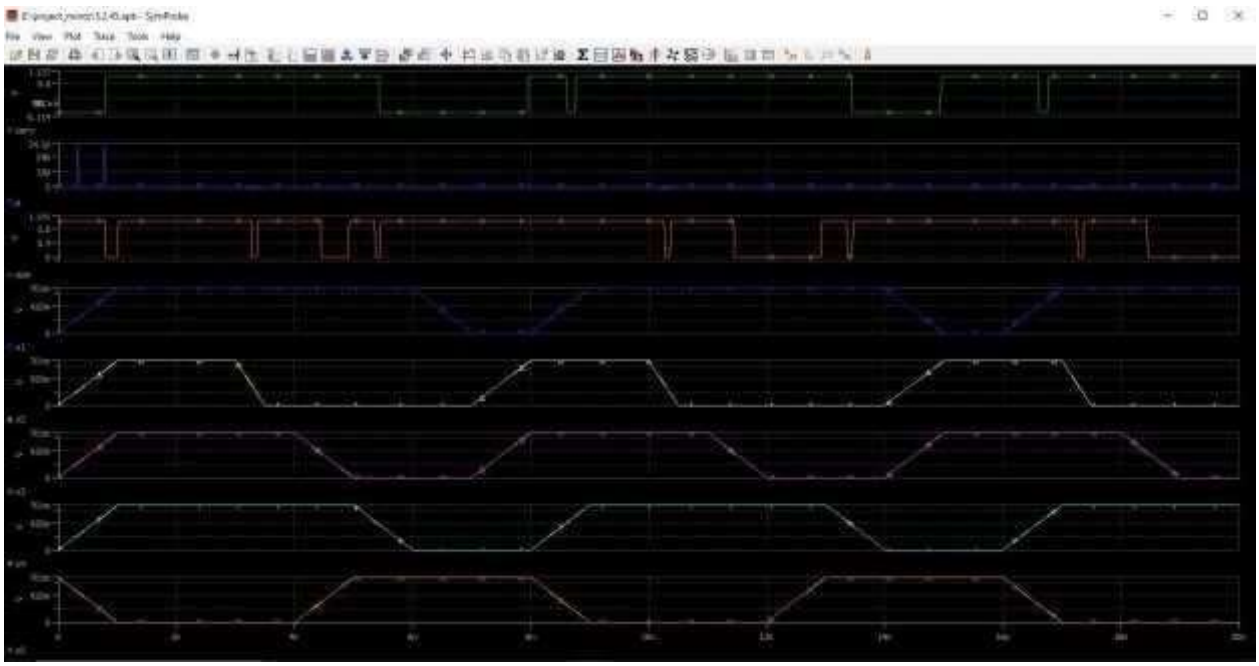


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

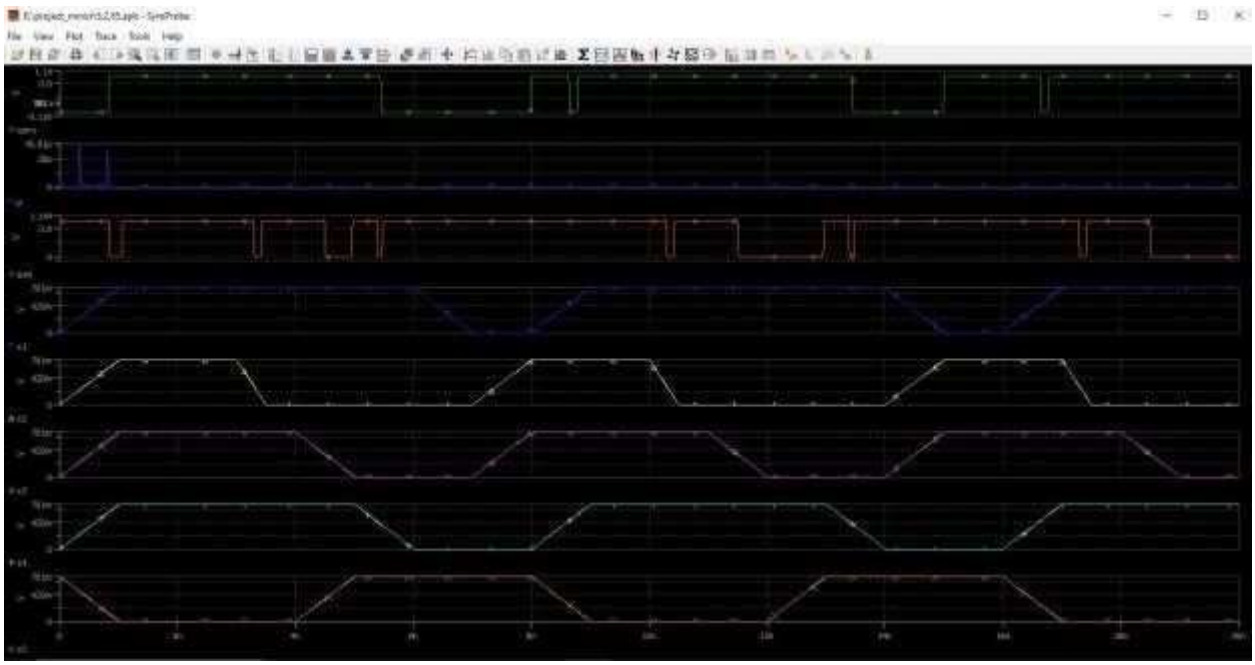


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

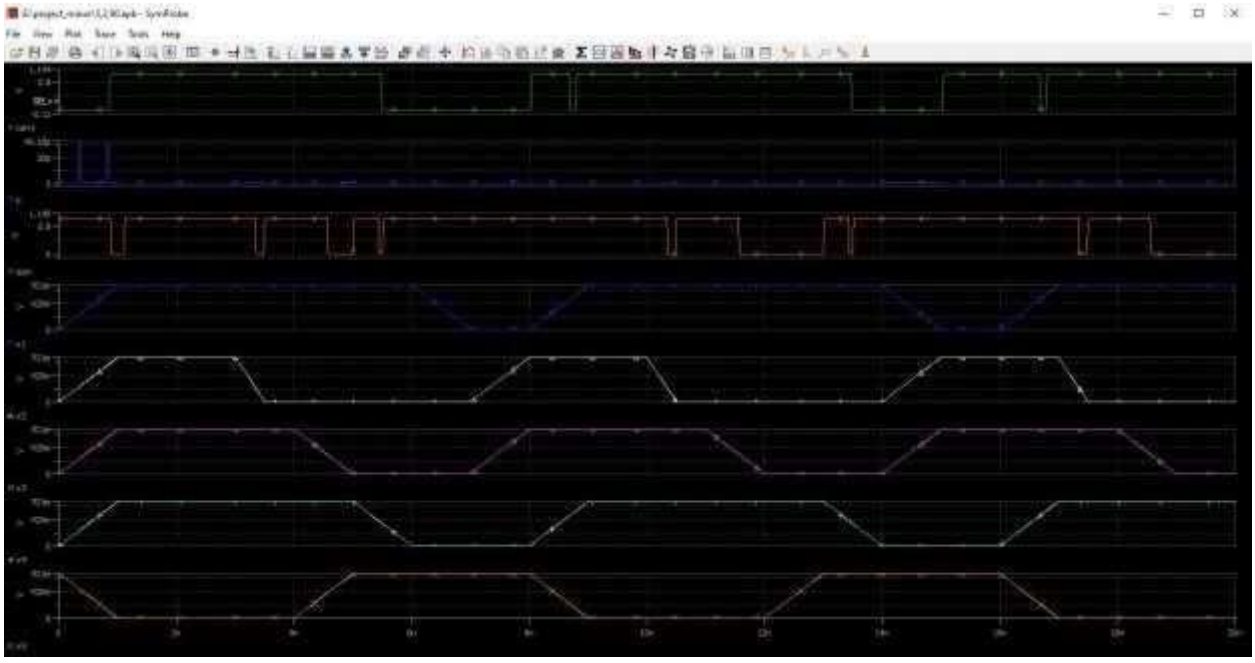


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

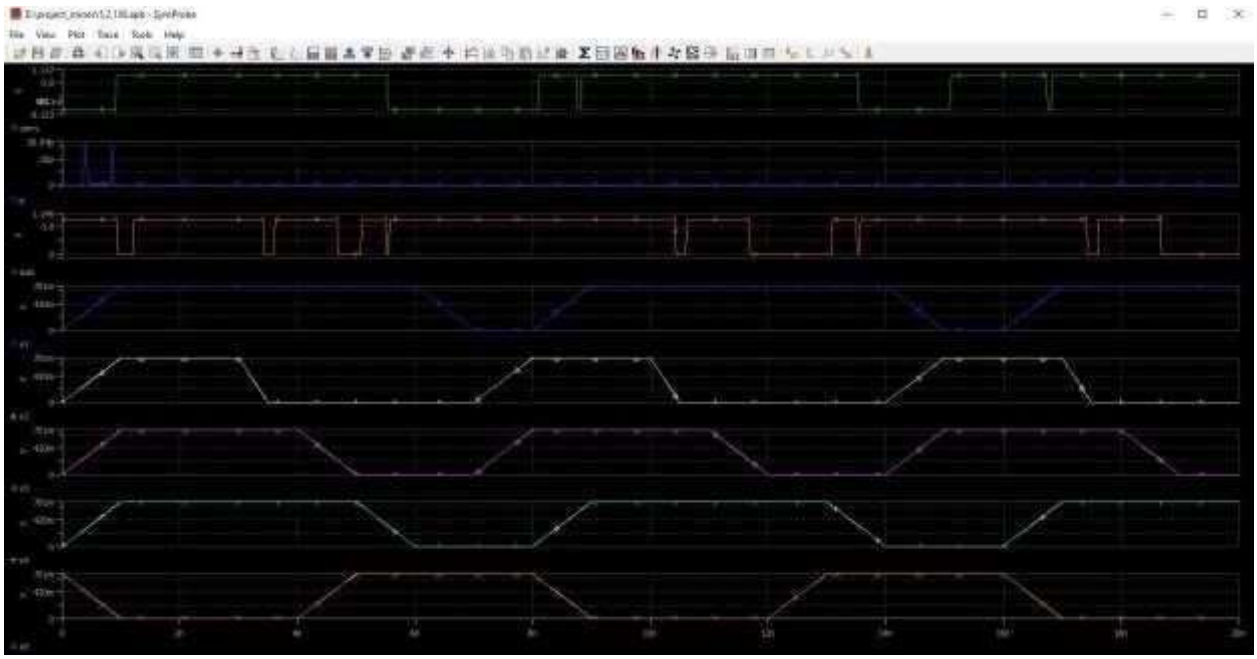


Fig 5.2 Circuit Of (5:2) 5 Input 2 Output Compressor power For Channel 22nm

TABLE 2.2 PERFORMANCE COMPARISON OF SIMULATED 5:2 COMPRESSOR IN TERMS OF POWER, DELAY

LENGTH OF THE CHANNEL(nm)	POWER (pW)	DELAY(S)
22	26p	6.64122e-10
32	28.87	7.11214e-10
45	31.4	7.40372e-10
65	45.81	7.6731e-10
90	49.18	7.89952e-10
130	50.54	6.39645e-10

APPLICATION :

This data multiplier with 4:2 approximate compressor is used to multiply two images with pixel by pixel. There are two major factors are considered to check the quality of the multiplied image. That are, Error Distance(ED) Peak Signal to Noise Ratio(PSNR) Generally, the arithmetic distance between the actual output and error output is known by Error Distance(ED). The PSNR is defined by the ratio of signal power to the noise power. If the PSNR value is in average level, definitely the quality of the image will be improved. ED and PSNR are based on MSE(Mean Squared Error). Figure 9:Transistor-level implementation of CML-based 5:2 approximation compressor:

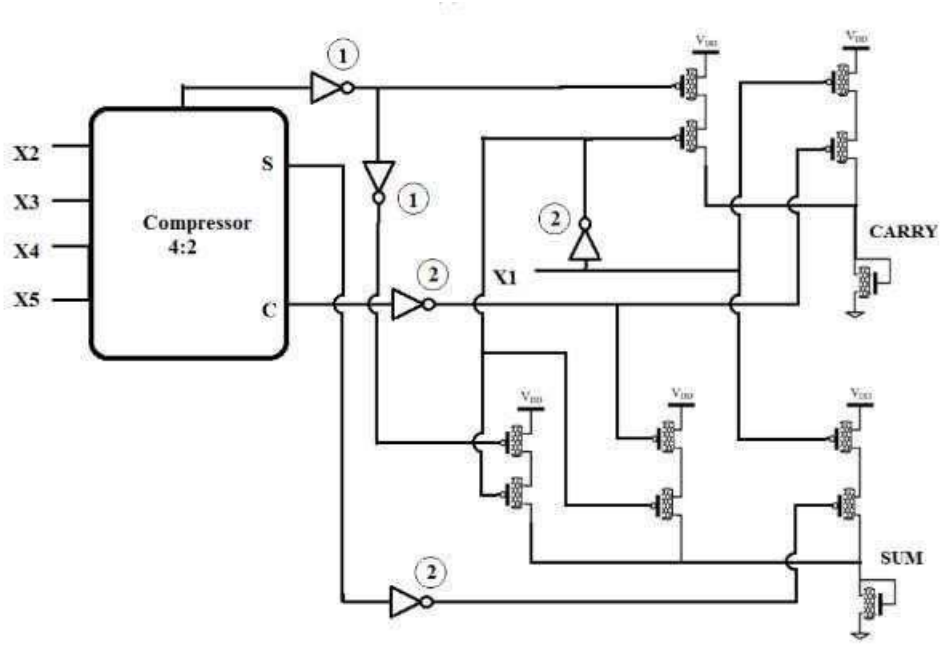


Fig 6.1

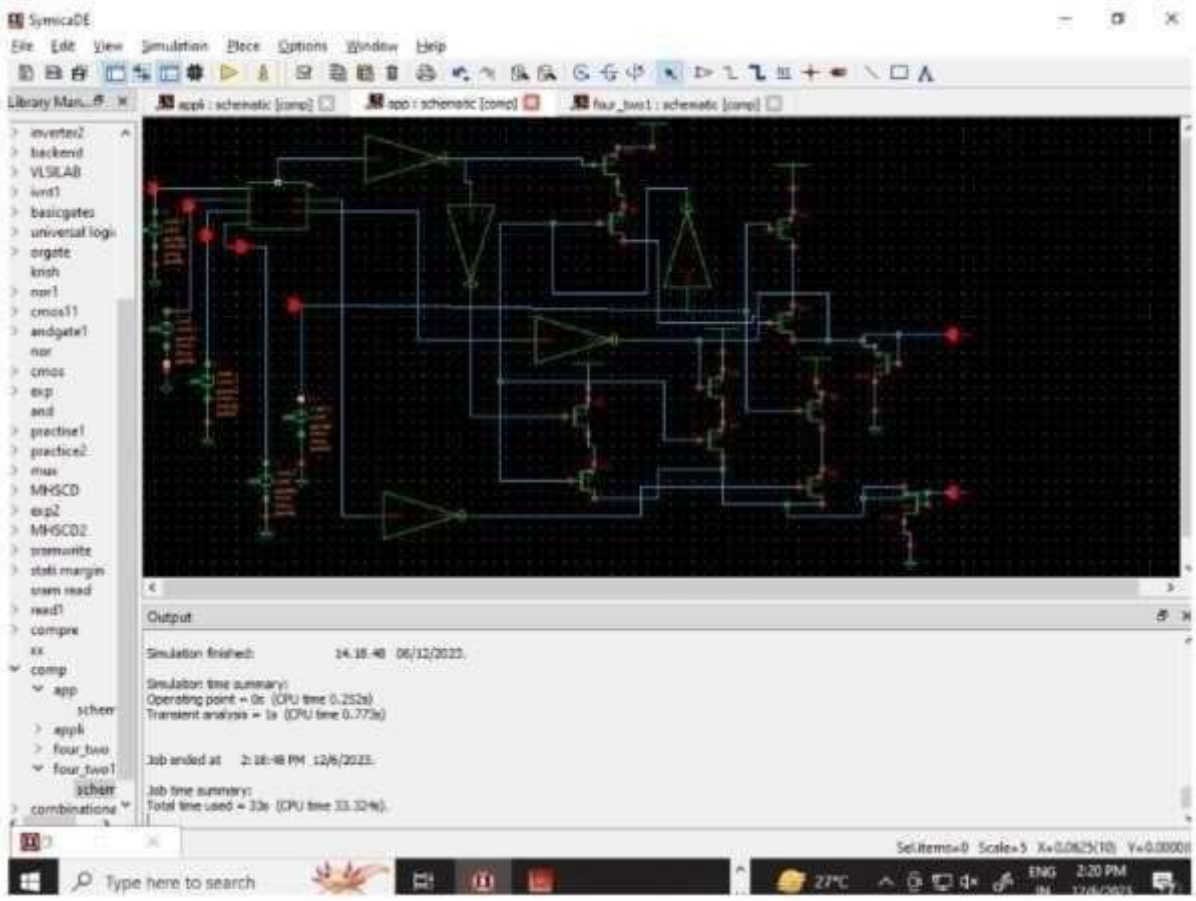


Fig 6.2

Inputs: x1,x2,x3,x4,x5 Outputs: sum, carry

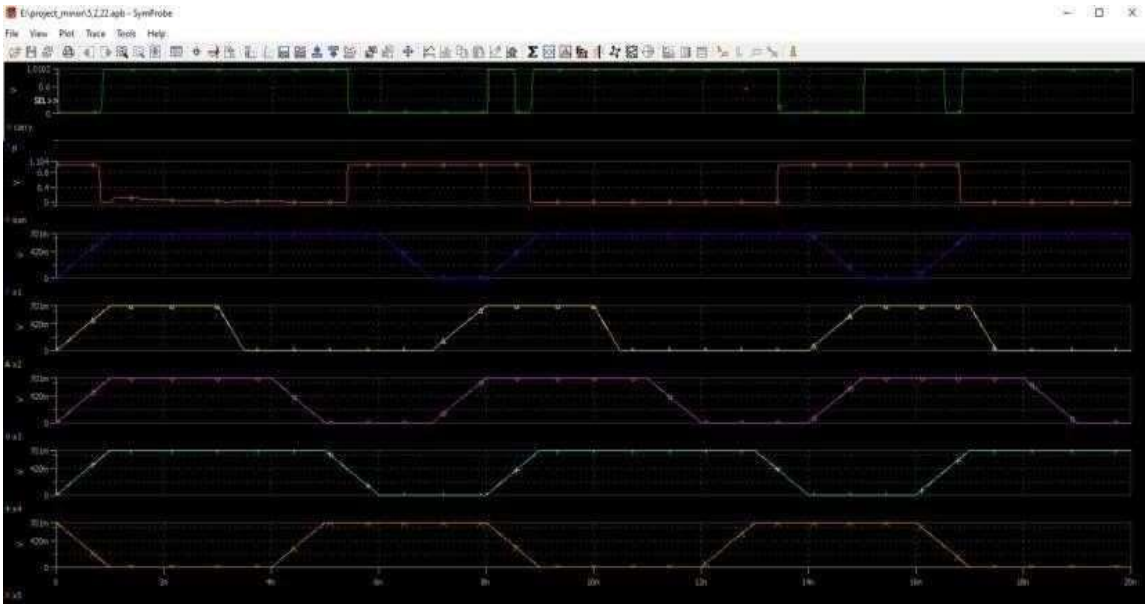


FIG 6.3 : OUTPUT

CHAPTER 5

CONCLUSION AN REFERENCE

5.1 CONCLUSION:

The compressor is a useful element that is widely used in VLSI circuits and systems. It is generally used as a processing element. The construction module is consists of different logic gates like xor, and, or , not etc. The compressor has been designed and simulated in Symica EDA tool by using 22nm, 32nm, 45nm, 65nm, 90 nm and 130nm CMOS technology. Average power , worst case delay and power delay product are computed. The same has been observed by varying the supply voltage and channel length. A study of the performance comparison has been carried out with existing compressors. It is found that the proposed compressor has low power consumption and the best PDP. A study of the performance comparison has been carried out with existing compressors. It is found that the proposed compressor has low power consumption and the best PDP. The suggested 8×8 approximate multiplier is implemented using the proposed compressors when using the Matlab software to multiply images. As the length of the channel of MOS transistor increases we can see a change in power and delay.

5.2 REFERENCES

[1] C.-H. Chang, J. Gu, and M. Zhang, “Ultra low-voltage lowpower CMOS 4-2 and 5-2 compressors for fast arithmetic circuits,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, pp. 1985-1997, 2004.
[2] D. Radhakrishnan and A. Preethy, “Low power CMOS pass logic 4-2 compressor for high-speed multiplication,” PROCEEDINGS OF THE IEEE MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS, vol. 43, pp. 1296-1299, 2000.
[3] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, “Design and analysis of approximate compressors for multiplication,” IEEE Transactions on Computers, vol. 64, pp. 984-994, 2015.
[4] B. K. Mohanty and A. Choubey, “Efficient Design for Radix-8 Booth Multiplier and Its Application in Lifting 2-D DWT,” Circuits, Systems, and Signal Processing, pp. 121, 2016. [5] S. TABRIZCHI, N. AZIMI, and K. NAVI, “Design a novel ternary half adder and multiplier based on carbon nano-tube field effect transistors (CNTFETs),” Frontiers, vol. 1, 2016.

[6] P. Aliparast, Z. D. Koozehkanani, and F. Nazari, “An ultra high speed digital 42 compressor in 65- nm CMOS,” International Journal of Computer Theory and Engineering, vol. 5, p. 593, 2013.
[7] A. Pishvaie, G. Jaberipur, and A. Jahanian, “Redesigned CMOS (4; 2) compressor for fast binary multipliers,” Canadian Journal of Electrical and Computer Engineering, vol. 36, pp. 111-115, 2013.
[8] P. Hasini and T. K. Murthy, “A Novel high-speed transistorized 8x8 Multiplier using 4-2 Compressors,” International Journal of Engineering Research and General Science, vol. 3, pp. 359- 365, 2015.
[9] O. Akbari, M. Kamal, A. Afzali-Kusha, and M. J. I. T. o. V. L. S. I. S. Pedram, "Dualquality 4: 2 compressors for utilizing in dynamic accuracy configurable multipliers," vol. 25, no. 4, pp. 1352- 1361, 2017.

5.3 APPENDICES:

- **Detailed Schematic Diagrams:**
  Include detailed circuit schematics of the proposed multiplier design based on 4:2 and 5:2 compressors in MOSFET technology.
- **Simulation Results:**
  Provide comprehensive tables and graphs illustrating simulation results for power consumption, speed, and accuracy. Include comparative analyses with other existing multiplier schemes for validation.
- **Resource Utilization Metrics:**
  Include data on resource utilization, such as chip area, transistor count, and other relevant metrics.
  Provide comparisons with existing multiplier designs in terms of resource efficiency.
- **Technology-Specific Challenges and Solutions**:
  Detail specific challenges encountered with MOSFET technology and elaborate on the solutions implemented in the proposed multiplier scheme.
- **Additional Methodological Details:**
  Offer supplementary information on specific methodologies employed, particularly in the integration of 4:2 and 5:2 compressors and approximate arithmetic techniques.
- **Fabrication Considerations:**
  If applicable, include information or considerations related to the physical fabrication of the proposed multiplier scheme.