Name:-

SARDAR MURAAD WAHEED

Roll No:-

2024-CET-18

Semester:-

2ND SEMESTER
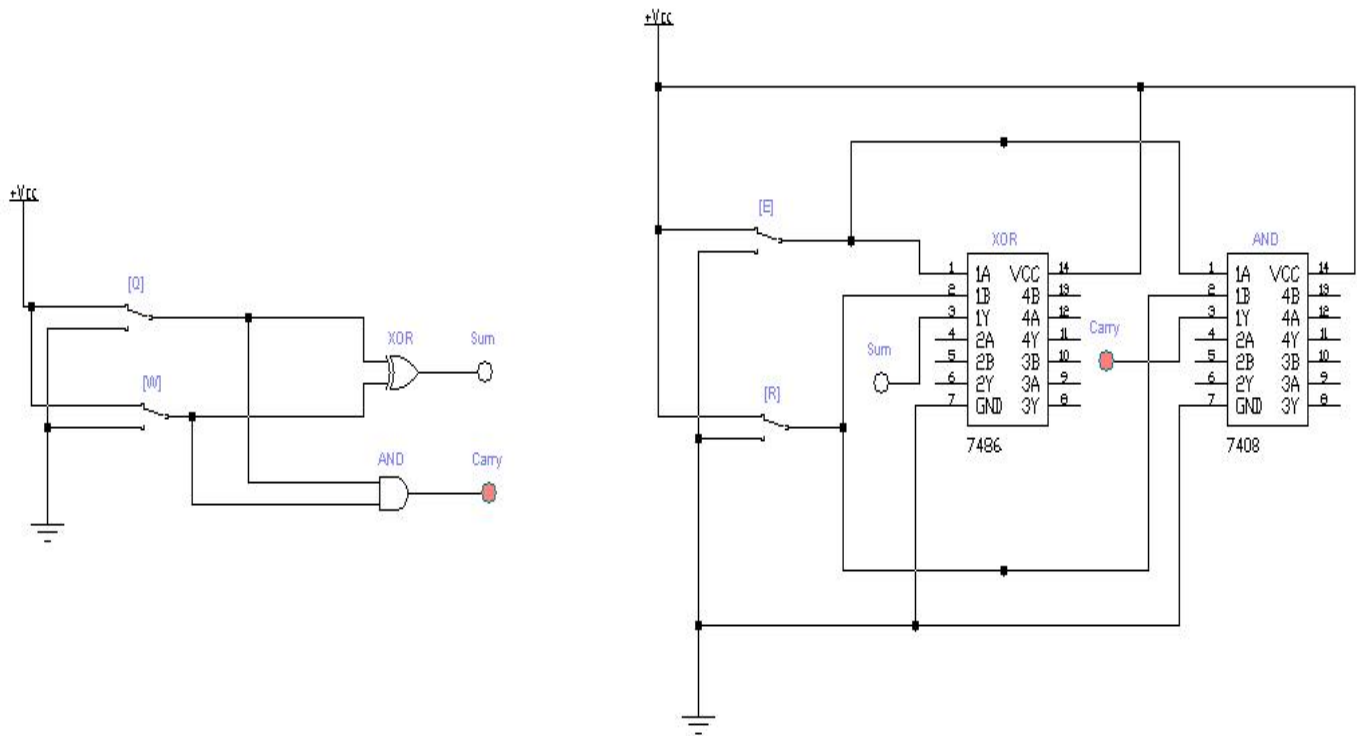
Subject:-

DLD

Submitted To:-

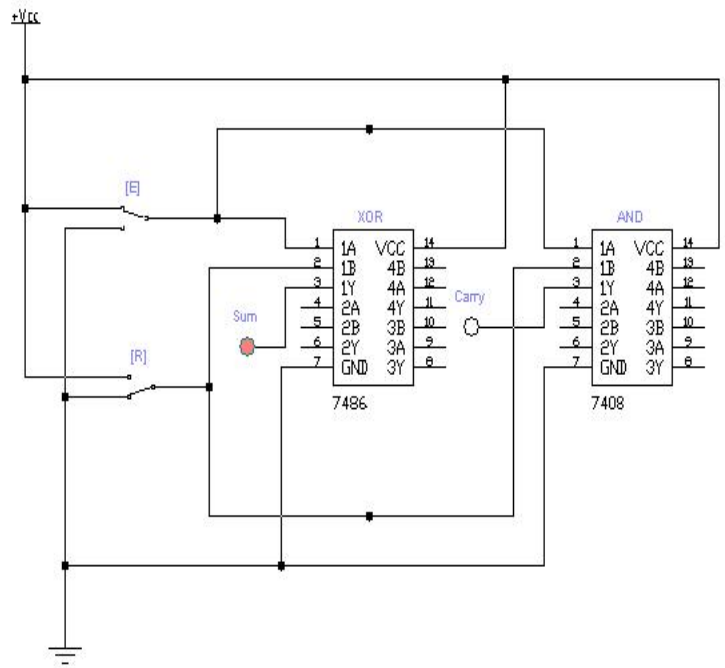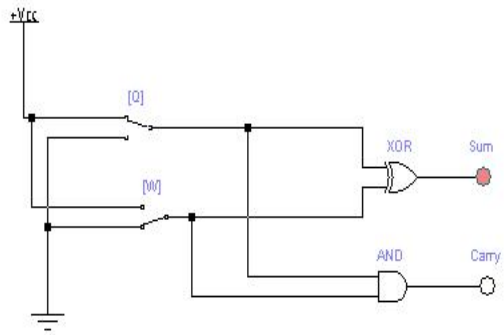ENGR.SIDRA RAFIQUE

Submitted Date:-

04-JUN-2025

Lab 4

Experiment on EWB

+Vcc

[Q]

XOR   Sum

[W]

AND   Carry

+Vcc

[E]

XOR

1A VCC 14
1B 4B   13
1Y 4A   12
2A 4Y   11
2B 3B   10
2Y 3A   9
GND 3Y   8

7486

Sum

[R]

Carry

AND

1A VCC 14
1B 4B   13
1Y 4A   12
2A 4Y   11
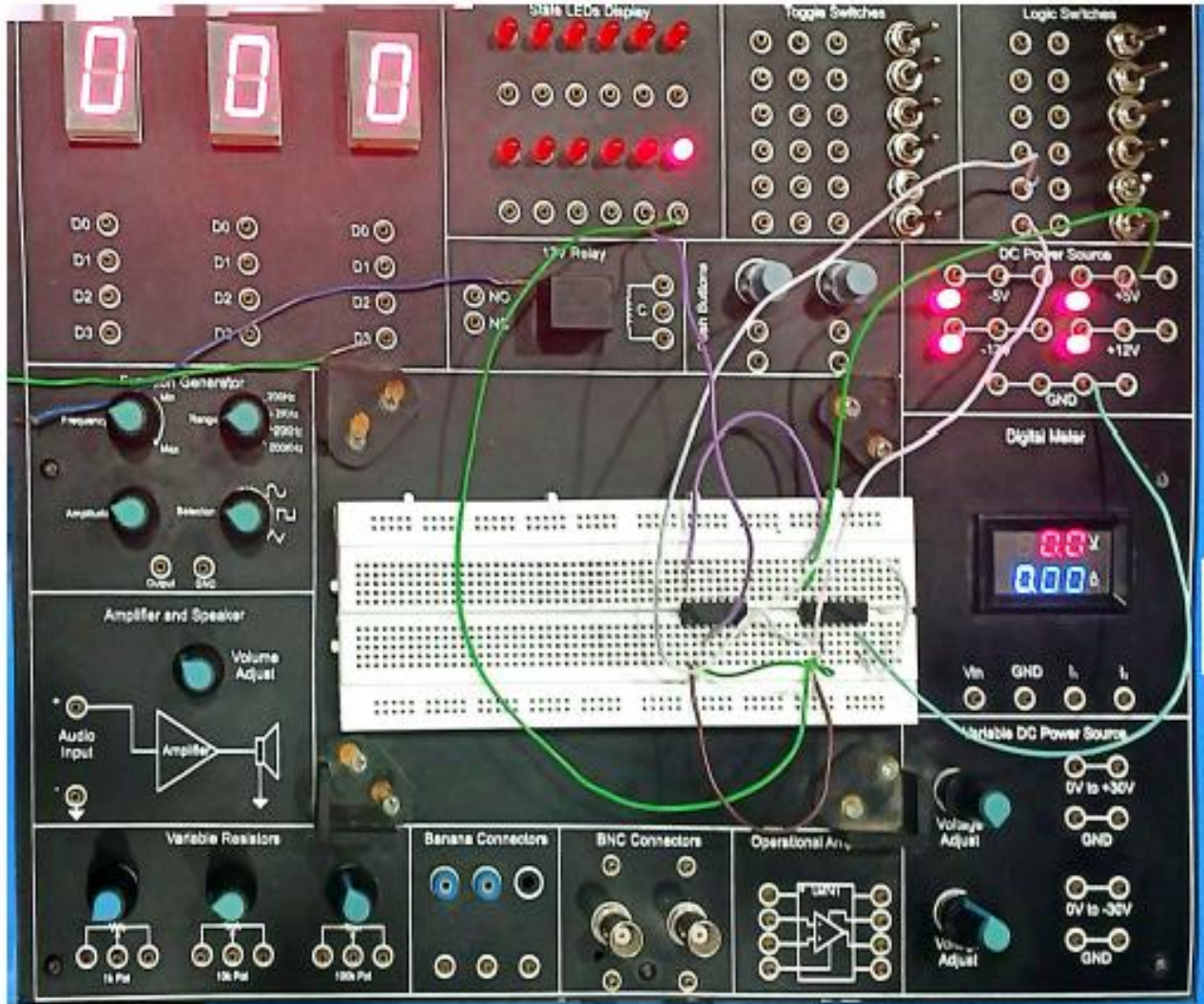2B 3B   10
2Y 3A   9
GND 3Y   8

7408

Carry Output

Sum Output

Experiment on Hardware

Simple Circuit Implementation

- Circuit shows the implementation of Half Adder using ICs of XOR and AND.

Complicated Circuit Implementation