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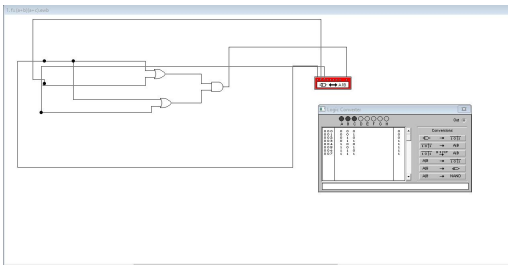
Group:-Computer Enginnering Technology
Subject:-DLD

Circuit No1:-

F= (A + B)(A + C)



Inputs:

Three input switches labeled **A**, **B**, and **C** on the left side.

Logic Gates:

Two OR gates:

- First OR gate has inputs A and B.
- Second OR gate has inputs A and C.

One AND gate:

- Takes the outputs of the two OR gates as its input.
- Output of the AND gate represents the final function f = (A + B)(A + C).

Output:

- The final output from the AND gate is connected to an output probe (highlighted in red), which likely indicates the current logic level (HIGH/LOW).

Logic Converter Tool:

- Located below the circuit.
- Displays the truth table for all combinations of A, B, and C.
- Outputs the result of the logic function f for each input combination.
- It confirms that the output matches the expression (A + B)(A + C).

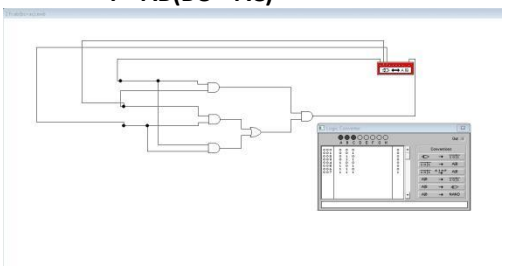
Truth Table Of This Gate:

A	B	C	F=(A+B)(A+C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Circuit No2:-

F= AB(BC + AC)



1. Inputs:
Three input switches labeled A, B, and C (left side of the circuit).

2. Gate Structure:

First AND Gate:
Inputs: A and B
Output: AB

Second AND Gate:
Inputs: B and C
Output: BC

Third AND Gate:
Inputs: A and C
Output: AC

OR Gate:
Inputs: BC and AC
Output: BC + AC

Final AND Gate:
Inputs: AB and (BC + AC)
Output: f = AB(BC + AC)

3. Output:

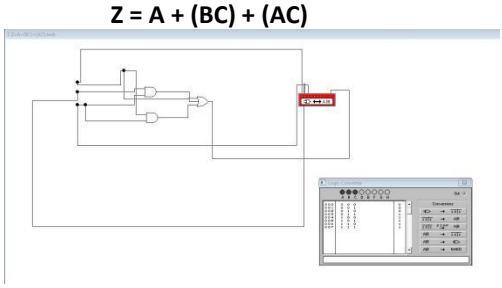
The final output from the last AND gate is connected to an output probe (highlighted in red), which likely reflects the current binary state (logic high/low).

Truth Table:

A	B	C	F= AB(BC + AC)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Circuit No3:-

Z = A + (BC) + (AC)



1. Inputs:

    Three input switches:
    A, B, and C (on the left side of the circuit).

2. Logic Gates and Connections:

    First AND Gate:
    Inputs: B and C
    Output: BC

    Second AND Gate:
    Inputs: A and C
    Output: AC

OR Gate:
Inputs: BC, AC, and A
Output: Z = A + BC + AC

3. Output:

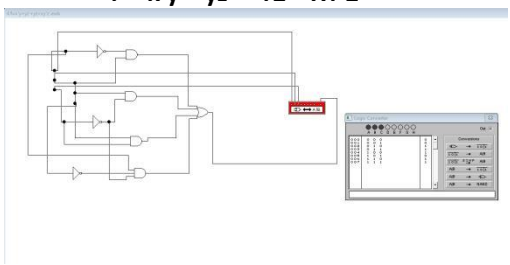
The final output from the OR gate is connected to an output probe (highlighted in red) to show the logic state of Z.

Truth Table:

A	B	C	Z=A+(BC)+(AC)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Circuit No4:-

F = x'y + yz' + YZ + XY'Z'



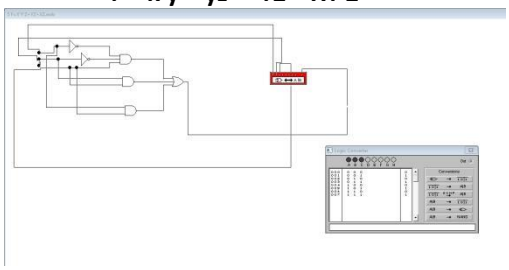
- **NOT Gates**:
  - A NOT gate inverts x to produce x
  - A NOT gate inverts z to produce z′
  - A NOT gate inverts y to produce y′
- **AND Gates**:
  - The first AND gate takes x′ and y y y to produce x′y
  - The second AND gate takes yand z′ to produce yz′
  - The third AND gate takes y and z z z to produce yz
  - The fourth AND gate takes x , y, and z′to produce xy′z′
- **OR Gate**: The outputs of the four AND gates (x′y, yz′, yz , and xy′z′) are fed into an OR gate to compute the final expression F=x′y+yz′+yz+xy′z′.
- **Output**: The output of the OR gate is the final function F F F.

Truth Table:

A	B	C	F = x'y + yz' + YZ + XY'Z'
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Circuit No5:-

F = x'y + yz' + YZ + XY'Z'



- **Inputs**: The circuit has three inputs: x , y, and z.
- **NOT Gates**:
  - A NOT gate inverts x to produce x’ .
  - A NOT gate inverts y to produce y’
- **AND Gates**:
  - The first AND gate takes x’ , y’’, and z to produce x’y’z
  - The second AND gate takes y and z to produce yz.
  - The third AND gate takes x and z to produce xz.
- **OR Gate**: The outputs of the three AND gates (x’y’z , yz, and xz) are fed into an OR gate to compute the final expression F=x’y’z+yz+xz
- **Output**: The output of the OR gate is the final function F.

Truth Table:

A	B	C	F = x'y + yz' + YZ + XY'Z'
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1