X2O Chip2Chip example project notes

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# Introduction

The ZYNQ device on the X2O power module is using AXI Chip2Chip links to provide fast communication path to the payload modules. Each link can use up to two GMT lanes, with the top bit rate limited by ZYNQ device at 3.75 Gbps.

# Example project

An example project is provided as a reference or a starting point for user’s projects.

Table 1 shows the example project details.

|  |  |
| --- | --- |
| **FPGA family** | Ultrascale+ |
| **Partnumber** | xcku15p-ffva1760-2-e |
| **MGT type** | GTH |
| **Lane count** | 1 |
| **Bit rate** | 3.75 Gbps |
| **Encoding** | 8b/10b |
| **PLL type** | CPLL |
| **Git link** | <https://github.com/madorskya/apex_ku15p.git> |
| **Project folder** | apex\_ku15p\_c2c\_mgt |
| **Git tag** | c2c\_mgt\_working |

Table . Example project details

Example project design structure is shown in Figure 1.

AXI

Inter-connect

BRAM 0

Chip2Chip IP

Figure . Example project structure

MGT wrapper

To ZYNQ

MGT

C2c\_adapter

BRAM 1

Table 2 below lists the components of the example design and shows some details about them.

|  |  |
| --- | --- |
| **Component** | **Notes** |
| MGT | Generated using standard Xilinx Transceiver Wizard. |
| MGT wrapper | Created from the example design provided by Transceiver Wizard, with minimal modifications. |
| C2c\_adapter | Custom module connecting Chip2Chip AXI stream RX and TX interfaces to the MGT ports. |
| Chip2Chip IP | Standard Xilinx Chip2Chip IP generated in Aurora 8b/10b configuration. However, note that this example design is not using Aurora IPs. |
| AXI interconnect | Standard Xilinx AXI interconnect IP. This interconnect can be expanded as needed for user’s logic. |
| BRAM 0 and 1 | Standard Xilinx BRAM controllers and BRAM IPs. These modules are provided for memory access tests, and can be replaced with user’s logic as needed. |

Table . Example design components.