ECE 554 Lab 1 Start Guide

What is a .QSF file?

- Serves many purposes:

a) What is the target FPGA
a) What files are part of build
b) What I/O voltage standards used for what FPGA pins
c) How do verilog signal names get mapped to specific FPGA pins

Excerpt from a .qsf file

```
#set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK4_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to clk
set_location_assignment PIN_AF14 -to clk
```

Verilog signal clk will be mapped to PIN_AF14
(which happens to be driven by a 50MHz clk on the board)

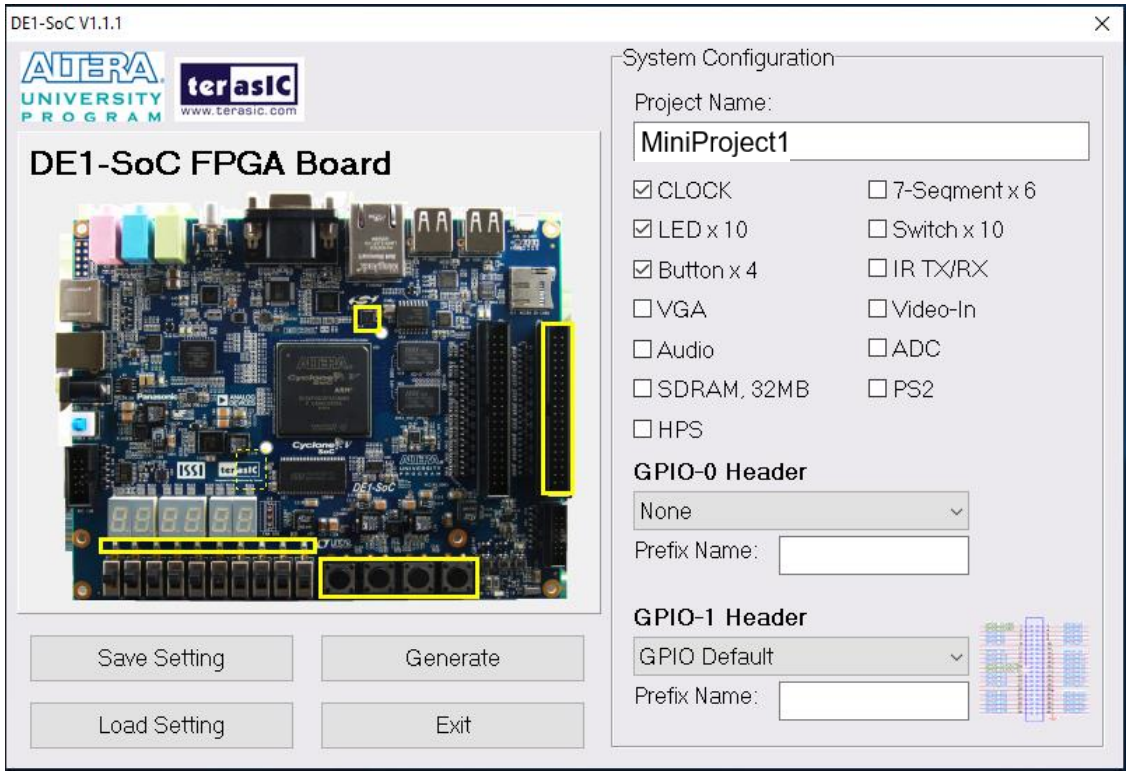
Verilog signal clk will use a 3.3V signal level with TTL defined VIL

Generate template .qsf & .qpf using system builder

- Set project name to “MiniProject1”

MiniProject1

- Select
  - clock
  - LED
  - Button
- Set GPIO-1 to GPIO Default
- Press “Generate”



Modify the Generated .qsf file:

- Copy the generated **.qsf** and **.qpf** files to your team's work area

- Edit the **.qpf** file to use the signal names we use.
  - CLOCK_50 becomes clk
  - KEY[0] becomes RST_n
  - GPIO[3] becomes TX
  - GPIO[5] becomes RX

- Use the LEDS[9:0] as you like for debug (or not).