**Problems Encountered and Solutions:**

* Our group was stuck on figuring out which clock edge to flop our design on.
  + We ended up standardizing all of our flopping on negedge.
* The hardest part was the bypassing – figuring out where and what to bypass was a difficult challenge.
  + Debugging was done by comparing the non-flopped run of Test1’s waveforms to our solution, which ran into difficulties as we encountered a lot of x’s that were hard to find out where they were coming from.
  + The solution was to flop the previous WB data (much simpler than we thought)
* One of our group members took it upon themselves to debug between lab sessions and found an error involving the *we* signal, which wasn’t getting properly initialized.
  + We were also incorrectly bypassing data because comparing an x to any value with a double equals is always true.
* Related: our handling of R0 was erroneous – we were bypassing things that were “attempting” to be written to it, causing errors.
  + The solution was to add another output of the mux that checked if R0 was being read/written to for avoiding this problem.