###
ECE755 Project Milestone #3 Optimizations
###

Our current design uses 4 instances of DNN in the GNN module.

The number of multipliers and adders were reduced to decrease power consumption and area at the expense of increased turnaround time (latency) in the DNN module. Number of multipliers were reduced from 24 to 8, and number of adders were reduced from 18 to 6.

###
The initial pipeline was:
###

P1	P2	P3
Aggregate X inputs Multiply aggregated X inputs with weights Accumulate multiplier outputs to calculate Layer-1 outputs	Apply ReLu to Layer-1 outputs Aggregate ReLu outputs Multiply aggregated ReLu outputs with weights Accumulate multiplier outputs to calculate final outputs	Send final output

###
The optimized pipeline is:
###

P1	P2	P3	P4	P5
Aggregate X inputs	Multiply aggregated X inputs with weights for Y6 and Y7	Accumulate Y6 and Y7 multiplier outputs to calculate Layer-1 outputs	Aggregate ReLu outputs	Accumulate multiplier outputs to calculate final outputs
Multiply aggregated X inputs with weights for Y4 and Y5	Accumulate Y4 and Y5 multiplier outputs to calculate Layer-1 outputs	ReLu for all Y4, Y5, Y6, Y7	Multiply aggregated ReLu outputs with weights	Send final output

###
We added a global rst_n signal in the dnn.sv and top.sv modules to eliminate the X-propagation to the outputs signals from the FSM in dnn.sv
###

This optimization has resulted in:

1. Decrease in area from ~16.62k cells to 9.59K cells

2. Reduction in power consumption from 2.238 mW to 1.62 mW

3. Increase in latency from 3 cycles to 5 cycles

###
We also encountered setup time violations on nodes:

    1. y6_aggr_p4_reg[*],
    2. y7_aggr_p4_reg,
    3. mul*_out_reg[20]

We fixed these timing errors, we adjusted the bit-widths of the following signals to minimize critical path delay:

    1. y*_relu_p3, y*_aggr_p4
    2. Internal multiplier signals: mulitiplicand1/2/3/4, mul*_out
    3. mac1/2

###