Verification Plan

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Introduction

Introduction

- A verification plan can be many things
  - Typically a mapping of requirements to verification targets

- For a directed test approach
  - Mapping of requirements to tests
  - Result is a list of tests to be implemented

- For CRV
  - Mapping of requirements to coverage and checkers
  - Result is **NOT** a list of tests to be implemented
  - Whatever tests closes the coverage model with all checkers enabled will do the job

Introduction

- To handle requirement mapping some tools are available
  - DOORS: Requirement management
  - Excel: Poor mans solution
  - Proprietary format (TXT, JSON, …)
    - Needs some proprietary scripting as well
  - EDA Tools
    - VManager (Cadence)
    - HVP – Hierarchical Verification Plan (Synopsys)
    - TestPlan Author (Siemens-EDA)

- We will use Excel (Or similar)

Verification Plan

Verification Plan

- A verification plan is requirement mapping to coverage or checkers
- It is always good to add an ID to all entries as then one can speak directly about them

ID	Design Requirement	Coverage	Verification Criteria	Priority	Type	Comment
<Int>	<Description>	Covergroup or similar	Explicit checker, score board, assertion or REF model, test or …	High/Medium /Low	Design/Protocol/ …	

Example

Example – SAT Filter

ID	Design Requirement	Coverage	Verification Criteria	Priority	Type	Comment
0	DR0	Reset coverpoint	All checkers enabled	Medium	Design	
1	DR1	N/A	Design inspection	Medium	Design	
2	DR2	Threshold coverpoint sSDT Value coverpoint	REF Model	High	Design	
3	DR3	N/A	Propagation Checker	High	Design	
4	DR4	sSDT coverage	Protocol Checker	High	Protocol	

DR0: It shall be possible to reset the state of the saturation filter by toggling the RST input signal

DR1: All signals shall react to the rising edge of the input CLK signal.

DR2: The saturation functionality of the design shall be evaluated with the threshold parameter value.
    If the data is below the limits it is propagated to the output on the next rising edge of the CLK signal.
    Otherwise, the data is saturated, and the out_data signal will be the threshold value instead.

DR3: The in_valid signal is always propagated to the output on next the rising edge of the CLK signal.

DR4: The SAT shall be compliant with the sSDT (simple SyoSil Data Transfer) protocol.

MARB

MARB

- Create a verification plan for the MARB following the same format
- Try to make it complete eventhough you do not have time to implement everything
- At examination then it is more important to have a complete verification plan than having everything implemented ☺