Homework 2

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Question 1

1. Write the logical expression that indicates Y's functional behaviour
2. Design a logic circuit network that realizes Y's functional behaviour
3. Construct a Karnaugh map
4. Using the Karnaugh map results, re-write the logical expression from part a above
5. Re-design the logical circuit network from b above and indicate what elements have been eliminated from the original logic circuit network.
6. Write the SOP and POS forms of the given truth table. For this truth table, which form is more efficient and convenient and why
7. Using universal gates NAND and NOR, draw the circuits that realize the logic for the SOP

Solution:

1. $Y = (A + B + C)\left(A + \overline{B} + C\right)\left(\overline{A} + \overline{B} + C\right)$

2.

A \ BC	00	01	11	10
0	0	1	1	0
1	1	1	1	0

3.
4. $Y = A\overline{B} + C$

5.

Two OR gates and $\overline{A}$ have been removed

6.

$$\text{SOP} = \overline{AB}C + \overline{A}BC + A\overline{BC} + A\overline{B}C + ABC$$
$$\text{POS} = Y = (A + B + C)\left(A + \overline{B} + C\right)\left(\overline{A} + \overline{B} + C\right)$$

The POS is more efficient and convenient as it has less terms and therefore requires less gates to construct.

7.

Question 2

1. Using Boolean algebra, show that the following two expressions are equivalent:

$$F_1 = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$
$$F_2 = (A + B + C)\left(A + B + \overline{C}\right)\left(A + \overline{B} + C\right)\left(\overline{A} + B + C\right)$$

These two expressions represent the majority function in sum-of-products and product-of-sums form.

2. Assuming that AND, OR, NAND and NOT gates are available, sketch the combinations that would realize the following:
   (a) $Y = AB\overline{C} + \overline{A + \overline{(B + C)}}$
   (b) $Z = B\left(A + \overline{\overline{B} + \overline{C}}\right) + A + \overline{\overline{(B + C)}}$
3. For the circuit shown below, determine the relationship between the output Z and the inputs A, B and C. Construct a truth table for the function
4. Provide a circuit diagram that implements the following Boolean function using four inputs (A, B, C, D):

$$F = \left(A + \overline{B}\right)\left(B + C + \overline{D}\right)\left(A + \overline{B} + \overline{C}\right)$$

That has don't care states $AB\overline{CD}$, $AB\overline{C}D$, $ABCD$, $ABC\overline{D}$
   (a) Implement the function above using only NAND gates.

Solution:

1.

$$\begin{aligned}
F_2 &= (A + B + C)\left(A + B + \overline{C}\right)\left(A + \overline{B} + C\right)\left(\overline{A} + B + C\right)\\
&= A + B + \overline{C}C\left(A + \overline{B} + C\right)\left(\overline{A} + B + C\right)\\
&= A + A\overline{B} + AC + AB + BC\left(\overline{A} + B + C\right)\\
&= A + AC + BC\left(\overline{A} + B + C\right)\\
&= A\left(\overline{A} + B + C\right) + AC\left(\overline{A} + B + C\right) + BC\left(\overline{A} + B + C\right)\\
&= AB + AC + ABC + AC + \overline{A}BC + BC + BC\\
&= AB + AC + ABC + \overline{A}BC + BC\\
&= ABC + AB\overline{C} + ABC + A\overline{B}C + ABC + \overline{A}BC + ABC + \overline{A}BC\\
&= ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC\\
F_1 &= ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC
\end{aligned}$$

$\therefore F_1 = F_2$

2. (a)

(b)

3.

$$Z = \overline{\overline{A}B + AC}$$

A	B	C	$\overline{\overline{A}B + AC}$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

4.

(a)

Question 3

A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations:

$$A(t+1) = \overline{x}y + xA + yA$$
$$B(t+1) = \overline{x}B + xA + \overline{x}\overline{A}$$
$$z = A + Bx$$

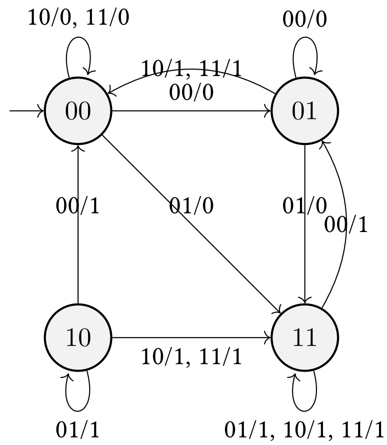
1. Draw the logic diagram of the circuit
2. Provide the state table for the sequential circuit.
3. Draw the corresponding state diagram.
4. Is this circuit a Mealy machine or a Moore Machine? Explain why

Solution:

1.

2.

Current State		Input		Next State		Output
A	B	x	y	A	B	z
0	0	0	0	0	1	0
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	1
1	0	0	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1



3.

4. This is a Mealy machine because the output depends on both the state and input.

Question 4

1. Convert each binary number to hexadecimal:
   (a) 10101010
   (b) 10101100
   (c) 10111011
2. Perform each subtraction in the 2's complement form:
   (a) $00110011 - 00010000$
   (b) $01100101 - 11101000$
3. Perform the following binary multiplications:
   (a) 1100×101
   (b) 1110×1110

Solution:

1. (a) AA

   (b) AC

   (c) BB

2. (a)

$$\begin{array}{c|cccccccc} & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ - & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ \hline & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ + & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ \hline & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 \end{array}$$

   (b)

$$\begin{array}{c|cccccccc} & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 \\ - & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ \hline & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 \\ + & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ \hline & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \end{array}$$

3. (a)

$$
\begin{array}{cccccccc}
 & & & & 1 & 1 & 0 & 0 \\
\times & & & & 0 & 1 & 0 & 1 \\
\hline
 & & & & 1 & 1 & 0 & 0 \\
 & & & 0 & 0 & 0 & 0 & \\
 & & 1 & 1 & 0 & 0 & & \\
+ & 0 & 0 & 0 & 0 & & & \\
\hline
 & 0 & 1 & 1 & 1 & 1 & 0 & 0
\end{array}
$$

(b)

$$
\begin{array}{cccccccc}
 & & & & 1 & 1 & 1 & 0 \\
\times & & & & 1 & 1 & 1 & 0 \\
\hline
 & & & & 0 & 0 & 0 & 0 \\
 & & & 1 & 1 & 1 & 0 & \\
 & & 1 & 1 & 1 & 0 & & \\
+ & 1 & 1 & 1 & 0 & & & \\
\hline
1 & 1 & 0 & 0 & 0 & 1 & 0 & 0
\end{array}
$$