Lab 4

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Part 1

Question 1

Mention the number of gates required in the implementation of the expression above.

Solution: 3 NOT Gates, 4 AND Gates each with 4 inputs, and 1 OR Gate with 3 inputs, in total 8 gates

Question 2

$$F = \overline{A}BCD + AB\overline{C}D + ABC\overline{D} + ABCD$$

Use the following methods to simplify the expression above:

1. Boolean algebra
2. Karnaugh mapping method

Solution:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

1.

$$\begin{aligned}
F &= \overline{A}BCD + AB\overline{C}D + ABC\overline{D} + ABCD \\
&= B\left(\overline{A}CD + A\overline{C}D + AC\overline{D} + ACD\right) \\
&= B\left(\overline{A}CD + A\left(\overline{C}D + C\overline{D} + CD\right)\right) \\
&= B\left(\overline{A}CD + A\left(\overline{C}D + C\right)\right) \\
&= B\left(\overline{A}CD + A\overline{C}D + AC\right) \\
&= B\overline{A}CD + BA\overline{C}D + BAC \\
&= BCD + BAD + BAC
\end{aligned}$$

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	1	1	1
10	0	0	0	0

2.

$$F = ABD + CDB + ABC$$

Question 3

Mention the number of gates required in the implementation of the minimized expression generated above.

Solution: 1 OR Gate with 3 inputs, 3 AND Gates each with three inputs, in total 4 gates.

Question 4

Assuming that each gate consumes the same power – 30mW, calculate the energy consumption for both circuits when both are in a chip that operates full-time in a day.

Solution:

Initial Circuit:

$$\begin{aligned} 8 \text{ gates} &= 8 \times 30 \\ &= 240\, mW \\ \text{In a day} &= 240 \times 24 \\ &= 5760\, mWh \end{aligned}$$

Optimized Circuit:

$$\begin{aligned} 4 \text{ gates} &= 4 \times 30 \\ &= 120\, mW \\ \text{In a day} &= 120 \times 24 \\ &= 2880\, mWh \end{aligned}$$

Question 5

Compute the energy savings in kWh.

Solution:

$$\begin{aligned}\text{Savings} &= 5760 - 2880 \\ &= 2880\,mW \\ &= 2.88\,kWh\end{aligned}$$

Therefore the optimized circuit is twice as efficient as the initial circuit.

Part 2

Question 6

$F1$

Solution:

$$F_1 = \overline{BD} + A\overline{C} + BD + C$$

Question 7

$F2$

Solution:

$$F_2 = \overline{B} + \overline{C}D + CD$$

Question 8

$F3$

Solution:

$$F_3 = \overline{C}D + B$$

Question 9

$F4$

Solution:

$$F_4 = \overline{BD} + \overline{B}C + B\overline{C}D + C\overline{D} + A$$

Question 10

$F5$

Solution:

$$F_5 = \overline{BD} + C\overline{D}$$

Question 11

$F6$

Solution:

$$F_6 = \overline{CD} + B\overline{C} + B\overline{D} + A$$

Question 12

$F7$

Solution:

$$F_7 = \overline{B}C + B\overline{C} + A + C\overline{D}$$

Part 3

Question 13

Construct the circuit below and name your file as D_FlipFlop1 and D_FlipFlop2 respectively. Construct the truth table and verify if they are same.

Solution:

D	$Q(t+1)$	$\overline{Q(t+1)}$
0	0	1
1	1	0

Question 14

Construct the circuit below and name your file as SR_FlipFlop1 and SR_FlipFlop2 respectively. Construct the truth table and verify if they are same.

Solution:

S	R	$Q(t+1)$	$\overline{Q(t+1)}$
0	0	$Q(t)$	$\overline{Q(t)}$
0	1	0	1
1	0	1	0
1	1	Invalid	Invalid

Question 15

Construct the circuit below and name your file as JK_FlipFlop1 and JK_FlipFlop2 respectively. Construct the truth table and verify if they are same. NB: You are to construct the JK_FlipFlop2.

Solution:

J	K	$Q(t+1)$	$\overline{Q(t+1)}$
0	0	$Q(t)$	$\overline{Q(t)}$
0	1	0	1
1	0	1	0
1	1	$\overline{Q(t)}$	$Q(t)$

Question 16

Construct the circuit below and name your file as T_FlipFlop1 and T_FlipFlop2 respectively. Construct the truth table and verify if they are same. NB: You are to construct the T_FlipFlop2.

Solution:

T	$Q(t+1)$	$\overline{Q(t+1)}$
0	$Q(t)$	$\overline{Q(t)}$
1	$\overline{Q(t)}$	$Q(t)$

Part 5

Question 17

Simulate and show screenshot of your circuit showing the display of:

1. 64
2. 128
3. 15

In hexadecimal being shown in the hex display.

Solution:

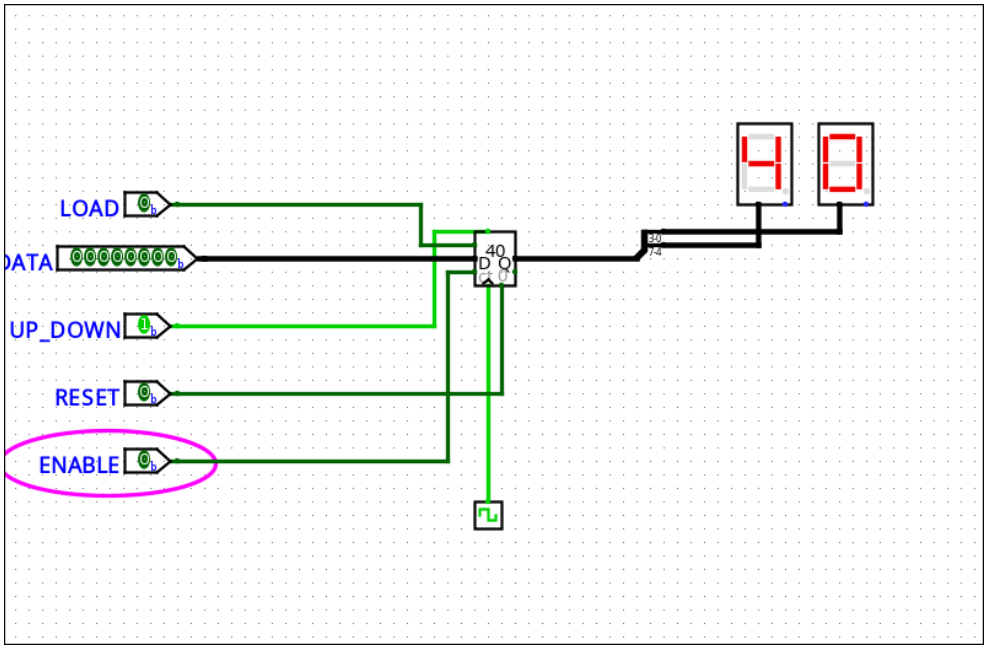

Figure 1: Hex 64

1.

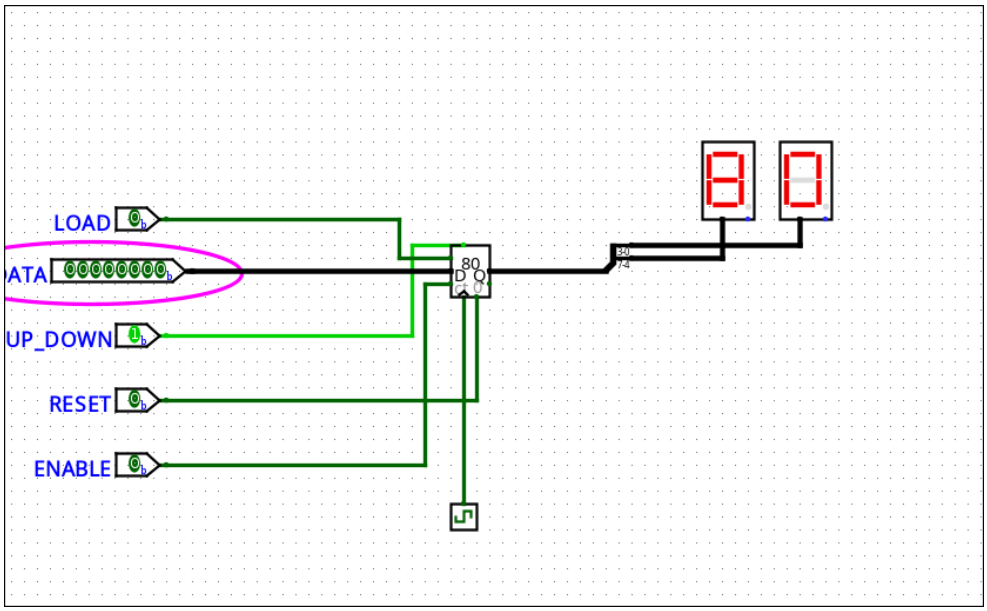

Figure 2: Hex 128

2.

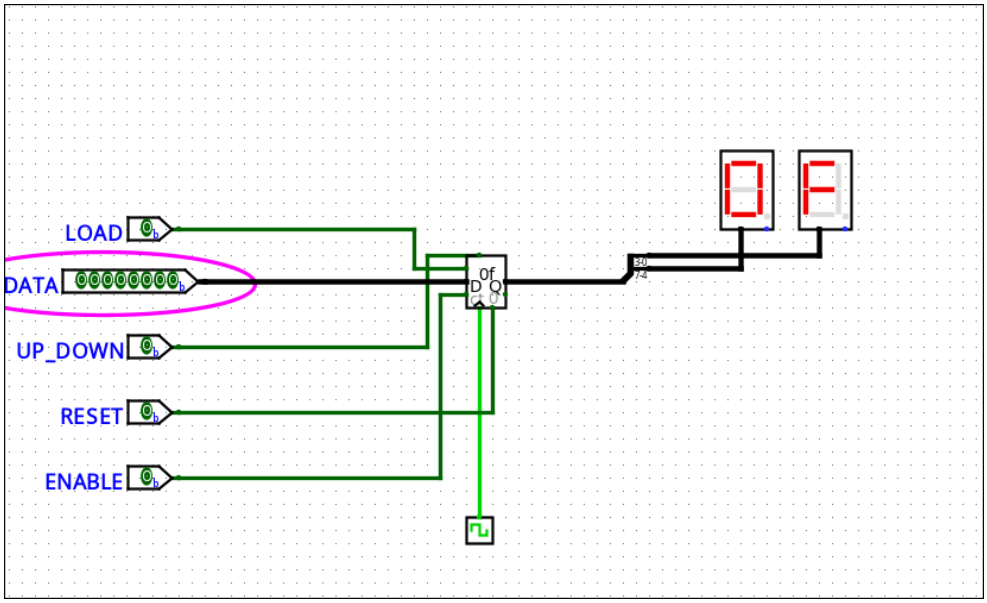

Figure 3: Hex 15

3.

Part 6

Question 18

What are the key differences between the D flip-flop, SR flip-flop, JK flip-flop, and T flip-flop in terms of functionality and behavior?

Solution:

D flip-flop The D flip-flop is a follower flip-flip, meaning that the output is the same as the input at the moment of the clock's pulse this differs from all the other flip-flops which have do logic operations on the input before it is stored.

SR flip-flop The SR flip-flop is a set-reset flip-flop, meaning that it has two inputs, one to set the output to 1 and the other to set the output to 0. The SR flip-flop has an invalid state where both inputs are 1.

JK flip-flop The JK flip-flip solves the invalid state of the SR flip-flop by toggling the output when both inputs J and K are 1. The JK flip-flop can be used to implement all the other types of flip-flops by integrating added logic operations on the inputs.

T flip-flop The T flip-flop is a toggle flip-flop, meaning that it toggles the output when the input is 1. It has a single input T and the output toggles based on this input on each clock pulse.

Question 19

How does the write enable (WE) pin control the writing operation in the memory cell? Why is this signal necessary in memory design?

Solution:

The write enable input determines whether the data input is stored or not by this boolean operation:

$$Q(t+1) = (\overline{\text{WE}} \cdot Q(t)) + (\text{WE} \cdot \text{Din})$$

This ensures when WE is on the data is stored as the right side of the expression will evaluate to the value of Din which is sufficient for the OR gate to output the value of Din.

This is necessary in memory design to prevent data from being written to the memory cell when it is not needed or when the data is not ready to be stored. This is important in ensuring that the memory cell is not corrupted by unwanted data.

Question 20

How does the 8-bit counter's design reflect the principles of sequential logic? What role do the clock and enable signals play in its operation?

Solution: The design of the 8-bit counter reflects the underlying principles of sequential logic as there is kept state in the counter and the current state of the counter is used to determine its next state. The clock signal is used to propagate clock pulses through the counter to allow it to change states, i.e. count up or down. The enable signal is used to control the counter's operation, when the enable signal is off the counter does not change state, no matter the clock signal.

Question 21

How does the counter behave when the Up/Down input is toggled? What observations can you make about its counting sequence in each mode?

Solution: When the up/down input is off / LOW the counter counts down, i.e. decrements by 1 on each clock pulse. When the up/down is on / HIGH the counter counts up, i.e. increments by 1 on each clock pulse. The counting sequence is linear in both modes with each clock pulse resulting in a change of exactly 1 in the counter's value.

Question 22

What happens when the load is turned on, the clock keeps ticking, the UP/DOWN is turned off, and the enable is turned on. How does your answer differ from when the load is turned on, some data is being inputted, clock keeps ticking, the UP/DOWN is turned on and the enable is turned on?

Solution: In this first instance when the load and enable are on, the clock is issuing pulses and the up/down counter is off the value of the counter is remains constant at 0 as no data is being inputted. In the second instance, when data is being inputted and up/down, load, and enable are turned on, the value of the counter remains constant at the value of the inputted data.

Question 23

Reflect on the overall design process and teamwork dynamics during the lab session. What were the key challenges faced by the team, and how were they addressed collaboratively? What lessons can be learned from the design and implementation process for future projects or improvements?

Solution: Some key challenges faced by the team were the complexity of the circuits and all the various tests that were required to ensure that the circuits were functioning correctly. These challenges were addressed collaboratively by breaking the testing process into smaller parts and ensuring that each part was functioning correctly before moving on to the and using the inbuilt testing tools of logisim to ensure that the circuits were functioning correctly.

During this lab session, I gained a deeper understanding of the principles and design of sequential logic circuits and how they are used practically in the design of memory cells and counters.