Lab 5

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Part 5: Analysis of Sequential Circuits

Question 1

Provide the state table for the sequential circuit.

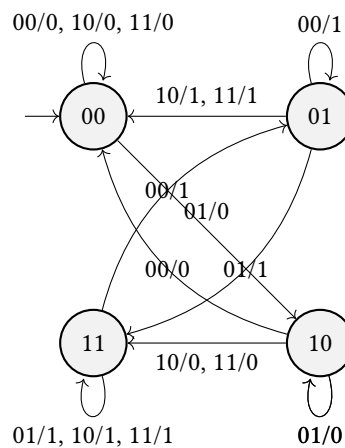$$A(t+1) = \overline{x}y + xA$$
$$B(t+1) = \overline{x}B + xA$$
$$z = B$$

Solution:

Current State		Input		Next State		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

Question 2

Draw the corresponding state diagram.

Solution:

REFLECTION QUESTIONS

Question 3

What role does the Memory Address Register (MAR) play in data transfer within a CPU, and how does it facilitate efficient memory access?

Solution: The MAR can store either the memory address from which data will be fetched, or the address to which data will be written and stored. This allows for efficient memory access as the lookup time for the reading or writing of data is reduced to a single operation due to the direct addressing of the memory location in a register which is much faster than if it was in memory.

Question 4

How does using a controlled buffer with an OE pin improve the data transportation to the data bus in your ALU design?

Solution: The data bus is the primary means of data transfer between parts of the CPU. The controlled buffer controlled by the OE pin allows for the data to be transferred to the data bus only when needed, reducing the power consumption of the ALU as the buffer is only active when data is actively being outputted.

Question 5

What challenges did you face while designing the 8-bit register and Memory Address Register? How did you resolve them?

Solution: My main challenge was intuitively understanding the bit order of the individual 1-bit register and how they came together to make the final output of the 8-bit register. I resolved this by dividing the 1-bit registers into two groups of 4 then starting the least significant bit on the right and the most significant bit on the left.