Lab 7

Madiba Hudson-Quansah

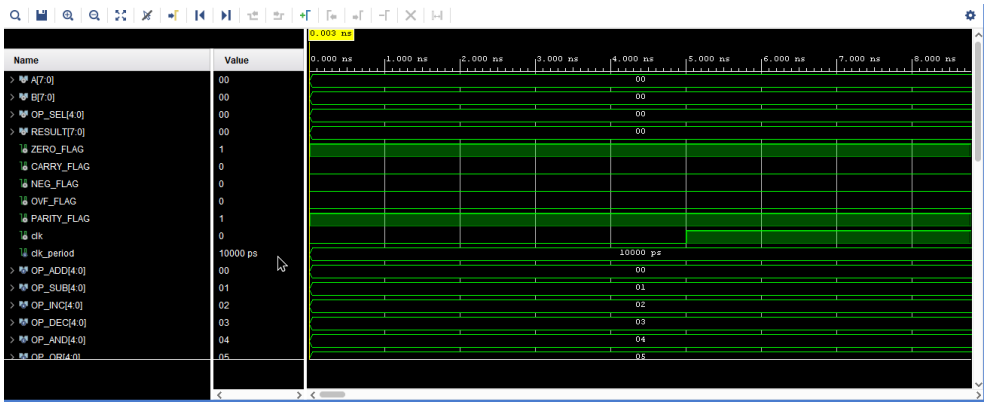

Figure 1: ALU 8 bit

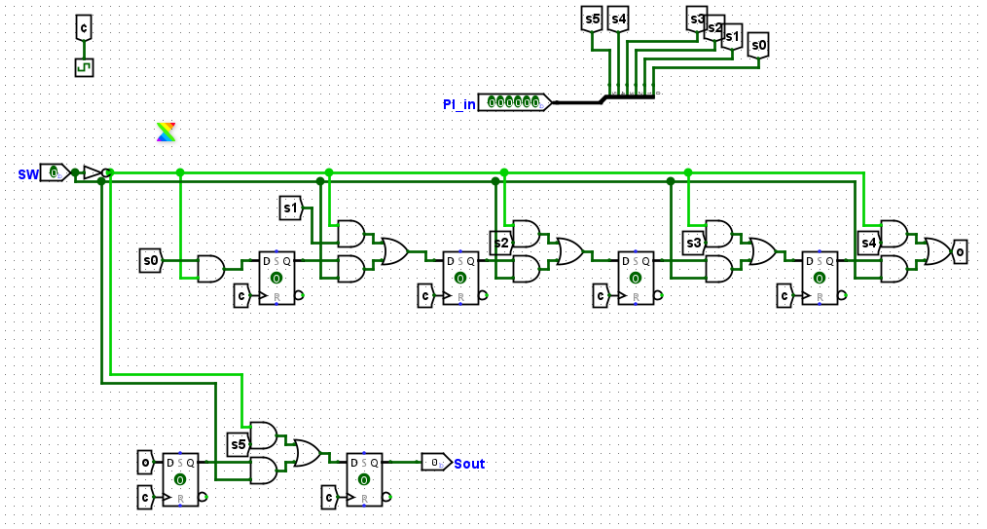

Figure 2: 6-bit Parallel-in / Serial-Out Register

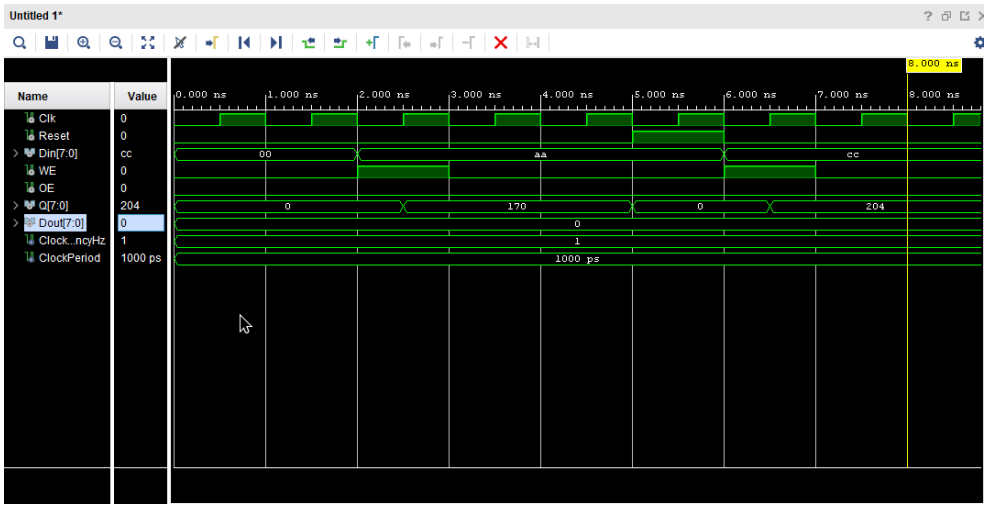

Figure 3: 8 bit Register test bench

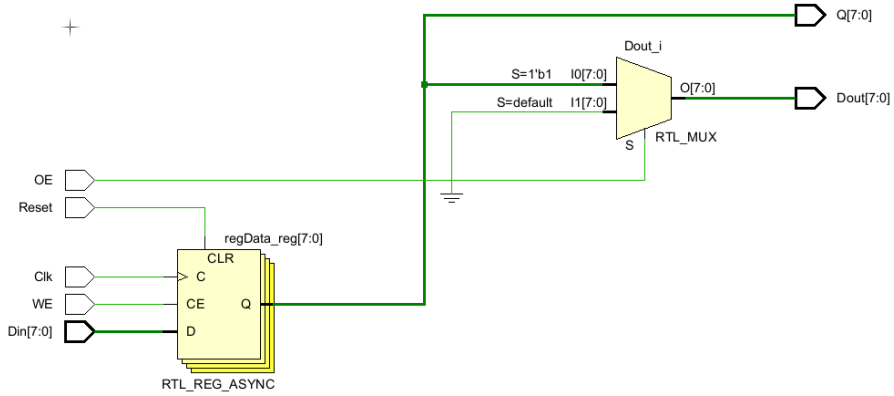

Figure 4: 8 bit Register schematic

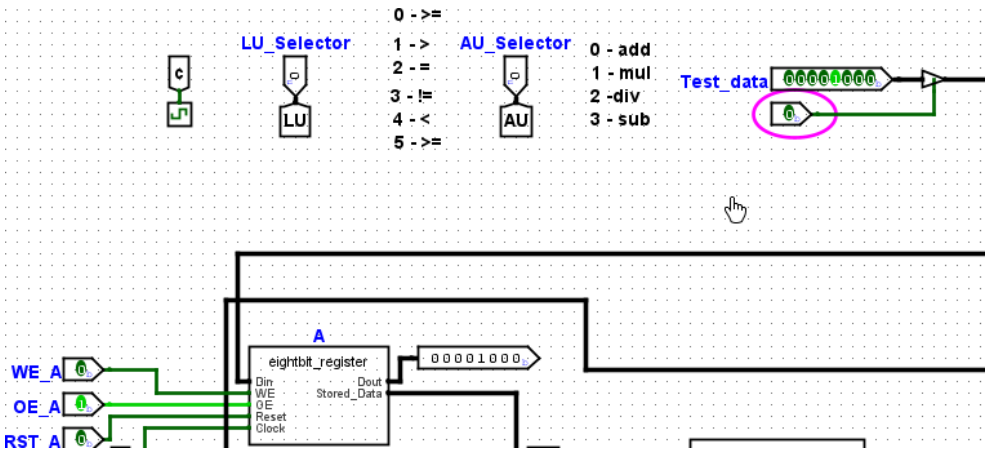

Figure 5: Datapath Register A Test

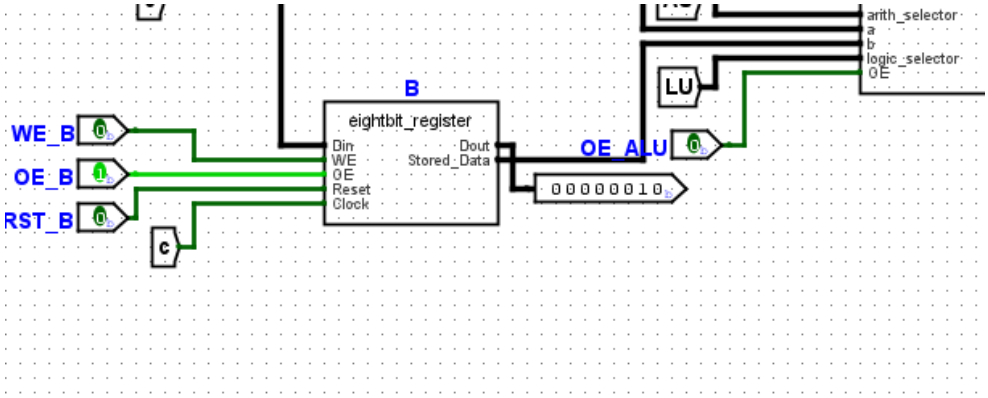

Figure 6: Datapath Register B Test

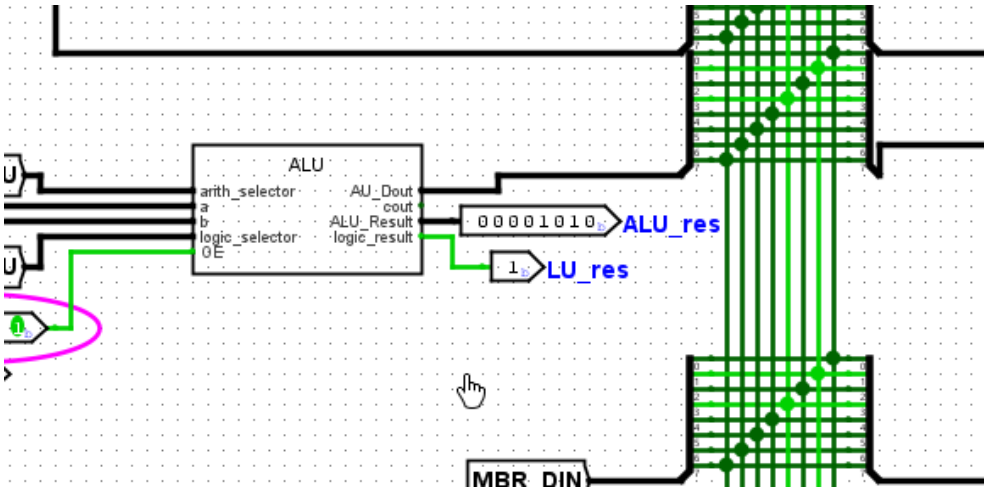

Figure 7: Datapath ALU Test

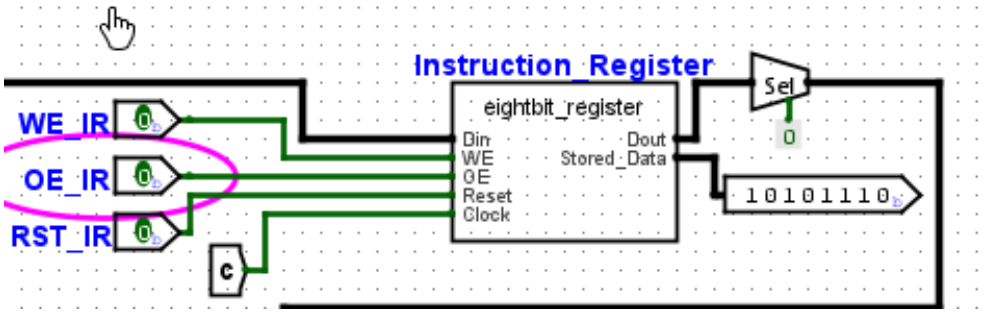

Figure 8: Datapath Instruction Register Test

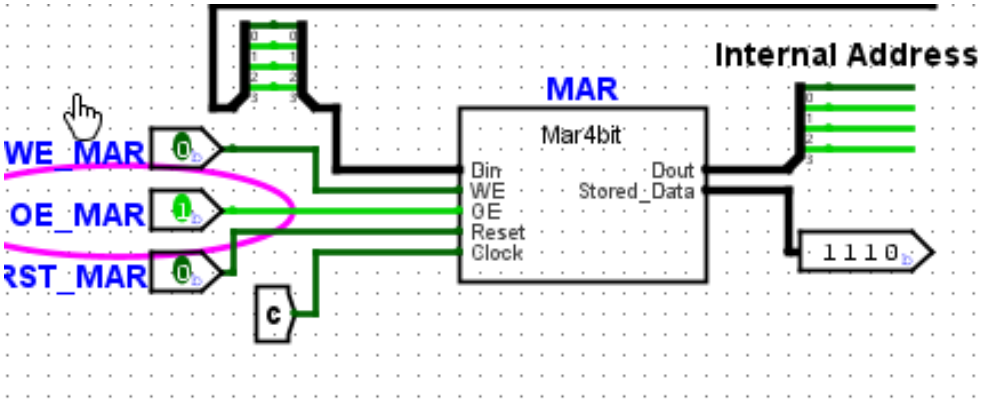

Figure 9: Datapath Memory Address Register Test

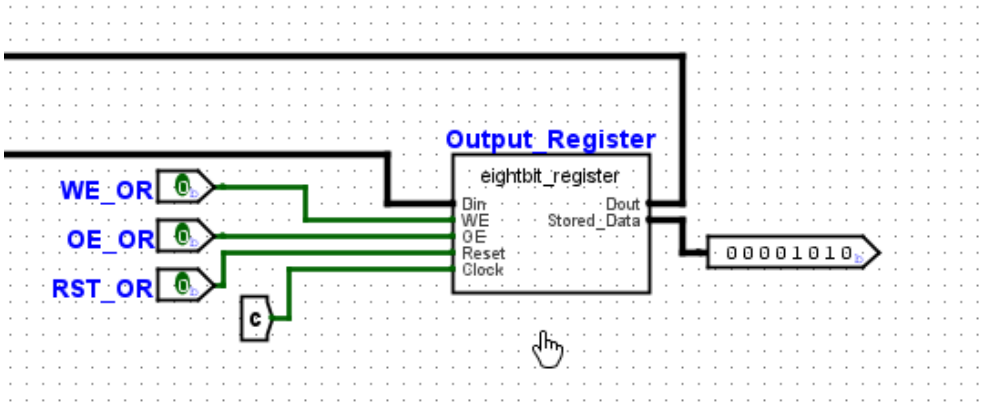

Figure 10: Datapath Output Register Test

Question 1

How does the size and structure of memory cells impact CPU performance?

Solution: The size of a memory structure determines the access latency of the memory, i.e. the larger the memory the slower read and writes to it will be. This affects the performance of the CPU as the CPU will have to wait for the memory to be read or written to before it can continue executing instructions. Therefore smaller memory structures are preferred for better CPU performance in computations.

Question 2

How does the choice of memory hierarchy affect CPU performance in real-world applications?

Solution: The choice of memory hierarchy determines the access latency of the memory, i.e. the larger the memory the slower read and writes to it will be. In real-world applications, the CPU will have to wait for the memory to be read or written to before it can continue executing instructions. Therefore smaller memory structures are preferred for better CPU performance in computations.

Question 3

Discuss the significance of pipelining in CPU design and its relationship with Datapath.

Solution: Pipelining is a technique used to increase instruction level parallelism through overlapping instruction execution stages. This improves CPU design by allowing multiple instructions to be executed simultaneously. For a CPU to be pipelined the Datapath has to support it through the use of registers to store intermediate results of the instruction execution stages, and the ability to independently perform the steps of Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write Back.

Question 4

Explain how the von Neumann architecture impacts modern CPU design and performance.

Solution: The Von Neumann architecture describes a shared memory computation model where instructions and data are stored in the same memory and accessed through the same bus. This can lead to performance issues as instructions and data cannot be accessed at the same time.

Question 5

How do advancements in memory technology, such as non-volatile memory and high-bandwidth memory, shape future CPU architectures?

Solution: Both non-volatile and high-bandwidth memory have implications of reducing memory access latency and increasing memory bandwidth. Non-volatile memory is memory that retains its state even if it is not powered, this can be used to store data that is not accessed as frequently allowing more frequently accesd data to be stored in faster memory. High-bandwidth memory allows for faster data transfer between the CPU and memory as a high-bandwidth allows for more data to be transferred in a given time period. This can be used to increase the performance of the CPU by reducing the time it takes to access memory.