

## Lab 2

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## Part 1

### Question 1

Draw the truth table for the above logical equations for a full adder.

**Solution:**

$a$	$b$	cin	$(a \oplus b) \oplus \text{cin}$	$a \cdot b + b \cdot \text{cin} + a \cdot \text{cin}$
0	0	0	0	0
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1
1	1	0	0	1
1	0	0	1	0
0	1	0	1	1

## Part 2

### Question 2

Compute the additions for the following as 2-bit additions. Indicate their Sum and Carry (overflow).

1.  $00 + 11$
2.  $10 + 01$
3.  $11 + 11$
4.  $01 + 11$

**Solution:**

1.

$$\begin{array}{r} 0 \ 0 \\ + \ 1 \ 1 \\ \hline 1 \ 1 \\ \text{Carry: } 0 \end{array}$$

2.

$$\begin{array}{r} 1 \ 0 \\ + \ 0 \ 1 \\ \hline 1 \ 1 \\ \text{Carry: } 0 \end{array}$$

3.

$$\begin{array}{r} 1 \ 1 \\ + \ 1 \ 1 \\ \hline 1 \ 0 \\ \text{Carry: } 1 \end{array}$$

4.

$$\begin{array}{r} 0 \ 1 \\ + \ 1 \ 1 \\ \hline 0 \ 0 \\ \text{Carry: } 1 \\ 1 \end{array}$$

## Part 3

### Question 3

Compute the arithmetic for the following as 2-bit subtractions using the 2's complement approach. Indicate their Sum and Carry (overflow).

1. 00 - 11
2. 10 - 01
3. 11 - 11
4. 01 - 11

### Solution:

1.

$$\begin{array}{r} 0 \ 0 \\ - 1 \ 1 \\ \hline 0 \ 0 \\ + 0 \ 1 \\ \hline 0 \ 1 \end{array}$$

Carry: 0

Two's Complement

2.

$$\begin{array}{r} 1 \ 0 \\ - 0 \ 1 \\ \hline 1 \ 0 \\ + 1 \ 1 \\ \hline 0 \ 1 \end{array}$$

Carry: 1

Two's Complement

3.

$$\begin{array}{r} 1 \ 1 \\ - 1 \ 1 \\ \hline 1 \ 1 \\ + 0 \ 1 \\ \hline 0 \ 0 \end{array}$$

Carry: 1

Two's Complement

4.

$$\begin{array}{r} 0 \ 1 \\ - 1 \ 1 \\ \hline 0 \ 1 \\ + 0 \ 1 \\ \hline 1 \ 0 \end{array}$$

Carry: 0

Two's Complement

## Part 4

### Question 4

Compute the additions for the following as 8-bit additions. Indicate their Sum and Carry.

1. 1010110 + 110100
2. 11001011 + 1011010

3. 110001 + 11100100
4. 1010001 + 11001

**Solution:**

1.

$$\begin{array}{r}
 0\ 1\ 0\ 1\ 0\ 1\ 1\ 0 \\
 +\ 0\ 0\ 1\ 1\ 0\ 1\ 0\ 0 \\
 \hline
 1\ 0\ 0\ 0\ 1\ 0\ 1\ 0 \\
 \text{Carry: 0}
 \end{array}$$

2.

$$\begin{array}{r}
 1\ 1\ 0\ 0\ 1\ 0\ 1\ 1 \\
 +\ 0\ 1\ 0\ 1\ 1\ 0\ 1\ 0 \\
 \hline
 0\ 0\ 1\ 0\ 0\ 1\ 0\ 1 \\
 \text{Carry: 1}
 \end{array}$$

3.

$$\begin{array}{r}
 0\ 0\ 1\ 1\ 0\ 0\ 0\ 1 \\
 +\ 1\ 1\ 1\ 0\ 0\ 1\ 0\ 0 \\
 \hline
 0\ 0\ 0\ 1\ 0\ 1\ 0\ 1 \\
 \text{Carry: 1}
 \end{array}$$

4.

$$\begin{array}{r}
 0\ 1\ 0\ 1\ 0\ 0\ 0\ 1 \\
 +\ 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1 \\
 \hline
 0\ 1\ 1\ 0\ 1\ 0\ 1\ 0 \\
 \text{Carry: 0}
 \end{array}$$

## Part 5

### Question 5

Compute the arithmetic for the following as 8-bit subtractions using the 2's complement approach. Indicate their Sum and Carry.

1. FF - E6
2. A5 - 6F
3. F2 - D7
4. 110001 - 11100100
5. 1010001 - 11001

**Solution:**

1.

$$\begin{array}{r}
 F\ F \\
 -\ E\ 6 \\
 \hline
 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\
 +\ 0\ 0\ 0\ 1\ 1\ 0\ 1\ 0 \\
 \hline
 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1 \\
 \hline
 1\ 9
 \end{array}$$

Carry: 1

Two's Complement

2.

$$\begin{array}{r} A \quad 5 \\ - \quad 6 \quad F \\ \hline 3 \quad 6 \\ \text{Carry: 1} \end{array}$$

3.

$$\begin{array}{r} F \quad 2 \\ - \quad D \quad 7 \\ \hline 1 \quad B \\ \text{Carry: 1} \end{array}$$

4.

$$\begin{array}{r} 0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \\ - \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \quad 0 \\ \hline 0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \\ + \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \\ \hline 0 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 1 \\ \text{Carry: 0} \end{array}$$

Two's Complement

5.

$$\begin{array}{r} 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \\ - \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \\ \hline 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \\ + \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1 \\ \hline 0 \quad 0 \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0 \\ \text{Carry: 1} \end{array}$$

Two's Complement

## Part 6

### Question 6

How does the digital logic of a full adder circuit differ from that of a half adder?

**Solution:** A full adder includes a carry-in bit, but a half adder does not.

### Question 7

What role does the XOR gate play in the implementation of a full adder circuit?

**Solution:** The XOR gate is used to calculate the sum component of the full adder using the formula  $(a \oplus b) \oplus \text{cin}$ .

### Question 8

How does the carry-out bit in a full adder circuit influence subsequent addition operations?

**Solution:** The carry-out bit is used as the carry-in bit for the next full adder in a series of full adders. This allows for the addition of numbers with more than one bit, pushing the carry bit to the next full adder in the series.

### Question 9

Can a full adder circuit be used to perform subtraction? If so, how?

**Solution:** Yes. To do this the two's complement of the subtrahend is calculated and added to the minuend. This complement can be done by inverting the bits and adding 1 to the least significant bit, which can be done using a NOT gate or an XOR for conditional inversion.

#### Question 10

What is the significance of the XOR and AND gates in a subtractor circuit?

**Solution:** In a purely subtractor circuit, the XOR gate is used to calculate the difference between the minuend and the subtrahend and the AND gate is used to calculate the borrow bit.