Madison Dimaculangan

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Location.Austin, Texas

Education
University of Texas, 2007
B.S. Electrical Engineering

Seeking employment opportunities in multiple industries to apply technical and leadership skills honed over ten years as a microprocessor test engineer in the semiconductor industry. Highly motivated and open to new fields and disciplines.

Skills

Leadership & Coordination	• led small teams of three to four engineers on multiple projects from pre-silicon test planning to bringup and performance characterization to production manufacturing • served in project management role to drive issue triage, management and resolution; both internally and customer-facing
Hardware Equipment	• **ATE test** - experience with both Credence Sapphire and Verigy 93k test program development, silicon performance characterization, and failure debug • **System Level test** - Linux and Windows based experience in application validation, CPU/GPU performance characterization, validating high speed IO, and failure debug
Programming Languages	• **Professional** - **Ruby**, **Perl**, **C++**, **Java,** and **VBA** programming languages to generate test programs and analysis scripts • **Web Development** - HTML5, CSS3, Bootstrap 4 (via online courses)
Other	• Microsoft Office, Atlassian JIRA/Bamboo/Confluence • Filipino Martial Arts (Pekiti Tirsia Kali)

Awards and Accomplishments

Awards
- **Executive Spotlight Award**, 2016
- **Spotlight Award**, 2018, 2016, 2008
- **Spirit of Success Award**, 2012

Accomplishments
- root caused fuse IP fails and validated fixes, resulting in 30% yield recovery
- root caused security IP fails and implemented patch, resulting in 15% yield recovery
- improved production screen for thermal IP, reducing test cost by $2.5 million
- identified failure mechanism for graphics IP fails, resulting in 95% yield recovery
- reduced test time of test flows by 25% by with a more efficient search algorithm

Experience

2008-2018

Member of Technical Staff, Product Development Engineer
Advanced Micro Devices, Austin, Texas

2018-2018

Silicon Debug Lead, Semi-Custom Program Management Team
- **Highlights**
  - Root caused false thermal shutdowns on system platforms to incorrect board connection to signal with hardcoded temperature threshold
  - Executed experiments on internal platforms to replicate customer failure observations, isolated failures, and provided feedback to designers and IP teams
  - Manually screened untested units to compensate for delays in automated test environment and enabled on-time delivery of engineering samples to customer
  - Assembled and delivered system platforms to engineers for bringup
- Triaged incoming customer issues, drive internal debug execution, summarize root cause
- Communicated daily with external customers to ensure alignment on priorities and progress
- Coordinated debug effort across validation, design and product development teams

2017-2018

7nm Product Engineer, Semi-Custom Product Development Team
- Coordinated content enablement across functional areas for integration into characterization flows
- Gathered hardware and software requirements to implement and execute characterization

- Generated and optimized characterization strategy and timeline execution to meet aggressive schedule

2013-2017

16nm Product Engineer, Semi-Custom Product Development Team

- **Products**: PlayStation 4, XBOX ONE S, XBOX ONE X processors
- **Highlights**
  - Led internal teams to debug third-party fuse IP
    - Executed ATE experiments to modulate fuse burn value and duration to validate robustness of the fuse IP's power delivery design
    - Executed ATE experiments to validate fuse IP's addressing design by programming adjacent and non-adjacent addresses
    - Implemented additional fuse stress tests at Wafer SORT and Final Test insertions to better measure yield of fuse IP. Stress tests also later served as volume validation of workarounds and design fixes.
  - Root caused and implemented workaround for intermittent failures in multiple IPs
    - Executed ATE experiments to isolate failures to initialization sequence of the security IP, which is required prior to testing all other IP
    - Validated workaround to separate initialization sequence from the stress portion of the patterns and retry only the initialization sequence on failure, reducing additional test time required
  - Executed unplanned system-level performance characterization experiments
    - Optimized ATE to system correlation, minimizing overkill and improving quality
    - Implemented new automation hooks in the characterization test program to quickly respond to customer's requests for unplanned characterization data and changing requirements
- Triaged internal issues, prioritized according to impact, and drove debug execution
- Designed experiments to test hypotheses, executed experiments and analyzed results
- Generated and executed test plan for system level test content bringup and characterization
- Implemented system level characterization flows in Java programming language

2012-2013

SCAN Test Engineer, Advanced Test and Characterization Team

- **Products**: A4/A6/A8/A10 APU processors for desktops and laptops
- **Highlights**: Debugged Scan pattern issues to improve yield and pattern quality
  - Root-caused zero-yield observation on GPU IP to initialization patterns by dividing patterns into segments and applying different voltages to each and isolating failure
  - Root-caused multiple IO IP patterns to various pattern quality issues including missing signals, inverted expected values, and incorrect initialization sequences.
  - Reported pattern delivery misses to design teams, resulting in much higher quality patterns delivered on future programs
- Generated and executed plan for SCAN test pattern bringup and production flow integration
- Synced with design teams on pattern delivery schedules and pattern quality expectations
- Implemented production screen and characterization flows for both Sapphire and 93k platforms
- Debugged pattern bringup failures and unexpected production yield fallout

2008-2012

System Level Test Engineer, Advanced Test and Characterization Team

- **Products**: Opteron (server), Athlon (desktops, laptops), Ax APU devices (desktops, laptops)
- **Highlights**: Redesigned search algorithms and automated analysis of characterization results
  - Streamlined existing two-step frequency search algorithm into single phase, reducing test time for all frequency searches
  - Implemented analysis scripts to automatically rank applications according to voltage or frequency measurement while also reporting average per-application run-times and offset between worst-case performance limiter and all other applications
- Implemented and executed Ruby content validation and characterization flows
- Performed performance-limiter studies across entire content suite to optimize characterization list.