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Modeling of the EMS VCS3 Voltage Controlled Filter as a Nonlinear Filter Network

Federico Fontana*, *Member, IEEE,* and Marco Civolani

Abstract

A previously developed nonlinear differential equation system, representative of the diode-based voltage-controlled filter on board of the EMS VCS3 analog synthesizer, can be modeled in terms of a filter network. The properties of this network can be converted block-by-block into a discrete-time version of the same model, in which the relationships existing between the system variables take the form of delay-free loops. In the presence of such loops, the discrete-time filter network is solved by iterating over a fixed-point scheme. Simulations running at 176.4 kHz show reasonable fidelity of the model in the regimes of interest, as well as shorter computation time compared to previous implementations of the same system. While reducing aliasing, such a sampling rate optimizes also the computation time as it requires fewer fixed-point iterations. The new model represents an improved alternative to previously developed voltage-controlled filter designs in the field of virtual analog.

Index Terms

Circuit modeling, Digital filters, Nonlinear systems, Voltage controlled filter.

EDICS Category: AUD-SYST Audio Processing Systems

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Modeling of the EMS VCS3 Voltage Controlled Filter as a Nonlinear Filter Network

I. Introduction

The diode-based voltage-controlled filter on board of the *Voltage Controlled for Studio with 3 Oscillators* (VCS3) analog monophonic synthesizer, designed by David Cockerell in 1969 and produced by Peter Zinovieff for the Electronic Music Studio Ltd in London (EMS), is a milestone in the history of electronic music instrument design. The filter incorporates many ideas from its renowned ancestor, the (transistor-based) Moog voltage-controlled filter [1], it was appreciated by many famous musicians of that time, and has been employed also in later musical productions [2].

Musical voltage-controlled filters have been object of research in the field of virtual analog. Stilson and Smith marked an important starting point in the linear modeling of this filter [3]. Later, the Moog filter nonlinearities were tackled by Huovilainen in 2004 by using a circuit-driven approach [4], and by Hélie in 2006 by using a model based on a Volterra expansion of the nonlinearities [5]. While substantially advancing the modeling of the VCF, both works left unanswered the question of how to simulate the instantaneous feedback effects in the presence of runtime changes of the filter parameters.

Research in diode-based voltage-controlled filter simulation began in 2008, with the publication of a nonlinear differential equation system modeling its basic features. In addition, it was computable in real time using a 4th-order explicit Runge-Kutta solver [6]. Importing fundamental knowledge of numerical scheme solutions to ordinary differential equations [7] (or ODEs) results in novel discrete-time computation of ODE-based models for the synthesis and processing of sound. Examples include the evaluation of nonlinear ODE solutions for wind instrument sound synthesis [8], and a comparison of different numerical schemes solving a nonlinear model of the clipping stage in guitar effects [9].

Wave digital filters can be effectively employed as well in the nonlinear analysis of guitar effects [10] and vacuum-tube guitar amplifiers [11].

The accurate real-time computation of these models is made inherently problematic by the presence of nonlinear components in the context of feedback circuits. Moreover, such circuits often allow the control of various parameters (including the amount of feedback) directly through knobs and via additional input signals. Digital simulators which use these controls need to implement solvers whose parameters can

be varied during the computation without introducing artifacts or excessive computational load. These additional constraints make the design of a reliable solver even more problematic.

Methods exist for the discrete-time modeling of nonlinear systems which take the issues of feedback and parameter variability into account. By working either in the Kirchhoff [12] or wave [13] domain, these methods permit numerical solvers to preserve most of the structural properties of the continuous system. In other words, such methods maintain an image of the analog signal flow in the computational procedure, including the feedback chain, time-varying gains and tunable components that change the characteristics of the system at runtime.

Such methods have paved the way for a general definition of a Kirchhoff-based digital filter solution of nonlinear ODE systems, which has allowed the successful simulation of sophisticated systems such as a series of masses connected by nonlinear springs [14], a digital version of the Dolby B CODEC [15], and, more recently, an intracellular signal transduction network governing the circadian cycles in living cells [16]. Compared to traditional ODE solvers based on the discretization of the differential equations, this approach allows the implementation of digital filter networks that establish a structural relationship with the original system. This approach, in particular, has led to a particularly robust and accurate solution of the linear model of the Moog voltage-controlled filter[1] [17].

Encouraged by these results, we have applied the same approach to the analysis and computation of the VCS3 nonlinear filter model [6]. The advantages of the application of the filter network approach essentially consists of i) performing a simple formal passivity analysis of the system, and ii) realizing a simple, efficient fixed-point solver that furthermore proves to be robust against runtime changes of the system's characteristic parameters. In particular, this solver saves about half the computation time compared to the Runge-Kutta solution [6] while maintaining close correspondence to offline simulation results obtained using the PSpice software (Taken here as a reference for its accuracy [18]).

The paper is organized as follows: Sec. II describes the analog circuit, its nonlinear ODE-based state-space representation, and the resulting filter network model; Sec. III contains the passivity analysis of the filter network; Sec. IV explains how the solution is computed; Sec. V proposes a map that sets the cutoff frequency of the system; Sec. VI provides figures from tests conducted on the system; Sec. VII discusses the model performances. Finally, the conclusions point out the current limits as well as potential developments of this research.

Audio files resulting from the simulations in Sec. VI can be retrieved from http://profs.sci.univr.it/

[1]This has been part of the filter palette of the SuperCollider real-time environment under the name MoogFF since 2007.

~fontana/TASL2009/.

II. MODEL

A. Analog Network

The analog network that realizes the VCS3 voltage controlled filter (abbreviated VCF from here on) is shown in Fig. 1. The diodes D1-D14 are kept forward biased by the current source transistor Q3. The control exerted on this current by Q4 through the voltage V_{CV} determines the characteristic point of the diodes. This point in particular sets the differential resistance, and hence the frequency cutoff parameter of the RC ladder formed by the diodes D1-D8 and capacitors C1-C4, by controlling the time constant of the equivalent nonlinear circuit.

Variations are added to the current flowing across the ladder by driving the transistor Q1 through the (audio) voltage signal V_{IN}. The cutoff applies to these variations if V_{IN} changes more rapidly than V_{CV}. For this reason the current is treated as a superposition of two components, I_0 and $i(t)$, that are respectively associated to the bias and the audio input. Typical voltages for the audio signal V_{IN} range between 1 mV and 1-1.5 V. The bias current can reach 150 μA when V_{CV} amounts to about 150 mV, these values result in a cutoff frequency around 10 kHz.

By feeding to Q2 the voltage over C4 through R_9 (56 kΩ) and R_{13} (0 to 500 kΩ) the ladder structure becomes part of a loop, giving rise to oscillations in the signal at the cutoff region. The variable gain resistor R_{13} is put in parallel with an operational amplifier from which the output voltage V_{OUT} is picked up.

The amplitude and persistence of these oscillations depends on the feedback gain $K = R_{13}/R_9$ [6]. By varying the resistance R_{13}, gains between 0 (open loop) and 500/56 ≈ 10 can be set.[2]

Both K and I_0 are set using knobs, that respectively control R_{13} and a dc voltage generator attached to V_{CV}. Furthermore, a sinusoidal or square wave tunable in the range [0,500] Hz can be added to this offset by making use of the LFO that is onboard the synthesizer.

B. Differential Model

The differential model [6] consists of a standard state-space representation of a nonlinear differential system with state $v_{C_1}, \ldots, v_{C_4}$ (corresponding to the voltage over the respective capacitors C1, ..., C4,

[2]Using recently restored VCS3 at the Conservatorio "G.B. Rossini" in Pesaro (Italy), the system oscillates above gains between 6 and 7. Furthermore gains close to 10 enable indefinitely long lasting oscillations, even in the presence of a null input signal due to thermal noise.

all having capacitance equal to C), input v_{IN} (corresponding to the voltage signal V_{IN}), and output v_{OUT} (corresponding to the voltage signal V_{OUT}):

$$\begin{cases} \dot{v}_{C_1} = \dfrac{I_0}{2C}\left(\tanh\dfrac{v_{IN}-v_{OUT}}{2V_T} + \tanh\dfrac{v_{C_2}-v_{C_1}}{2\gamma}\right) \\ \dot{v}_{C_2} = \dfrac{I_0}{2C}\left(\tanh\dfrac{v_{C_3}-v_{C_2}}{2\gamma} - \tanh\dfrac{v_{C_2}-v_{C_1}}{2\gamma}\right) \\ \dot{v}_{C_3} = \dfrac{I_0}{2C}\left(\tanh\dfrac{v_{C_4}-v_{C_3}}{2\gamma} - \tanh\dfrac{v_{C_3}-v_{C_2}}{2\gamma}\right) \\ \dot{v}_{C_4} = \dfrac{I_0}{2C}\left(-\tanh\dfrac{v_{C_4}}{6\gamma} - \tanh\dfrac{v_{C_4}-v_{C_3}}{2\gamma}\right) \\ v_{OUT} = (K+1/2)\, v_{C_4} \end{cases} \tag{1}$$

in which $\eta = 1.836$, $V_T = 26$ mV, $\gamma = \eta V_T = 48$ mV, and $C = 0.1$ μF.

It is easy to see that the system has a fixed point at the origin corresponding to null charge at the capacitors. At this point the system energy is null, independently of the bias current. In fact, I_0 is treated as a system parameter, not as a signal.

Once solved using an explicit fourth-order Runge-Kutta scheme, this system provides accurate real-time simulations of the VCF on a 2 GHz Core 2 Duo MacBook laptop under the PureData processing environment [19], in which the whole solving procedure was realized in C++ [6] and, later, in Java [20]. The Runge-Kutta solution was tested against off-line PSpice simulations of the analog network of Fig. 1 using sinusoidal chirps as inputs to the filter and comparing spectrograms of the corresponding outputs. Its perceived quality received positive feedback from an expert audience [20].

A derivation of the differential model from the analog circuit is proposed in the appendix.[3]

C. Filter Network Model

The system (1) can be straightforwardly translated to the filter network of Fig. 2, in which we have distributed the functional relationships into elementary filter blocks that are connected together. Noticeably, these blocks are structurally simple. The network in fact contains gains and adders, four integrators, and five memoryless nonlinearities denoting a common function, the hyperbolic tangent.

The complexity of the network comes from the delay-free loops that are nested inside it, reflecting the instantaneous relationships that are provided by the nonlinear differential system. Their existence makes the translation of the network into a computational procedure a difficult task that is further complicated by the presence of the nonlinear blocks across loops. Conversely, the presence of linear transfer functions

[3]Unfortunately, the algebra developed in [6] to obtain the same model contains a small, substantial typo that nullifies the derivation.

such as the integrators does not pose specific problems, since methods exist that transform these functions into corresponding discrete-time filter blocks [21].

In general, a network model of a nonlinear differential equation system transfers the complexity of the system to the network structure. Once we find a convenient way to compute this structure, then the individual blocks (either linear or nonlinear) usually raise minor computational issues. Therefore, the reason why we choose to compute a network instead of a numerical method capable of computing the whole equation set (e.g. Runge-Kutta), is that if we find an efficient way to solve the delay-free loops in the network, then we i) obtain a simple control layer, preserving the direct access to the analog filter parameters in the discrete-time system, particularly I_0 and K in the case of the VCF; ii) gain complete local control on the accuracy of the continuous-time to discrete-time transformation, and iii) have possibilities to realize a faster computation procedure compared to traditional numerical integration methods.

In Sec. IV we will assess the approximation introduced by the discrete-time versions of the integrators. Additionally, the error resulting from the numerical solution of the delay-free loops will be quantified.

III. Passivity of the Filter Network

Before addressing computational issues, an analysis of system passivity can be done. Passivity depends on the power flowing across a system. If the inflow of power is always nonnegative, then the system can be said to be passive [22]. Space-state representations of electrical circuits, such as the system (1), must preserve passivity. Otherwise, a model can emit and store more energy than it absorbs across a period of time, even if the modeled circuit is passive. Finally, passivity is the starting point for investigating the stability of a system. We do not demonstrate stability for our VCF model, meanwhile providing hints for figuring out this property.

In our analysis, we will look at the continuous-time network of Fig. 2 as an interconnection of passive nested loops. We then show that their passivity implies passivity of the whole network. By mapping the integrators into passive discrete-time blocks, it will be easily demonstrated that the overall discrete-time system is passive as well.

A. Continuous-Time Filter Network

While demonstrating the passivity of the continuous-time filter network, we will make use of the following results from control theory [22]:

- a nonlinear resistive characteristic $y = f(x)$, such that $xy \geq 0$ for every x, is passive;

- a transfer function $H(s)$ which i) has no poles in $\mathrm{Re}\{s\} > 0$, ii) is such that $\mathrm{Re}\{H(j\omega)\} \geq 0$ for every ω that is not a pole for $H(j\omega)$, and iii) has only simple poles with positive residuals on the imaginary axis, is called *positive real* and corresponds to a passive system;
- the negative feedback connection of two passive systems is passive.

Let us consider the subnetwork $\mathcal{F}_{2\gamma}$ in Fig. 3. It consists of a nonlinearity in negative feedback with the integrator, along with two loop specific gains. Now, from the above results:

1) $H(s) = 1/s$ is a positive real transfer function.
2) $y = \frac{I_0}{2C} \tanh \frac{x}{2\gamma}$ is a passive characteristic.

Thus, $\mathcal{F}_{2\gamma}$ is passive.

An identical result holds if we in particular select the loop with the lowest gain in the network. Since the gain in series with the integrator is equal to $1/(6\gamma)$, we will label this subnetwork as $\mathcal{F}_{6\gamma}$.

In the case of the simple loop shown in Fig. 3, passivity can be also checked directly. In fact, $\mathcal{F}_{2\gamma}$ is described by the state-space representation $|\dot{X}\ Y|^T = |f(X,U)\ h(X,U)|^T$ with input $U = |x_{IN}\ y_{IN}|^T$, state $X = x_{OUT}$, output $Y = |x_{OUT}\ \ y_{OUT}|^T$, where

$$\begin{aligned} f(X,U) &= \frac{I_0}{2C}\left(U_1 + \tanh\frac{U_2 - X}{2\gamma}\right) \\ h(X,U) &= \left|X \ \ \tanh\frac{U_2 - X}{2\gamma}\right|^T. \end{aligned}$$

The time derivative of the storage function $V(X) = CX^2/I_0$ is given by

$$\begin{aligned} V'(X)f(X,U) &= X\left(U_1 + \tanh\frac{U_2 - X}{2\gamma}\right) \\ &= Y_1U_1 + Y_2U_2 + Y_2(X - U_2). \end{aligned}$$

Moreover,

$$(X - U_2)Y_2 = -(U_2 - X)\tanh\frac{U_2 - X}{2\gamma} \leq 0.$$

Hence,

$$\frac{d}{dt}V\big(X(t)\big) \leq U(t)^T Y(t),$$

proving that $\mathcal{F}_{2\gamma}$ is passive (note that V is proportional to the energy $(C/2)v_C^2$ stored inside the capacitance).

An identical result holds for $\mathcal{F}_{6\gamma}$.

Passivity can be addressed also using formal tools drawn from electrical network theory. From (12) in the appendix, we evince that γ puts the current i_D in relation with the voltage v_D measured over each diode in the VCF. Hence, $\mathcal{F}_{6\gamma}$ models the nonlinear RC series formed by the six diodes D9-D14

and capacitor C4. Similarly, the three blocks $\mathcal{F}_{2\gamma}$ respectively model the series D7-C3-D8, D5-C2-D6, and D3-C1-D4. If we treat each block separately, then we have that the block resistance R is coupled to the corresponding capacitance C through the voltage reflectance $(1 - RCs)/(1 + RCs)$. This reflectance provides dissipation, hence passivity, even if R randomly varies along time across any positive range. Thus, each block is passive in particular for any nonlinear resistive characteristic [23].

Now, it is true that $\mathcal{F}_{6\gamma}$ is in negative feedback with the above loop, $\mathcal{F}_{2\gamma}$. Hence, the resulting subnetwork $\mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma}$ (see also Fig. 4) is formed by the negative feedback loop of two passive systems. Similarly to what we did for $\mathcal{F}_{6\gamma}$ and $\mathcal{F}_{2\gamma}$, we conclude that $\mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma}$ is a passive subnetwork.

We can apply this result recursively: by connecting $\mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma}$ via a negative feedback to the above nearest loop, $\mathcal{F}_{2\gamma}$, we in fact obtain the following subnetwork:

$$(\mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma}) \circ \mathcal{F}_{2\gamma} = \mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma} \circ \mathcal{F}_{2\gamma},$$

which is again passive. One further recursion leads to the conclusion that the feed-forward part

$$\mathcal{F} = \mathcal{F}_{6\gamma} \circ \mathcal{F}_{2\gamma} \circ \mathcal{F}_{2\gamma} \circ \mathcal{F}_{2\gamma}$$

of the VCF chain is passive.

The feedback branch of the VCF consists of two positive gains equal to $K + 1/2$ and $1/(2V_T)$ respectively in series with an hyperbolic tangent block. We call this branch $\mathcal{G}$. As shown earlier, $\mathcal{G}$ is passive. The subtraction $v_{IN} - v_{OUT}$ (represented by the top left adder in Fig. 2 shown in Fig. 4 as well) implies that $\mathcal{G}$ forms a loop with $\mathcal{F}$ by means of negative feedback. Hence, $\mathcal{F} \circ \mathcal{G}$ is passive.

B. Discrete-Time Filter Network

The considerations we have made in the previous subsection ensure that the filter network is passive. This conclusion is not surprising since, as explained in Sec. II, the system (1) does not model the bias current as a signal nor considers the activity of the operational amplifier. Interestingly, identical considerations can be exported one-by-one to any discrete-time network in which every block is transformed into a digital component that preserves passivity [24]. In the case of the VCF, care must be paid only to the integrators: All the other elements of the network in fact need no transformation. The nonlinearities, in particular, preserve dissipation (and, hence, passivity) during the transformation since they can be exported to the discrete-time network directly.

A *discrete* positive real function $H_D(z)$, $z \in \mathbb{C}$, is analytic in $|z| > 1$ and such that $\mathrm{Re}[H_D(z)] \geq 0$ in $|z| \geq 1$. Analogously to the continuous-time case, it defines a passive block. It is straightforward to

verify that the bilinear transformation [25] maps analog integrators $H(s) = 1/s$ into digital filters having a discrete positive real transfer function of the form

$$H_D(z) = \frac{1}{2F_S}\frac{1+z^{-1}}{1-z^{-1}}, \tag{2}$$

where F_S is the sampling rate of the digital system. Thus, applying the bilinear transformation to the integrators ultimately ensures that the discrete-time network is passive.

We know from nonlinear control theory that passivity is not sufficient for proving stability in a system [22]. Specifically, the integrators in the VCF may store energy indefinitely from a dc component traveling across the network. As an experiment, we biased the audio input v_{IN} by superimposing a 10 volts dc (a very unusually large offset for this circuit), and have shown that the system responds to such a component by adding a dc component to v_{OUT} that amounts to a few millivolts. Even in this case, then, the VCF model reveals stable behavior.

The existence of an upper limit to the stored energy in a system can be proved through the definition of a suitable Lyapunov function [26]. Even if we have not proved the Lyapunov stability of the VCF network model, yet a storage function of the complete system is probably an aggregation of functions V similar to that defined in Sec. III-A (adapting inputs, states, and outputs to the complete system).

IV. Computation of the Filter Network

A. Selection of a Numerical Solver

Fig. 2 illustrates that at every temporal step the output $v_{OUT}[n]$ takes a value that, while it is instantaneously fed back into the network, does not perturb the system. In other words, any output sample must satisfy an implicit nonlinear equation which can be written as (by making use of the notation introduced in Sec. III)

$$(\mathcal{F} \circ \mathcal{G})\,(v_{OUT}) = v_{OUT}. \tag{3}$$

In particular, if the repeated computation of (3) made by starting from a value $v^*_{OUT}[n]$ converges to $v_{OUT}[n]$, then we can approximate the solution by updating the value $v^*_{OUT}[n]$ in the computation of $(\mathcal{F}\circ\mathcal{G})\,(v^*_{OUT}[n])$ until the absolute difference $|v^*_{OUT}[n]-(\mathcal{F}\circ\mathcal{G})\,(v^*_{OUT}[n])|$ falls below a given tolerance. The fixed-point solver—a numerical recipe that has been long used to solve nonlinear systems—is based exactly on this assumption [22].

In the next section it will be shown that the VCF filter network can be computed using a fixed-point solver, if sufficiently high sampling rates are used. In fact, under these rates the network possesses a

constant $M_p < 1$ such that:

$$|(\mathcal{F} \circ \mathcal{G})(v_{OUT}) - (\mathcal{F} \circ \mathcal{G})(v^*_{OUT})| \leq M_p |v_{OUT} - v^*_{OUT}|. \tag{4}$$

M_p is called a *Lipshitz* constant [16], [22]. An exact calculation of M_p has not been attempted in this paper. However, its dependency on the model parameters K and I_0 and the sampling rate F_S can be estimated in the particular case of convergence toward the null fixed point (i.e., $v_{OUT} = 0$).

We can first swap (due to linearity) the positions of the fourth (i.e. lowest) digital integrator and gain $I_0/(2C)$ in Fig. 2, then formulate a relationship between the input signal x_4 to this integrator and the output v_{OUT}. By recalling that (2) implies

$$v_{C_4}[n] = \frac{1}{2F_S} x_4[n] + s_4[n], \tag{5}$$

with the state s_4 of the integrator being equal to

$$s_4[n] = \frac{1}{2F_S} x_4[n-1] + v_{C_4}[n-1], \tag{6}$$

then we get

$$\begin{aligned} v_{OUT}[n] &= \left(K + \frac{1}{2}\right) \frac{I_0}{2C} v_{C_4}[n] \\ &= \left(K + \frac{1}{2}\right) \frac{I_0}{2C} \left(\frac{1}{2F_S} x_4[n] + s_4[n]\right) \\ &= \left(K + \frac{1}{2}\right) \frac{I_0}{2C} \left(\frac{-1}{2F_S} x_4[n] + \frac{1}{F_S} \sum_{i=0}^{n} x_4[i]\right). \end{aligned} \tag{7}$$

in which the summation in the last formula is obtained by recursively substituting (6) and (5) in (7), that corresponds to replacing the IIR formulation (2) of the discrete-time integrator with the FIR version. By considering that x_4 is a function of v_{OUT} in its own, and neglecting the term $-x_4[n]/(2F_S)$ for simplifying the notation, then the substitution of (7) into (4) in the case of the null solution $(\mathcal{F} \circ \mathcal{G})(0) = 0$ yields

$$(K + \frac{1}{2}) \frac{I_0}{2C} \frac{1}{F_S} \left| \sum_{i=0}^{n} x_4(v^*_{OUT}[i]) \right| \leq M_p \left| v^*_{OUT}[n] \right|. \tag{8}$$

Hence, the Lipshitz inequality can, in principle, be satisfied if the term $(K + \frac{1}{2}) I_0/(2CF_S)$ is reasonably small. Since we lack the exact dependency of x_4 from v^*_{OUT} we cannot provide precise boundaries for M_p. In spite of this, we speculate that higher sampling rates benefit the convergence of the fixed-point solver, whereas higher values of K and I_0 do not.

The dependency on sampling rate has general validity: numerical ODE solvers converge faster when the discretization step is set to be smaller [9]. Ultimately, this means that bigger computational effort needed to synthesize sound at higher sampling rates is counterbalanced (on average) by less fixed-point

iterations during the computation of every sample. Conversely, the dependencies on K and I_0 suggest that higher feedback gains and cutoff frequencies are more computationally demanding. In Sec. VII we will show why the factor $(K+1/2)$ is not critical, while the value I_0 can seriously affect the convergence of the fixed-point solver.

Alternative, more efficient schemes are employed in numerical analysis. In the field of virtual analog it is common to encounter implicit systems that are solved using Newton-Raphson or quasi-Newton methods [9]. In Sec. VII we will see that, concerning our VCF model, the fixed-point solver is sufficiently fast for guaranteeing satisfactory real-time performances on current hardware without sacrificing on the accuracy of the solution. (Simulations done with explicit fourth-order Runge-Kutta have been object of previous research [6].)

B. Selection of a Fixed-Point Scheme and Resulting Algorithm

An explicit fixed point scheme can be obtained by computing the signal along the path highlighted by the bold line in Fig. 2. Note that this particular scheme approximates the discrete-time computation of $\mathcal{F} \circ \mathcal{G}$, since every adder belonging to the feed-forward subnetwork $\mathcal{F}$ is explicitly computed by using the previously iterated value of the signal incoming from the bottom branch.

Assuming a typical relative tolerance equal to 10^{-4} (this corresponds to computing the numerical solution with a relative error of -80 dB at every step) the fixed-point solver is realized by the following portion of pseudo-code, in which $u_1, \ldots, u_5$ are respectively the outputs from the hyperbolic tangent blocks of Fig. 2 in top-down order, $s_1, \ldots, s_4$ are the states (6) of the digital integrators in the same order, and asterisks denote values computed at the previous iteration:

Set $v^*_{OUT} = v^*_{C1} = \ldots = v^*_{C4} = 0$
Set $u^*_1 = \ldots = u^*_5 = 0$
Set $s_1 = \ldots = s_4 = 0$
repeat
  Read v_{IN}
  repeat
    Compute $u_1 = \tanh \frac{v^*_{OUT} - v_{IN}}{2V_T}$
    Compute $v_{C1} = \frac{I_0}{2C} \frac{1}{2F_S}(u^*_2 + u_1) + s_1$
    Compute $u_2 = \tanh \frac{v^*_{C2} - v_{C1}}{2\gamma}$
    Compute $v_{C2} = \frac{I_0}{2C} \frac{1}{2F_S}(u^*_3 - u_2) + s_2$
    Compute $u_3 = \tanh \frac{v^*_{C3} - v_{C2}}{2\gamma}$

12: Compute $v_{C3} = \frac{I_0}{2C}\frac{1}{2F_S}(u_4^* - u_3) + s_3$

13: Compute $u_4 = \tanh\frac{v_{C4}^* - v_{C3}}{2\gamma}$

14: Compute $v_{C4} = \frac{I_0}{2C}\frac{1}{2F_S}(-u_5^* - u_4) + s_4$

15: Compute $u_5 = \tanh\frac{v_{C4}}{6\gamma}$

16: Compute $v_{OUT} = (K + 1/2)v_{C4}$

17: **until** $|v_{OUT} - v_{OUT}^*| < 10^{-4}|v_{OUT}^*|$

18: Compute s_1, s_2, s_3, s_4

19: **until** The dsp goes off.

Lines 8, 10, 12, and 14, implement the recurrent input/output relationship (5) for each integrator. The network state is updated at line 18 by computing (6) again for each integrator.

Every iteration asks the processor to compute (refer to Fig. 2) ten multiplies, each by the respective gain coefficient, one multiply-and-add (5) for every integrator, five images of a hyperbolic tangent function, and eight sums. The state of the integrators is refreshed using (6) *after* the fixed-point scheme has converged to the solution.

Since several large multiplying coefficients are involved, the computations can be more easily implemented in floating-point hardware. In particular, the proposed procedure runs efficiently in current general purpose CPU's providing specific DSP-oriented micro-code optimizations [27].

C. Accuracy of the Discrete-Time Integrators

We next discuss the precision of the analog-to-digital transformation.

Fig. 5 shows that the discrete-time transfer function $H_D(z)$ (2) obtained by bilinear transformation of $H(s) = 1/s$ differs by less than 1 dB at $\pi/3 \approx 1$ rad/s. For example, if the sampling rate is set to $F_S = 120$ kHz this difference is located at approximately $(120/2)/3 = 20$ kHz, a typical upper limit of audible frequencies. The bilinear transformation, hence, ensures an overall magnitude frequency deviation below 1 dB when the digital integrators work at 120 kHz.

Notably, the same map does not introduce deviations in the phase: Since $\arg\{H_D(e^{i\omega})\} = -\pi/2$ if $0 < \omega < \pi/2$, then the phase responses of the analog and discrete-time integrator are identical in this angular frequency range. This property is especially desirable in the VCF model, whose integrators are spread over the filter network in such a way that phase deviations in these components may introduce audible artifacts in the system response.

As we will see in the next section, in absence of methods for limiting the aliasing, the VCF must be simulated using sampling rates that are above twice the perceived bandwidth in humans. Our simulations

run at $4 \cdot 44.1 = 176.4$ kHz. In Sec. VII it will be shown that this choice of the sampling rate is not critical from a computation viewpoint.

V. Cutoff Frequency Map

In Sec. II we have seen that the cutoff frequency is shifted by varying the resistive components of the RC ladder. Since each diode has a differential resistance $r_d = \eta V_T / I_0$ [6], the equivalent time constant 1/RC of the ladder is proportional to the factor $1/(r_d C) = I_0/(\eta C V_T)$. By experimenting with several sampling rates during the computation of the responses (appearing in the next section), we have empirically found the following relationship between the analog angular frequency ω_0 and the bias current: $\omega_0 = I_0/(8CV_T)$. In practice we used the frequency warping $\omega = 2F_S \tan(\pi f/F_S)$ induced by the bilinear transformation, mapping angular frequencies ω of the analog signals into frequency values f of the discrete-time signals, then checked that the bias current

$$I_0 = 8CV_T\omega_0 = 8CV_T 2F_S \tan(\frac{\pi f_0}{F_S}), \tag{9}$$

provided an accurate positioning of the cutoff frequency f_0 of the discrete-time system across a broad range of sampling rates. Eq. (9), in conclusion, yields the bias current I_0 that sets the cutoff point of the discrete-time model at f_0.

The frequency warping map determines a nonlinear inverse relationship between F_S and I_0. As a consequence, if the sampling rate is increased holding the same cutoff frequency, then the decrease in the bias current of the discrete-time model is not proportionally smaller. In Sec. VII we will see the consequences of this dependency on the control of the computational load, occurring during simulations in which the cutoff frequency is set to large values.

VI. System Response

Inspection of the dynamic behavior of the filter network in response to a certain number of inputs gives an idea of the characteristics of the system. First, we examine what happens at several feedback gain and cutoff frequency values by simply injecting discrete-time impulses having different amplitudes, i.e., $v_{IN}[n] = A_0\,\delta[n]$. $A_0 = 0$ dB corresponds to a reference amplitude of 1 V, normally a large input value for the VCF.

For small feedback values the VCF network behaves essentially as a tunable linear lowpass filter in series with a dynamic gain. Figs. 6a-6c, in fact, show that values of K between 1 and 4 give rise to a smooth resonance peak followed by a cutoff region, whose shape is not affected by the input amplitude.

The nonlinear effects become prominent for higher values of K. In this range, distortion increases proportionally with the cutoff frequency value. The feedback value and cutoff point also set the characteristics of the oscillations. Figs. 6a-6c show that at $K = 6$ the decay time of such oscillations depends on the energy of the input signal as well.

For large feedback values, distorted self-oscillations arise which saturate the dynamics independently of the input amplitude and type. Fig. 6d illustrates the effect of a very high K value, using a 0 dB impulse. In this case the system saturates for every choice of the cutoff frequency.

The transition from lowpass to oscillatory behavior is especially interesting to test. The spectrogram in Fig. 7 (audio file `vcf_changedInputGain.wav`) is obtained by increasing the amplitude A_0 of a discrete sine wave having a constant frequency equal to 500 Hz. The amplitude of the sinusoid grows exponentially across 10 s by linearly varying its value in dB over the range [-80,0], while constantly keeping f_0 at 10 kHz. Only the range [-40,0] is plotted, as lower amplitudes produces a spectrum containing only the input and the resonance frequency, as in the left part of this spectrogram.

As the amplitude of v_{IN} increases, it can be seen that side components of the resonance arise in positions that are odd multiplies of the frequency of the input signal. Furthermore, when the amplitude of the input is turned beyond -10 dB then the resonance frequency slides down to lower values. In fact, due to the specific nonlinear model used for describing the transistors [6], the application of high voltages to the base of the BJT's Q1 and Q2 under sufficient feedback gain values determines an appreciable net dc current that is superimposed on I_0, hence reducing the bias of the ladder and, consequently, its differential resistance. This resonance "sliding" is also seen in PSpice simulations of the analog network of Fig. 1 and it can be heard by turning up the amplitude of the VCS3 oscillators when the VCF resonates.

If we instead vary the cutoff frequency across time, then we obtain different distortion effects. The spectrogram in Fig. 8 results by feeding the system with an input sine wave having a frequency of 500 Hz and a constant amplitude A_0 equal to -40 dB. While keeping $K = 6$, f_0 is swept across the range [0,14] kHz in 10 s. Under these conditions a swept tone at the resonance frequency is output from the system together with the first odd distortion component. At a lower dynamics, and for cutoff values below about 4 kHz, a component whose frequency is the absolute difference between the swept tone and its main distortion component is produced, along with its own first odd side component due to the input tone (The resulting sound can be heard from `vcf_changedCutoffFreq.wav`). The almost complete corruption of the output occurring when f_0 is turned beyond 12 kHz is discussed in the next section.

VII. PERFORMANCES

Fig. 9 (left) shows numbers of iterations needed, using the -80 dB error tolerance, to compute the spectrogram of Fig. 7. Changes in the amplitude of the input signal are not critical in terms of computational effort. At most 51 iterations are needed to compute the output: this maximum occurs when the amplitude of the input signal amounts to -70 dB. On average, 14.2 iterations are needed to compute the output.

Similar figures are obtained when K is swept from 0 to 10, even using high frequency and amplitude input signals and large cutoff values. For instance, if the system has a cutoff frequency of 10 kHz and is fed with a 10 s sinusoid having amplitude of 1 V and frequency amounting to 5 kHz, then we have a peak of 37 iterations (at about $K = 2$) and 11.8 iterations on average (Fig. 9, center). Repeating the same simulation with the amplitude of the input signal set to 1 mV results in a peak of 56 iterations at about $K = 9.5$, and 14.4 iterations on average (Fig. 9, right).

Different results are obtained when the cutoff frequency is varied instead: Fig. 10 shows iterations needed to compute the spectrogram of Fig. 8. As opposed to input amplitude and feedback, increasing the cutoff frequency causes the number of iterations to explode exponentially. In our simulation the fixed-point search goes out of control when f_0 becomes larger than 12 kHz. Bounding the search doesn't help: The same spectrogram shows that the output signal (heard by listening to `vcf_changedCutoffFreq.wav`) is overwhelmed by numerical artifacts if the iteration scheme is forced to break after 100 loops. Running the same simulation using a larger input amplitude shifts the exponential curve ahead by few kHz, causing convergence failure at higher frequencies, but without changing the general trend shown in Fig. 10.

The impact on computational load caused by changes in cutoff frequency, as opposed to feedback gain, can be interpreted by keeping in mind the inequality (8). In fact, the factor $(K+1/2)I_0$ in this inequality is increased by about 26 dB by moving K from 0 to 10. Conversely, it is increased by about 40 dB as f_0 moves upward across the range [0.1,10] kHz, causing I_0 to grow according to Eq. (9).

Variations in the sampling rate have negligible influence on the relative range of I_0, that always amounts to about 40 dB in the rates of interest. In parallel, due to the warping effect that we have seen in Sec. V, the value of I_0 is left almost unchanged by varying F_s above 176.4 kHz, if the cutoff frequency is set to values around 12 kHz. This implies that increasing the sampling rate does not help reduce the impact on computational load of the cutoff frequency.[4]

[4]On the other hand, the filter onboard our VCS3 machine cuts off at about 5 kHz when the resonance knob is turned at maximum. In this sense, the performance of the model is more than satisfactory.

Another artifact that appears in the discrete-time model, called aliasing, is caused by the spectral energy that is produced by the nonlinear blocks beyond the Nyquist frequency, $F_S/2$. As opposed to what happens in an analog system, this energy is reflected back to the discrete-time frequency domain. In our case, a component of the hyperbolic tangent that should be at frequency $F_S/2 + \tilde{f}$ falls at $F_S/2 - \tilde{f}$ instead. Clearly, aliasing gives rise to artifacts as soon as the reflected components reach the audible band with an energy sufficient for their perception.

Under high dynamics the VCF generates considerable distortion components that cannot be confined below the Nyquist frequency even if sampling at 176.4 kHz. The spectrogram in Fig. 11 is obtained by linearly sweeping a -40 dB sine tone across the range [0,20] kHz in 10 s, with $f_0 = 10$ kHz and $K = 6$. The genuine analog distortion components can be recognized by having a common focus at the coordinate point (10,10) kHz. In fact, when the input signal has this frequency then all the sums and differences between the cutoff and input frequency fall out of the range [0,20] kHz, as is shown in this spectrogram. Conversely, the other spectral lines which spread over the spectrogram are caused by aliasing.

Techniques for attenuating or removing aliasing from virtual analog designs are mainly based on the algebraic manipulations of nonlinearities to control their spectral behavior [28]. One popular strategy consists of substituting the nonlinear function with a truncated version of its Taylor series. This strategy works well when the series converges to the nonlinear function. Unfortunately this condition is not always true for our model, as the amplitude values entering the nonlinear network blocks go often beyond the domain of convergence of the Taylor series of the hyperbolic tangent ($[-\pi/2, \pi/2]$, even smaller if few terms are summed).

In alternative to Taylor series, Volterra series can be employed as a model of the entire nonlinear system while keeping aliasing under control [5]. Besides possible computational issues arising when such a model must be implemented in real time, this approach can become problematic due to restrictions in the convergence domain of these series.

Finally, we wondered whether decreasing the sampling rate saves simulation time. If so, then the corresponding increment in the efficiency should be traded with the loss in accuracy. Perhaps surprisingly, the answer is negative [9]. In fact, we have found that a reduction of the sampling rate *increases* the computational effort.

The histograms in Fig. 12 show how many times the fixed-point solver converges in the iterations specified by the abscissa. (Black bars: $F_S = 4 \cdot 44.1$ kHz; grey bars: $F_S = 3 \cdot 44.1$ kHz; white bars: $F_S = 2 \cdot 44.1$ kHz.) Occurrences of the data are expressed logarithmically: for instance, the grey bar

having edge amounting to 4 at abscissa 45 means that in a simulation running at $F_S = 3 \cdot 44.1$ kHz, the fixed-point solver has converged $10^4 = 10000$ times in between 41 and 50 iterations. All the data have been obtained by feeding the system with a 500 Hz sine tone having amplitude $A_0 = 0$ dB, with $f_0 = 10$ kHz and $K = 6$. Outputs at 1 s ($F_S = 4 \cdot 44.1$ kHz), 1.33 s ($F_S = 3 \cdot 44.1$ kHz), and 2 s ($F_S = 2 \cdot 44.1$ kHz) have been considered in order to collect the same number of data for all histograms. These simulation times ensure also that the system works in stationary regime along the simulation.

It is evident from Fig. 12 that reducing the sampling rate increases the iterations. Under the simulation conditions outlined above, the system makes on average 11.12, 35.66, and 93.4 iterations for computing every sample at 4, 3, and 2 times 44.1 kHz respectively. The number of samples that must be processed is proportional to the sampling rate, hence switching from $4 \cdot 44.1$ to $3 \cdot 44.1$ kHz does not result in lighter computation since the iterations correspondingly increase by a factor three on average. Switching down to $2 \cdot 44.1$ kHz even increases the computational burden. As validation, when computing these histograms using Matlab software, we have obtained 1 s simulation times equal to 1.19 s ($F_S = 4 \cdot 44.1$ kHz), 2.76 s ($F_S = 3 \cdot 44.1$ kHz), and 5.07 s ($F_S = 2 \cdot 44.1$ kHz) to find the black, gray, and white bars, respectively.

Sampling rates of 6 and 8 times 44.1 kHz do not improve the computational performance, resulting in average iterations amounting to 9.83 and 8.74, respectively. On the other hand the use of such rates brings benefits in terms of aliasing reduction. In general, the optimization of the model performance needs further experimentation aimed at assessing the computational cost in connection with the effects of aliasing for different sampling rates and for various filter parameter settings.

Our Matlab procedure simulates signals at $4 \cdot 44.1$ kHz without any specific optimization at approximately half real time, on a Linux laptop powered by two 2.53 GHz Core 2 Duo Intel processors, with one processor allocated to Matlab. Using the same hardware and CPU resources, a Java program for the PureData processing environment has been developed, that runs in real time at $8 \cdot 44.1$ kHz provided that the cutoff frequency is kept below approximately 10 kHz.

VIII. Conclusion

Starting from a differential equation system that models the nonlinear characteristics of the VCS3 diode-based VCF, we have derived a filter network model that computes this system directly. Once coupled with existing techniques for the discrete-time synthesis [29] and manipulation of virtual analog sounds [30], this model may be productively used as a digital audio effect.

In spite of its complexity due to the presence of nested delay-free loops populated with algebraic nonlinearities, such a filter network leads to interesting results:

- application of well-known results of nonlinear control theory demonstrate that the system is passive;
- once the positive realness of the integrators is preserved during the analog-to-digital transformation, passivity is maintained in every discrete-time realization of the network;
- a specific fixed-point solution is identified;
- the resulting computational procedure is accurate, yet affordable on most DSP architectures available today on the market.

Tests show that the procedure is optimally computed by setting the sampling rate at four times the conventional frequency of 44.1 kHz. Furthermore, this rate contributes to reduced aliasing.

The same tests illuminate the limits of the current realization of the filter network. One of these limits, which resists the use of higher sampling rates (but may be relaxed through the use of more stable numerical schemes), is found in the exponential explosion of fixed-point iterations. This situation occurs when a fairly large feedback gain is set, and the cutoff frequency is pushed beyond a threshold value that typically floats somewhere above 10 kHz depending on the amplitude of the input signal.

Another limit is posed by the differential equation model, which inherently treats the bias current as a parameter instead of a signal. A reformulation of the equations, aimed at modeling this current as a signal, would enable users to experiment with control signals containing audible frequencies. This situation happens in the VCS3, for instance, when the VCF is biased using a 500 Hz square wave coming from the LFO on top of the voltage offset.

In the near future we will conduct measurements on the VCS3 hardware, to gain systematic information about the characteristic signals and the noise floor produced by the synthesizer. Besides enabling a comparison with the real system, such measurements in particular would assist finding a lower bound for the accuracy of the fixed-point solver, and an upper limit for the aliasing generated by digital model.

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APPENDIX

DERIVATION OF THE SYSTEM (1)

The voltage equations holding for every loop in the RC ladder of the circuit in Figure 1 form the following system:

$$\begin{cases} v_{D_3} + v_{C_2} - v_{D_4} - v_{C_1} = 0 \\ v_{D_5} + v_{C_3} - v_{D_6} - v_{C_2} = 0 \\ v_{D_7} + v_{C_4} - v_{D_8} - v_{C_3} = 0 \\ 3v_{D_9} - 3v_{D_{10}} - v_{C_4} = 0 \end{cases} . \tag{10}$$

By recalling the known diode characteristic

$$i_D = I_{inv}\left(e^{\frac{qv_D}{\eta kT}} - 1\right) \approx I_{inv}\left(e^{\frac{qv_D}{\eta kT}}\right), \tag{11}$$

the voltage at every diode can be figured out as

$$v_D = \eta V_T \ln\left(\frac{i_D}{I_{inv}}\right) = \gamma \ln\left(\frac{i_D}{I_{inv}}\right), \tag{12}$$

with $V_T = kT/q$.

The current flowing across every diode is the superposition of half the bias I_0, the signal $i(t)$, and the current components traversing the capacitors on the way to the diode itself. After reformulating every current i_D in (12) in terms of this superposition, the respective voltage v_D can be expressed in (10) as a logarithmic function of the current:

$$\begin{cases} \gamma \ln\left(\frac{I_0/2+i-i_{C_1}}{I_0/2-i+i_{C_1}}\right) + v_{C_2} - v_{C_1} = 0 \\ \gamma \ln\left(\frac{I_0/2+i-i_{C_1}-i_{C_2}}{I_0/2-i+i_{C_1}+i_{C_2}}\right) + v_{C_3} - v_{C_2} = 0 \\ \gamma \ln\left(\frac{I_0/2+i-i_{C_1}-i_{C_2}-i_{C_3}}{I_0/2-i+i_{C_1}+i_{C_2}+i_{C_3}}\right) + v_{C_4} - v_{C_3} = 0 \\ 3\gamma \ln\left(\frac{I_0/2+i-i_{C_1}-i_{C_2}-i_{C_3}-i_{C_4}}{I_0/2-i+i_{C_1}+i_{C_2}+i_{C_3}+i_{C_4}}\right) - v_{C_4} = 0 \end{cases} , \tag{13}$$

or, equivalently:

$$\begin{cases} \frac{I_0/2+i-i_{C_1}}{I_0/2-i+i_{C_1}} = e^{\frac{v_{C_1}-v_{C_2}}{\gamma}} \\ \frac{I_0/2+i-i_{C_1}-i_{C_2}}{I_0/2-i+i_{C_1}+i_{C_2}} = e^{\frac{v_{C_2}-v_{C_3}}{\gamma}} \\ \frac{I_0/2+i-i_{C_1}-i_{C_2}-i_{C_3}}{I_0/2-i+i_{C_1}+i_{C_2}+i_{C_3}} = e^{\frac{v_{C_3}-v_{C_4}}{\gamma}} \\ \frac{I_0/2+i-i_{C_1}-i_{C_2}-i_{C_3}-i_{C_4}}{I_0/2-i+i_{C_1}+i_{C_2}+i_{C_3}+i_{C_4}} = e^{\frac{v_{C_4}}{3\gamma}} \end{cases} . \tag{14}$$

By recalling the current-to-voltage relationship for the capacitor, $\dot{v}_C = i_C/C$, the equations in (14) can

be rearranged into the following system:

$$\begin{cases} \dot{v}_{C_1} = \frac{I_0}{2C_1}\frac{1-e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}{1+e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}} + \frac{i}{C_1} \\ \dot{v}_{C_2} = \frac{I_0}{2C_2}\frac{1-e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}{1+e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}} - \frac{C_1}{C_2}\dot{v}_{C_1} + \frac{i}{C_2} \\ \dot{v}_{C_3} = \frac{I_0}{2C_3}\frac{1-e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}{1+e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}} - \frac{C_1}{C_3}\dot{v}_{C_1} - \frac{C_2}{C_3}\dot{v}_{C_2} + \frac{i}{C_3} \\ \dot{v}_{C_4} = \frac{I_0}{2C_4}\frac{1-e^{\frac{v_{C_4}}{3\gamma}}}{1+e^{\frac{v_{C_4}}{3\gamma}}} - \frac{C_1}{C_4}\dot{v}_{C_1} - \frac{C_2}{C_4}\dot{v}_{C_2} - \frac{C_3}{C_4}\dot{v}_{C_3} + \frac{i}{C_4} \end{cases}. \tag{15}$$

Since $C_1 = C_2 = C_3 = C_4 = C$:

$$\begin{cases} \dot{v}_{C_1} = \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}{1+e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}} + \frac{i}{C} \\ \dot{v}_{C_2} = \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}{1+e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}} - \dot{v}_{C_1} + \frac{i}{C} \\ \dot{v}_{C_3} = \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}{1+e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}} - \dot{v}_{C_1} - \dot{v}_{C_2} + \frac{i}{C} \\ \dot{v}_{C_4} = \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_4}}{3\gamma}}}{1+e^{\frac{v_{C_4}}{3\gamma}}} - \dot{v}_{C_1} - \dot{v}_{C_2} - \dot{v}_{C_3} + \frac{i}{C} \end{cases}. \tag{16}$$

In matrix form:

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \dot{v}_{C_1} \\ \dot{v}_{C_2} \\ \dot{v}_{C_3} \\ \dot{v}_{C_4} \end{bmatrix} = \begin{bmatrix} \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}{1+e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}} + \frac{i}{C} \\ \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}{1+e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}} + \frac{i}{C} \\ \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}{1+e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}} + \frac{i}{C} \\ \frac{I_0}{2C}\frac{1-e^{\frac{v_{C_4}}{3\gamma}}}{1+e^{\frac{v_{C_4}}{3\gamma}}} + \frac{i}{C} \end{bmatrix},$$

and finally, solving in the voltage derivatives:

$$\begin{cases} \dot{v}_{C_1} = \frac{I_0}{2C}\left(\frac{1-e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}{1+e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}\right) + \frac{i}{C} \\ \dot{v}_{C_2} = \frac{I_0}{2C}\left(-\frac{1-e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}}{1+e^{\frac{v_{C_1}-v_{C_2}}{\gamma}}} + \frac{1-e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}{1+e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}\right) \\ \dot{v}_{C_3} = \frac{I_0}{2C}\left(-\frac{1-e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}}{1+e^{\frac{v_{C_2}-v_{C_3}}{\gamma}}} + \frac{1-e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}{1+e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}\right) \\ \dot{v}_{C_4} = \frac{I_0}{2C}\left(-\frac{1-e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}}{1+e^{\frac{v_{C_3}-v_{C_4}}{\gamma}}} + \frac{1-e^{\frac{v_{C_4}}{3\gamma}}}{1+e^{\frac{v_{C_4}}{3\gamma}}}\right) \end{cases}. \tag{17}$$

Considering that:

$$\tanh x = \frac{e^x - e^{-x}}{e^x + e^{-x}} = \frac{e^{2x}-1}{e^{2x}+1} = \frac{1-e^{-2x}}{1+e^{-2x}}, \tag{18}$$

then (17) can be rewritten as:

$$\begin{cases} \dot{v}_{C_1} = \frac{I_0}{2C}\tanh\frac{v_{C_2}-v_{C_1}}{2\gamma} + \frac{i}{C} \\ \dot{v}_{C_2} = \frac{I_0}{2C}\left(\tanh\frac{v_{C_3}-v_{C_2}}{2\gamma} - \tanh\frac{v_{C_2}-v_{C_1}}{2\gamma}\right) \\ \dot{v}_{C_3} = \frac{I_0}{2C}\left(\tanh\frac{v_{C_4}-v_{C_3}}{2\gamma} - \tanh\frac{v_{C_3}-v_{C_2}}{2\gamma}\right) \\ \dot{v}_{C_4} = \frac{I_0}{2C}\left(-\tanh\frac{v_{C_4}-v_{C_3}}{2\gamma} - \tanh\frac{v_{C_4}}{6\gamma}\right) \end{cases}. \tag{19}$$

The relationship between $i(t)$ and the input and output voltage can be found by applying the *Ebers-Moll* model for BJT's. In fact, the application of this model to the differential amplifier at the bottom of the RC ladder, illustrated in Figure 13, leads to the two following equations:

$$\begin{aligned} i_{C_1} &= I_{ES_1}\left(e^{\frac{v_{BE_1}}{V_T}} - 1\right) \approx I_{ES_1}\left(e^{\frac{v_{BE_1}}{V_T}}\right) \\ i_{C_2} &= I_{ES_2}\left(e^{\frac{v_{BE_2}}{V_T}} - 1\right) \approx I_{ES_2}\left(e^{\frac{v_{BE_2}}{V_T}}\right) \end{aligned}, \tag{20}$$

where I_{ES} is the inverse current flowing across the diode between the base and the emitter. The corresponding voltages are:

$$v_{BE_1} = V_T \ln\left(\frac{i_{C_1}}{I_{ES_1}}\right) \quad \text{and} \quad v_{BE_2} = V_T \ln\left(\frac{i_{C_2}}{I_{ES_2}}\right).$$

Since the two BJT's are identical, the difference between the base-emitter voltages on Q1 and Q2 is equal to

$$v_{BE_2} - v_{BE_1} = V_T \ln\frac{i_{C_2} I_{ES_1}}{i_{C_1} I_{ES_2}} = V_T \ln\frac{i_{C_2}}{i_{C_1}}. \tag{21}$$

Now, from:

$$v_{BE_2} - v_{BE_1} = (v_{B_2} - v_E) - (v_{B_1} - v_E) = v_{B_2} - v_{B_1}, \tag{22}$$

Eq. (21) can be rewritten in the difference $v_{B_2} - v_{B_1}$:

$$e^{\frac{v_{B_2}-v_{B_1}}{V_T}} = \frac{i_{C_2}}{i_{C_1}}. \tag{23}$$

From here, the current i_E at the emitter is:

$$i_E = i_{C_1} + i_{C_2} = i_{C_1} + i_{C_1} e^{\frac{v_{B_2}-v_{B_1}}{V_T}}, \tag{24}$$

hence:

$$\begin{aligned} i_{C_1} &= \frac{i_E}{1+e^{\frac{v_{B_2}-v_{B_1}}{V_T}}} = \frac{2i_E}{2\left(1+e^{\frac{v_{B_2}-v_{B_1}}{V_T}}\right)} \\ &= \frac{i_E}{2}\left(\frac{1+1+e^{\frac{v_{B_2}-v_{B_1}}{V_T}}-e^{\frac{v_{B_2}-v_{B_1}}{V_T}}}{1+e^{\frac{v_{B_2}-v_{B_1}}{V_T}}}\right) \\ &= \frac{i_E}{2}\left(1+\frac{1-e^{\frac{v_{B_2}-v_{B_1}}{V_T}}}{1+e^{\frac{v_{B_2}-v_{B_1}}{V_T}}}\right) \\ &= \frac{i_E}{2}\left(1+\tanh\frac{v_{B_1}-v_{B_2}}{2V_T}\right), \end{aligned} \tag{25}$$

and, by (24) and (25):

$$\begin{aligned} i_{C_2} &= i_E - i_{C_1} \\ &= \frac{i_E}{2}\left(1-\tanh\frac{v_{B_1}-v_{B_2}}{2V_T}\right). \end{aligned} \tag{26}$$

In the analog circuit of Fig. 1 the dc is filtered out from the input signal by the capacitor C5. The capacitor C6 plays a similar role, by filtering any dc back-propagating from the output. These capacitors can be neglected, as the audio signals that are processed by DSP hardware are normally free from this component. Hence, we can set the voltage signals at the input and output point to be respectively equal to the voltages at the base of the transistors Q1 and Q2: $v_{IN} = v_{B_1}$, and $v_{OUT} = v_{B_2}$. Moreover, $i_{C_1} = I_0/2 + i$ and $i_{C_2} = I_0/2 - i$. Finally, $i_E = I_0$. These relationships can be used together with Eqs. (25) and (26), to write:

$$i(t) = \frac{i_{C_1} - i_{C_2}}{2} = \frac{I_0}{2}\tanh\frac{v_{IN}-v_{OUT}}{2V_T}. \tag{27}$$

Substituting (27) in (19), we complete the first four equations of (1).

At this point, an equation linking v_{OUT} to v_{C_4} can be figured out from the feedback circuit. Besides C5 and C6, whose role has been explained above, in Fig. 1 there are two further capacitors, C7 and C8, that block dc in the feedback loop. Since op-amp is modeled as a gain parameter and I_0 is not a signal, C7 and C8 can been omitted as well. In this way, we can write the following linear relationship:

$$v_{OUT} = v_{C_{4+}}\frac{R_9+R_{13}}{R_9} - v_{C_{4-}}\frac{R_{13}}{R_9}, \tag{28}$$

in which $v_{C_{4+}}$ and $v_{C_{4-}}$ are the voltages measured at the right and left edge of the capacitor with respect to the ground: $v_{C_4} = v_{C_{4+}} - v_{C_{4-}}$. Since the differential amplifier imposes the condition $v_{C_{4+}} = -v_{C_{4-}}$,

it descends:

$$\begin{aligned} v_{OUT} &= v_{C_{4+}} \frac{R_9 + R_{13}}{R_9} + v_{C_{4+}} \frac{R_{13}}{R_9} \\ &= v_{C_{4+}} + 2 v_{C_{4+}} \frac{R_{13}}{R_9} \\ &= \frac{v_{C_4}}{2} + v_{C_4} \frac{R_{13}}{R_9} = (\frac{1}{2} + \frac{R_{13}}{R_9})\, v_{C_4}, \end{aligned} \tag{29}$$

that is the last equation in (1) once we set $K = R_{13}/R_9$.

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LIST OF FIGURES

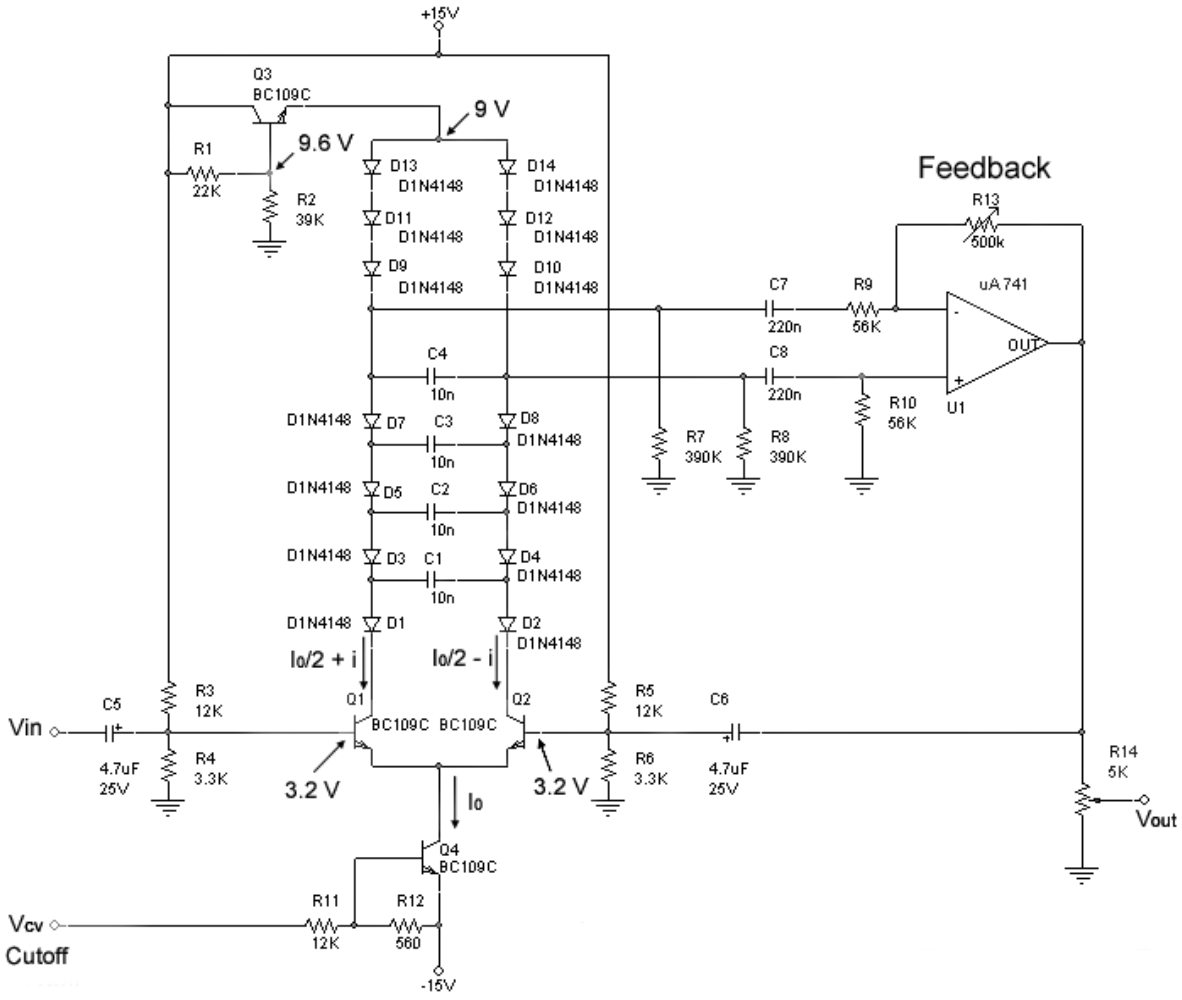


Fig. 1. EMS VCS3 VCF analog circuit.

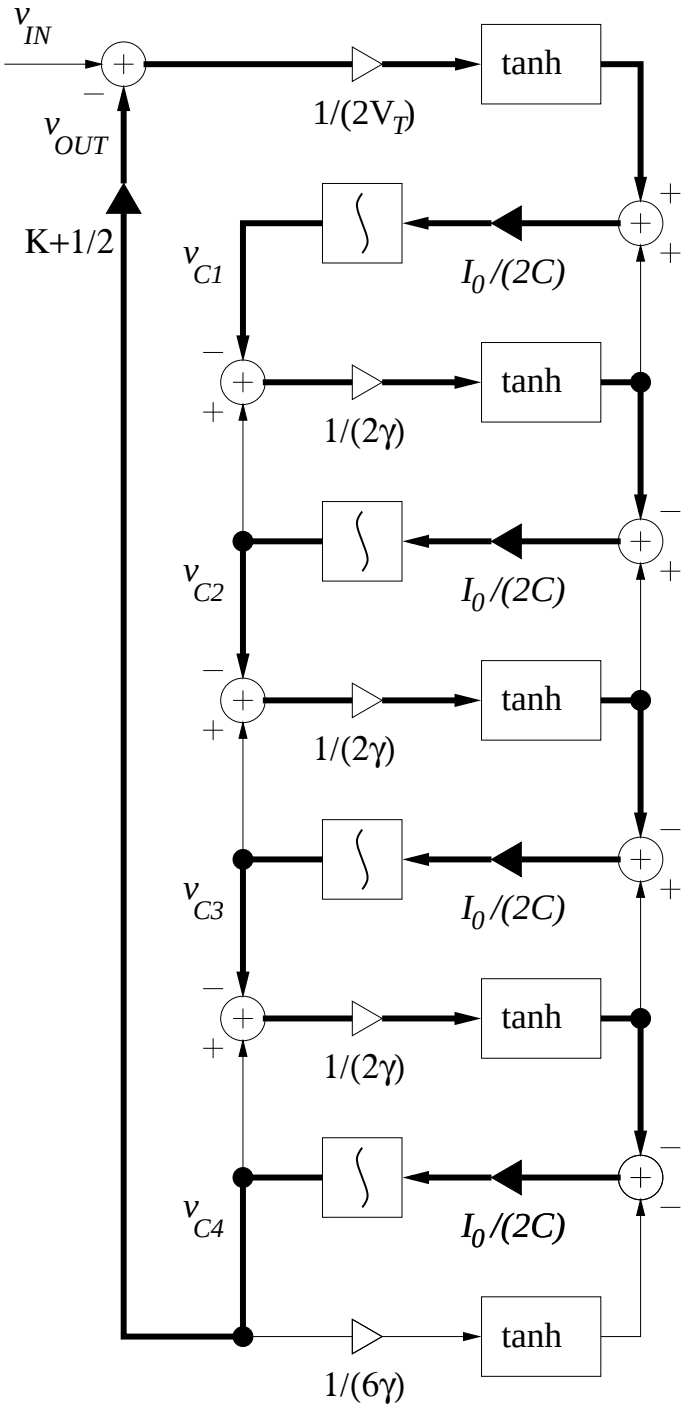


Fig. 2. Network model of the VCF. Black-filled gains can be varied at runtime. The fixed-point solution (Sec. IV) is computed along the bold branches.

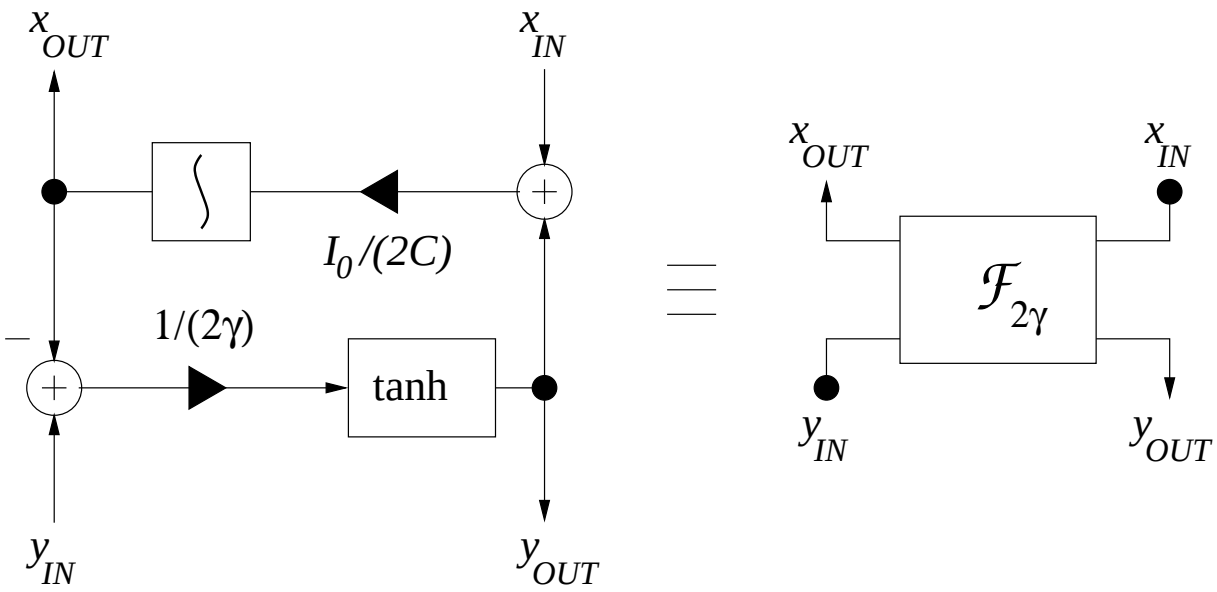


Fig. 3. Elementary loop $\mathcal{F}_{2\gamma}$.

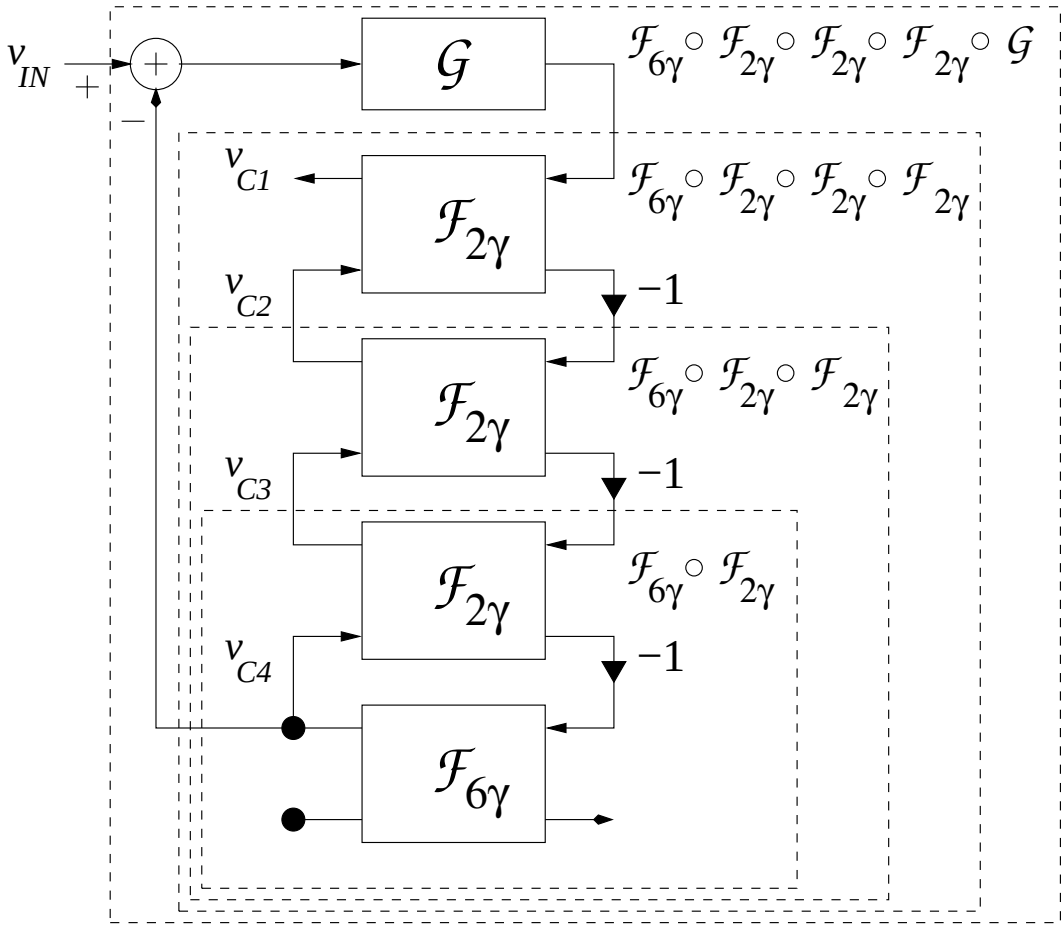


Fig. 4. Block diagram of the VCF network model. Dashed boxes delimit negative loops and their compositions.

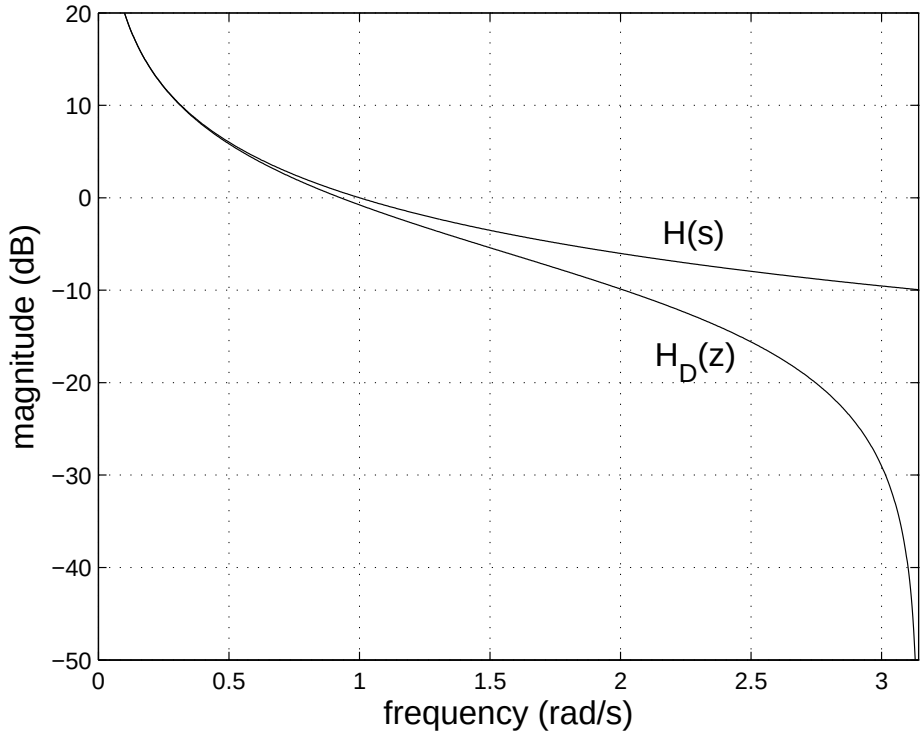
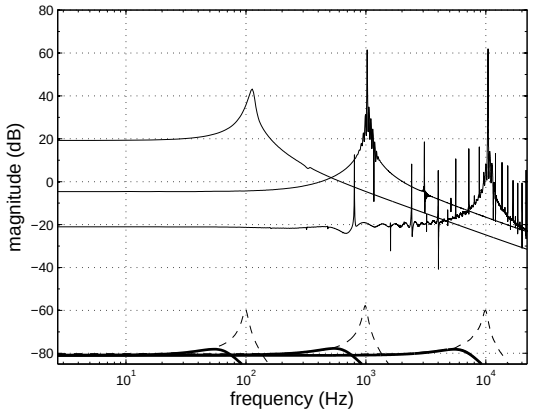
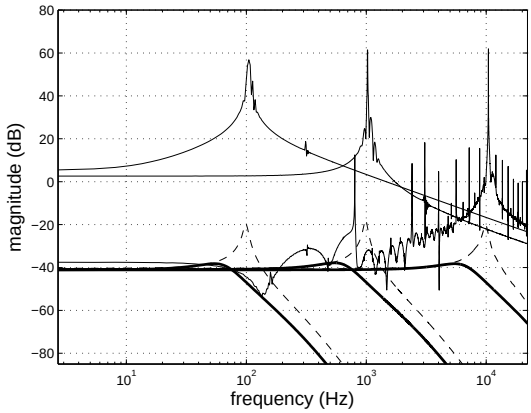


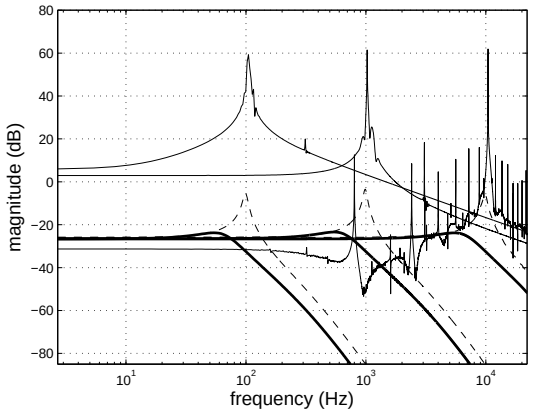
Fig. 5. Magnitude response of $H(s) = 1/s$ vs. digital version $H_D(z)$ (2) obtained by bilinear transformation.



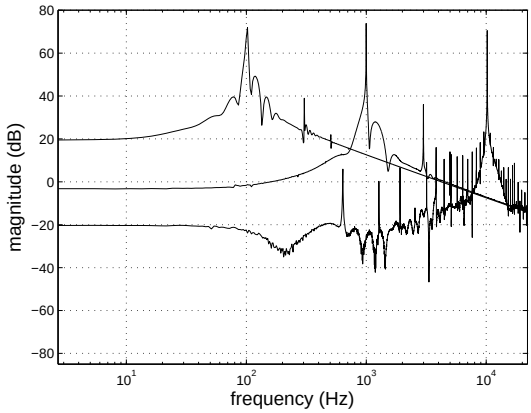
(a) $A_0 = -80$ dB, K =1 (bold), 4 (dashed), 6 (normal)



(b) $A_0 = -40$ dB, K =1 (bold), 4 (dashed), 6 (normal)



(c) $A_0 = 0$ dB, K =1 (bold), 4 (dashed), 6 (normal)



(d) $A_0 = 0$ dB, $K = 12$

Fig. 6. Magnitude responses of the model for varying impulse amplitude and feedback gain. Cutoff frequency set to 0.1, 1, 10 kHz. $F_S = 176.4$ kHz.

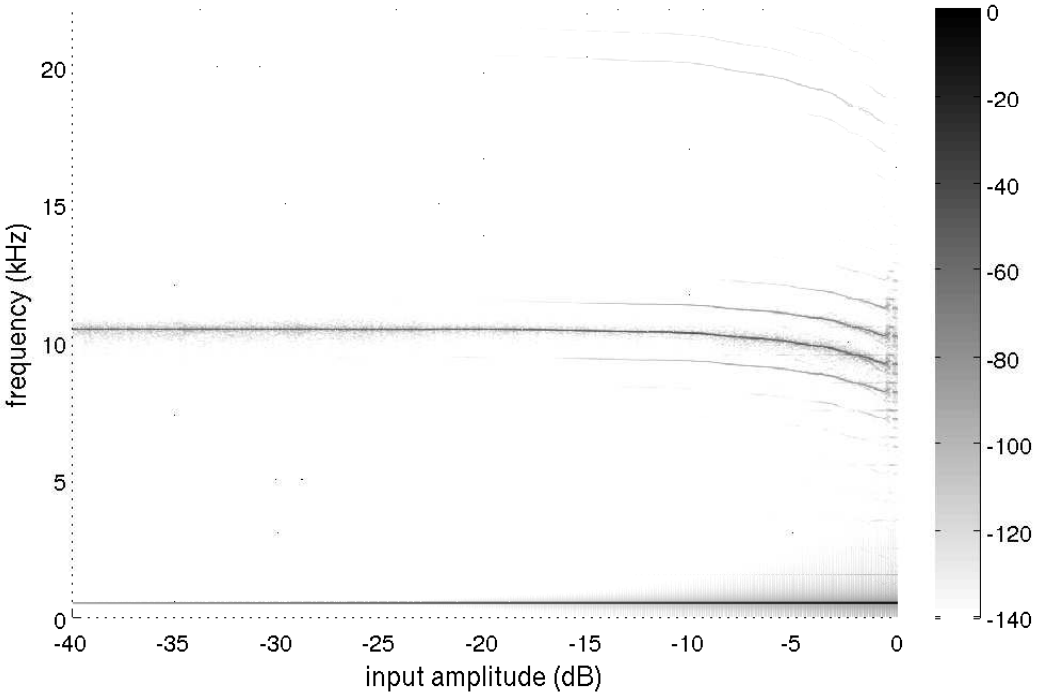


Fig. 7. Spectrogram of v_{OUT}, with $v_{IN}[n] = A_0 \sin(2\pi 500\, n/F_S)$. A_0 increasing from -80 to 0 dB across 10 s — only the range [-40,0] is plotted. $f_0 = 10$ kHz. $K = 6$. $F_S = 176.4$ kHz. Normalized 0 dB (black color) corresponding to a magnitude of -37 dB.

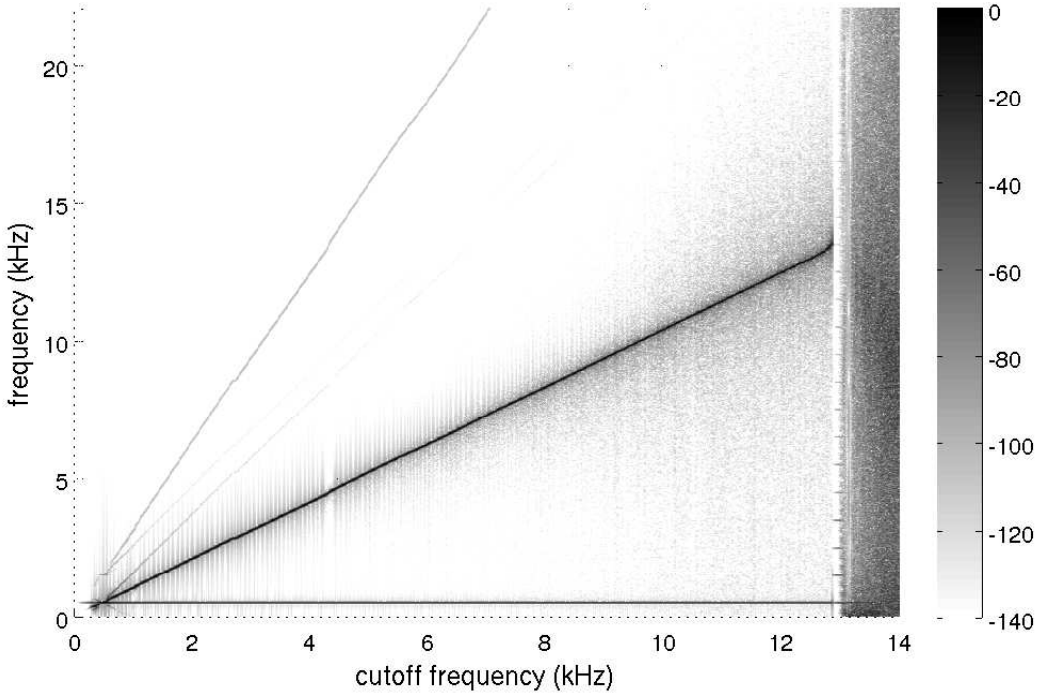


Fig. 8. Spectrogram of v_{OUT}, with $v_{IN}[n] = A_0 \sin(2\pi 500\, n/F_S)$. $A_0 = -40$ dB. f_0 increasing from 0 to 14 kHz across 10 s. $K = 6$. $F_S = 176.4$ kHz. Normalized 0 dB (black color) corresponding to a magnitude of -82 dB.

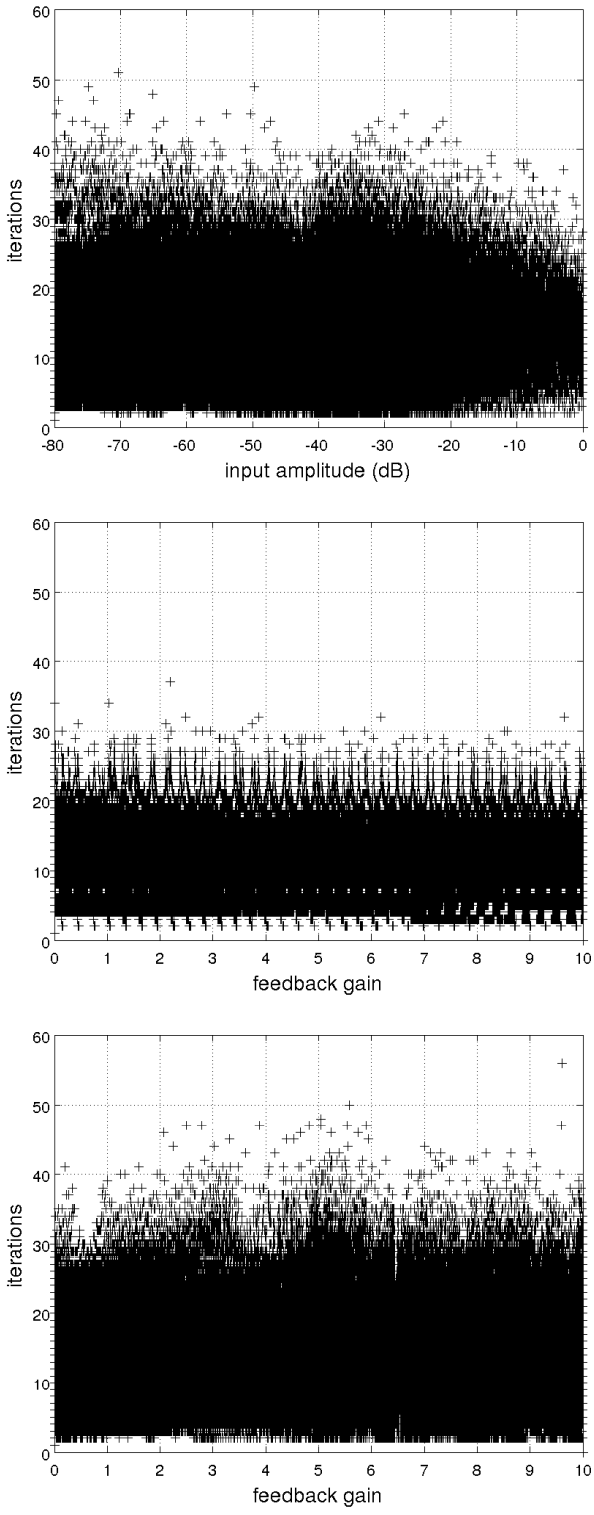


Fig. 9. Iterations needed to compute the output signal providing the spectrogram of Fig. 7 (left); for $0 < K < 10$, $f_0 = 10$ kHz, $v_{IN}[n] = A_0 \sin(2\pi 5000\, n/F_S)$, $A_0 = 0$ dB (center); same as before, but with $A_0 = -60$ dB (right);

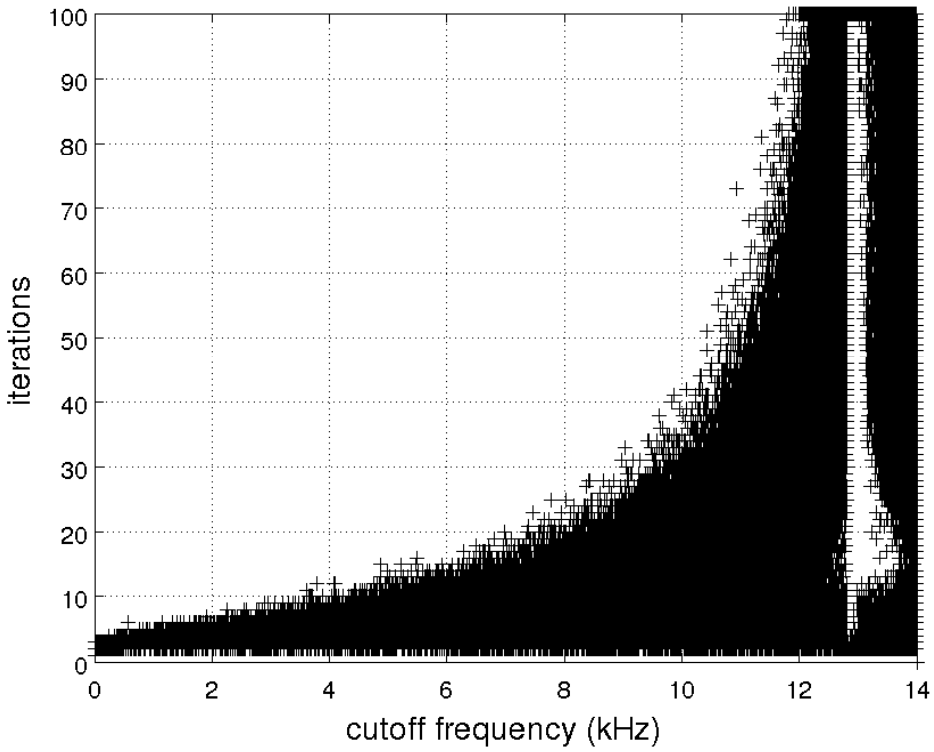
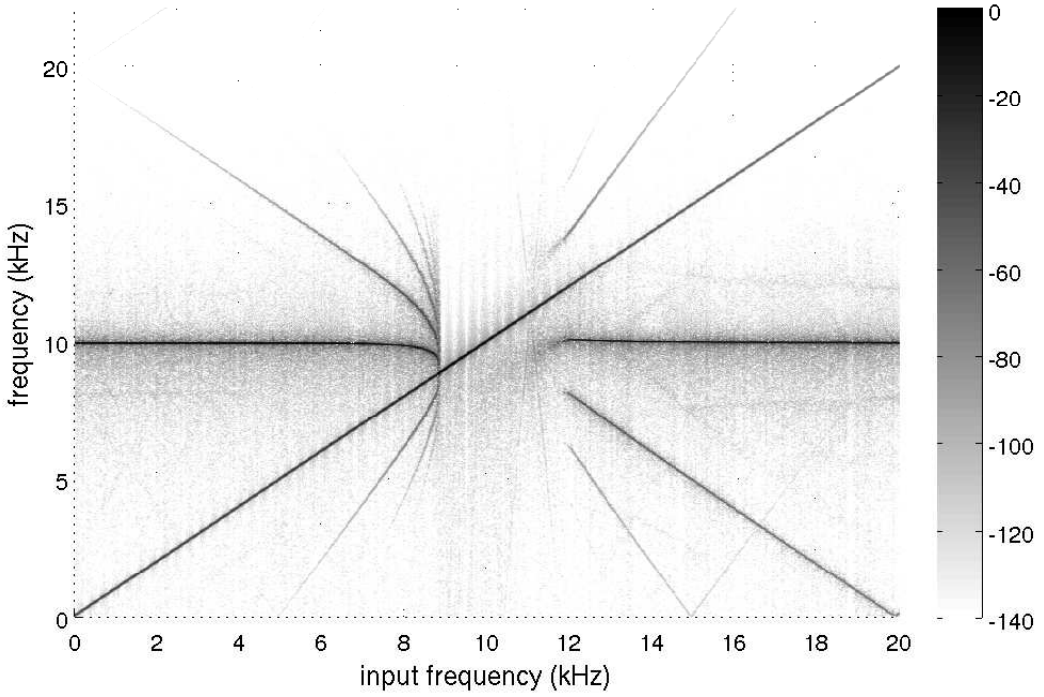


Fig. 10. Iterations needed to compute the output signal providing the spectrogram of Fig. 8.



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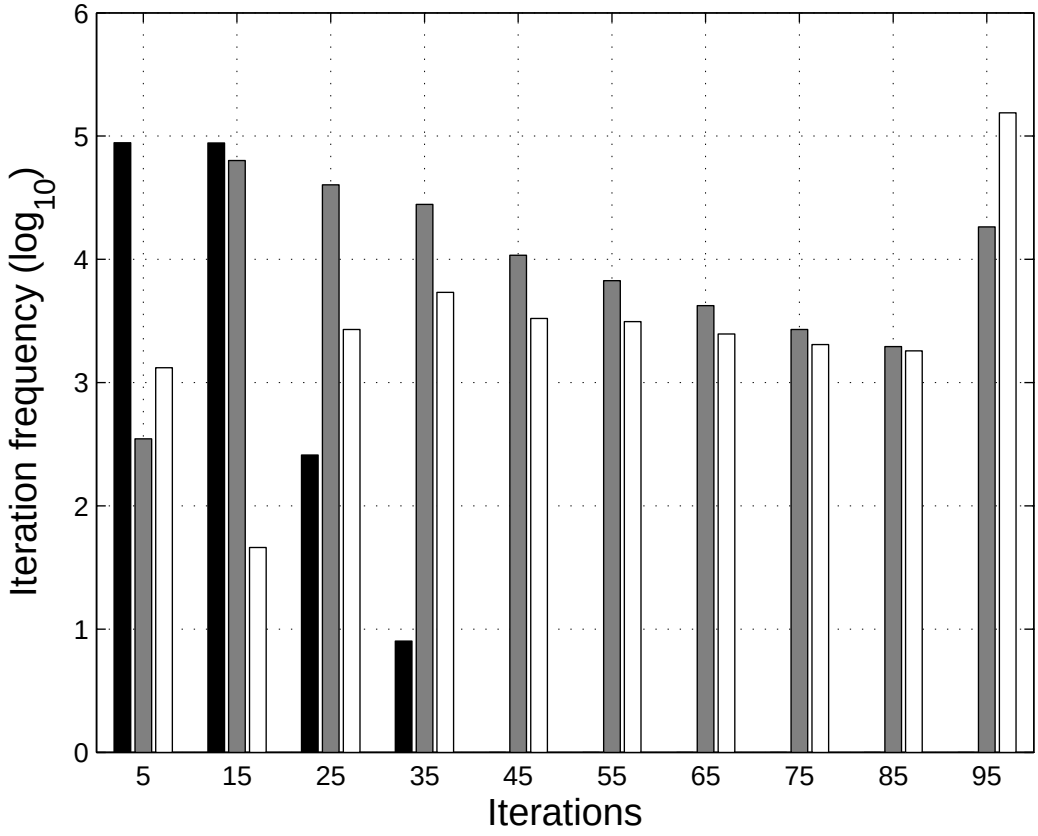

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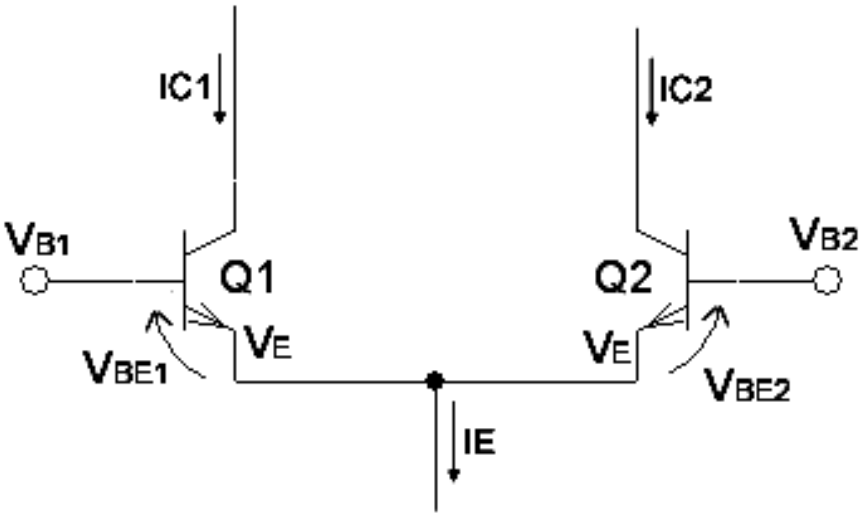

Fig. 13. Differential amplifier at the base of the ladder in the VCF.

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