TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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1 Introduction

The objective of this laboratory assignment is to develop an audio amplifier circuit with two separate stages: a gain stage and an output stage.

The circuit is composed of a voltage source and a resistor connected to an input coupling capacitor. Additionally, theres a bias circuit made of two resistors. In the gain stage we have a transistor and two resistors. There is also a bypass capacitor. The chosen architecture of the output stage is a transistor and a resistor. Finally, theres an output coupling capacitor and another resistor.

In Section 2, a theoretical analysis of the circuit shown in Figure 1 is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

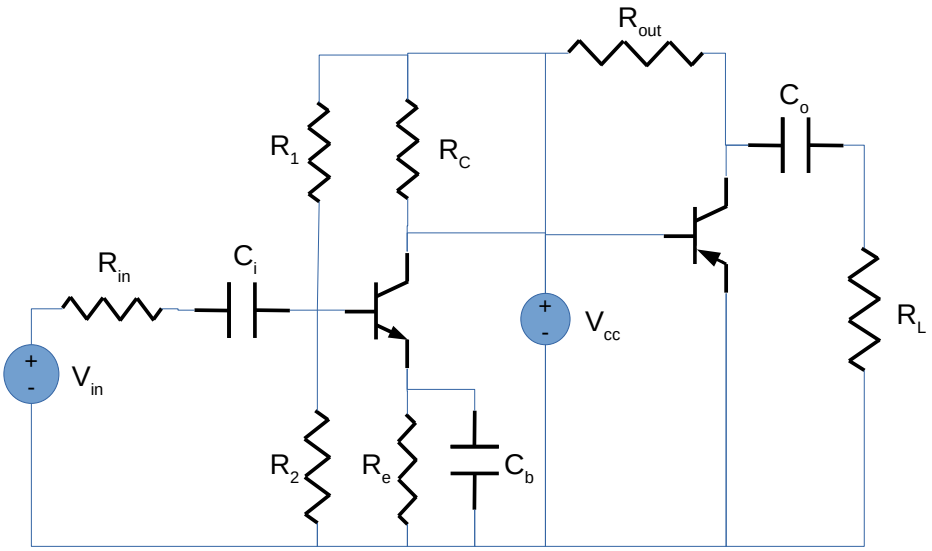

Figure 1: Audio amplifier circuit.

2 Theoretical Analysis

In this section, the Audio amplifier is analysed theoretically.

2.1 OP analysis

The operating point analysis of the circuit was made by using the DC incremental BJT model for the circuit, ignoring the capacitors. The results, using the equations shown in the lectures, are shown in table 1.

Name	Value[V]/[A]
$*I_{B1}$	5.0044156608772456e-05
$*I_{C1}$	0.008942890785987638
$*I_{E1}$	0.00899293494259641
V_{emit}	0.899293494259641
V_{coll}	3.0571092140123621
$*I_{E2}$	0.082428907859876388
$*I_{C2}$	0.082067852634909774
V_{emit2}	3.7571092140123614

Table 1: Theoretical OP values. Values with * are currents in Ampere.

2.2 Gain and Impedance

With the DC results, we are able to calculate the input impedance, output impedance and gain of each stage of the circuit, as well as of the full circuit. The results are shown below.

Name	Value[dB]/[Ohm]
$Gain(gainstage)$	48.392206272605911
$*Inputimpedance(gainstage)$	484.43363013271278
$*Outputimpedance(gainstage)$	886.2848161275748
$Gain(outputstage)$	0.99194759275934863
$*Inputimpedance(outputstage)$	8598.8553592252501
$*Outputimpedance(outputstage)$	0.30217300712502043
$Gain$	47.959428944728415
$*Inputimpedance$	484.43363013271278
$*Outputimpedance$	3.9819689370779106

Table 2: Theoretical gain and impedance values. Values with * are impedances in Ohm

3 Simulation Analysis

3.1 Operating Point

The simulated results of the operating point analysis of the amplifier circuit are shown below in Table 3.

Name	Value [V]
v(base)	1.580921e+00
v(coll)	3.894195e+00
v(emit)	8.726323e-01
v(emit2)	4.708670e+00
v(in)	0.000000e+00
v(in2)	0.000000e+00
v(out)	0.000000e+00
v(vcc)	1.200000e+01
(v(coll)-v(emit))-(v(base)-v(emit))	2.313274e+00
v(emit2)-(v(emit2)-v(coll))	3.894195e+00

Table 3: Simulated operating point results.

The relative error for the node voltages is aproximately -3.05% for v(emit), -21.5% for v(coll) and 20% for V(emit2). These errors are considerably big, and are caused by the theoretical model used (BJT incrementl model). We can see that the results for VCE-VBE for the NPN BJT and the results for VEC-VEB for the PNP transistor confirm that they are operating in the Forward Active Region, like is intended for this circuit.

3.2 Frequency Analysis

The simulated results for the output impedance, input impedance, lower and upper 3dB cut off frequencies and the voltage gain are shown in tables 4 and 5, for a frequency in the pass-band region.

Output Impedance:

Name	Value [Ohm]
v(out)[40]/(v(dummy1)[40]/100)	1.007074e+01,6.164229e-01

Table 4: Simulated output impedance result.

Voltage Gain (dB), cut off frequencies, input impedance and merit:

Name	Value [db]/[Ohm]
vecmax(vdb(out))	3.793449e+01
f1	1.589183e+06
f2	4.742703e+01
v(in2)[40]/((v(in)[40]-v(in2)[40])/100)	5.676643e+02,-8.56442e+01
(vecmax(v(out))*(f1-f2))/(1781.508*f2)	1.615358e+02,8.141213e+02

Table 5: Voltage Gain (dB), cut off frequencies, input impedance and merit simulated reults.For the variables with two values, only the first one is of interest (frequency analysis).

The relative errors of each one are: Error(Voltage Gain)=26.4% Error(Input Impedance)=14.5% Error(Output Impedance)=60%

These values are extremely high due to approximations made with the incremental BJT model.

3.3 Gain's frequency response

The plot of the Voltage Gain frequency response is shown below.

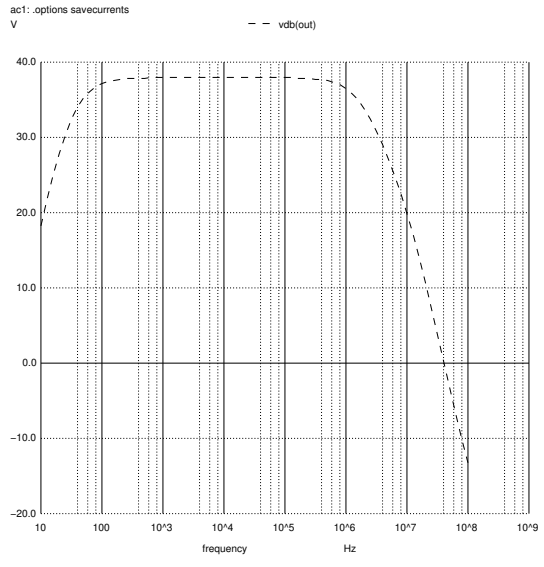

Figure 2: Voltage Gain frequency response.

In the theoretical analysis, only the pass-band gain value was obtained. We can see that even this value isn't constant in the pass-band. Before the lower cutt of frequency, we could compare the simulated result to a linear response of 20dB/dec. After the upper cutt of frequency, we can compare the graph to a linear response of -20dB/dec.

4 Conclusion

In this laboratory assignment the objective of creating an audio amplifier circuit was achieved. By comparing the theoretical and simulated results we could see that there was a significant error caused by the approximations made for the theoretical transistor model and by not considering the capacitors in the theoretical analysis. The total cost of the circuit is 1781.508 MU and the merit is 161.535. Both of these values were significantly improved by changing the capacitance of the coupling capacitors and of the bypass capacitor, to improve the bandwidth value.