Circuit Theory and Electronics Fundamentals

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1 Introduction

The objective of this laboratory assignment is to develop an AC/DC converter circuit using an envelope detector and a voltage regulator.

In Section 2, a theoretical analysis of the circuit shown in Figure 1 is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

2 Theoretical Analysis

In this section, the output voltage, voltage ripple and envelope detector output of the circuit are all analysed theoretically.

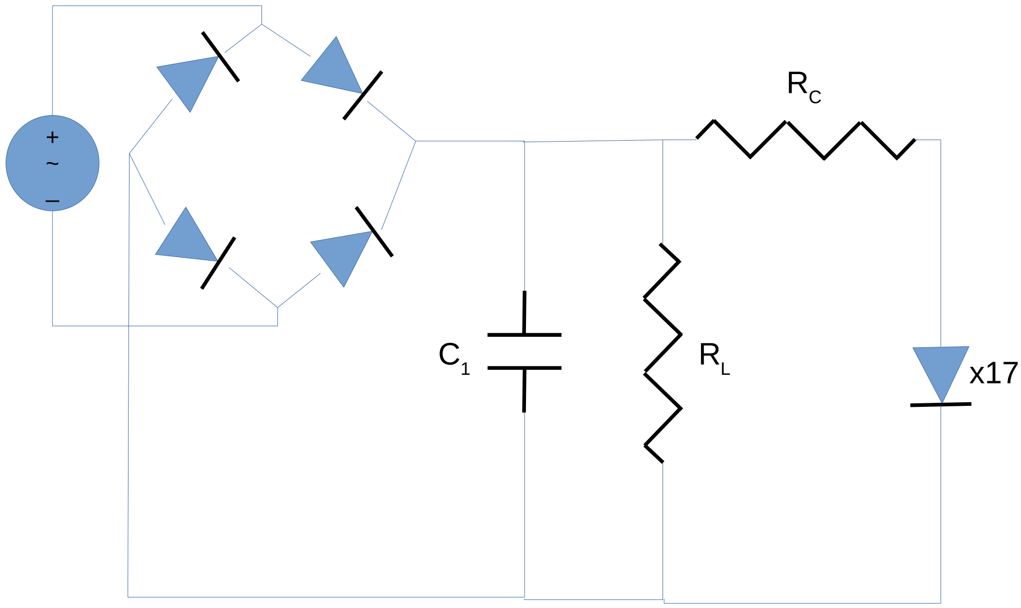

Figure 1: AC/DC converter circuit.

2.1 Envelope detector

Using an ideal diode model, we plotted the time response of the output voltage, as shown in figure .

First we calculated t_off

$$tOFF = (1/w) * atan(1/w/R/C). \tag{1}$$

The output voltage of the envelope detector varies accordingly with t_off:
For t<t_off

$$vO(t) = v_s(t). \tag{2}$$

For t>t_off

$$vO(t) = abs(A * cos(w * tOFF) * exp(-(t(i) - tOFF)/R/C)). \tag{3}$$

To simplify the calculations, we plotted for t>t_off with the condition that if the full rectifier output was superior to $abs(A * cos(w * tOFF) * exp(-(t(i) - tOFF)/R/C))$, vO(t) would be equal to that output, so as not to calculate t_ON.

2.2 Output Voltage

We obtain the output voltage using a voltage regulator circuit.

First we calculate v_e

$$v_e = vO - median(vO). \tag{4}$$

Then we use a voltage divider vo = (rd/(rd+R)) * vs

$$vo = (rd/(rd + R)) * vs \tag{5}$$

And lastly, we can calculate the voltage output

$$Vout = VD + vo; \tag{6}$$

3 Simulation Analysis

3.1 Envelope detector

The simulated results of the envelope detector output are compared to the theoretical results as shown below in Figures 2 and 3, respectively.

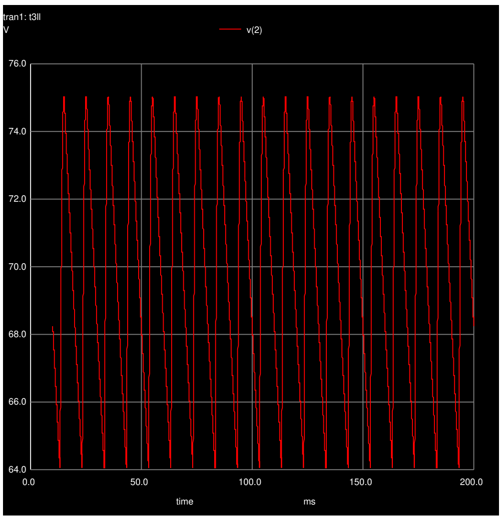

Figure 2: Simulated Envelope detector voltage output

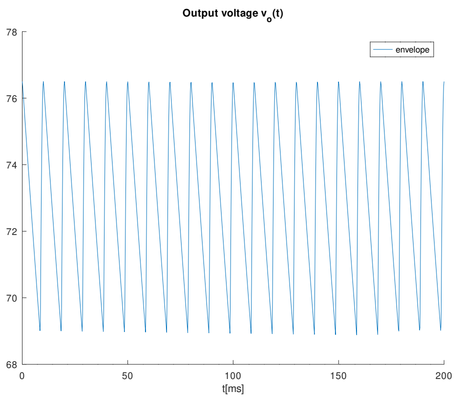

Figure 3: Theoritical Envelope detector voltage output

The theoretical ripple in the envelope detector is considerably smaller than the simulated one, due to the approximations made in the theoretical diode model.

3.2 Output Voltage

The simulated results of the voltage output are compared to the theoretical results as shown below in Figures 4 and 5, respectively.

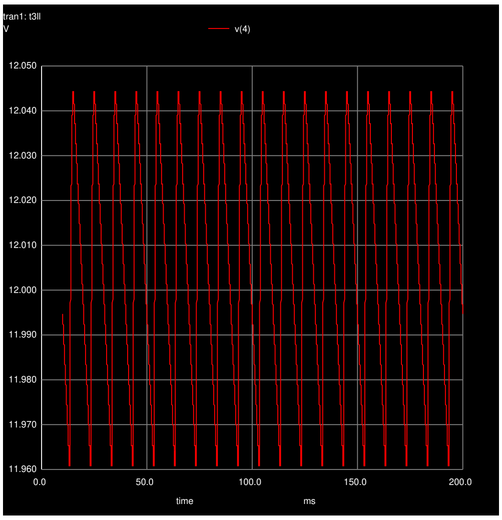

Figure 4: Simulated voltage output.

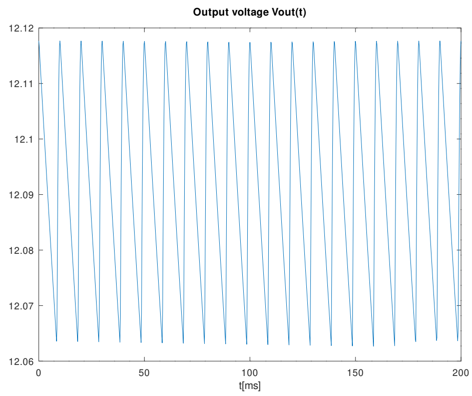

Figure 5: Theoritical voltage output.

Once again, the theoretical ripple is considerably smaller than the simulated one, due to the approximations made in the theoretical diode model.

It is also notable that the output voltage values are always higher than both 12V and the simulation's values, which vary between higher and lower than 12V.

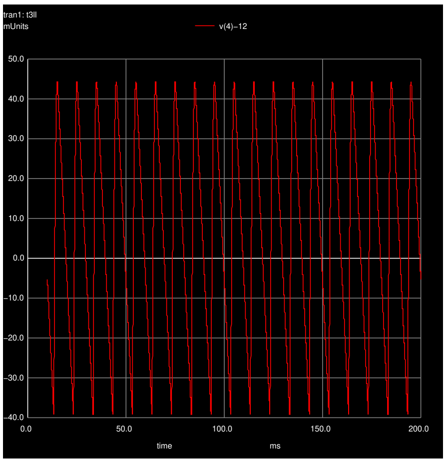

Figure 6: Simulated voltage output error.

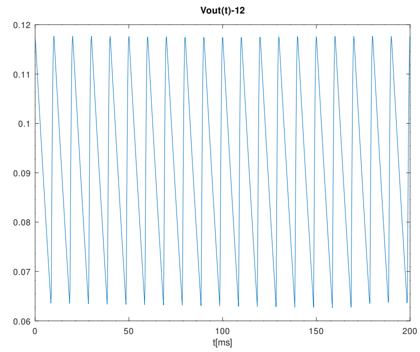

Figure 7: Theoritical voltage output error.

The voltage output errors (V_{out} - 12) of the simulation and the theoretical analysis are shown above in Figures 6 and 7, respectively.

The output voltage error is always positive and higher than the simulation's, which varies between positive and negative.

Comparing the Voltage ripple and VDC of the simulated and theoretical analysis in tables 1 and 2, respectively:

Name	**Value [V]**
mean(v(4))	1.200575e+01
vecmax(v(4))-vecmin(v(4))	8.361910e-02
(1/(29.8*(vecmax(v(4))-vecmin(v(4))+abs(mean(v(4)-12))+10e-06)))	3.754540e-01

Table 1: Simulated results. mean(v(4)) is the average outuput voltage and vecmax(v(4))-vecmin(v(4)) is the maximum value of ripple. The last value is the merit of the circuit.

Name	**Value[V]**
V_{DC}	12.091397286523476
V_{ripple}	0.055004191018202 42

Table 2: Theoretical values. V_{DC} is the average outuput voltage.

The relative error for the average output voltage is aproximately 0.713%. The relative error for the maximum ripple is aproximately -34.22%. These errors are once again due to the approximations made in the theoretical diode model.

The merit value is 3.754540e-01.

4 Conclusion

In this laboratory assignment the objective of creating an AC/DC converter circuit was achieved. By comparing the theoretical and simulated results we could see that there was a significant error caused by the approximations made for the theoretical diode model. The total cost of the circuit is 29.8 MU and the merit is 3.754540e-01.