ECE 481/581 - ASIC: Modeling & Synthesis

Design Automation

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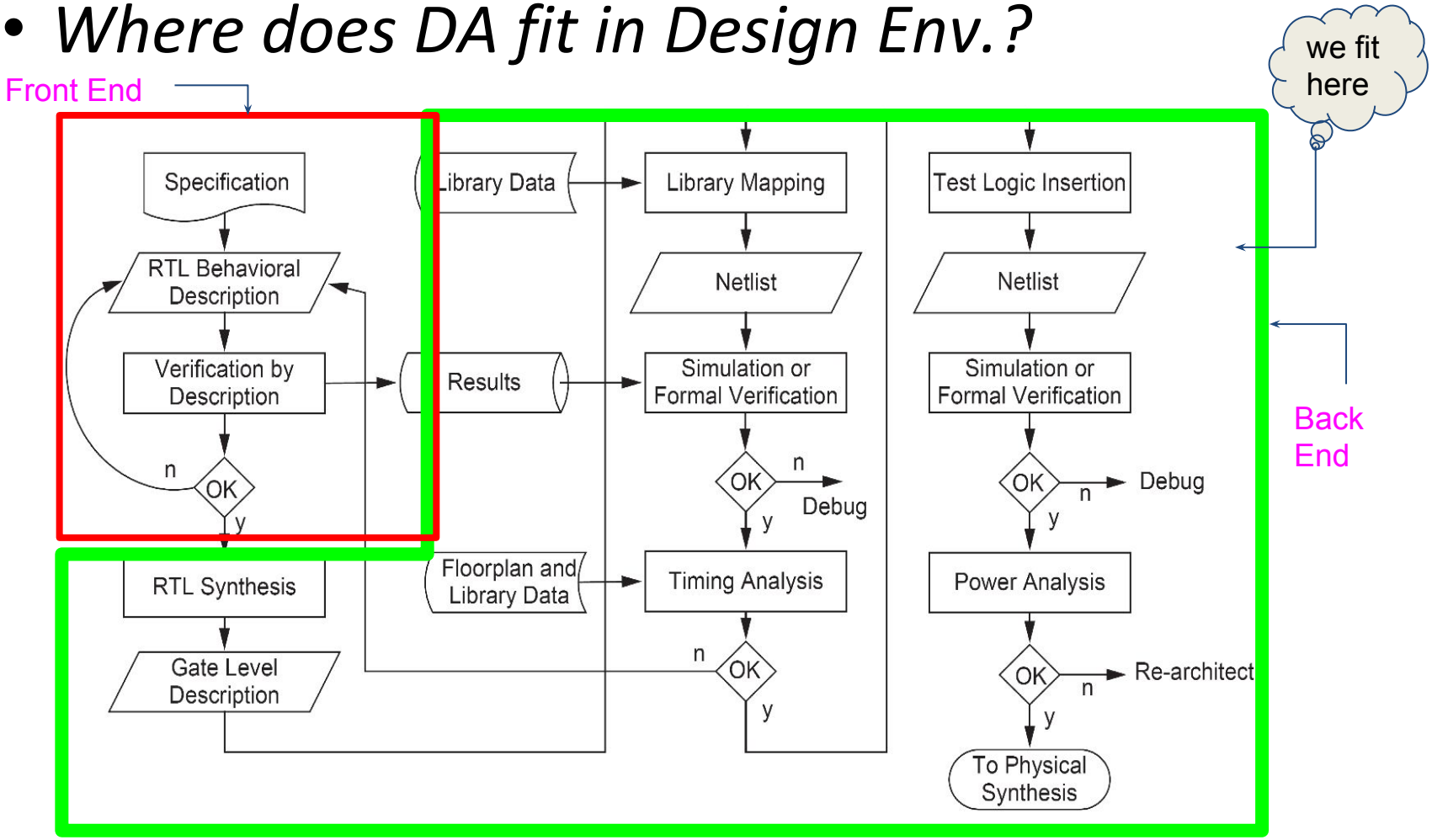
Final Project Presentation

Introduction

- **Project Overview**:
  - *tcl* scripts to automate design synthesis
    - Find components (cells/nets/ports...) and report their attributes (timing margin/cell count...)
    - Script had to be design independent
  - Wrote two scripts as a part of the final project
    - Script #1 : Finding timing paths, total cells, etc.
    - Script #2 : Finding max and min timing margins, etc.
- Applications of our design:
  - Accelerate design process in design tools such Design Compiler and IC Compiler

Introduction

- *Where does DA fit in Design Env.?*



Script #1

- Problem Statement:
  - Report timing information for a given user input
  - User given inputs :
    - Top N paths
    - Worst Negative Slack (WNS)
  - Outputs:
    - All cells in the N paths/ for N paths with WNS
    - Total number of times cells appear in those paths
    - Total cell delay for those cells in the form of a histogram.

Script Generation

Algorithm for Script #1 :

1. Get user input
   - path N
   - WNS X
   - OR both
2. Based on the input:
   a. All the cells that are in those N number of paths
   b. Report number of times each cell appeared in those paths
   c. Total cell count and total cell delay in the maximum timing path
   d. Histogram generation of total cell counts

Steps to Find Max Timing path

- Get argument options : path or WNS or both.

```
# Parse the user inputs
set option [lindex $args 0]
set value1 [lindex $args 1]
set option2 [lindex $args 2]
set value2 [lindex $args 3]
```

- Use of *report_timing* command to find desired output.

1. -path N

```
# Perform the operation
report_timing -path full -delay max -nworst $Npath -sort_by slack
```

2. -WNS N (default 1 path)

```
    # Perform the operation
report_timing -path full -delay max -sort_by slack -slack_lesser_than $wns
```

Output

report_timing

- *command provides a report of timing information for the current design*

```
dc_shell> path_timing -path 3
"****************************************************************************
'Path_timing script"
        3 path specified only
****************************************************************************


****************************************
Report : timing
        -path full
        -delay min_fall
        -max_paths 1
Design : simpleAnd
Version: G-2012.06
Date   : Sat Mar 18 13:15:11 2017
****************************************

Operating Conditions: ff0p95v125c   Library: saed32hvt_ff0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: D1_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: D_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  simpleAnd          ForQA                 saed32hvt_ff0p95v125c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  D1_reg/CLK (DFFX1_HVT)                   0.00       0.00 r
  D1_reg/Q (DFFX1_HVT)                     0.08       0.08 f
  U11/Y (OR3X1_HVT)                        0.04       0.12 f
  U19/Y (AND3X1_HVT)                       0.04       0.16 f
  D_reg/D (DFFX1_HVT)                      0.01       0.18 f
  data arrival time                                   0.18

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  D_reg/CLK (DFFX1_HVT)                    0.00       0.00 r
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                  -0.18
  -----------------------------------------------------------
  slack (MET)                                         0.18
```

Total Cell Count

- *"get_attributes"* to find all the combinational cell.

```
  set cells 0
set cellFound 0
array set count_cell {}
set all_paths [get_timing_paths -nworst 10 -path_type full -slack_lesser_than 10]

# To find the Total Number of cells in the Max Timing Path
    foreach_in_collection path $all_paths {
    set  start [get_attribute $path startpoint]
            set  path_start [get_attribute $start full_name]
    #echo sizeof_collection [get_attribute $path startpoint]
    set end [get_attribute $path endpoint]
    set path_end [get_attribute $end full_name]
    #echo "------------------------------------------------------------"
    #puts "**Path between : $path_start - $path_end**"
        set all_points [get_attribute $path points]
    foreach_in_collection point $all_points {
        set start [get_attribute $point object]
        set name [get_attribute $start full_name]
        set cell_name [get_cells -of_object "$name"]
        set cell [get_attribute $cell_name full_name]
```

Continued…..

Store in the array the name and count of cells

```
#only if the gate is a combinational cell
if {$t_cell=="true"} {
    if {[array size count_cell]==0} {
     set count_cell($cell) 1
     set count 1
     #echo [format "%10s %10s" $cell $count ]
    } else { foreach { name_cell count} [array get count_cell] {
                if {[string match $name_cell $cell]} {
              set newcount [expr 1 + $count]
              #set newcount [expr $ewcount/2]
              set count_cell($cell) $newcount
              set cellFound 1
             # echo [format "%10s %10s" $name_cell $count]
              break
             # echo [format "%10s %10s" $name_cell $newcount]
         } else { set cellFound 0 }}
         if {$cellFound==0} { set count_cell($cell) 1}
         }}}}
echo " ********************************************************************** "
echo " The Total number of cell counts in the Maximum Timing Path "
foreach { name_cell count} [array get count_cell] { echo [format "%10s %10s" $name_cell [expr $count/2]] }
echo " ********************************************************************** "
```

Steps in Histogram Generation

- Obtain the array in the form , {cell_a, count, cell_b, count, cell_c, count….}
- For every cell of the array
  - Display “*” , count number of times which signifies the number of times the cell appears in the design

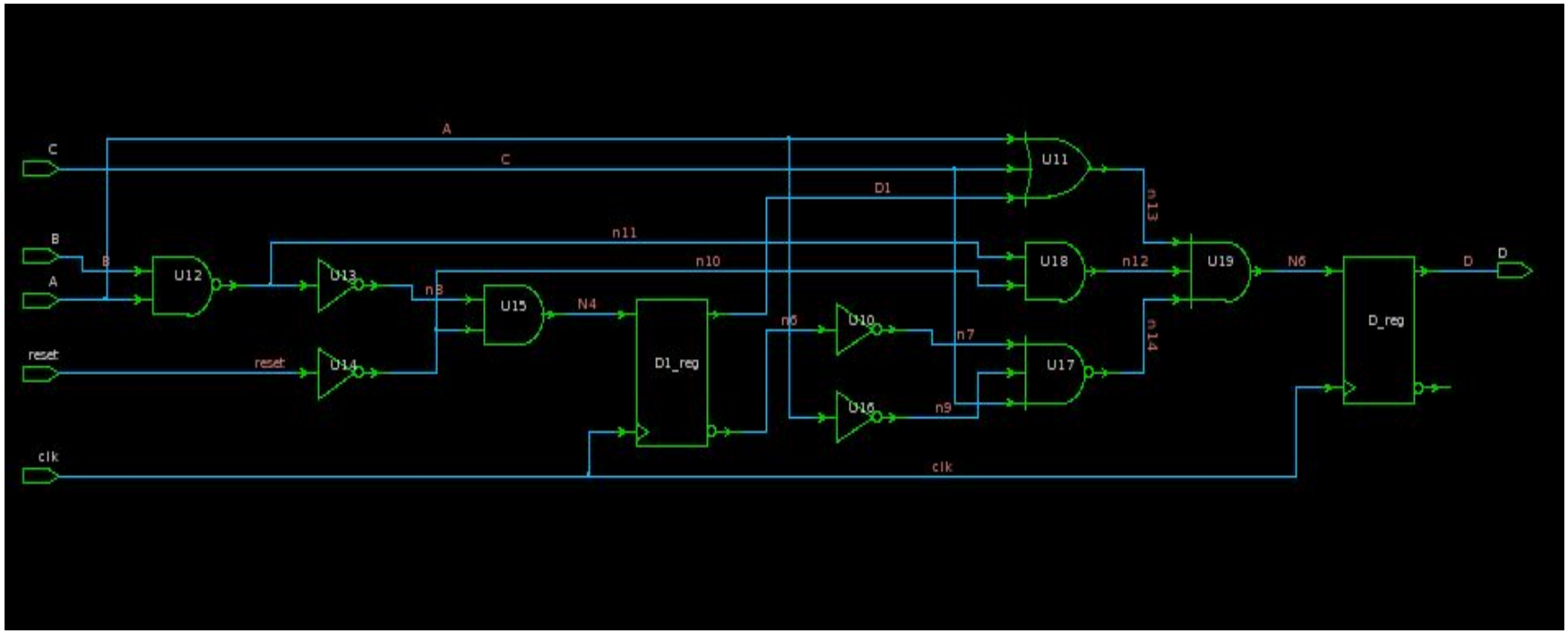
```
foreach element [array names count_cell] {
    puts -nonewline "cell($element) "
    for {set i 0} {$i <= [expr $count_cell($element)/2 - 1]} {incr i} {
        #echo $count_cell($element)
        puts -nonewline "*"
    }
    puts -nonewline "[expr $count_cell($element)/2]"
        #echo $count_cell($element)
    puts "\n"
}
```

Output

```
 ****************************************************************************
 The Total number of cell counts in the Maximum Timing Path
       U16           2
       U12           8
       U17           2
       U13           2
       U18           4
       U11           2
       U15           2
       U19           8
 ****************************************************************************
cell(U16) **2

cell(U12) ********8

cell(U17) **2

cell(U13) **2

cell(U18) ****4

cell(U11) **2

cell(U15) **2

cell(U19) ********8
```

Script #1 - Test and verification

- Test Sample Design - **SimpleAnd**



- Verified the outputs by using report timing and manually counting the cells

Live Demonstration #Script 1

Script #2

- Problem Statement:
  - Maximum and minimum timing paths
  - Inputs :

    Cell, Nets, I/O Ports
  - Outputs:

    Min and max timing margin for each of the cells

    Min and max timing for each of the cell on the other side of sequentials

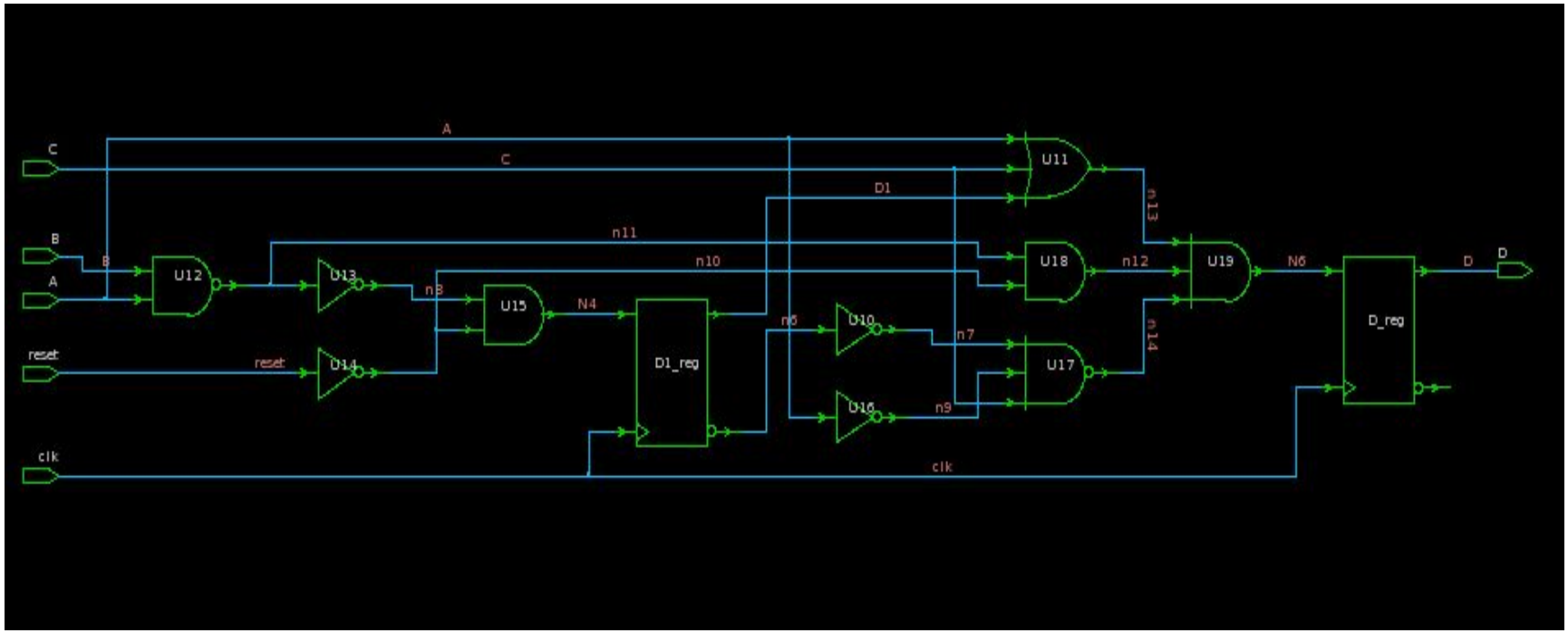
Script Generation

Steps divided into Two parts:

1. Finding Min and Max Margin of cells, given an input
2. Max Timing margin on other side of sequential

Script #2 - Test and verification

- SimpleAnd:



Each Cell Margin

- Set arg options; -cells or -nets or -port.

```
################################################
# Parse the user inputs
set com_args0 [lindex $args 0]
set com_args1 [lindex $args 1]
# Default maximum timing paths to report
set Npath 100
################################################
```

- report_timing for each cell in the maximum timing paths

```
report_timing -path full -delay max -nworst $Npath
        report_timing -path full -delay min
```

Outputs

- Output of report timing for a max timing path

```
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
simpleAnd          ForQA                 saed32hvt_ff0p95v

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
D1_reg/CLK (DFFX1_HVT)                   0.00       0.00 r
D1_reg/QN (DFFX1_HVT)                    0.06       0.06 r
U10/Y (INVX0_HVT)                        0.03       0.09 f
U17/Y (NAND3X0_HVT)                      0.03       0.12 r
U19/Y (AND3X1_HVT)                       0.05       0.17 r
D_reg/D (DFFX1_HVT)                      0.01       0.18 r
data arrival time                                   0.18

clock clk (rise edge)                    0.05       0.05
clock network delay (ideal)              0.00       0.05
D_reg/CLK (DFFX1_HVT)                    0.00       0.05 r
library setup time                      -0.03       0.02
data required time                                  0.02
-----------------------------------------------------------
data required time                                  0.02
data arrival time                                  -0.18
-----------------------------------------------------------
slack (VIOLATED)                                   -0.16
```

Timing Margin on Sequential

- *report_timing*: **to** and **from** ports with their **min** and **max** delays

```
report_timing -from $port -nworst $Npath
report_timing -from $port -delay max -nworst $Npath
report_timing -from $port -delay min
```

```
report_timing -to $port -delay max -nworst $Npath
report_timing -to $port -delay min
```

- Find the max timing margin on the other side of the sequential in the max timing path

```
echo "*****************************************************************"
echo "Max margin on other side of sequential in the max timing paths"
echo "*****************************************************************"
echo ""
report_timing -delay max_fall -nworst $Npath
report_timing -delay max_rise -nworst $Npath
```

Outputs

```
****************************************************************************
Max margin on other side of sequential in the max timing paths
****************************************************************************


****************************************
Report : timing
        -path full
        -delay max_fall
        -max_paths 100
Design : simpleAnd
Version: G-2012.06
Date   : Sat Mar 18 13:55:35 2017
****************************************

Operating Conditions: ff0p95v125c   Library: saed32hvt_ff0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: D1_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: D_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  simpleAnd          ForQA                 saed32hvt_ff0p95v125c

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  D1_reg/CLK (DFFX1_HVT)                   0.00       0.00 r
  D1_reg/QN (DFFX1_HVT)                    0.06       0.06 f
  U16/Y (INVX0_HVT)                        0.02       0.08 r
  U17/Y (NAND3X0_HVT)                      0.04       0.12 f
  U19/Y (AND3X1_HVT)                       0.05       0.17 f
  D_reg/D (DFFX1_HVT)                      0.01       0.19 f
  data arrival time                                   0.19

  clock clk (rise edge)                    0.05       0.05
  clock network delay (ideal)              0.00       0.05
  D_reg/CLK (DFFX1_HVT)                    0.00       0.05 r
  library setup time                      -0.02       0.03
  data required time                                  0.03
  ------------------------------------------------------------
  data required time                                  0.03
  data arrival time                                  -0.19
  ------------------------------------------------------------
  slack (VIOLATED)                                   -0.15


****************************************
```

```
Report : timing
        -path full
        -delay max_rise
        -nworst 100
        -max_paths 100
Design : simpleAnd
Version: G-2012.06
Date   : Sat Mar 18 13:55:39 2017
****************************************

Operating Conditions: ff0p95v125c   Library: saed32hvt_ff0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: D1_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: D_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  simpleAnd          ForQA                 saed32hvt_ff0p95v125c

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  D1_reg/CLK (DFFX1_HVT)                   0.00       0.00 r
  D1_reg/Q (DFFX1_HVT)                     0.08       0.08 r
  U11/Y (OR3X1_HVT)                        0.05       0.12 r
  U19/Y (AND3X1_HVT)                       0.04       0.17 r
  D_reg/D (DFFX1_HVT)                      0.01       0.18 r
  data arrival time                                   0.18

  clock clk (rise edge)                    0.05       0.05
  clock network delay (ideal)              0.00       0.05
  D_reg/CLK (DFFX1_HVT)                    0.00       0.05 r
  library setup time                      -0.03       0.02
  data required time                                  0.02
  ------------------------------------------------------------
  data required time                                  0.02
  data arrival time                                  -0.18
  ------------------------------------------------------------
  slack (VIOLATED)                                   -0.16
```

Live Demonstration # Script 2

Design Steps Followed

- Understand the specifications
- Research and search the DC commands manual for possible useful commands
- Develop the command line argument to suit the requirements
- Develop the Tcl script with procedure for user inputs
- Develop Tcl code to achieve the functionality
- Run the tests to verify that the task was finished

Design challenges Faced

- Understanding the requirements and the appearance of a histogram.
  - Ex: Should we implement using tool generated histograms or download tcl packages or should we write our own code.
  - Addressed the issue with continuous feedback from Prof on implementation

- Parsing the values into a list from a file to count the total number of cells.

- Most of the command attributes present in the dc_shell do not give the output, so had hard time figuring out what command to use.

References

- Books
  - Using Tcl With Synopsys® Tools Version M-2016.12, December 2016
  - IC Compiler™ Variables and Attributes Version M-2016.12, December 2016
- Google
- Tcl Wiki Page
- Research:
  - man *report_timing*
  - help *timing*
  - *report_timing* help
- Big thanks to Professor Patwary!

thank you!