ITE 聯陽半導體 ITE Tech. Inc.

IT8728F

Environment Control – Low Pin Count Input / Output (EC - LPC I/O)

Preliminary Specification V0.4.2

(For E Version)

ITE TECH. INC.

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Please note that the IT8728F V0.4.2 is applicable only to the E version.

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Revision History

Section	Revision	Page No.
-	• E version initial release.	-

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1. Features

- **Low Pin Count Interface**
  - Complies with Intel Low Pin Count Interface Specification Rev. 1.1
  - Supports LDRQ#, SERIRQ protocols
  - Supports PCI PME# Interfaces

- **ACPI & LANDesk Compliant**
  - ACPI V. 2.0 compliant
  - Register sets compatible with “Plug and Play ISA Specification V. 1.0a”
  - LANDesk 3.X compliant
  - Supports 8 logical devices

- **Enhanced Hardware Monitor**
  - Built-in 8-bit Analog to Digital Converter
  - 3 thermal inputs from either remote thermal resistor or thermal diode or diode-connected transistor, the temperature sensor of the current mode
  - 7 voltage monitor inputs (3VSB and VBAT measured internally)
  - 1 chassis open detection input with low power Flip-Flop dual-powered by battery or 3VSB
  - Watch Dog comparison of all monitored values
  - SST/PECI/AMDTSI/PCH SM-Link I/F supporting external temperature reading for fan control

- **Fan Speed Controller**
  - Provides fan on-off and PWM control
  - Supports 5 programmable Pulse Width Modulation (PWM) outputs
  - 256 steps of PWM mode
  - Monitors 5 fan tachometer inputs
  - Provides fan close-loop control

- **SmartGuardian Controller**
  - Provides programmably automatic fan speed control
  - Supports mix-and-match for temperature inputs and fan speed control outputs
  - Overrides fan speed controller during catastrophic situations
  - Provides audible over temperature warning

- **Two 16C550 UARTs**
  - Supports two standard Serial Ports

- **Consumer Remote Control (TV remote) IR with Power-up Feature**
  - Supports two CIR Ports

- **IEEE 1284 Parallel Port**
  - Standard mode -- Bi-directional SPP compliant
  - Enhanced mode -- EPP V. 1.7 and V. 1.9 compliant
  - High-speed mode -- ECP, IEEE 1284 compliant
  - Back-drive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port

- **Floppy Disk Controller**
  - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
    Enhanced digital data separator
  - 3-Mode drives supported
  - Supports automatic write protection via software

- **Keyboard Controller**
  - 8042 compatible with PS/2 keyboard and mouse
  - Hardware KBC
  - GateA20 and Keyboard reset output
  - Supports Multiple keyboard power-on events (Any Keys, 2-5 Sequential Keys, 1-3 simultaneous Keys)
  - Supports mouse double-click and/or mouse move power on events

- **57 General Purpose I/O Pins**
  - Input mode supports either switch de-bounce or programmable external IRQ input routing
  - Output mode supports 2 sets of programmable LED blinking periods

- **Watch Dog Timer**
  - Time resolution 1 minute or 1 second, maximum 65535 minutes or 65535 seconds
  - Output to KRST# and PWRGD when expired

- **ITE’s Innovative Automatic Power-failure Resume and Power Button De-bounce**

- **Eco-design of Energy-using Product (EuP), Extra Low Power S5 Control**

- **Intel DSW Support**

- **Over Voltage/Under Voltage Protection (OVP/UVP)**
  - Supports two modes: force-type and notice type
- **5VAUX_SW Control**
- **AMD CPU Power Sequence Controller**
  - Built-in enhanced voltage comparator
- **Built-in 32.768 kHz Oscillator**
- **Single 24/48 MHz Clock Input**
- **3VSB and VBAT Supported**
- **+3.3V Power Supply**
- **Two Sets of SMBus Isolation Supported**
- **Bus Selection**
- **Case Open Detection**
- **ResetconIN/OUT with De-bounce**
- **128-Pin QFP**
- **RoHS Compliant (100% Green Available)**

2. General Description

The IT8728F is a highly integrated Super I/O using the Low Pin Count Interface. It provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, including H/W Monitor and Fan Speed Controller. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.1". The IT8728F is ACPI & LANDesk compliant.

The IT8728F features an enhanced hardware monitor providing three thermal inputs from remote thermal resistors, or thermal diode or diode-connected transistor (2N3904/2N3906). The device employs ITE's innovative intelligent automatic Fan ON/OFF & speed control functions (SmartGuardian) to protect the system while reducing the system noise and power consumption. The Fan Speed Controller can control up to five fan speeds through five separate 256 steps of Pulse Width Modulation (PWM) output pins and monitor up to five FANs' Tachometer inputs.

In addition, it features two 16C550 standard compatible enhanced UARTs performing asynchronous communication, one multi-mode high-performance parallel port supporting bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9), and IEEE 1284 compliant Extended Capabilities Port (ECP), one high-performance 2.88MB floppy disk controller with digital data separator, supporting two drives in 360K/720K/1.2M/1.44M/2.88M format, one integrated Keyboard Controller, eight GPIO ports controlling up to 57 GPIO pins, which can be individually enabled or disabled via software configuration registers, and IR interface supported.

Regarding eco-design of Energy-using Product (EuP), IT8728F provides not only a solution to reducing power consumption in S5 State but also Keyboard, Mouse, RI# and CIR wakeup events in S3/S5 State.

The IT8728F utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled, the inputs are inhibited with the clock disabled and the outputs are tri-stated. The device requires a single 24/48 MHz clock input and operates with +3.3V power supply. The IT8728F is available in 128-pin QFP (Quad Flat Package).

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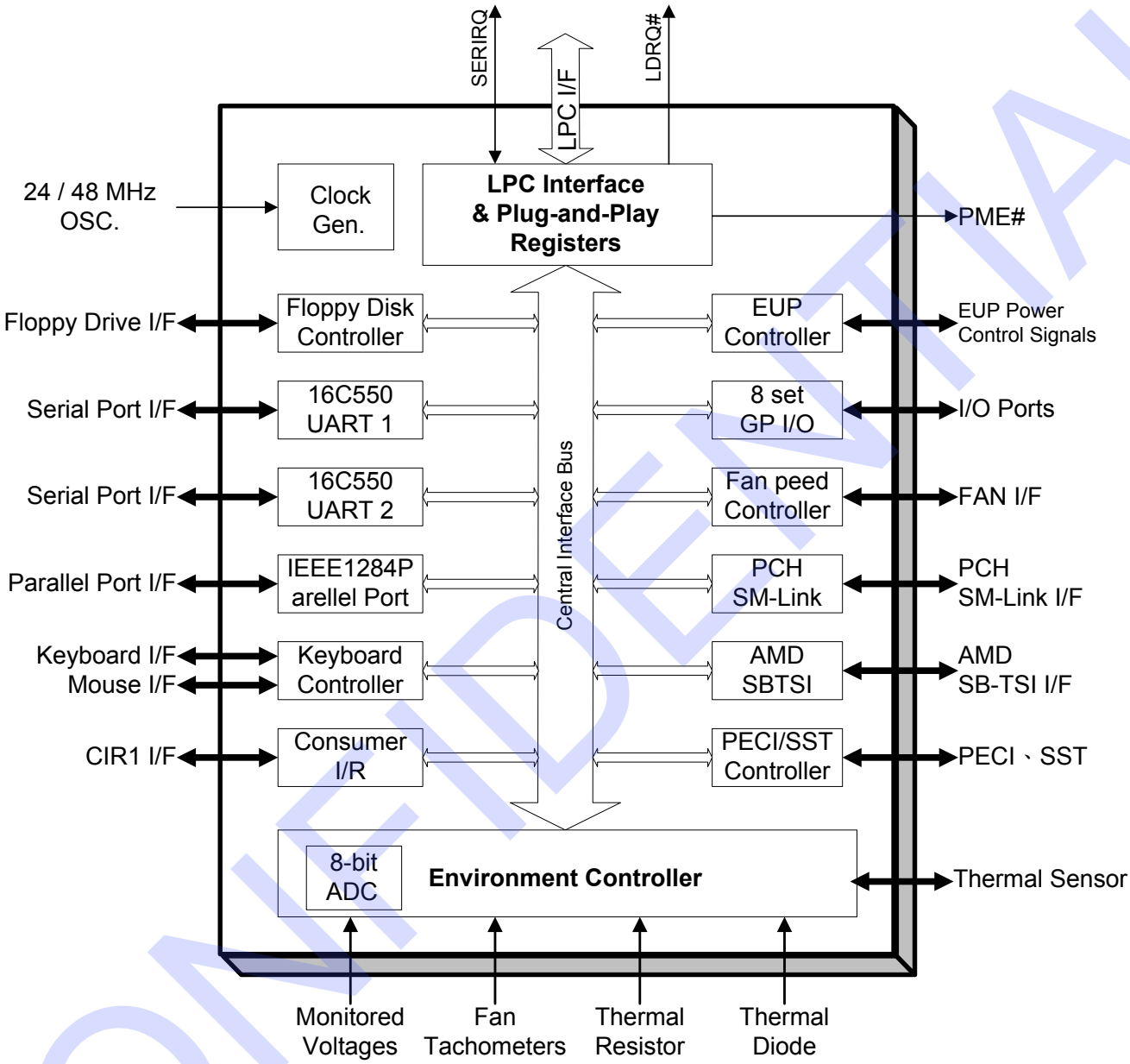
3. Block Diagram



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4. Pin Configuration

Figure 4-1. IT8728F 128-QFP

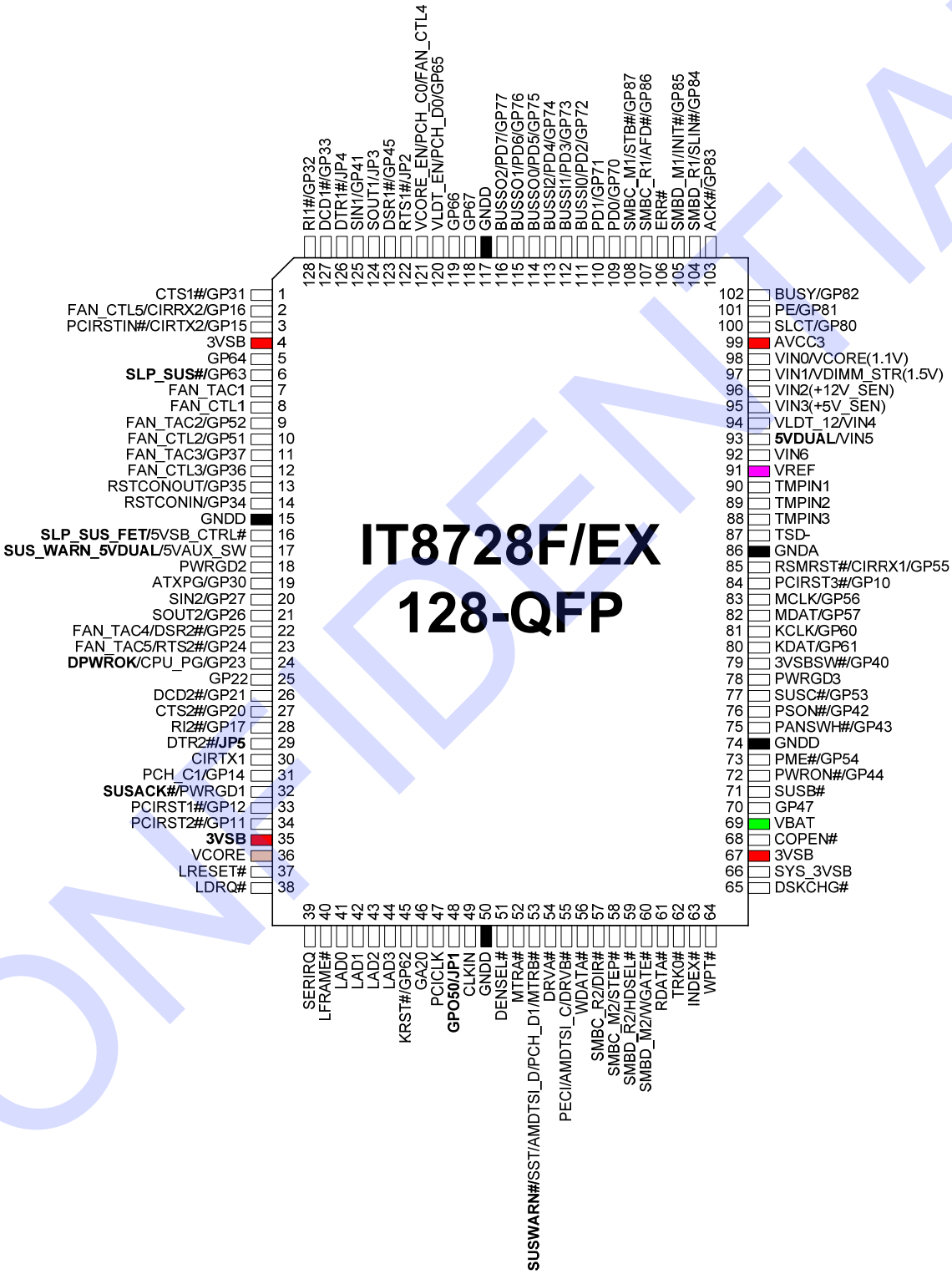

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CTS1#/GP31	33	PCIRST1#/GP12	65	DSKCHG#	97	VIN1/ VIDMM_STR(1.5V)
2	FAN_CTL5/ CIRRX2/GP16	34	PCIRST2#/GP11	66	SYS_3VSB	98	VIN0/ VCORE(1.1V)
3	PCIRSTIN#/ CIRTX2/GP15	35	3VSB	67	3VSB	99	AVCC3
4	3VSB	36	VCORE	68	COPEN#	100	SLCT/GP80
5	GP64	37	LRESET#	69	VBAT	101	PE/GP81
6	SLP_SUS#/GP63	38	LDRQ#	70	GP47	102	BUSY/GP82
7	FAN_TAC1	39	SERIRQ	71	SUSB#	103	ACK#/GP83
8	FAN_CTL1	40	LFRAME#	72	PWRON#/GP44	104	SMBD_R1/SLIN#/ GP84
9	FAN_TAC2/GP52	41	LAD0	73	PME#/GP54	105	SMBD_M1/INIT#/ GP85
10	FAN_CTL2/GP51	42	LAD1	74	GNDD	106	ERR#
11	FAN_TAC3/GP37	43	LAD2	75	PANSWH#/GP43	107	SMBC_R1/AFD#/ GP86
12	FAN_CTL3/GP36	44	LAD3	76	PSON#/GP42	108	SMBC_M1/STB#/ GP87
13	RSTCONOUT/GP35	45	KRST#/GP62	77	SUSC#/GP53	109	PD0/GP70
14	RSTCONIN/GP34	46	GA20	78	PWRGD3	110	PD1/GP71
15	GNDD	47	PCICLK	79	3VSBSW#/GP40	111	BUSSI0/PD2/ GP72
16	SLP_SUS/FET/ 5VSB_CTRL#	48	GPO50/JP1	80	KDAT/GP61	112	BUSSI1/PD3/ GP73
17	SUS_WARN_5VDUAL /5VAUX_SW	49	CLKIN	81	KCLK/GP60	113	BUSSI2/PD4/ GP74
18	PWRGD2	50	GNDD	82	MDAT/GP57	114	BUSSO0/PD5/ GP75
19	ATXPG/GP30	51	DENSEL#	83	MCLK/GP56	115	BUSSO1/PD6/ GP76
20	SIN2/GP27	52	MTRA#	84	PCIRST3#/GP10	116	BUSUO2/PD7/ GP77
21	SOUT2/GP26	53	SUSWARN#/SST/ AMDTSI_D/PCH_D/ MTRB#	85	RSMRST#/CIRRX1/ GP55	117	GNDD
22	FAN_TAC4/DSR2#/ GP25	54	DRVA#	86	GNDA	118	GP67
23	FAN_TAC5/RTS2#/ GP24	55	PECI/AMDTSI_C/ DRVB#	87	TSD-	119	GP66
24	DPWORK/ CPU_PG/GP23	56	WDATA#	88	TMPIN3	120	VLDT_EN/ PCH_D0/GP65
25	GP22	57	SMBC_R2/DIR#	89	TMPIN2	121	VCORE_EN/PCH_ C0/FAN_CTL4
26	DCD2#/GP21	58	SMBC_M2/STEP#	90	TMPIN1	122	RTS1#/JP2
27	CTS2#/GP20	59	SMBD_R2/HDSEL#	91	VREF	123	DSR1#/GP45
28	RI2#/GP17	60	SMBD_M2/WGATE#	92	VIN6	124	SOUT1/JP3
29	DTR2#/JP5	61	RDATA#	93	5VDUAL/VIN5	125	SIN1/GP41
30	CIRTX1	62	TRK0#	94	VLDT_12/VIN4	126	DTR1#/JP4
31	PCH_C1/GP14	63	INDEX#	95	VIN3(+5V_SEN)	127	DCD1#/GP33
32	SUSACK#/ PWRGD1	64	WPT#	96	VIN2(+12_SEN)	128	RI1#/GP32

5. Pin Description

The IT8728F is a 3.3V voltage part. It is just for 3.3V application.

- The I/O buffer output pads are backdrive protected.
- The LPC interface pins are 3.3V only
- The Hardware Monitoring analog pins are 3.3V only . (VIN0~7 and TEMPIN11~3 etc.)
- The input voltage for all other pins is 5V tolerance(ex. ATXPG、FAN_TAC etc)
- For DO pins, It is not 5V tolerant and should not be pull-up to 5V

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35, 67	**3VSB**	PWR	-	***+3.3V Standby Power Supply***
99	**AVCC3**	PWR	-	***+3.3V Analog Power Supply***
69	**VBAT**	PWR	-	***+3V Battery Supply***
36	**VCORE**	AO	-	***Internal Power supply(1.8V)*** It is required to connect this pin with the external capacitance.
15, 50, 74, 117	**GNDD**	GND	-	***Digital Ground***
86	**GNDA**	GND	-	***Analog Ground***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
37	**LRESET#**	DI	AVCC3	***LPC RESET #*** EC block will not be reset by LRESET#, which is controlled by AVCC3 PWRGD.
38	**LDRQ#**	DO8	AVCC3	***LPC DMA Request #*** This is an encoded signal for DMA channel select.
39	**SERIRQ**	DIO16	AVCC3	***Serial IRQ***
40	**LFRAME#**	DI	AVCC3	***LPC Frame #*** This signal indicates the start of the LPC cycle.
41-44	**LAD[0:3]**	DIO16	AVCC3	***LPC Address / Data 0-3*** 4-bit LPC address/bi-directional data lines. LAD0 is LSB and LAD3 is MSB.
47	**PCICLK**	DI	AVCC3	***PCI Clock*** 33 MHz PCI clock input for LPC I/F and SERIRQ.
73	**PME#**	DOD8	3VSB	***Power Management Event #*** The first function of this pin is Power Management Event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state.
	GP54	DIOD8	3VSB	***General Purpose I/O 54*** The second function of this pin is General Purpose I/O Port 5 Bit 4.

Table 5-3. Pin Description of GPI/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
48	**GPO50**	DIOD8	AVCC3	***General Purpose I/O Output 50*** The function of this pin is General Purpose I/O Port 5 Bit 0.
	JP1	DI	3VSB	***Power-On Strapping 1*** For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
28	**RI2#**	DI	3VSB	***Ring Indicator 2 #*** The first function of this pin is Ring Indicator 2 #.
	GP17	DIOD8	AVCC3	***General Purpose I/O 17*** The second function of this pin is General Purpose I/O Port 1 Bit 7.
29	**DTR2#**	DO8	AVCC3	***Data Terminal Ready 2 #*** The function of this pin is Data Terminal Ready 2 #.
	JP5	DI	AVCC3	***Power-On Strapping 5*** For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
27	**CTS2#**	DI	AVCC3	***Clear to Send 2 #*** The first function of this pin is Clear to Send 2 #. Please refer to the description of CTS1# in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP20	DIOD8	3VSB	***General Purpose I/O 20*** The second function of this pin is General Purpose I/O Port 2 Bit 0.
26	**DCD2#**	DI	AVCC3	***Data Carrier Detect 2 #*** The first function of this pin is Data Carrier Detect 2 #. Please refer to the description of DCD1# in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP21	DIOD8	3VSB	***General Purpose I/O 21*** The second function of this pin is General Purpose I/O Port 2 Bit 1.
25	**GP22**	DIOD8	3VSB	***General Purpose I/O 22*** The function of this pin is General Purpose I/O Port 2 Bit 2.
24	**DPWROK**	DOD8	3VSB	***3VSB Power OK Output*** The first function of this pin is 3VSB Power OK Output. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	CPU_PG	DOD8	AVCC3	***CPU Power-good*** The second function of this pin is to indicate that CPU power-good is ready. The external pull high resistor is required. The function configuration of this pin is determined by the power-on strapping option (JP4).
	GP23	DIOD8	3VSB	***General Purpose I/O 23*** The third function of this pin is General Purpose I/O Port 2 Bit 3.
23	**FAN_TAC5**	DI	AVCC3	***FAN Tachometer Input 5*** The first function of this pin is Fan Tachometer Input 5. 0 to +5V amplitude fan tachometer input.
	RTS2#	DO8	AVCC3	***Request to Send 2 #*** The second function of this pin is Request to Send 2 #. Please refer to the description of RTS1# in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP24	DIOD8	3VSB	***General Purpose I/O 24*** The third function of this pin is General Purpose I/O Port 2 Bit 4.

Pin(s) No.	Symbol	Attribute	Power	Description
22	FAN_TAC4	DI	AVCC3	***FAN Tachometer input 4*** The first function of this pin is Fan Tachometer Input 4. 0 to +5V amplitude fan tachometer input.
	DSR2#	DI	AVCC3	***Data Set Ready 2 #*** The second function of this pin is Data Set Ready 2 #. Please refer to the description of DSR1# in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP25	DIOD8	3VSB	***General Purpose I/O 25*** The third function of this pin is General Purpose I/O Port 2 Bit 5.
21	SOUT2	DO8	AVCC3	***Serial Data Output 2*** The first function of this pin is Serial Data Output 2. Please refer to the description of SOUT1 in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP26	DIOD8	3VSB	***General Purpose I/O 26*** The second function of this pin is General Purpose I/O Port 2 Bit 6.
20	SIN2	DI	AVCC3	***Serial Data Input 2*** The first function of this pin is Serial Data Input 2. Please refer to the description of SIN1 in Table 5-7. Pin Description of Serial Port 1 Signals on page 18.
	GP27	DIOD8	3VSB	***General Purpose I/O 27*** The second function of this pin is General Purpose I/O Port 2 Bit 7.
118	GP67	DIOD8	VBAT	***General Purpose I/O 67*** The second function of this output pin is General Purpose I/O Port 6 Bit 7.
119	GP66	DIOD8	VBAT	***General Purpose I/O 66*** The function of this pin is General Purpose I/O Port 6 Bit 6.
120	VLDT_EN	DOD8	AVCC3	***VLDT Enable*** The first function of this pin is to enable VLDT Voltage. The external pull high resistor is required. The function configuration of this pin is determined by the power-on strapping option (JP4).
	PCH_D0	DOD8	AVCC3	***PCH SM-Link Data 0 Pin*** The second function of this pin is PCH SM-Link Data.
	GP65	DIOD8	3VSB	***General Purpose I/O 65*** The third function of this pin is General Purpose I/O Port 6 Bit 5.

Table 5-4. Pin Description of Hardware Monitor Signals

Pin(s) No.	Symbol	Attribute	Power	Description
98	VIN0	AI	AVCC3	***Voltage Analog Input 0*** The first function of this pin is 0 to 3.072V FSR Analog Input.
	VCORE (1.1V)	AI	AVCC3	***VCORE (1.1V) Analog Inputs*** The second function of this pin is VCORE (1.1V) Analog Input. The function configuration of this pin is determined by the power-on strapping option (JP4).
97	VIN1	AI	AVCC3	***Voltage Analog Input 1*** The first function of this pin is 0 to 3.072V FSR Analog Input.
	VDIMM_STR	AI		***VDIMM DUAL STR (1.5V) Analog Input*** The second function of this pin is VDIMM DUAL STR (1.5V) Analog Input. The function configuration of this pin is determined by the power-on strapping option (JP4).
96	VIN2 (+12V_SEN)	AI	AVCC3	***Voltage Analog Input 2 (+12V power detector)*** The function of this pin is 0 to 3.072V FSR Analog Input. Besides, it is the power detector for PWRGD1/2/3. Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
95	VIN3 (+5V_SEN)	AI	AVCC3	***Voltage Analog Input 3 (+5V power detector)*** The function of this pin is 0 to 3.072V FSR Analog Input. Besides, it is the power detector for PWRGD1/2/3. Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
94	VIN4	AI	AVCC3	***Voltage Analog Input 4*** The first function of this pin is 0 to 3.072V FSR Analog Input.
	VLDT_12	AI	AVCC3	***VLDT (1.2V) Analog Inputs*** The second function of this pin is VLDT (1.2V) Analog Input. The function configuration of this pin is determined by the power-on strapping option (JP4).
93	5VDUAL	AI	AVCC3	***Systme 5VDUAL Monitor*** The first function of this pin is analog input for system 5VDUAL monitor. When the voltage drops below 0.7V, the 5VDUAL monitor circuit will assert SUSACK#. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	VIN5	AI	AVCC3	***Voltage Analog Input 5*** The second function of this pin is 0 to 3.072V FSR Analog Input.
92	VIN6	AI	AVCC3	***Voltage Analog Input 6*** The function of this pin is 0 to 3.072V FSR Analog Input.
91	VREF	AO	AVCC3	***Reference Voltage Output (2.8V)*** Regulated and referred voltage for external temperature sensors and negative voltage monitors.
88-90	TMPIN[1:3]	AI	AVCC3	***External Thermal Inputs [1:3]*** These pins are connected to thermistors [1:3] or thermal temperature sensors.
87	TS_D-	AI	AVCC3	***Thermal Diode Negative Input***
7	FAN_TAC1	DI	AVCC3	***Fan Tachometer Input 1*** The function of this pin is Fan Tachometer Input 1, 0 to +5V amplitude fan tachometer input.

Pin(s) No.	Symbol	Attribute	Power	Description
9	FAN_TAC2	DI	AVCC3	***Fan Tachometer Input 2*** The first function of this pin is Fan Tachometer Input 2, 0 to +5V amplitude fan tachometer input.
	GP52	DIOD8	AVCC3	***General Purpose I/O 52*** The second function of this pin is General Purpose I/O Port 5 Bit 2.
11	FAN_TAC3	DI	AVCC3	***Fan Tachometer Input 3*** The first function of this pin is Fan Tachometer Input 3, 0 to +5V amplitude fan tachometer input.
	GP37	DIOD8	AVCC3	***General Purpose I/O 37*** The second function of this pin is General Purpose I/O Port 3 Bit 7.
19	ATXPG	DI	AVCC3	***ATX Power Good*** The first function of this pin is ATX Power Good. For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect **AND** SUSB# **AND** VIN2(+12V_SEN) **AND** VIN3(+5V_SEN) **AND** ATXPG). Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
	GP30	DIOD8	AVCC3	***General Purpose I/O 30*** The second function of this pin is General Purpose I/O Port 3 Bit 0.
18	PWRGD2	DOD8	AVCC3	***Power Good Output 2 with 50ms Delay Time*** The function of this pin is Power Good Output 2. For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect **AND** SUSB# **AND** VIN2(+12V_SEN) **AND** VIN3(+5V_SEN) **AND** ATXPG). Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
17	SUS_WARN_5V DUAL	DOD8	3VSB	***5VDUAL Power Control***The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	5VAUX_SW	DOD8	3VSB	***5VAUX Power Switch Control*** It is the inverse of 3VSBSW# and can be used as active control for the register at S5 and S3 stage. Please refer to section 11.16 5VAUX_SW Power Control on page 196 for the detail.
16	SLP_SUS_FET	DOD8	3VSB	***Sleep Power Control Output*** The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	5VSB_CTRL#	DOD8	3VSB	***5VSB_CTRL# Power Control Signal*** Please refer to section 11.15 Energy-using Product (EuP) Power Control Signal Timings on page 195 for the detail.
14	RSTCONIN	DI	3VSB	***Reset Connect Input*** The first function of this pin is Reset Connect Input.
	GP34	DIOD8	AVCC3	***General Purpose I/O 34*** The second function of this pin is General Purpose I/O Port 3 Bit 4.
13	RSTCONOUT	DOD8	3VSB	***Reset Connect Output*** The first function of this pin is Reset Connect Output with de-bounced.
	GP35	DIOD8	AVCC3	***General Purpose I/O 35*** The second function of this pin is General Purpose I/O Port 3 Bit 5.

Pin(s) No.	Symbol	Attribute	Power	Description
6	**SLP_SUS#**	DI	3VSB	***Deep Sleep Indication*** From CPT PCH, when asserted low, this signal indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	GP63	DIOD8	AVCC3	***General Purpose I/O 63*** The function of this pin is General Purpose I/O Port 6 Bit 3.
5	**GP64**	DIOD8	AVCC3	***General Purpose I/O 64*** The second function of this pin is General Purpose I/O Port 6 Bit 4.
68	**COPEN#**	DIOD8	3VSB or VBAT	***Case Open Detection #*** The Case Open Detection is connected to a specially designed low power CMOS flip-flop dual-powered by battery or 3VSB for case open state preservation during power loss.

Table 5-5. Pin Description of Fan Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
8	**FAN_CTL1**	DOD8	AVCC3	***Fan Control Output 1*** The function of this pin is Fan Control Output 1. (PWM output signal to Fan's FET.)
10	**FAN_CTL2**	DOD8	AVCC3	***Fan Control Output 2*** The first function of this pin is Fan Control Output 2. (PWM output signal to Fan's FET.)
	GP51	DIOD8	AVCC3	***General Purpose I/O 51*** The second function of this pin is General Purpose I/O Port 5 Bit 1.
12	**FAN_CTL3**	DOD8	AVCC3	***Fan Control Output 3*** The first function of this pin is Fan Control Output 3. (PWM output signal to Fan's FET.)
	GP36	DIOD8	AVCC3	***General Purpose I/O 36*** The second function of this pin is General Purpose I/O Port 3 Bit 6.
121	**VCORE_EN**	DOD8	AVCC3	***VCORE Enable*** The first function of this pin is VCORE Enable, which is to enable the PWM controller for CPU core voltage. The external pull high resistor is required. The function configuration of this pin is determined by the power-on strapping option (JP4).
	PCH_C0	DIOD8	AVCC3	***PCH SM-Link Clock Pin 0*** The second function of this pin is PCH SM-Link Clock.
	FAN_CTL4	DOD8	AVCC3	***Fan Control Output 4*** The third function of this pin is Fan Control Output 4. (PWM output signal to Fan's FET.)
2	**FAN_CTL5**	DOD8	AVCC3	***Fan Control Output 5*** The first function of this pin is Fan Control Output 5. (PWM output signal to Fan's FET.)
	CIRRX2	DI	AVCC3	***Consumer Infrared Receive Input 2*** The second function of this pin is Consumer Infrared Receive Input 2.
	GP16	DIOD8	AVCC3	***General Purpose I/O 16*** The third function of this pin is General Purpose I/O Port 1 Bit 6.

Table 5-6. Pin Description of Infrared Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
30	**CIRTX1**	DO8	AVCC3	***Consumer Infrared Transmit Output 1*** The function of this pin is Consumer Infrared Transmit Output 1.
85	**RSMRST#**	DOD8	3VSB	***Resume Reset #*** The first function of this pin is Resume Reset #. It is a power good signal of SYS_3VSB.
	CIRRX1	DI	3VSB	***Consumer Infrared Receive Input 1*** The second function of this pin is Consumer Infrared Transmit Input 1.
	GP55	DIOD8	3VSB	***General Purpose I/O 55*** The third function of this pin is General Purpose I/O Port 5 Bit 5.
3	**PCIRSTIN#**	DI	AVCC3	***PCI Reset Input #*** The first function of this pin is the PCI Reset Input #. (for PCIRST2# only)
	CIRTX2	DO8	AVCC3	***Consumer Infrared Transmit Output 2*** The second function of this pin is Consumer Infrared Transmit Output 2.
	GP15	DIOD8	AVCC3	***General Purpose I/O 15*** The third function of this pin is General Purpose I/O Port 1 Bit 5.
2	**FAN_CTL5**	DOD8	AVCC3	***Fan Control Output 5*** The first function of this pin is Fan Control Output 5. (PWM output signal to Fan's FET.)
	CIRRX2	DI	AVCC3	***Consumer Infrared Receive Input 2*** The second function of this pin is Consumer Infrared Receive Input 2.
	GP16	DIOD8	AVCC3	***General Purpose I/O 16*** The third function of this pin is General Purpose I/O Port 1 Bit 6.
66	**SYS_3VSB**	AI	3VSB	***System 3.3V Standby Power Detector*** The function of this pin is System Standby Power Detector for RSMRST# output and EuP signal Control. Please refer to Figure 7-1. IT8728F EUP Applications Circuitry for Intel ICH on page 38 ,section 11.15 Energy-using Product (EuP) Power Control Signal Timings on page 195 and section 11.18 DSW Timings for the detail.
70	**GP47**	DIOD8	AVCC3	***General Purpose I/O 47*** The function of this pin is General Purpose I/O Port 4 Bit 7.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
128	RI1#	DI	3VSB	***Ring Indicator 1 #*** When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
	GP32	DIOD8	AVCC3	***General Purpose I/O 32*** The second function of this pin is General Purpose I/O Port 3 Bit 2.
127	DCD1#	DI	AVCC3	***Data Carrier Detect 1 #*** When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
	GP33	DIOD8	AVCC3	***General Purpose I/O 33*** The second function of this pin is General Purpose I/O Port 3 Bit 3.
126	DTR1#	DO8	AVCC3	***Data Terminal Ready 1 #*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
	JP4	DI	AVCC3	***Power-On Strapping 4*** For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
125	SIN1	DI	AVCC3	***Serial Data Input 1*** This input receives serial data from the communications link.
	GP41	DIOD8	3VSB	***General Purpose I/O 41*** The second function of this pin is General Purpose I/O Port 4 Bit 1.
124	SOUT1	DO8	AVCC3	***Serial Data Output 1*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
	JP3	DI	AVCC3	***Power-On Strapping 3*** For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
123	DSR1#	DI	AVCC3	***Data Set Ready 1 #*** When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
	GP45	DIOD8	3VSB	***General Purpose I/O 45*** The second function of this pin is General Purpose I/O Port 4 Bit 5.

Pin(s) No.	Symbol	Attribute	Power	Description
122	RTS1#	DO8	AVCC3	***Request to Send 1 #*** When this signal is low, the output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. For the power-on strapping option, please refer to Table 7-1. Power On Strapping Options on page 37.
1	CTS1#	DI	AVCC3	***Clear to Send 1 #*** When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
	GP31	DIOD8	AVCC3	***General Purpose I/O 31*** The second function of this pin is General Purpose I/O Port 3 Bit 1.

Table 5-8. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	SLCT	DI	AVCC3	***Printer Select*** The first function of this pin is Printer Select. This signal goes high when the line printer has been selected.
	GP80	DIOD24	3VSB	***General Purpose I/O 80*** The second General Purpose I/O 80function of this pin is General Purpose I/O Port 8 Bit 0. The function will be SLTC if LDN3 (parallel port) is enabled; otherwise, GP80.
101	PE	DI	AVCC3	***Printer Paper End*** The first function of this pin is Printer Paper End. This signal is set high by the printer when it runs out of paper.
	GP81	DIOD8	3VSB	***General Purpose I/O 81*** The second function of this pin is General Purpose I/O Port 8 Bit 1. The function will be PE if LDN3 (parallel port) is enabled; otherwise, GP81.
102	BUSY	DI	AVCC3	***Printer Busy*** The first function of this pin is Printer Busy. This signal goes high when the line printer has a local operation in progress and cannot accept any data.
	GP82	DIOD8	3VSB	***General Purpose I/O 82*** The second function of this pin is General Purpose I/O Port 8 Bit 2. The function will be BUSY when LDN3 (parallel port) is enabled; otherwise, GP82.
103	ACK#	DI	AVCC3	***Printer Acknowledge #*** The first function of this pin is Printer Acknowledge #. This signal goes low to indicate that the printer has already received a character and is ready to accept another one.
	GP83	DIOD8	3VSB	***General Purpose I/O 83*** The second function of this pin is General Purpose I/O Port 8 Bit 3. The function will be ACK# if LDN3 (parallel port) is enabled; otherwise, GP83.

Pin(s) No.	Symbol	Attribute	Power	Description
104	SMBD_R1	IO_SW	3VSB	***SMBus Isolation Set 1*** The first function of this pin is SMBus Isolation Circuit.
	SLIN#	DIO24	AVCC3	***Printer Select Input #*** The second function of this pin is Printer Select Input #. When this signal is low, the printer is selected and it is derived from the complement of bit 3 of Control Port Register (Base Address 1 + 02h) (refer to page 156).
	GP84	DIOD24	3VSB	***General Purpose I/O 84*** The third function of this pin is General Purpose I/O Port 8 Bit 4. The function will be SLIN# if LDN3 (parallel port) is enabled; otherwise, GP84.
105	SMBD_M1	IO_SW	3VSB	***SMBus Isolation Set 1*** The first function of this pin is SMBus Isolation Circuit.
	INIT#	DIO24	AVCC3	***Printer Initialize #*** The second function of this pin is Printer Initialize #. When this signal is low, the printer is selected and it is derived from the complement of bit 2 of Control Port Register (Base Address 1 + 02h) (refer to page 156).
	GP85	DIOD24	3VSB	***General Purpose I/O 85*** The third function of this pin is General Purpose I/O Port 8 Bit 5. The function will be INIT# if LDN3 (parallel port) is enabled; otherwise, GP85.
106	ERR#	DI	AVCC3	***Printer Error #*** The function of this pin is Printer Error #, which will be configured by programming the software configuration registers (LDN3 (parallel port) enabled). When this signal is low, it indicates that the printer has encountered an error and the error message can be read from bit 3 of Status Port Register (Base Address 1 + 01h) (refer to page 156).
107	SMBC_R1	IO_SW	3VSB	***SMBus Isolation Set 1*** The first function of this pin is SMBus Isolation Circuit.
	AFD#	DIO24	AVCC3	***Printer Auto Line Feed #*** The second function of this pin is Printer Auto Line Feed #. When this signal is low, it is derived from the complement of bit 1 of Control Port **Register** (Base Address 1 + 02h) (refer to page 156) and is used to advance one line after each line is printed.
	GP86	DIOD24	3VSB	***General Purpose I/O 86*** The third function of this pin is General Purpose I/O Port 8 Bit 6. The function will be AFD# if LDN3 (parallel port) is enabled; otherwise, GP86.
108	SMBC_M1	IO_SW	3VSB	***SMBus Isolation Set 1*** The first function of this pin is SMBus Isolation Circuit.
	STB#	DI	AVCC3	***Printer Strobe #*** The second function of this pin is Printer Strobe. When this signal is low, it is the complement of bit 0 of Control Port Register (Base Address 1 + 02h) (refer to page 156) and is used to strobe the printing data into the printer.
	GP87	DIOD24	3VSB	***General Purpose I/O 87*** The third function of this pin is General Purpose I/O Port 8 Bit 7. The function will be STB# if LDN3 (parallel port) is enabled; otherwise, GP87.

Pin(s) No.	Symbol	Attribute	Power	Description
109-110	**PD[0:1]**	DIO24	AVCC3	***Parallel Port Data [0:1]*** The first function of these pins is Parallel Port Data [0:1]. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
	GP7[0:1]	DIOD24	3VSB	***General Purpose I/O 7 [0:1]*** The second function of these pins is General Purpose I/O Port 0-1. The function will be PD[0:1] if LDN3 (parallel port) is enabled; otherwise; GP7[0:1].
111-113	**BUSSI[0:2]**	DI	AVCC3	***Bus Selection Input [0:2]*** The first function of these pins, enabled in default, is Bus Selection Input [0:2].
	PD[2:4]	DI	AVCC3	***Parallel Port Data [2:4]*** The second function of these pins is Parallel Port Data [2:4]. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
	GP7[2:4]	DIOD24	3VSB	***General Purpose I/O 7 [2:4]*** The third function of these pins is General Purpose I/O Port 2-4. The function will be PD[2:4] if LDN3 (parallel port) is enabled; otherwise; GP7[2:4].
114-116	**BUSSO[0:2]**	DOD24	AVCC3	***Bus Selection Output [0:2]*** The first function of these pins, enabled in default, is Bus Selection Output [0:2].
	PD[5:7]	DI	AVCC3	***Parallel Port Data [5:7]*** The second function of these pins is Parallel Port Data [5:7]. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
	GP7[5:7]	DIOD24	3VSB	***General Purpose I/O 7[5:7]*** The third function of these pins is General Purpose I/O Port 5-7. The function will be PD[5:7] if LDN3 (parallel port) is enabled; otherwise; GP7[5:7].

Table 5-9. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
51	DENSEL#	DO24L	AVCC3	***FDD Density Select #*** DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
52	MTRA#	DO24L	AVCC3	***FDD Motor A Enable #*** This signal is active low.
53	SUSWARN#	DI	3VSB	***SUSWARN#*** The first function of this pin is a signal form CPT PCH. When this signal is low, it indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	SST	SST	AVCC3	***SST*** The second function of this pin is SST. Specifically when External Thermal Sensor Host (SST、PECI、AMDTSI、PCH SM-Link) is enabled (bit 6-4 of EC Index 0Ah), the function of this pin is selected as SST or ETS_DAT.
	AMDTSI_D	DIOD24	AVCC3	***AMDTSI I/F Data Pin*** The third function of this pin is AMDTSI I/F Data.
	PCH_D1	DIOD24	AVCC3	***PCH SM-Link Set 1 Data Pin*** The fourth function of this pin is PCH SM-Link Data.
	MTRB#	DO24L	AVCC3	***FDD Motor B Enable #*** The fifth function of this pin is FDD Motor B #. This signal is active low.
54	DRVA#	DO24L	AVCC3	***FDD Drive A Enable #*** This signal is active low.
55	PECI	PECI	AVCC3	***PECI (for 1.05V I/F)*** The first function of this pin is PECI. Specifically when External Thermal Sensor Host (SST、PECI、AMDTSI、PCH SM-Link) is enabled (bit 6-4 of EC Index 0Ah), this pin is selected as PECI or ETS_CLK.
	AMDTSI_C	DIOD24	AVCC3	***AMDTSI I/F Clock Pin*** The secondd function of this pin is AMDTSI I/F Clock.
	DRVB#	DO24L	AVCC3	***FDD Drive B Enable #*** The third function of this pin is FDD Drive B #. This signal is active low.
56	WDATA#	DO24L	AVCC3	***FDD Write Serial Data to Drive #*** This signal is active low.
57	SMBC_R2	IO_SW	3VSB	***SMBus Isolation Set 2*** The first function of this pin is SMBus Isolation Circuit.
	DIR#	DO24L	AVCC3	***FDD Head Direction #*** The second function of this pin is FDD DIR#. Step in when this signal is low and step out when high during a SEEK operation.
58	SMBC_M2	IO_SW	3VSB	***SMBus Isolation Set 2*** The first function of this pin is SMBus Isolation Circuit.
	STEP#	DO24L	AVCC3	***FDD Step Pulse #*** The second function of this pin is FDD STEP#. This signal is active low.
59	SMBD_R2	IO_SW	3VSB	***SMBus Isolation Set 2*** The first function of this pin is SMBus Isolation Circuit.
	HDSEL#	DO24L	AVCC3	***FDD Head Select #*** The second function of this pin is FDD HDSEL#. This signal is active low.

Pin(s) No.	Symbol	Attribute	Power	Description
60	SMBD_M2	IO_SW	3VSB	***SMBus Isolation Set 2*** The first function of this pin is SMBus Isolation Circuit.
	WGATE#	DO24L	AVCC3	***FDD Write Gate Enable #*** The second function of this pin is FDD WGATE#. This signal is active low.
61	RDATA#	DI	AVCC3	***FDD Read Disk Data #*** This signal is active low. It is serial data input from FDD.
62	TRK0#	DI	AVCC3	***FDD Track 0 #*** This signal is active low. It indicates that the head of the selected drive is on track 0.
63	INDEX#	DI	AVCC3	***FDD Index #*** This signal is active low. It indicates the beginning of a disk track.
64	WPT#	DI	AVCC3	***FDD Write Protect #*** This signal is active low. It indicates that the disk of the selected drive is write-protected.
65	DSKCHG#	DI	AVCC3	***FDD Disk Change #*** This signal is active low. It senses whether the drive door has been opened or a diskette has been changed.

Table 5-10. Pin Description of GPIO Function

Pin(s) No.	Symbol	Attribute	Power	Description
31	PCH_C1	DIOD8	AVCC3	***PCH SM-Link Set 1 Clock Pin*** The first function of this pin is PCH SM-Link Clock.
	GP14	DIOD8	AVCC3	***General Purpose I/O 14*** The second function of this pin is General Purpose I/O Port 1 Bit 4.
32	SUSACK#	DOD8	3VSB	***SUSACK#*** The first function of this pin is SUSACK# Output. When the 5VDUAL pin drops below 0.7V, SIO will issue SUSACK# to PCH. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	PWRGD1	DOD8	AVCC3	***Power Good Output 1 with 30ms Delay Time*** The second function of this pin is Power Good Output 1. For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect **AND** SUSB# **AND** VIN2(+12V_SEN) **AND** VIN3(+5V_SEN) **AND** ATXPG). Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
33	PCIRST1#	DO8	AVCC3	***PCI Reset 1 #*** The first function of this pin is PCI Reset 1 #, which is a buffer of LRESET#.
	GP12	DIOD8	AVCC3	***General Purpose I/O 12*** The second function of this pin is General Purpose I/O Port 1 Bit 2.
34	PCIRST2#	DO8	AVCC3	***PCI Reset 2 #*** The first function of this pin is PCI Reset 2 #, which is a buffer of LRESET# / PCIRSTIN#.
	GP11	DIOD8	AVCC3	***General Purpose I/O 11*** The second function of this pin is General Purpose I/O Port 1 Bit 1.

Pin(s) No.	Symbol	Attribute	Power	Description
84	**PCIRST3#**	DOD8	3VSB	***PCI Reset 3 #*** The first function of this pin is PCI Reset 3 #, which is a buffer of LRESET#.
	GP10	DIOD8	3VSB	***General Purpose I/O 10*** The second function of this pin is General Purpose I/O Port 1 Bit 0.

Table 5-11. Pin Description of Keyboard Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
80	**KDAT**	DIOD24	3VSB	***Keyboard Data*** The first function of this pin is Keyboard Data.
	GP61	DIOD24	AVCC3	***General Purpose I/O 61*** The second function of this pin is General Purpose I/O Port 6 Bit 1. This set supports Simple I/O function only. This pin doesn't support internal pull-up.
81	**KCLK**	DIOD24	3VSB	***Keyboard Clock*** The first function of this pin is Keyboard Clock.
	GP60	DIOD24	AVCC3	***General Purpose I/O 60*** The second function of this pin is General Purpose I/O Port 6 Bit 0. This set supports Simple I/O function only. This pin doesn't support internal pull-up.
82	**MDAT**	DIOD24	3VSB	***PS/2 Mouse Data*** The first function of this pin is PS/2 Mouse Data.
	GP57	DIOD24	AVCC3	***General Purpose I/O 57*** The second function of this pin is General Purpose I/O Port 5 Bit 7. This pin doesn't support internal pull-up.
83	**MCLK**	DIOD24	3VSB	***PS/2 Mouse Clock*** The first function of this pin is PS/2 Mouse Clock.
	GP56	DIOD24	AVCC3	***General Purpose I/O 56*** The second function of this pin is General Purpose I/O Port 5 Bit 6. This pin doesn't support internal pull-up.
45	**KRST#**	DO8	AVCC3	***Keyboard Reset #*** The first function of this pin is Keyboard Reset #.
	GP62	DIOD8	AVCC3	***General Purpose I/O 62*** The second function of this pin is General Purpose I/O Port 6 Bit 2. This set supports Simple I/O function only.
46	**GA20**	DO8	AVCC3	***Gate Address 20***

Table 5-12. DSW (Deep Sleep Well) Signals

Pin(s) No.	Symbol	Attribute	Power	Description
16	SLP_SUS_FET	DOD8	3VSB	***Sleep Power Control Output*** The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	5VSB_CTRL#	DOD8	3VSB	***5VSB_CTRL# Power Control Signal*** Please refer to section 11.15 Energy-using Product (EuP) Power Control Signal Timings on page 195 for the detail. The function configuration of this pin is determined by the power-on strapping option (JP1=1).
17	SUS_WARN_5VDUAL	DOD8	3VSB	***5VDUAL Power Control*** The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	5VAUX_SW	DOD8	3VSB	***5VAUX Power Switch Control*** It is the inverse of 3VSBSW# and can be used as active control for the register at S5 and S3 stage. Please refer to section 11.16 5VAUX_SW Power Control on page 196 for the detail.
24	DPWROK	DOD8	3VSB	***3VSB Power OK Output*** The first function of this pin is 3VSB Power OK output. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	CPU_PG	DOD8	AVCC3	***CPU Power-good*** The second function of this pin is to indicate that CPU power-good is ready. The external pull-high resistor is required. The function configuration of this pin is determined by the power-on strapping option (JP4).
	GP23	DIOD8	3VSB	***General Purpose I/O 23*** The third function of this pin is General Purpose I/O Port 2 Bit 3.
32	SUSACK#	DOD8	3VSB	***SUSACK#*** The first function of this pin is SUSACK# output. When 5VDUAL pin drops below 0.7V. SIO will issue SUSACK# to PCH. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	PWRGD1	DOD8	AVCC3	***Power Good Output 1 with 30ms Delay Time*** The function of this pin is Power Good Output 1. For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect **AND** SUSB# **AND** VIN2(+12V_SEN) **AND** VIN3(+5V_SEN) **AND** ATXPG). Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.

Pin(s) No.	Symbol	Attribute	Power	Description
53	**SUSWARN#**	DI	3VSB	***SUSWARN#*** The first function of this pin is a signal form CPT PCH. When this signal is low, it indicates PCH is in the deep sleep state. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	SST	SST	AVCC3	***SST*** The second function of this pin is SST. Specifically when External Thermal Sensor Host (SST、PECI、AMDTSI、PCH SM-Link) is enabled (bit 6-4 of EC Index 0Ah), the function of this pin is selected as SST or ETS_DAT.
	AMDTSI_D	DIOD24	AVCC3	***AMDTSI I/F Data*** The third function of this pin is AMDTSI I/F Data.
	PCH_D1	DIOD24	AVCC3	***PCH SM-Link Set 1 Data*** The fourth function of this pin is PCH SM-Link Data.
	MTRB#	DO24L	AVCC3	***FDD Motor B Enable #*** The fifth function of this pin is FDD Motor B #. This signal is active low.
93	**5VDUAL**	AI	AVCC3	***Systme 5VDUAL Monitor*** The first function of this pin is analog input for system 5VDUAL monitor. When the voltage drops below 0.7V, the 5VDUAL monitor circuit will assert SUSACK#. The function configuration of this pin is determined by the power-on strapping option (JP1=0).
	VIN5	AI	AVCC3	***Voltage Analog Input 5*** The second function of this pin is 0 to 3.072V FSR Analog Input.

Table 5-13. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	**CLKIN**	DI	AVCC3	***24 or 48 MHz Clock Input***
72	**PWRON#**	DOD8	3VSB	***Power On Request Output #*** The first function of this pin is Power On Request Output #.
	GP44	DIOD8	3VSB	***General Purpose I/O44*** The second function of this pin is General Purpose I/O Port 4 Bit 4.
75	**PANSWH#**	DI	3VSB	***Main Power Switch Button Input #*** The first function of this pin is Main Power Switch Button Input #.
	GP43	DIOD8	3VSB	***General Purpose I/O 43*** The second function of this pin is General Purpose I/O Port 4 Bit 3.
76	**PSON#**	DOD8	3VSB	***Power Supply On-Off Output #*** The first function of this pin is Power Supply On-Off Control Output #.
	GP42	DIOD8	3VSB	***General Purpose I/O 42*** The second function of this pin is General Purpose I/O Port 4 Bit 2.
71	**SUSB#**	DI	3VSB	***SUSB # Input*** The function of this pin is SUSB# Input.
77	**SUSC#**	DI	3VSB	***SUSC# Input*** The first function of this pin is SUSC# Input.

Pin(s) No.	Symbol	Attribute	Power	Description
	GP53	DIOD8	3VSB	***General Purpose I/O 53*** The second function of this pin is General Purpose I/O Port 5 Bit 3.
78	**PWRGD3**	DOD8	3VSB	***Power Good Output 3 with 150ms Delay Time*** The function of this pin is Power Good Output 3. For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect **AND** SUSB# **AND** VIN2(+12V_SEN) **AND** VIN3(+5V_SEN) **AND** ATXPG). Please refer to section 11.13 PWRGD1, PWRGD2, PWRGD3 on page 193 for the detail.
79	**3VSBSW#**	DO8	3VSB	***3VSBSW#*** The first function of this pin is 3VSBSW#.
	GP40	DIOD8	3VSB	***General Purpose I/O 40*** The second function of this pin is General Purpose I/O Port 4 Bit 0.

IO Cell:
DO8: 8mA Digital Output buffer
DOD8: 8mA Digital Open-Drain Output buffer
DO16: 16mA Digital Output buffer
DO24: 24mA Digital Output buffer
DO24L: 24mA shink/8mA drive Digital Output buffer

DIO8: 8mA Digital Input/Output buffer
DIOD8: 8mA Digital Open-Drain Input/Output buffer
DIO16: 16mA Digital Input/Output buffer
DIOD16: 16mA Digital Open-Drain Input/Output buffer
DIO24: 24mA Digital Input/Output buffer
DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input
AI: Analog Input
AO: Analog Output

SST: Special design for SST interface
PECI: Special design for PECI interface
IO_SW: Special type of Input/Output; pins of this type connected in pairs through a switch

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6. List of GPIO Pins

Table 6-1. GPIO Alternate Function

Group	Bit	Pin Loc.	1st Func	Condition	2nd Func	Condition	3rd Func	Condition	4th Func	Condition	Output Driving (mA)	Note
GPIO 1x	0	84	PCIRST3# (DOD8)		GP10 (DIOD8)	25h<0>=1					8mA	
	1	34	PCIRST2# (DO8)		GP11 (DIOD8)	25h<1>=1					8mA	
	2	33	PCIRST1# (DO8)		GP12 (DIOD8)	25h<2>=1					8mA	
	3											
	4	31	PCH_C1 (DIOD8)	2Ah<2>=1	GP14 (DIOD8)	25h<4>=1					8mA	
	5	3	PCIRSTIN# (DI)	2Ch<2>=1	CIRTX2 (DO8)	CIR IER<7>=1	GP15 (DIOD8)	25h<5>=1			8mA	
	6	2	FAN_CTL5 (DOD8)	EC Index 0Bh<3:2>	CIRRX2 (DI)	CIR IER<6>=1	GP16 (DIOD8)	25h<6>=1			8mA	
	7	28	RI2# (DI)		GP17 (DIOD8)	25h<7>=1					8mA	
GP IO2x	0	27	CTS2# (DI)	26h<0>=0	GP20 (DIOD8)	26h< 0>=1					8mA	
	1	26	DCD2# (DI)	26h<1>=0	GP21 (DIOD8)	26h<1>=1					8mA	
	2	25	GP22 (DIOD8)	26h<2>=1							8mA	
	3	24	DPWROK (DOD8)	JP1=0	CPU_PG (DOD8)	JP4=0	GP23 (DIOD8)	26h<3>=1			8mA	
	4	23	FAN_TAC5 (DI)		RTS2# (DO8)	26h<4>=0	GP24 (DIOD8)	26h<4>=1			8mA	
	5	22	FAN_TAC4 (DI)		DSR2# (DI)	26h<5>=0	GP25 (DIOD8)	26h<5>=1			8mA	
	6	21	SOUT2# (DO8)	26h<6>=0	GP26 (DIOD8)	26h<6>=1					8mA	

Group	Bit	Pin Loc.	1st Func	Condition	2nd Func	Condition	3rd Func	Condition	4th Func	Condition	Output Driving (mA)	Note
	7	20	SIN2# (DI)	26h<7>=0	GP27 (DIOD8)	26h<7>=1					8mA	
GPIO 3x	0	19	ATXPG (DI)	27h<0>=0 2Ch<0>=1	GP30 (DIOD8)	27h<0>=1					8mA	
	1	1	CTS1# (DI)	27h<1>=0 LDN1 enable	GP31 (DIOD8)	27h<1>=1					8mA	
	2	128	RI1# (DI)	27h<2>=0 LDN1 enable	GP32 (DIOD8)	27h<2>=1					8mA	
	3	127	DCD# (DI)	27h<3>=0 LDN1 enable	GP33 (DIOD8)	27h<3>=1					8mA	
	4	14	RSTCONIN (DI)		GP34 (DIOD8)	27h<4>=1					8mA	
	5	13	RSTCONOUT (DOD8)		GP35 (DIOD8)	27h<5>=1					8mA	
	6	12	FAN_CTL3 (DOD8)		GP36 (DIOD8)	27h<6>=1					8mA	
	7	11	FAN_TAC3 (DI)		GP37 (DIOD8)	27h<7>=1					8mA	
GP IO4x	0	79	3VSBSW# (DO8)	2Ah<7>=1	GP40 (DIOD8)	28h<0>=1					8mA	
	1	125	SIN1 (DI)		GP41 (DIOD8)	28h<1>=1					8mA	
	2	76	PSON# (DOD8)		GP42 (DIOD8)	28h<2>=1					8mA	
	3	75	PANSWH# (DI)		GP43 (DIOD8)	28h<3>=1					8mA	
	4	72	PWRON# (DOD8)		GP44 (DIOD8)	28h<4>=1					8mA	
	5	123	DSR1# (DI)		GP45 (DIOD8)	28h<5>=1					8mA	
	6											
	7	70	GP47 (DIOD8)	28h<7>=1								

Group	Bit	Pin Loc.	1st Func	Condition	2nd Func	Condition	3rd Func	Condition	4th Func	Condition	Output Driving (mA)	Note
GPIO 5x	0	48	GP50 (DIOD8)	29h<0>=1							8mA	
	1	10	FAN_CTL2 (DOD8)		GP51 (DIOD8)	29h<1>=1					8mA	
	2	9	FAN_TAC2 (DI)		GP52 (DIOD8)	29h<2>=1					8mA	
	3	77	SUSC# (DI)		GP53 (DIOD8)	29h<3>=1					8mA	
	4	73	PME# (DOD8)		GP54 (DIOD8)	29h<4>=1					8mA	
	5	85	RSMRST# (DOD8)		CIRRX1 (DI)	29h<5>=0	GP55 (DIOD8)	29h<5>=1			8mA	
	6	83	MCLK (DIOD24)		GP56 (DIOD24)	29h<6>=1					24mA	No Internal Pull-up Simple I/O Only
	7	82	MDAT (DIOD24)		GP57 (DIOD24)	29h<6>=1					24mA	No Internal Pull-up Simple I/O Only
GP IO6x	0	81	KCLK (DIOD24)		GP60 (DIOD24)	29h<6>=1					24mA	No Internal Pull-up Simple I/O Only
	1	80	KDAT (DIOD24)		GP61 (DIOD24)	29h<6>=1					24mA	No Internal Pull-up Simple I/O Only
	2	45	KRST# (DO8)		GP62 (DIOD16)	29h<6>=1					16mA	Simple I/O Only
	3	6	SLP_SUS# (DI)	JP1=0	GP63 (DIOD8)						8mA	Simple I/O Only
	4	5	GP64 (DIOD8)	Default							8mA	Simple I/O Only
	5	120	VLDT_EN (DOD8)	JP4=0	PCH_C0 (DIOD8)	2Ah<2>=1	GP65 (DOD8)				8mA	Simple I/O Only
	6	119	GP66 (DIOD8)	Default							8mA	Simple I/O Only This GPIO pad is

Group	Bit	Pin Loc.	1st Func	Condition	2nd Func	Condition	3rd Func	Condition	4th Func	Condition	Output Driving (mA)	Note
	7	118	GP67 (DIOD8)	Default							8mA	powered by VBAT, register is powered by 3VSB
GPIO 7x	0	109	PD0 (DIO24)		GP70 (DIOD24)						8mA	Simple I/O Only
	1	110	PD1 (DIO24)		GP71 (DIOD24)						8mA	Simple I/O Only
	2	111	BUSSI0 (DI)		PD2 (DIO24)		GP72 (DIOD24)				8mA	Simple I/O Only
	3	112	BUSSI1 (DI)		PD3 (DIO24)		GP73 (DIOD24)				8mA	Simple I/O Only
	4	113	BUSSI2 (DI)		PD4 (DIO24)		GP74 (DIOD24)				8mA	Simple I/O Only
	5	114	BUSSO0 (DO)		PD5 (DIO24)		GP75 (DIOD24)				8mA	Simple I/O Only
	6	115	BUSSO1 (DO)		PD6 (DIO24)		GP76 (DIOD24)				8mA	Simple I/O Only
	7	116	BUSSO2 (DO)		PD7 (DIO24)		GP77 (DIOD24)				8mA	Simple I/O Only
GP IO8x	0	100	SLCT# (DI)		GP80 (DIOD24)						8mA	Simple I/O Only
	1	101	PE# (DI)		GP81 (DIOD8)						8mA	Simple I/O Only
	2	102	BUSY# (DI)		GP82 (DIOD8)						8mA	Simple I/O Only
	3	103	ACK# (DI)		GP83 (DIOD8)						8mA	Simple I/O Only
	4	104	SMBD_R (IO_SW)		SLIN# (DIO24)		GP84 (DIOD24)				24mA	Simple I/O Only
	5	105	SMBD_M (IO_SW)		INIT# (DIO24)		GP85 (DIOD24)				24mA	Simple I/O Only
	6	107	SMBC_R (IO_SW)		AFD# (DIO24)		GP86 (DIOD24)				24mA	Simple I/O Only

Group	Bit	Pin Loc.	1st Func	Condition	2nd Func	Condition	3rd Func	Condition	4th Func	Condition	Output Driving (mA)	Note
	7	108	SMBC_M (IO_SW)		STB# (DI)		GP87 (DIOD24)				24mA	Simple I/O Only

Table 6-2. GPIO Registers and Power Pads Table

(✓: Power by 3VSB - : Power by AVCC3; ×: Unsupported by this chip)

GP I/O Group 1	**GPIO10**	**GPIO11**	**GPIO12**	**GPIO13**	**GPIO14**	**GPIO15**	**GPIO16**	**GPIO17**
Pad power	✓	-	-	-	-	-	-	-
Global Register Index 25h<bit0-7>	✓	-	-	-	-	-	-	-
Pin polarity (Index B0h)	-	-	-	-	-	-	-	-
Internal pull-up enable (Index B8h)	✓	✓	✓	✓	✓	✓	✓	✓
Simple I/O Enable (Index C0h)	✓	-	-	-	-	-	-	-
Output/Input Selection (Index C8h)	✓	-	-	-	-	-	-	-
GP I/O Group 2	**GPIO20**	**GPIO21**	**GPIO22**	**GPIO23**	**GPIO24**	**GPIO25**	**GPIO26**	**GPIO27**
Pad power	✓	✓	✓	✓	✓	✓	✓	✓
Global Register Index 26<bit0-7>	✓	✓	✓	✓	✓	✓	✓	✓
Pin polarity (Index B1h)	✓	✓	✓	✓	✓	✓	✓	✓
Internal pull-up enable (Index B9h)	-	-	-	-	-	-	-	-
Simple I/O Enable (Index C1h)	✓	✓	✓	✓	✓	✓	✓	✓
Output/Input Selection (Index C9h)	✓	✓	✓	✓	✓	✓	✓	✓
GP I/O Group 3	**GPIO30**	**GPIO31**	**GPIO32**	**GPIO33**	**GPIO34**	**GPIO35**	**GPIO36**	**GPIO37**
Pad power	-	-	-	-	-	-	-	-
Global Register Index 27h<bit0-7>	-	-	-	-	-	-	-	-
Pin polarity (Index B2h)	-	-	-	-	-	-	-	-
Internal pull-up enable (Index BAh)	-	-	-	-	-	-	-	-
Simple I/O Enable (Index C2h)	-	-	-	-	-	-	-	-
Output/Input Selection (Index CAh)	-	-	-	-	-	-	-	-
GP I/O Group 4	**GPIO40**	**GPIO41**	**GPIO42**	**GPIO43**	**GPIO44**	**GPIO45**	**GPIO46**	**GPIO47**
Pad power	✓	✓	✓	✓	✓	✓	×	-
Global Register Index 28h<bit0-7>	✓	✓	✓	✓	✓	✓	×	-
Pin polarity (Index B3h)	-	-	-	-	-	-	×	-
Internal pull-up enable (Index BBh)	-	-	-	-	-	-	×	-
Simple I/O Enable (Index C3h)	✓	✓	✓	✓	✓	✓	×	-
Output/Input Selection (Index CBh)	✓	✓	✓	✓	✓	✓	×	-
GP I/O Group 5	**GPIO50**	**GPIO51**	**GPIO52**	**GPIO53**	**GPIO54**	**GPIO55**	**GPIO56**	**GPIO57**
Pad power	-	-	-	✓	✓	✓	-	-
Global Register Index 29h<bit0-7>	-	-	-	✓	✓	✓	-	-
Pin polarity (Index B4h)	-	-	-	-	-	-	-	-
Internal pull-up enable (Index BCh)	-	-	-	-	-	-	-	-
Simple I/O Enable (Index C4h)	-	-	-	✓	✓	✓	-	-
Output/Input Selection (Index CCh)	-	-	-	✓	✓	✓	-	-
Note:	GP56、GP57 Enabled by Index 29h<bit 6>=1							

GP I/O Group 6	GPIO60	GPIO61	GPIO62	GPIO63	GPIO64	GPIO65	GPIO66	GPIO67
Pad power	-	-	-	-	-	-	-	-
Global Register Index 29h<bit 7-6>	-	-	-	-	-	-	-	-
Internal pull-up enable (Index BDh)	-	-	-	-	-	-	-	-
Output/Input Selection (Index CDh)	-	-	-	✓	✓	✓	✓	✓
Note:	GP60~GP62 Enabled by Index 29h<bit 6>=1 GP63~GP67 Enabled by Index 29h<bit 7>=1							
GP I/O Group 7	**GPIO70**	**GPIO71**	**GPIO72**	**GPIO73**	**GPIO74**	**GPIO75**	**GPIO76**	**GPIO77**
Pad power	✓	✓	✓	✓	✓	✓	✓	✓
Output/Input Selection (Index CEh)	✓	✓	✓	✓	✓	✓	✓	✓
Note:	For GP70~GP77 Simple IO Enable: a. Parallel Port Disable: LDN3\Index30h=00h b. Bus Selection Disable: LDN7\IndexE9h<bit 5>=1							
GP I/O Group 8	**GPIO80**	**GPIO81**	**GPIO82**	**GPIO83**	**GPIO84**	**GPIO85**	**GPIO86**	**GPIO87**
Pad power	✓	✓	✓	✓	✓	✓	✓	✓
Output/Input Selection (Index CFh)	✓	✓	✓	✓	✓	✓	✓	✓
Note:	For GP80~GP87 Simple IO Enable: a. Parallel Port Disable: LDN3\Index30h=00h b. SMBus Isolation Disable: Global Index2Ch<bit 7>=1							

7. Power On Strapping Options and Special Pin Routings

Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP1 Pin 48	DSW_EUP_SEL	Internal 3VSB_OK	1	EUP
			0	DSW *Note1
JP2 Pin 122	WDT_EN	Internal VCC-OK/ LRESET#	1	Disable WDT to rest PWROK
			0	Enable WDT to rest PWROK
JP3 Pin 124	FAN_CTL_SEL	Internal VCC-OK	1	The default value of EC Index 63h/6Bh/73h is 80h.
			0	The default value of EC Index 63h/6Bh/73h is 00h.
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
JP5 Pin 29	UOVMODE_SEL	Internal VCC-OK	1	Notice Type *Note2
			0	Reserved

Note:

1. Pull-down with 8.2k ohm is recommanded.
2. This function must be pull-up to 3VSB.

Figure 7-1. IT8728F EUP Applications Circuitry for Intel ICH

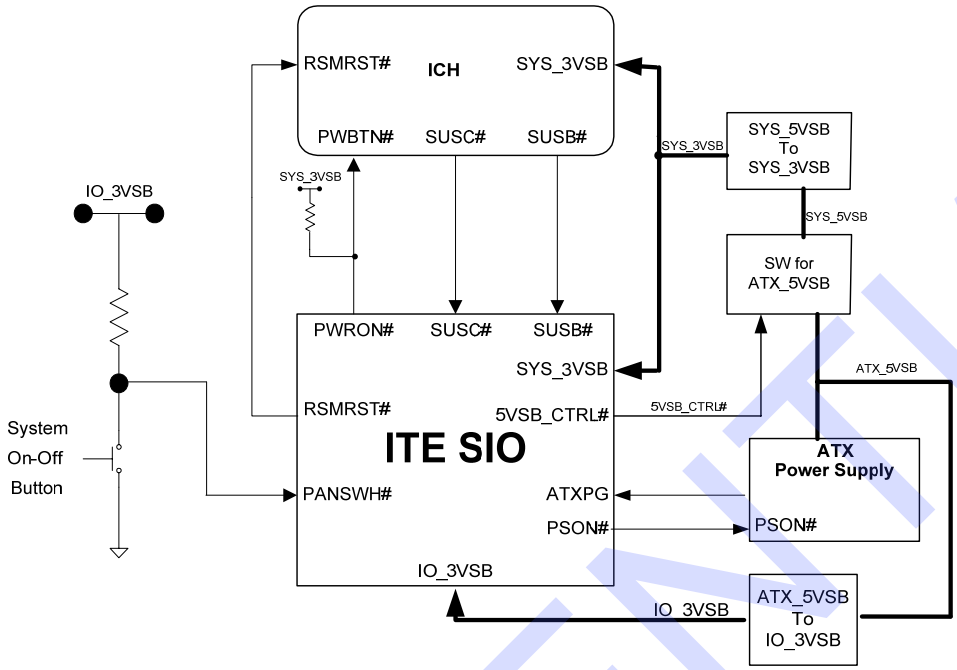
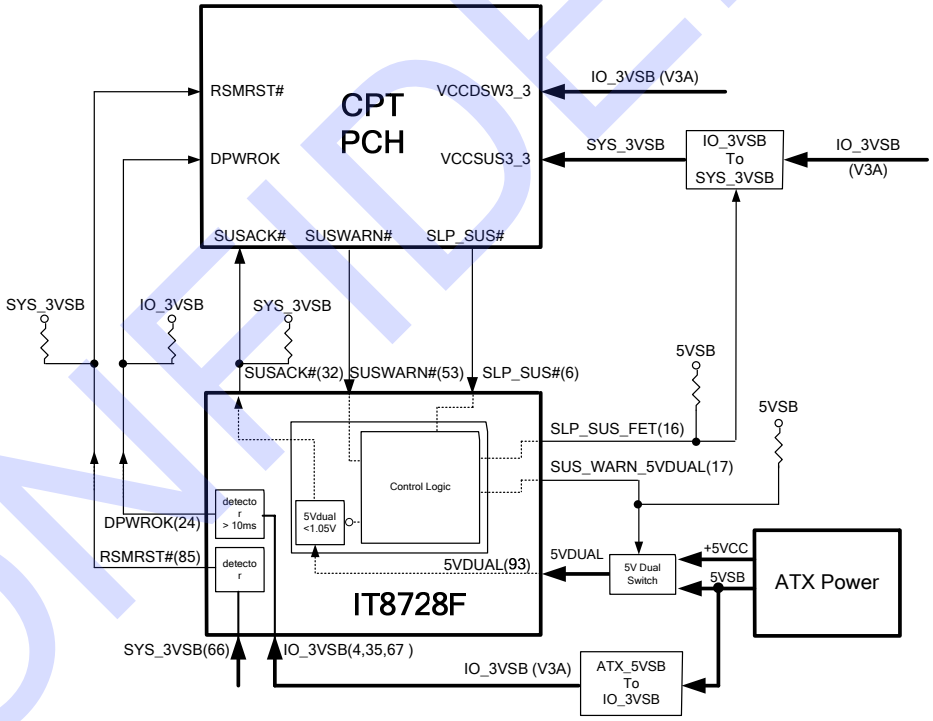


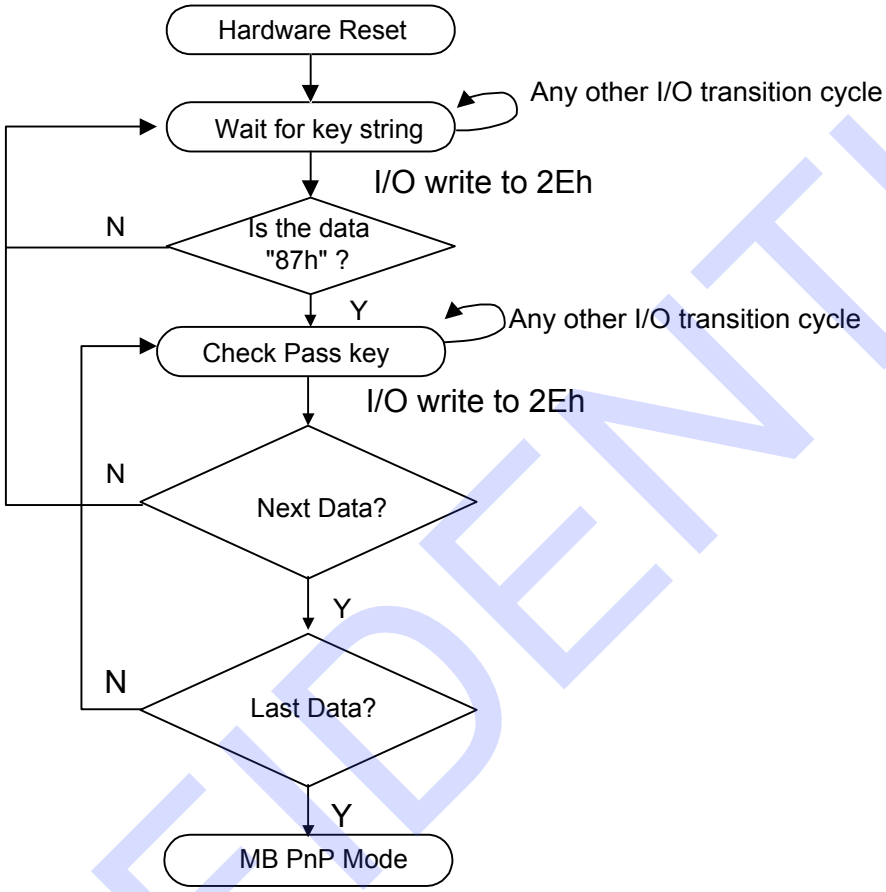
Figure 7-2. IT8728F DSW Applications Circuitry for Intel CPT/PCH



8. Configuration

8.1 Configuring Sequence

After a hardware reset or power-on reset, the IT8728F enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is ”1”.



There are three steps below to completing the configuration setup:

(1) Enter MB PnP Mode
(2) Modify data of configuration registers
(3) Exit MB PnP Mode

The undesired result may occur if the MB PnP Mode is not exited properly.

(1) Enter MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are required to be performed during the Wait for Key state and in order to ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

		Address Port	Data Port
	87h, 01h, 55h, 55h;	2Eh	2Fh
or	87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modify Data of Configuration Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to “1” to exit the MB PnP Mode.

8.2 Configuration Registers

All registers except APC/PME registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	28h	Chip ID Byte 2
All	22h	W-R	01h	Chip Version
All	23h	R/W	00h	Clock Selection Register
All	24h	R/W	00h	Special Register
07h Note1	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register Bit 0 powered by 3VSB.
07h Note1	26h	R/W	F3h	GPIO Set 2 Multi-Function Pin Selection Register Bit 7-0 powered by 3VSB.
07h Note1	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h Note1	28h	R/W	00h	GPIO Set 4 Multi-Function Pin Selection Register Bit 7-0 powered by 3VSB.
07h Note1	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register Bit 5-3 powered by 3VSB.
07h Note1	2Ah	R/W	00h	Special Function Selection Register 1 Bit 7-0 powered by 3VSB.
All	2Bh	R/W	0100s000b	Special Function Selection Register 2
07h Note1	2Ch	R/W	03h	Special Function Selection Register 3 Bit 7-0 powered by 3VSB.
07h	2Dh	R/W	00h	Special Function Selection Register 4
F4h Note1	2Eh	R/W	00h	Test 1 Register
F4h Note1	2Fh	R/W	00h	Test 2 Register

Note 1: These registers can be read from all LDNs.

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register 1
01h	F1h	R/W	50h	Serial Port 1 Special Configuration Register 2

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select Note2
03h	F0h	R/W	03h Note2	Parallel Port Special Configuration Register

Note 2: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

Table 8-6. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register
04h	F9h	R/W	-	Over Voltage/Under Voltage Protection (UVP/OVP)
04h	FAh	R/W	-	Special Configuration Register 1
04h	FBh	R/W	-	Special Configuration Register 2

Table 8-7. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	01h	KBC(Keyboard) Activate
05h	60h	R/W	00h	KBC(Keyboard) Data Base Address MSB Register
05h	61h	R/W	60h	KBC(Keyboard) Data Base Address LSB Register
05h	62h	R/W	00h	KBC(Keyboard) Command Base Address MSB Register
05h	63h	R/W	64h	KBC(Keyboard) Command Base Address LSB Register
05h	70h	R/W	01h	KBC(Keyboard) Interrupt Level Select
05h	71h	R-R/W	02h	KBC(Keyboard) Interrupt Type Note3
05h	F0h	R/W	48h	KBC(Keyboard) Special Configuration Register

Table 8-8. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC(Mouse) Activate
06h	70h	R/W	0Ch	KBC(Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC(Mouse) Interrupt Type Note3
06h	F0h	R/W	00h	KBC(Mouse) Special Configuration Register

Note 3: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

Table 8-9. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	64h	R/W	00h	Serial Flash I/F Base Address MSB Register
07h	65h	R/W	00h	Serial Flash I/F Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	20h	Watch Dog Timer Configuration Register
07h	73h	R/W	38h	Watch Dog Timer Time-out Value (LSB) Register
07h	74h	R/W	00h	Watch Dog Timer Time-out Value (MSB) Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B8h	R/W	20h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
07h	C0h	R/W	01h	Simple I/O Set 1 Enable Register Bit 0 powered by 3VSB.
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register Bit 7-0 powered by 3VSB.
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	40h	Simple I/O Set 4 Enable Register Bit 7-0 powered by 3VSB.
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register Bit 7-0 powered by 3VSB.
07h	C8h	R/W	01h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	40h	Simple I/O Set 4 Output Enable Register Bit 7-0 powered by 3VSB.
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register Bit 7-0 powered by 3VSB.

LDN	Index	R/W	Reset	Configuration Register or Action
07h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register Bit 7-0 powered by 3VSB.
07h	CEh	R/W	00h	Simple I/O Set 7 Output Enable Register Bit 7-0 powered by 3VSB.
07h	CFh	R/W	00h	Simple I/O Set 8 Output Enable Register Bit 7-0 powered by 3VSB.
07h	E0h	R/W	00h	Panel Button De-bounce 0 Input Pin Mapping Register
07h	E1h	R/W	00h	Panel Button De-bounce 1 Input Pin Mapping Register
07h	E2h	R/W	00h	IRQ External Routing 0 Input Pin Mapping Register
07h	E3h	R/W	00h	IRQ External Routing 1 Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ External Routing 1-0 Interrupt Level Selection Registers
07h	E9h	R/W	00000---b	Bus Select Control Register
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register Bit 7-0 powered by 3VSB.
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register Bit 7-0 powered by 3VSB.
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register Bit 7-0 powered by 3VSB.
07h	FAh	R/W	00h	GP LED Blinking 2 Pin Mapping Register Bit 7-0 powered by 3VSB.
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register Bit 7-0 powered by 3VSB.

Table 8-10. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ah	30h	R/W	00h	Consumer IR Activate
0Ah	60h	R/W	03h	Consumer IR Base Address MSB Register
0Ah	61h	R/W	10h	Consumer IR Base Address LSB Register
0Ah	70h	R/W	0Bh	Consumer IR Interrupt Level Select
0Ah	F0h	R/W	06h	Consumer IR Special Configuration Register

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-11. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM port
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST data port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 KBC	Base1 + Base2	KBC
LDN=A Consumer IR	Base + (0 -7)	

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and the software is not required to clear them.

Bit	Description
7-2	**Reserved**
1	Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is, **read/write,** which is to select the current logical devices. By reading data from or writing data to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This register is Chip ID Byte 1 and **read only**. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=28h)

This register is Chip ID Byte 2 and **read only**. Bits [7:0]=21h when read.

8.3.5 Chip Version (Index=22h, Default=01h)

Bit	Description
7-4	**Reserved**
3-0	**Version** 000b for AX~CX version 001b for DX, EX version The part no. is IT8728F/EX.

8.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**Clock Source Select of Watch Dog Timer** 0: Internal oscillating clock (Default) 1: External CLKIN
3	**Reserved**
2	**PWRGD3 Timing Selection** 0: 150ms 1: 300ms
1	**Reserved**
0	**CLKIN Frequency** 0: 48 MHz (Default) 1: 24 MHz

8.3.7 Special Register (Index=24h, Default=00h)

Bit	Description
7-0	**Reserved**

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 28** 0: RI2# (Default) 1: GP17
6	**Function Selection of Pin 2** 0: FAN_CTL5 if bits[3:2] of EC index 0Bh ≠ 11b CIRRX2 if bit6 of CIR IER = 1 1: GP16
5	**Function Selection of Pin 3** 0: PCIRSTIN# if bit2 of index 2C is 1 CIRTX2 if bit7 of CIR IER = 1 (Default) 1: GP15
4	**Function Selection of Pin 31** 0: PCH_C1, if bit2 of index 2A is 1 1: GP14
3	**Reserved**
2	**Function Selection of Pin 33** 0: PCIRST1# (Default) 1: GP12
1	**Function Selection of Pin 34** 0: PCIRST2# (Default) 1: GP11
0	**Function Selection of Pin 84** 0: PCIRST3# (Default) 1: GP10

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=F3h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 20** 0: SIN2 1: GP27 (Default)
6	**Function Selection of Pin 21** 0: SOUT2 1: GP26 (Default)
5	**Function Selection of Pin 22** 0: DSR2# 1: GP25 / FAN_TAC4 (Default)
4	**Function Selection of Pin 23**

Bit	Description
	0: RTS2# 1: GP24 / FAN_TAC5 (Default)
3	**Function Selection of Pin 24** 0: CPU_PG, if JP4=0 1: GP23 (Default)
2	**Function Selection of Pin 25** 0: Reserved 1: GP22 (Default)
1	**Function Selection of Pin 26** 0: DCD2# 1: GP21 (Default)
0	**Function Selection of Pin 27** 0: CTS2# 1: GP20 (Default)

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 11** 0: FAN_TAC3 (Default) 1: GP37
6	**Function Selection of Pin 12** 0: FAN_CTL3 (Default) 1: GP36
5	**Function Selection of Pin 13** 0: RSTCONOUT 1: GP35
4	**Function Selection of Pin 14** 0: RSTCONIN 1: GP34
3	**Function Selection of Pin 127** 0: DCD1# if COM1 enable 1: GP33
2	**Function Selection of Pin 128** 0: RI1# if COM1 enable 1: GP32
1	**Function Selection of Pin 1** 0: CTS1# if COM1 enable 1: GP31
0	**Function Selection of Pin 19** 0: ATXPG (Default) 1: GP30

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 70** 0: Reserved 1: GP47
6	**Reserved**
5	**Function Selection of Pin 123** 0: DSR1# (Default) 1: GP45
4	**Function Selection of Pin 72** 0: PWRON# (Default) 1: GP44
3	**Function Selection of Pin 75** 0: PANSWH# (Default) 1: GP43
2	**Function Selection of Pin 76** 0: PSON# (Default) 1: GP42
1	**Function Selection of Pin 125** 0: SIN1 (Default) 1: GP44
0	**Function Selection of Pin 79** 0: 3VSBSW# (Default) 1: GP40

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 120** 0: VLDT_EN (JP4=0) 1: GP65
6	**Function Selection of Pin 83, 82, 81, 80, 45** 0: MCLK, MDAT, KCLK, KDAT, KRST# (Default) 1: GP56, GP57, GP60, GP61, GP62
5	**Function Selection of Pin 85** 0: CIRRX1 or RSMRST# (Default) RSMRST# is an open-drain output function, which is active low about 60ms when 3VSB is powered on. 1: GP55
4	**Function Selection of Pin 73** 0: PME# (Default) 1: GP54
3	**Function Selection of Pin 77** 0: SUSC# (Default) 1: GP53
2	**Function Selection of Pin 9** 0: FAN_TAC2 (Default) 1: GP52
1	**Function Selection of Pin 10** 0: FAN_CTL2 (Default) 1: GP51
0	**Function Selection of Pin 48** 0: Reserved 1: GPO50

8.3.13 Special Function Selection Register 1 (Index=2Ah, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Enable 3VSBSW# (For System Suspend-to-RAM)** 0: 3VSBSW# is always inactive. (Default) 1: 3VSBSW# is enabled. It will be (NOT SUSB#) NAND SUSC#.
6	**Multi-Function Selection of Pin 53** 0: MTRB#. (Default) 1: External Thermal Sensor Data Specifically when External Thermal Sensor Host is enabled (bit 6-4 of EC Index 0Ah), the function of this pin is selected as SST or ETS_DAT.
5	**PWRGD1/2/3 Reset by RSTCONIN** 0: Disable (Default) 1: Enable
4	**Reserved**
3	**PCH SM-Link Data Pin Selection** 0: Pin 120 (Default) 1: Pin 53
2	**PCH SM-Link Clock Pin Selection** 0: Pin 121 (Default) 1: Pin 31
1	**Reserved**
0	**Delay Time Selection of 3VSBSW# Rising Edge to PWRGD3 Rising Edge**

8.3.14 Special Function Selection Register 2 (Index=2Bh, Default=0100s000b)

Bit	Description
7-3	**Reserved**
2-0	**PANSWH# Mask Time** 000: Default 001: 1 second 010: 2 seconds 011: 3 seconds 100: 4 seconds

8.3.15 Special Function Selection Register 3 (Index=2Ch, Default=03h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**SMBus Isolation on Parallel Port I/F** 0: Bypass(Default, AVCC3 ON) 1: Isolation (AVCC3 OFF) **Note:** Parallel Port Function must be disabled when SMBus Isolation is used.
6	**K8 PWRON_SEL if JP4=0** 0: Normal (Default) 1: Software disabled
5	**Reserved**
4	**PS2 Mouse Double Click Wake-up Mode Selection** 0: 3-Byte mode (Default) 1: 4-Byte mode
3	**SMBus Isolation on FDD I/F** 0: Bypass(Default, AVCC3 ON) 1: Isolation (AVCC3 OFF) **Note:** FDC must be disabled.
2	**Enable PCIRSTIN# of Pin 3** 0: Disable(Default) 1: Enable
1	**Reserved**
0	**VIN3 Function Selection** 0: External VIN3 voltage sensor 1: Internal Voltage Divider for ACC3. (Default)

8.3.16 Test 1 Register (Index=2Eh, Default=00h)

This register is reserved for ITE and should not be set.

8.3.17 Test 2 Register (Index=2Fh, Default=00h)

This register is reserved for ITE and should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC Enable** 1: Enable 0: Disable

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only**, with "0h" for Base Address [15:12].
3-0	Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**Read/write**; mapped as Base Address [7:3]
2-0	**Read only** as "000b"

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	**Reserved** with default "0h"
3-0	Please refer to Table 8-12 Interrupt Level Mapping Table.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	**Reserved** with default "00h."
2-0	**DMA Channel Select for FDC** Please refer to Table 8-13 DMA Channel Mapping Table on page 78.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-5	**Reserved** with default "00h"
4	**Internal Pull-up Control of FDD I/F Input Pin** 0: Disable 1: Enable
3	**IRQ Type** 1: IRQ sharing 0: Normal IRQ
2	1: Swap Floppy Drives A, B 0: Normal
1	1: 3-mode 0: AT-mode
0	1: Software Write Protect 0: Normal

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	**Reserved** with default “00h”
3-2	**FDD B Data Rate Table Select (DRT1-0)**
1-0	**FDD A Data Rate Table Select (DRT1-0)**

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 1 Enable** 1: Enable 0: Disable

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as “000b”

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	**Reserved** with default “0h”
3-0	**Interrupt Select Level for Serial Port 1** Please refer to Table 8-12 Interrupt Level Mapping Table.

8.5.5 Serial Port 1 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6-4	**Serial Port 1 Mode** 000: Standard (default) Else : Reserved Please refer to Note 8-1on page 78.
3	**Reserved** with default “0”
2-1	**Clock Source** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	**IRQ Type** 1: IRQ sharing 0: Normal

8.5.6 Serial Port 1 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7-0	**Reserved**

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 2 Enable** 1: Enable 0: Disable

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with "0h" for Base Address [15:12]
3-0	**Read/write**, mapped as Base Address [11:8]

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address [7:3]
2-0	**Read only** as "000b"

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	**Reserved** with default "0h"
3-0	**Interrupt Level Select for Serial Port 2** Please refer to Table 8-12 Interrupt Level Mapping Table.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6-4	**Serial Port 2 Mode** 000: Standard (default) Else: Reserved Please refer to Note 8-1on page 78.
3	**Reserved** with default "0"
2-1	**Clock Source** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	**IRQ Type** 1: IRQ sharing 0: Normal

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7-0	**Reserved**

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Parallel Port Enable** 1: Enable 0: Disable **Note:** Bus selection and SMBus isolation must be disabled when this function is enabled.

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2]
1-0	**Read only** as “00b”

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2]
1-0	**Read only** as “00b”

8.7.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	**Reserved** with default “0h”
3-0	**Interrupt Level Select for Parallel Port** Please refer to Table 8-12 Interrupt Level Mapping Table.

8.7.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	**Reserved** with default “00h”
2-0	**DMA Channel Select for Parallel Port** Please refer to Table 8-13 DMA Channel Mapping Table on page 78.

8.7.8 Parallel Port Special Configuration Register (Index=F0h, Default=0Bh)

Bit	Description
7-6	**Port-80 Output Selection** 00: Normal Port-80 (for 7-Seg decod data) 01: EC Index 29h Reading 10: EC Index 2Ah Reading 11: EC Index 2Bh Reading
5-4	**Reserved**
3	**Port-80 Function** 1: Disable 0: Enable
2	**IRQ Type** 1: IRQ sharing 0: Normal
1-0	**Parallel Port Modes** 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode These bits are independent. If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled except when bit 2 of Parallel Port Primary Base Address LSB Register is set to 1 in accordance with the EPP specification.

8.8 Environment Controller Configuration Registers (LDN=04h)

8.8.1 Environment Controller Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Environment Controller Enable** 1: Enable 0: Disable This is a read/write register.

8.8.2 Environment Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.8.3 Environment Controller Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as “000b”

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as “000b.”

8.8.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	**Reserved** with default “0h”
3-0	**Interrupt Level Select for Environment Controller** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.8.7 APC/PME Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	This bit is set to 1 when 3VSB is off and becomes ineffective if 0 is written to it. Write 1 to clear this bit.
6-5	**Reserved** with default “00b”
4	**PS/2 Mouse Event** 0: Disable 1: Enable
3	**Keyboard Event** 0: Disable 1: Enable
2-1	**Reserved**
0	**CIR Event** 0: Disable 1: Enable

8.8.8 APC/PME Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	This bit is set to 1 when AVCC3 is on at the previous AC power failure whereas 0 when AVCC3 is off.
6-5	**Reserved**
4	0: No PS/2 mouse event detected 1: PS/2 mouse event detected
3	0: No keyboard event detected 1: Keyboard event detected
2-1	**Reserved**
0	0: No CIR event detected 1: CIR event detected

8.8.9 APC/PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	**PER and PSR Normal Run Access Enable**
6	**PME# Output Control** 0: Enable 1: Disable
5	This bit is restored automatically to the previous AVCC3 state before the power failure occurs. **Note:** AC failure resume can be made by either IO or South Bridge. For the use of IO, the BIOS needs to be set as the following: LDN4 F4<5> and LDN4 F2<5> setting: 1 X :Always ON 0 1 :Memory 0 0 :Always OFF For the use of South Bridge, F4 bit 5 and F4 bit 6 need to be set to 1.
4	**Reserved**
3	**Keyboard event mode selection when AVCC3 is on** 1: Determined by PCR 2 0: Pulse falling edge on KCLK
2	**Mouse event when AVCC3 is off** 1: Click key twice sequentially 0: Pulse falling edge on MCLK

Bit	Description
1	**Mouse event when AVCC3 is on** 1: Click key twice sequentially 0: Pulse falling edge on MCLK
0	**CIRRX1 Pin Selection** 1: Pin 84 0: Pin 85

8.8.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-6	**Reserved**
5	**Reserved; must be 0b**
4-1	**Reserved**
0	**IRQ Type** 1: IRQ sharing 0: Normal

8.8.11 APC/PME Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	**Auto-swap of KCLK/KDAT and MCLK/MDAT** 0: Enable (Default) 1: Disable
6	**Gate Extra PWRON# Pulse at First 3VSB Power-on** 0: None gating (Default) 1: Gating **Note:** AC failure resume can be made by either IO or South Bridge. For the use of IO, the BIOS needs to be set as the following: LDN4 F4<5> and LDN4 F2<5> setting: 1 X :Always ON 0 1 :Memory 0 0 :Always OFF For the use of South Bridge, F4 bit 5 and F4 bit 6 need to be set to 1.
5	**PSON# state when 3VSB is switched from off to on** 0: High-Z (power OFF in default) 1: Inverting of SUSB#
4	**Reserved**
3-2	**Key Number of Keyboard Power-up Event** 00: 5 Key string mode, 3 keys simultaneous mode 01: 4 Key string mode, 2 keys simultaneous mode 10: 3 Key string mode, 1 key simultaneous mode 11: 2 Key string mode, Reserved (Not valid for simultaneous mode)
1-0	**Mode Selection of Keyboard Power-up Event** 00: KCLK falling edge 01: Key string mode 10: Simultaneous key stroke mode 11: Reserved

8.8.12 APC/PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	**Reserved (should be "00")**
5-0	**Indicate which Identification Key Code or CIR code register to be read/written via 0xF6** 00h~04h: Key code 20h~32h: CIR code 34h~37h: VBAT registers 38h~3Eh: VBAT registers

8.8.13 APC/PME Special Code Data Register (Index=F6h)

There are 5 bytes for the Key String mode, 3 bytes for Stroke Keys at the same time mode and CIR event codes.

8.8.14 Over Voltage/Under Voltage Protection (UVP/OVP) (Index=F9h)

Please refer to power-on strapping option (JP5) for the detail.

Bit	Description
7	**Notice Mode UVP/OVP Enable** 0: Disable 1: Enable
6-5	**Force Mode UVP Delay Time** 00: 0ms 01: 50ms 10: 100ms 11: 200ms
4-3	**Notice Mode PSON# Pull-up Time** 00: 0.5 second 01: 1 second 10: 2 seconds 11: 4 seconds
2	**Reserved**
1	**Force Mode Status (JP5=0)** 0: Disable 1: Enable
0	**Notice Mode Status (JP5=1)** 0: Disable 1: Enable

8.8.15 Special Configuration Register 1 (Index=FAh)

Bit	Description
7-5	**Reserved**
4	**EuP Wake-up Event** 0: Disable 1: Enable
3	**RI2# Wake-up Event** 0: Disable 1: Enable
2	**RI1# Wake-up Event** 0: Disable

	1: Enable
1	**5VSB_CTRL#** 0: Disable 1: Enable
0	**5VAUX_SW** 0: Disable 1: Enable

8.8.16 Special Configuration Register 2 (Index=FBh)

Bit	Description
7-4	**Reserved**
3	**RI2# Wake-up Event Status** 0: No RI2# event detected 1: RI2# event detected
2	**RI1# Wake-up Event Status** 0: No RI1# event detected 1: RI1# event detected
1-0	**Resume Timing from AC Fail Resume** 00: 2 seconds 01: 4 seconds 10: 8 seconds 11: 12 seconds

8.9 KBC(Keyboard) Configuration Registers (LDN=05h)

8.9.1 KBC(Keyboard) Activate (Index=30h, Default=01h)

Bit	Description
7-1	**Reserved**
0	**KBC(Keyboard) Enable** 1: Enable 0: Disable

8.9.2 KBC(Keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12]
3-0	**Read/write,** mapped as Base Address [11:8]

8.9.3 KBC(Keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0]

8.9.4 KBC(Keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.9.5 KBC(Keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0]

8.9.6 KBC(Keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	**Reserved** with default "0h"
3-0	**Interrupt Level Select for KBC(Keyboard)** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.9.7 KBC(Keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type set for KBC(Keyboard) and is **read only** as "02h" when bit 0 of the KBC(Keyboard) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.9.8 KBC(Keyboard) Special Configuration Register (Index=F0h, Default=08h)

Bit	Description
7-5	**Reserved** Must be "000b"
4	**IRQ Type** 1: IRQ sharing 0: Normal
3	**KBC Clock** 1: 8 MHz 0: 12 MHz
2	**KBC Lock** 1: Enable 0: Disable
1	**Interrupt Type Change Enable** 1: The interrupt type for KBC(Keyboard) can be changed. 0: The interrupt type for KBC(Keyboard) is fixed.
0	**Reserved**

8.10 KBC(Mouse) Configuration Registers (LDN=06h)

8.10.1 KBC(Mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**KBC(Mouse) Enable** 1: Enable 0: Disable

8.10.2 KBC(Mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	**Reserved** with default “0h”
3-0	**Interrupt Level Select for KBC(Mouse)** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.10.3 KBC(Mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type set for KBC(Mouse) and is **read only** as “02h” when bit 0 of the KBC(Mouse) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.10.4 KBC(Mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	**Reserved** with default “00h”
1	**IRQ Type** 1: IRQ sharing 0: Normal
0	**Interrupt Type Change Enable** 1: The interrupt type for KBC(Mouse) can be changed. 0: The interrupt type for KBC(Mouse) is fixed.

8.11 GPIO Configuration Registers (LDN=07h)

8.11.1 SMI# Normal Run Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12]
3-0	**Read/write**, mapped as Base Address [11:8]

8.11.2 SMI# Normal Run Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-2	**Read/write**, mapped as Base Address [7:2]
1-0	**Read only** as “00b”

8.11.3 Simple I/O Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12]
3-0	**Read/write**, mapped as Base Address [11:8]

8.11.4 Simple I/O Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0]

8.11.5 Serial Flash I/F Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address [15:12]
3-0	**Read/write**, mapped as Base Address [11:8]

8.11.6 Serial Flash I/F Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-3	**Read/write**, mapped as Base Address [7:3]
2-0	**Read only** as “000b”

8.11.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	**Reserved**
3-0	**Interrupt Level Select for Panel Button De-bounce** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.11.8 Watch Dog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	WDT is reset upon a CIR interrupt.
6	WDT is reset upon a KBC(Mouse) interrupt.
5	WDT is reset upon a KBC(Keyboard) interrupt.
4	**Reserved**
3-2	**Reserved**
1	**Force Time-out** This bit is self-cleared.
0	**WDT Status** 1: WDT value is equal to 0. 0: WDT value is not is equal to 0.

8.11.9 Watch Dog Timer Configuration Register (Index=72h, Default=001s0000b)

Bit	Description
7	**WDT Time-out Value Select 1** 1: Second 0: Minute
6	**WDT Output through KRST (pulse) Enable** 1: Enable 0: Disable
5	**WDT Time-out Value Extra Select** 1: 64ms x WDT Timer-out value (default = 4s) 0: Determined by WDT Time-out value select 1 (bit 7 of this register)
4	**WDT Output through PWRGD Enable** 1: Enable 0: Disable *During LRESET# this bit is selected by JP2 power-on strapping option.*
3-0	**Interrupt Level Select for WDT** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.11.10 Watch Dog Timer Time-out Value (LSB) Register (Index=73h, Default=38h)

Bit	Description
7-0	**WDT Time-out Value 7-0**

8.11.11 Watch Dog Timer Time-out Value (MSB) Register (Index=74h, Default=00h)

Bit	Description
7-0	**WDT Time-out Value 15-8**

8.11.12 GPIO Pin Set 1, 2, 3, 4, and 5 Polarity Registers (Index=B0h, B1h, B2h, B3h and B4h, Default=00h)

These registers are to program the GPIO pin type for polarity inverting or non-inverting.

Bit	Description
7-0	**GPIO Polarity Select** 1: Inverting 0: Non-inverting

8.11.13 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh, BDh, Default=20h, 00h, 00h, 00h, 00h, and 00h)

These registers are to enable the GPIO pin internal pull-up except for GP56, GP57, GP60, and GP61, which have no internal pull-up.

Bit	Description
7-0	**GPIO Pin Internal Pull-up** 1: Enable 0: Disable

8.11.14 Simple I/O Set 1, 2, 3, 4 and 5 Enable Registers (Index=C0h, C1h, C2h, C3h and C4h, Default=01h, 00h, 00h, 40h, and 00h)

These registers are to select the function as the Simple I/O function or the Alternate function.

Bit	Description
7-0	1: Simple I/O function 0: Alternate function

8.11.15 Simple I/O Set 1, 2, 3, 4, 5, 6, 7 and 8 Output Enable Registers (Index=C8h, C9h, CAh, CBh, CCh, CDh, CEh and CFh, Default=01h, 00h, 00h, 40h, 00h, 00h, 00h and 00h)

These registers are to determine the direction of the Simple I/O.

Bit	Description
7-0	0: Input mode 1: Output mode

8.11.16 Panel Button De-bounce 0 Input Pin Mapping Register (Index=E0h, Default=00h)

Bit	Description
7	**Reserved**
6	**IRQ Enable**
5-0	**Input Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.17 Panel Button De-bounce 1 Input Pin Mapping Register (Index=E1h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Input Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.18 IRQ External Routing 1-0 Input Pin Mapping Registers (Index=E3h-E2h, Default=00h)

Bit	Description
7	**Reserved**
6	**IRQ Enable**
5-0	**Input Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.19 IRQ External Routing 1-0 Interrupt Level Selection Registers (Index=E4h, Default=00h)

Bit	Description
7-4	**Interrupt Level Select for IRQ External Routing 1** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.
3-0	**Interrupt Level Select for IRQ External Routing 0** Please refer to Table 8-12 Interrupt Level Mapping Table on page 78.

8.11.20 Bus Select Control Register (Index=E9h, Default=00000---b)

Bit	Description
7-6	**Reset Selection** 00: RSMRST# 01: LRESET#f 10: PWRGD1/2/3 11: Reserved
5	**Bus Selection Disable** 0: Enable 1: Disable **Note:** Parallel Port function must be disabled when Bus Selection function is enabled.
4	**Bus Select Output Enable** 0: Transparent mode 1: Enable register output
3	**Bit[2:0] Reading Select** This bit will select the reading of bit [2:0]. 0: Bus select input [2:0] 1: Bus select output register value
2-0	**Bus Select Input/Output [2:0]** These three bits are bus select Input/output register. When reading, they will report the status of the bus select input if bit 3 = 0 or the values of the bus select output registers if bit 3 = 1. The values of bus select output registers will not be shown on the bus select output pins unless bit 4 = 1.

8.11.21 SMI# Control Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6	This bit is to enable the generation of an SMI# due to KBC(Mouse)'s IRQ (EN_MIRQ).
5	This bit is to enable the generation of an SMI# due to KBC(Keyboard)'s IRQ (EN_KIRQ).
4	This bit is to enable the generation of an SMI# due to Environment Controller's IRQ (EN_ECIRQ).
3	This bit is to enable the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	This bit is to enable the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	This bit is to enable the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	This bit is to enable the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

8.11.22 SMI# Control Register 2 (Index=F1h, Default=00h)

Bit	Description
7	**Reserved**
6	0: Edge trigger 1: Level trigger
5-3	**Reserved**
2	This bit is to enable the generation of an SMI# due to WDT's IRQ (EN_WDT).
1	This bit is to enable the generation of an SMI# due to CIR's IRQ (EN_CIR).
0	This bit is to enable the generation of an SMI# due to PBD's IRQ (EN_PBD).

8.11.23 SMI# Status Register 1 (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	**Reserved**
6	**KBC (PS/2 Mouse)'s IRQ**
5	**KBC(Keyboard)'s IRQ**
4	**Environment Controller's IRQ**
3	**Parallel Port's IRQ**
2	**Serial Port 2's IRQ**
1	**Serial Port 1's IRQ**
0	**FDC's IRQ**

8.11.24 SMI# Status Register 2 (Index=F3h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7-6	**Panel Button De-bounce Status 1-0** Writing 1 will reset the status. 0: None detected 1: Detected
5-4	**Reserved**
3	**Reserved**
2	**WDT's IRQ**
1	**CIR's IRQ**
0	**PBD's IRQ**

8.11.25 SMI# Pin Mapping Register (Index=F4h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**SMI# Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.26 Hardware Monitor Thermal Output Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Thermal Output Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.27 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Alert Beep Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.28 Keyboard Lock Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Keyboard Lock Pin Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.29 GP LED Blinking 1 Pin Mapping Register (Index=F8h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 1 Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.30 GP LED Blinking 1 Control Register (Index=F9h, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 1 Short Low Pulse Enable**
2-1	**GP LED 1 Frequency Control** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 1 Output Low Enable**

8.11.31 GP LED Blinking 2 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 2 Location** Please refer to Table 8-14 Location Mapping Table on page 79.

8.11.32 GP LED Blinking 2 Control Register (Index=FBh, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 2 Short Low Pulse Enable**
2-1	**GP LED 2 Frequency Control** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/2 Hz
0	**GP LED Blinking 2 Output Low Enable**

8.12 Consumer IR Configuration Registers (LDN=0Ah)

8.12.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Consumer IR Enable** 1: Enable 0: Disable

8.12.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.12.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as "000b"

8.12.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	**Reserved** with default "0h"
3-0	**Interrupt Level Select for Consumer IR** Please refer to Table 8-12 Interrupt Level Mapping Table.

8.12.5 Consumer IR Special Configuration Register (Index=F0h, Default=06h)

Bit	Description
7-1	**Reserved** with default "00h"
0	**IRQ Type** 1: IRQ sharing 0: Normal

Note 8-1
Except the standard mode, COM1 and COM2 cannot be selected in the same mode.

Table 8-12 Interrupt Level Mapping Table

Value	Description
Fh-Dh	Not Valid
Ch	IRQ12
3h	IRQ3
2h	Not Valid
1h	IRQ1
0h	No Interrupt Selected
Else	Not Valid

Table 8-13 DMA Channel Mapping Table

Value	Description
7h-5h	Invalid
4h	No DMA Channel Selected
3h	DMA3
2h	DMA2
1h	DMA1
0h	DMA0

Table 8-14 Location Mapping Table

Location	Description
001 000	GP10 (Pin 84). Powered by 3VSB.
001 001	GP11 (Pin 34).
001 010	GP12 (Pin 33).
001 011	Reserved
001 100	GP14 (Pin 31).
001 101	GP15 (Pin 3).
001 110	GP16 (Pin 2).
001 111	GP17 (Pin 28).
010 000	GP20 (Pin 27). Powered by 3VSB.
010 001	GP21 (Pin 26). Powered by 3VSB.
010 010	GP22 (Pin 25). Powered by 3VSB.
010 011	GP23 (Pin 24). Powered by 3VSB.
010 100	GP24 (Pin 23). Powered by 3VSB.
010 101	GP25 (Pin 22). Powered by 3VSB.
010 110	GP26 (Pin 21). Powered by 3VSB.
010 111	GP27 (Pin 20). Powered by 3VSB.
011 000	GP30 (Pin 19).
011 001	GP31 (Pin 1).
011 010	GP32 (Pin 128).
011 011	GP33 (Pin 127).
011 100	GP34 (Pin 14).
011 101	GP35 (Pin 13).
011 110	GP36 (Pin 12).
011 111	GP37 (Pin 11).
100 000	GP40 (Pin 79). Powered by 3VSB.
100 001	GP41 (Pin 125). Powered by 3VSB.
100 010	GP42 (Pin 76). Powered by 3VSB.
100 011	GP43 (Pin 75). Powered by 3VSB.
100 100	GP44 (Pin 72). Powered by 3VSB.
100 101	GP45 (Pin 124). Powered by 3VSB.
100 111	GP47 (Pin 70).
101 000	GP50 (Pin 48).
101 001	GP51 (Pin 10).
101 010	GP52 (Pin 9).
101 011	GP53 (Pin 77). Powered by 3VSB.
101 100	GP54 (Pin 73). Powered by 3VSB.
101 101	GP55 (Pin 85). Powered by 3VSB.
101 110	GP56 (Pin 83).
101 111	GP57 (Pin 82).
Else	Reserved

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9. Functional Description

9.1 LPC Interface

The IT8728F supports the peripheral side of the LPC I/F as described in the LPC Interface Specification Rev.1.1. In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (the same as PCICLK.)), the IT8728F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8728F supports the required transfer cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will react according to the DMA requests from the DMA devices in the Super I/O modules, and decide whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and respond with an SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. Nevertheless, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there are at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8728F follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface most PC chipsets. The IT8728F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turn-around state of the current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enters the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when the situation that one SIRQ Slave detects its input IRQn/events have been changed happens, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

Figure 9-1. Start Frame Timing

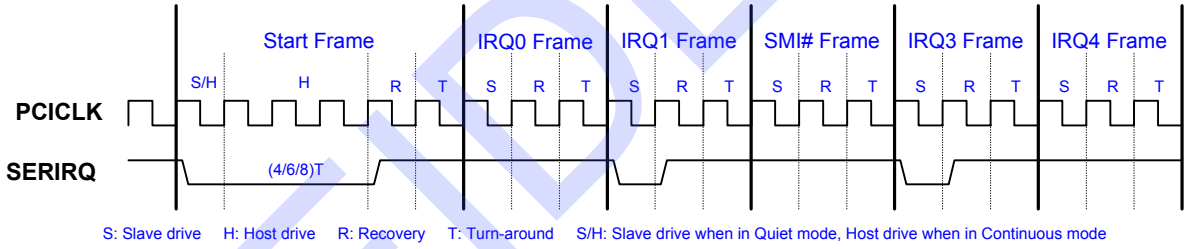
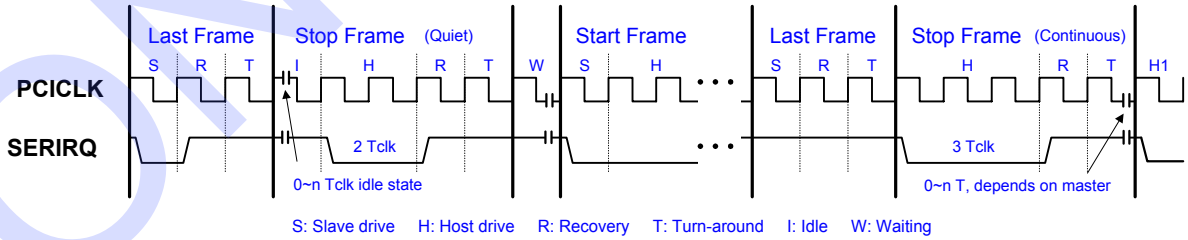


Figure 9-2. Stop Frame Timing



9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn/ Events	#of Clocks Past Start	IT8728F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8728F provides eight sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 25h, 26h, 27h, 28h and 29h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=07h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into eight registers. The accessed I/O ports are programmable and are five consecutive I/O ports (Base Address+0, Base Address+1, Base Address+2, Base Address+3, Base Address+4, Base Address+5, Base Address+6, Base Address+7). Base Address is programmed on the registers of GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=62h and 63h).

The Alternate function provides several special functions for users, including Watch Dog Timer, SMI# output routing, External Interrupt routing, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, Thermal output routing, and Beep output routing. The last two are sub-functions of the Hardware Monitor. (GPIO set 6, 7, 8 support the simple I/O function only.)

The Panel Button De-bounce is an input function. After it is enabled, a related status bit will be set when an active low pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. Panel Button De-bounce Interrupt will be issued if any of the status bit is set. However, the newly set status will not issue another interrupt unless the previous status bit is cleared before being set.

The Key Lock function locks the keyboard to inhibit the keyboard interface. The way of programming is to set bit 2 on the register Index F0h of KBC(Keyboard) (LDN=5). The pin location mapping, Index F7h also must be programmed correctly.

The Blinking function provides a low frequency blink output. By connecting to some external components, it can be used to control a power LED. There are several frequencies for selection.

The Watch Dog Timer (WDT) function is constituted by a time counter, a time-out status register, and the timer reset control logic. The time-out status bit may be mapped to an interrupt or KRST# through the WDT configuration register. The WDT has a programmable time-out ranging from 1 to 65535 minutes or 1 to 65535 seconds. The unit, either a minute or a second, is also programmable via bit 7 of the WDT configuration register. When the WDT Time-out Value register is set to a non-zero value, the WDT loads the value and begin counting down from the value. When the value reaches to 0, the WDT status register will be set. There are several system events including a CIR interrupt, a Keyboard Interrupt, a Mouse Interrupt that can reload the non-zero value into the WDT. The effect on the WDT for each of the events may be enabled or disabled through bits in the WDT control register. No matter what the value in the time counter is, the host may force a time-out to occur by writing a "1" to bit 1 of the WDT configuration register.

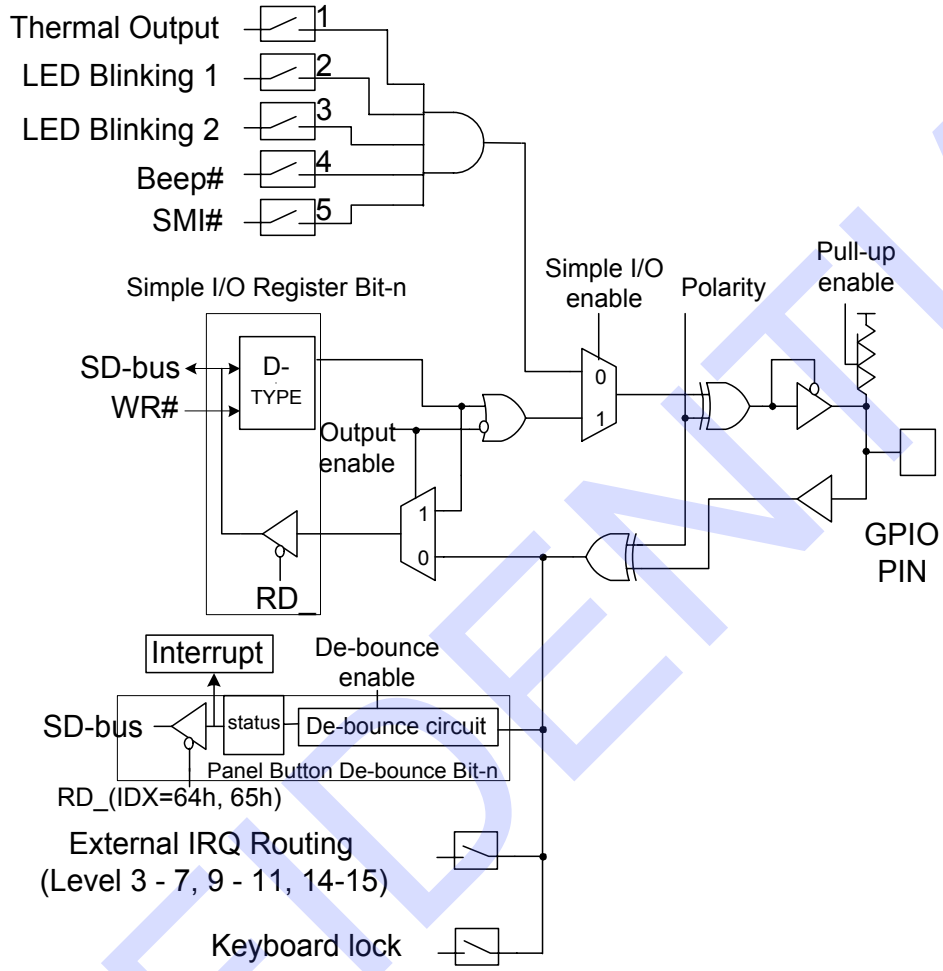
The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8728F. The interrupts are redirected as the SMI# output via the SMI# Control Register 1 and SMI# Control Register 2. The SMI# Status Register 1 and 2 are used to read the status of the SMI input event. All the SMI# Status Register bits can be cleared when the corresponding source events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# Control Register 2 no matter whether the events of the corresponding sources are invalidated or not. The SMI# events can be programmed as the pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_PBDIRQ or PBDIRQ) or (EN_KIRQ and KIRQ) or (EN_MIRQ and

MIRQ) or (EN_CIR and CIR_IRQ) or (EN_WDT and WDT_IRQ)

Figure 9-3. General Logic of GPIO Function



9.4 Advanced Power Supply Control and Power Management Event (PME#)

The circuit for advanced power supply control (APC) provides power-up events including Keyboard, Mouse, CIR and RI1#. When any of these events is activated, PWRON# will perform a low state until AVCC3 is switched to the ON state.
Here are the details of these events:

1. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously.
2. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means clicking on any mouse button twice sequentially.
3. Receiving CIR pattern matches the previous one stored at the APC/PME Special Code Index and Data Register.
4. Detection of RI1# falling edge.

The PANSWH# and PSON# are especially designed for the system. PANSWH# serves as a main power switch input, which is wire-AND to the APC output PWRON#. PSON# is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the SUSB# input until PANSWH# becomes active when the 3VSB is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, index F4h, bit 5). The gating circuit also provides an auto-restore function. After bit 5 of PCR1 is set, the previous PSON# state will be restored when the 3VSB is switched from OFF to ON.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all power-up events except switch-on event when the 3VSB state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the keyboard power-up event and APC conditions. Bit 4 is used to mask the PANSWH# power-on event on the PWRON# pin. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

A CIR event is generated if the input CIR RX pattern is the same as that previously stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length (in bytes). Bit 7-4 are used when AVCC3 is on and Bit 3-0 when AVCC3 goes OFF. The length represented in each 4-bit will be incremented by 3 internally as the actual length is to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always in the last several bytes. Thus, the system designer can program the IT8728F to generate a CIR PME# event as any keys when AVCC3 is ON and a special key (i.e. POWER-ON) when AVCC3 is OFF.

All APC registers (Index=F0h, F2h, F4h, F5h, F6h, FAh and FBh) are powered by back-up power (VBAT) when 3VSB is OFF.

PME# is used to wake up the system from low-power states (S1-S5).There will be five events of APC to generate PME#. A falling edge on these pins issues PME# events if the enable bits are set.

9.5 Environment Controller

The Environment Controller (EC), built in the IT8728F, includes seven voltage inputs, three temperature sensor inputs, five FAN Tachometer inputs, and five sets of advanced FAN Controllers. The EC monitors the hardware environment and implements the environmental control for personal computers.

The IT8728F contains an 8-bit ADC (Analog-to-Digital Converter), which is responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs ranging from 0V to 3.3V to 8-bit digital byte. With additional external components, the analog inputs can be made to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 3.3V. Through external thermistors or thermal diodes, the temperature sensor inputs can be converted into 8-bit digital byte, enabling the sensor inputs to monitor the temperature of various components. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

FAN Tachometer inputs are digital inputs with an acceptable range from 0V to 5V, and are responsible for measuring the FAN's Tachometer pulse periods.

The EC of the IT8728F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs. Both of the LPC Bus and Serial Bus interfaces are supported to accommodate the needs for various applications.

9.5.1 Interface

LPC Bus: The Environment Controller of the IT8728F decodes two addresses.

Table 9-1. Address Map on LPC Bus

Register or Port	Address
Address register of EC	Base+05h
Data register of EC	Base+06h

Note 1: The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index=60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

9.5.2 Registers

9.5.2.1 Address Port (Base+05h, Default=00h)

Bit	Description
7	**Outstanding; read only** This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	**Index** Internal Address of RAM and Registers.

Table 9-2. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration Register
01h	R	00h	Interrupt Status Register 1
02h	R	00h	Interrupt Status Register 2
03h	R	00h	Interrupt Status Register 3
04h	R/W	00h	SMI# Mask Register 1
05h	R/W	00h	SMI# Mask Register 2
06h	R/W	00h	SMI# Mask Register 3
07h	R/W	00h	Interrupt Mask Interrupt Mask 1
08h	R/W	00h	Interrupt Mask Interrupt Mask 2
09h	R/W	80h	Interrupt Mask Interrupt Mask 3
0Ah	R/W	58h	Interface Selection Register
0Bh	R/W	0Fh	Fan PWM Smoothing Step Frequency Selection Register
0Ch	R/W	00h	Fan Tachometer Control Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	07h	Fan Controller Main Control Register
14h	R/W	40h	FAN_CTL Control Register
15h	R/W	00h	FAN_CTL1 PWM Control Register
16h	R/W	00h	FAN_CTL2 PWM Control Register
17h	R/W	00h	FAN_CTL3 PWM Control Register
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
20h	R	-	VIN0 Voltage Reading Register
21h	R	-	VIN1 Voltage Reading Register
22h	R	-	VIN2 Voltage Reading Register
23h	R	-	VIN3 Voltage Reading Register
24h	R	-	VIN4 Voltage Reading Register
25h	R	-	VIN5 Voltage Reading Register
26h	R	-	VIN6 Voltage Reading Register
28h	R	-	VBAT Voltage Reading Register

Index	R/W	Default	Registers or Action
29h	R	-	TMPIN1 Temperature Reading Register
2Ah	R	-	TMPIN2 Temperature Reading Register
2Bh	R	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register
52h	R/W	7Fh	TMPIN1 Thermal Output Limit Register
53h	R/W	7Fh	TMPIN2 Thermal Output Limit Register
54h	R/W	7Fh	TMPIN3 Thermal Output Limit Register
55h	R/W	40h	ADC Temperature Extra Channel Enable Register
56h	R/W	00h	Thermal Diode 1 Zero Degree Adjust Register
57h	R/W	00h	Thermal Diode 2 Zero Degree Adjust Register
58h	R	90h	ITE Vendor ID Register
59h	R/W	00h	Thermal Diode 3 Zero Degree Adjust Register
5Bh	R	12h	Core ID Register
5Ch	R/W	60h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register

Index	R/W	Default	Registers or Action
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
62h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
63h	R/W	00h/80h	FAN_CTL1 SmartGuardian Automatic Mode Start PWM Register
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Control Register
65h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode △-Temperature Register
66h	R/W	0Fh	FAN_CTL1 Target Zone Register
68h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
6Ah	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
6Bh	R/W	00h/80h	FAN_CTL2 SmartGuardian Automatic Mode Start PWM Register
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Control Register
6Dh	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode △-Temperature Register
6Eh	R/W	0Fh	FAN_CTL2 Target Zone Register
70h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
72h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Full Speed Register
73h	R/W	00h/80h	FAN_CTL3 SmartGuardian Automatic Mode Start PWM Register
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Control Register
75h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode △-Temperature Register
76h	R/W	0Fh	FAN_CTL3 Target Zone Register
80h	R	-	Fan Tachometer 4 Reading LSB Register
81h	R	-	Fan Tachometer 4 Reading MSB Register
82h	R	-	Fan Tachometer 5 Reading LSB Register
83h	R	-	Fan Tachometer 5 Reading MSB Register
84h	R/W	-	Fan Tachometer 4 Limit LSB Register
85h	R/W	-	Fan Tachometer 4 Limit MSB Register
86h	R/W	-	Fan Tachometer 5 Limit LSB Register
87h	R/W	-	Fan Tachometer 5 Limit MSB Register
88h	R/W	-00h	External Temperature Sensor Host Status Register
89h	R/W	00h	External Temperature Sensor Host Target Address Register

Index	R/W	Default	Registers or Action
8Ah	R/W	00h	External Temperature Sensor Host Write Length Register
8Bh	R/W	00h	External Temperature Sensor Host Read Length Register
8Ch	R/W	00h	External Temperature Sensor Host Command (Write Data 1) Register
8Dh	R/W	00h	External Temperature Sensor Write Data (2-8) Register
8Eh	R/W	00h	External Temperature Sensor Host Control Register
8Fh	R	--h	External Temperature Sensor Read Data (1-16) Register
90h	R/W	FFh	Special FAN Control Mode Extra Vector A Temperature Limit of Fan Start Register
91h	R/W	00h	Special FAN Control Mode Extra Vector A Slope Register
92h	R/W	00h	Special FAN Control Mode Extra Vector A △-Temperature Register
94h	R/W	FFh	Special FAN Control Mode Extra Vector B Temperature Limit of Fan Start Register
95h	R/W	00h	Special FAN Control Mode Extra Vector B Slope Register
96h	R/W	00h	Special FAN Control Mode Extra Vector B △-Temperature Register
98h	R/W	00000b	PCH/AMDTSI Host Status Register
99h	R/W	00h	PCH/AMDTSI Host Target Address Register
9Ch	R/W	00h	PCH/AMDTSI Host Command Register
9Dh	R/W	--h	PCH/AMDTSI Write Data Register
9Eh	R/W	00h	PCH/AMDTSI Host Control Register
9Fh	R/W	--h	PCH/AMDTSI Read Data (1-16) Register

9.5.2.2 Register Description

9.5.2.2.1 Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	**Initialization** A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0”.
6	R/W	**Update VBAT Voltage Reading**
5	R/W	**COPEN# Cleared** Write “1” to clear COPEN#. **Note:** The COPEN# status register (Index 01h<bit4>) will be cleared when first writing this register and then reading Index 01h<bit4>.
4	R	**Read only; always “1”**
3	R/W	**INT_Clear** A “1” disables the SMI# and IRQ outputs while the contents of interrupt status bits remain unchanged.
2	R/W	**IRQ Enable** This bit is to enable the IRQ Interrupt output.
1	R/W	**SMI# Enable** A “1” enables the SMI# Interrupt output.
0	R/W	**Start** A “1” enables the startup of monitoring operations and a “0” sets the monitoring operation in the STANDBY mode.

9.5.2.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7	R	**Reserved**
6	R	A "1" indicates the FAN_TAC5 Count limit has been reached.
5	R	**Reserved**
4	R	**COPEN# Status** A "1" indicates a Case Open event has occurred. **Note:** The COPEN# status register (Index 01h<bit4>) will be cleared when first writing Index 00h<bit5> and then reading this register.
3-0	R	A "1" indicates the FAN_TAC4-1 Count limit has been reached.

9.5.2.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	A "1" indicates a High or Low limit of VIN7-0 has been reached.

9.5.2.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	**Reserved**
2-0	R	A "1" indicates a High or Low limit of Temperature 3-1 has been reached.

9.5.2.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6	R/W	A "1" disables the FAN_TAC5 interrupt status bit for SMI#.
5	R/W	**Reserved**
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for SMI#.
3-0	R/W	A "1" disables the FAN_TAC4-1 interrupt status bit for SMI#.

9.5.2.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for SMI#.

9.5.2.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for SMI#.

9.5.2.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6	R/W	A "1" disables the FAN_TAC5 interrupt status bit for IRQ.
5	R/W	**Reserved**
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for IRQ.
3-0	R/W	A "1" disables the FAN_TAC4-1 interrupt status bit for IRQ.

9.5.2.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for IRQ.

9.5.2.2.10 Interrupt Mask Register 3 (Index=09h, Default=80h)

Bit	R/W	Description
7	R/W	A "1" disables the External Thermal Sensor interrupt.
6-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for IRQ.

9.5.2.2.11 Interface Selection Register (Index=0Ah, Default=58h)

Bit	R/W	Description
7	R/W	**Pseudo-EOC (End of Conversion of ADC)** A Pseudo-EOC bit can speed up the setup time of FAN speed in the SmartGuardian automatic mode. (Write 1 to the bit then write 0.)
6	R/W	**External Thermal Sensor SMB Host Enable** 0: SMB Disable 1: SMB Enable
5-4	R/W	**SST/PECI Selection** 00: Disable 01: SST Slave Device 10: PECI 11: SST Host
3	R/W	**SST/PECI Host Controller Clock Selection** 0: 32MHz generated internally 1: 24MHz
2	R/W	**SST/PECI Host Controller (Auto Speed No-change Tolerance) t-bit 1 Setting** 0: (2 host clocks) no less than 1 host clock 1: (1 host clock) less than 1 host clock
1	R/W	**Reserved**
0	R/W	**PECI 2.0/3.0 Host Controller Hardware AWFCS Enable** 0: Disable 1: Enable

9.5.2.2.12 Fan PWM Smoothing Step Frequency Selection Register (Index=0Bh, Default=0Fh)

Bit	R/W	Description
7-6	R/W	**FAN PWM Smoothing Step Frequency Selection** 00: 1Hz 01: 16Hz 10: 8Hz 11: 4Hz
5-4	R/W	**Reserved** Must be “00b”
3-2	R/W	**FAN_CTL5 Selection** 00: The same as FAN_CTL1 01: The same as FAN_CTL2 10: The same as FAN_CTL3 11: None
1-0	R/W	**FAN_CTL4 Selection** 00: The same as FAN_CTL1 01: The same as FAN_CTL2 10: The same as FAN_CTL3 11: None

9.5.2.2.13 Fan Tachometer Control Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7	R/W	**TMPIN3 Enhanced Interrupt Mode Enable** 0: Original mode 1: The interrupt will be generated when TMPIN3 is higher than the high limit or lower than the low limit.
6	R/W	**TMPIN2 Enhanced Interrupt Mode Enable** 0: Original mode 1: The interrupt will be generated when TMPIN2 is higher than the high limit or lower than the low limit.
5	R/W	**FAN_TAC5 Enable** 0: Disable 1: Enable
4	R/W	**FAN_TAC4 Enable** 0: Disable 1: Enable
3	R/W	**TMPIN1 Enhanced Interrupt Mode Enable** 0: Original mode 1: The interrupt will be generated when TMPIN1 is higher than the high limit or lower than the low limit.
2-0	R/W	**Reserved**

9.5.2.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	**Count Number of Internal Clock per Revolution**

9.5.2.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.16 Fan Controller Main Control Register (Index=13h, Default=07h)

Bit	R/W	Description
7	R	**Reserved**
6-4	R/W	**FAN_TAC3-1 Enable** 0: Disable 1: Enable
3	R/W	**Full Speed Control of FAN_CTL Automatic Mode** 0: The full speeds of FAN_CTL1-3 automatic mode are independent. 1: All FAN_CTL1-3 will enter their respective full speeds when the temperature exceeds the full Speed Temperature Limit.
2-0	R/W	**FAN_CTL3-1 Output Mode Selection** 0: ON/OFF mode 1: SmartGuardian mode

9.5.2.2.17 FAN_CTL Control Register (Index=14h, Default=40h)

Bit	R/W	Description
7	R/W	**FAN_CTL Polarity (for all FANs)** 0: Active low 1: Active high
6-4	R/W	**PWM Base Clock Select (for FAN1, 3)** 000: 48MHz (PWM Frequency=187.5kHz) 001: 24MHz (PWM Frequency=93.75kHz) 010: 12MHz (PWM Frequency=46.87kHz) 011: 8MHz (PWM Frequency=31.25kHz) 100: 6MHz (PWM Frequency=23.43kHz) (Default) 101: 3MHz (PWM Frequency=11.7kHz) 110: 1.5MHz (PWM Frequency=5.86kHz) 111: 51kHz (PWM Frequency=200Hz)
3	R/W	**PWM Minimum Duty Select (for FAN1, 3)** 0: 0 % For a given PWM value, the actual duty is PWM/256 X 100%. 1: 20 % For a given PWM value (except 00h), the actual duty is (PWM+64)/320 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	**FAN_CTL ON/OFF Mode Control** These bits are only available when the relative output modes are selected in the ON/OFF mode. 0: OFF 1: ON

9.5.2.2.18 FAN_CTL 1-3 PWM Control Register (Index=15h,16h,17h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL1-3 PWM Mode Automatic/Software Operation Selection** 0: Software operation 1: Automatic operation
6-0	R/W	**When bit 7 =0:** **Bit 7-0 of Index 63h, 6Bh, 73h: 256 Steps of PWM Control When in Software Operation** **When bit 7 =1:** **Bit 2: Tachometer Closed-loop Mode Enable Bit** 0: Disable 1: Enable **Bit 1-0: Temperature Input Selection** 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved **Bit 6-3: Reserved**

9.5.2.2.19 Fan Tachometer 1-3 Extended Reading Registers (Index=18h-1Ah)

Bit	R/W	Description
7-0	R	**Count Number of Internal Clock per Revolution [15:8]**

9.5.2.2.20 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh-1Dh)

Bit	R/W	Description
7-0	R	**Limit Value [15:8]**

9.5.2.2.21 VIN6-0 Voltage Reading Registers (Index=26h-20h)

Bit	R/W	Description
7-0	R	**Voltage Reading Value** Note: For monitoring Internal AVCC3 If LDN7, Index 2Ch<bit 0>=1, AVCC3 voltage = VIN3 reading value * 2 * 12mV

9.5.2.2.22 3VSB Voltage Reading Registers (Index=27h)

Bit	R/W	Description
7-0	R	**Internal 3VSB Voltage Reading Value** The 3VSB voltage = reading value * 2 * 12mV

9.5.2.2.23 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R	**VBAT Voltage Reading Value** **Note:** 1. The VBAT voltage = reading value * 2 * 12mV

9.5.2.2.24 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R	**Temperature Reading Value**

9.5.2.2.25 VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.2.2.26 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value**

9.5.2.2.27 TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.2.2.28 TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value**

9.5.2.2.29 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	**ADC VIN7-0 Scan Enable**

9.5.2.2.30 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	**SST/PECI Host Temperature Reading Report Register Selection** 00: None 01: TMPIN1 Temperature Reading Register.(Index 29h) 10: TMPIN2 Temperature Reading Register.(Index 2Ah) 11: TMPIN3 Temperature Reading Register.(Index 2Bh)
5-3	R/W	TMPIN3-1 is enabled in the Thermal Resistor mode.
2-0	R/W	TMPIN3-1 is enabled in the Thermal Diode (or Diode-connected Transistor) mode.

9.5.2.2.31 TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Thermal Output Limit Value**

9.5.2.2.32 ADC Temperature Extra Channel Enable Register (Index=55h, Default=40h)

Bit	R/W	Description
7	R/W	**Reserved**
6-4	R/W	**FAN_CTRL2 PWM Base Clock Select** 000: 48MHz (PWM Frequency=187.5kHz) 001: 24MHz (PWM Frequency=93.75kHz) 010: 12MHz (PWM Frequency=46.87kHz) 011: 8MHz (PWM Frequency=31.25kHz) 100: 6MHz (PWM Frequency=23.43kHz) (Default) 101: 3MHz (PWM Frequency=11.7kHz) 110: 1.5MHz (PWM Frequency=5.86kHz) 111: 51kHz (PWM Frequency=200Hz)
3	R/W	**FAN_CTRL2 PWM Minimum Duty Select** 0: 0 % For a given PWM value, the actual duty is PWM/256 X 100%. 1: 20 % For a given PWM value (except 00h), the actual duty is (PWM+64)/320 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	VIN6-4 is enabled in the Thermal Resistor mode.

9.5.2.2.33 Thermal Diode Zero Degree Adjust 3-1 Registers (Index=59h, 57h, 56h, Default=00h)

These registers are **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode Zero Degree Voltage Value**

9.5.2.2.34 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID; read Only**

9.5.2.2.35 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID; read Only**

9.5.2.2.36 Beep Event Enable Register (Index=5Ch, Default=60h)

Bit	R/W	Description
7	R/W	**Thermal Diode Zero Degree Adjust Register Write Enable**
6-4	R/W	**ADC Clock Selection** 000: 500kHz 001: 250kHz 010: 125K 011: 62.5kHz 100: 31.25kHz 101: 24MHz 110: 1MHz(Default) 111: 2MHz
3	R/W	**Reserved**
2	R/W	This bit can enable the beep action when TMPINs exceed the limit
1	R/W	This bit can enable the beep action when VINs exceed the limit.
0	R/W	This bit can enable the beep action when FAN_TACs exceed the limit.

9.5.2.2.37 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Tone=500/(bits[7:4]+1)
3-0	R/W	**Frequency Divisor** Frequency=10K/(bits[3:0]+1)

9.5.2.2.38 Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Tone=500/(bits[7:4]+1).
3-0	R/W	**Frequency Divisor** Frequency=10K/(bits[3:0]+1)

9.5.2.2.39 Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Tone=500/(bits[7:4]+1)
3-0	R/W	**Frequency Divisor** Frequency=10K/(bits[3:0]+1)

9.5.2.2.40 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan OFF**

9.5.2.2.41 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Start**

9.5.2.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers (Index=72h, 6Ah, 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Full Speed**

9.5.2.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers (Index=73h, 6Bh, 63h, Default=00h/80h)

The default value of these registers is selected by JP3

For Original Fan Control Mode:

Bit	R/W	Description
7-0	R/W	**When bit 7 of index 15h, 16h, 17h =0:** 256 Steps of PWM Control When in Software Operation **When bit 7 of index 15h, 16h, 17h =1:** PWM Value

For Tachometer Closed-loop Mode:

Bit	R/W	Description
7-0	R/W	**Initial Value of Target RPM** RPM = 16 * Bit[7:0]

9.5.2.2.44 FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h)

For Original Fan Control Mode:

Bit	R/W	Description
7	R/W	**FAN Smoothing** This bit enables the FAN PWM smoothing change. 0: Disable 1: Enable
6-0	R/W	**Slope PWM Bit[6:0]** Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/℃

For Tachometer Closed-loop Mode:

Bit	R/W	Description
5-0	R/W	**Slope of Target RPM** Slope = 8 * Bit[5:0] (RPM/℃)

9.5.2.2.45 FAN_CTL3-1 SmartGuardian Automatic Mode △-Temperature Registers (Index=75h, 6Dh, 65h, Default=00h)

Bit	R/W	Description
7	R/W	**Direct-Down Control** This bit is to determine the PWM linear changing decreasing mode. 0: Slow decreasing mode 1: Direct decreasing mode
6	R/W	**FAN Full Limit Control as Thermal out Reached** When the relevant enable bit is set and the FAN output mode is selected as Automatic mode by bit7 of EC index 15h, 16h, 17h, the corresponding FAN output will be forced to full PWM if any thermal output limit is reached. 0: Disable 1: Enable
5	-	**Reserved**
4-0	R/W	**△-Temperature Interval [4:0]**

9.5.2.2.46 FAN_CTL3-1 Target Zone Registers (Index=76h, 6Eh, 66h, Default=0Fh)

For Tachometer Closed-loop Mode:

Bit	R/W	Description
3-0	R/W	**Target Zone Boundary** Target Zone = Target RPM +/- (8 * bit[3:0]) (RPM/℃)

9.5.2.2.47 Fan Tachometer 4-5 Reading LSB Registers (Index=80h,82h)

Bit	R/W	Description
7-0	R	**Count Number of Internal Clock per Revolution**

9.5.2.2.48 Fan Tachometer 4-5 Reading MSB Registers (Index=81h,83h)

Bit	R/W	Description
7-0	R	**Count Number of Internal Clock per Revolution**

9.5.2.2.49 Fan Tachometer 4-5 Limit LSB Registers (Index=84h,86h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.50 Fan Tachometer 4-5 Limit MSB Registers (Index=85h,87h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.2.2.51 External Temperature Sensor Host Status Register (Index=88h, Default= -00h)

Bit	R/W	Description
7	R/W	**Data FIFO Pointer Clear** Writing 1 clears the Read/Write Data FIFO pointers. 0: No action It always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers cleared Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
6	R/WC	**SST Bus Abnormal/Contention Error** This bit reports the SST/PECI line status. 0: No error 1: Abnormal/Contention error
5	R/WC	**SST Slave Message Phase t-bit Extend over Error/SST or PECI Received Error Code** This bit reports the SST/PECI line status and received error code (8000h-81FFh). 0: No error 1: Error found
4	R/WC	**SST/PECI Line High-Z Status/Failed** This bit reports the SST/PECI line High-Z status. 0: SST/PECI line does not drive High-Z. 1: SST/PECI line drives High-Z.
3	R/WC	**Write_FCS_ERR** Writing 1 clears this bit. In the SST/PECI mode, it reports Write FCS error. 0: No Error 1: Write FCS error
2	R/WC	**NotValid/Read_FCS_ERR** Writing 1 clears this bit. In the SST/PECI mode, it reports Read FCS error. 0: No Error 1: Read FCS error
1	R/WC	**Finish (FNSH)** Writing 1 clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	**Host Busy (BUSY)** 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.5.2.2.52 External Temperature Sensor Host Target Address Register (Index=89h, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Target Address Register (HAddr [7:0])** This register is the Target Address field of the SST/PECI protocol.

9.5.2.2.53 External Temperature Sensor Host Write Length Register (Index=8Ah, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Write Length Register (HW_length [7:0])** This register is the Write Length field of the SST/PECI protocol.

9.5.2.2.54 External Temperature Sensor Host Read Length Register (Index=8Bh, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Read Length Register (HR_length [7:0])** This register is the Read Length field of the SST/PECI protocol.

9.5.2.2.55 External Temperature Sensor Host Command (Write Data 1) Register (Index=8Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Command Register (HCMD [7:0])** This register is the command field of the protocol. In the PECI/SST mode, it is the command (Write Data 1) byte.

9.5.2.2.56 External Temperature Sensor Write Data (2-8) Register (Index=8Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	**Write Data (2-8) [7:0] (in SST/PECI mode)** This is a 16-byte FIFO register, which is only valid in the PECI/SST mode.

9.5.2.2.57 External Temperature Sensor Host Control Register (Index=8Eh, Default=00h)

Bit	R/W	Description
7-6	R/W	**Auto-Start Control (Auto-START)** The host will start the transaction in a regular rate automatically. 00: 32 Hz 01: 16 Hz 10: 8 Hz 11: 4 Hz
5	R/W	**Auto-Start (Auto-START)** 0: Disable 1: Enable The host will start the transaction in a regular rate, which is determined by bit [6:5] automatically.
4	R/W	**SST/PECI Host Auto-abort at FCS Error** This bit enables the SST/PECI host to abort the transaction when an error occurs to FCS. 0: Disable 1: Enable
3	R/W	**Auto-Start Two-Domain Enable** 0: One-Domain 1: Two-Domain
2	R/W	**SST**/PECI **Contention Control** This bit enables the SST/PECI bus contention control. 0: Disable 1: Enable When the SST/PECI bus is contentious, the host will abort the transaction.
1	R/W	**SST/PECI_idle_High** This bit sets the SST/PECI bus idle-high in the SST/PECI host mode. 0: SST/PECI idle low 1: SST/PECI idle high
0	R/W	**Start (START)** This bit is **write-only**. Writing 0 to it during transaction will issue a “kill process” and bit 4 of 88h register will be set. Writing 1 to it during the “NOT BUSY” state (bit 0 of 88h = 0) will start a transaction. Writing 1 to it during the “BUSY” state (bit 0 of 88h = 1) will

Bit	R/W	Description
		not issue any transaction. So, the programmer should check the “BUSY” status before issuing a transaction. 0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.

9.5.2.2.58 External Temperature Sensor Read Data (1-16) Register (Index=8Fh, Default=--h)

Bit	R/W	Description
7-0	R/W	**Read Data (1-16) [7:0]** This is a 32-byte FIFO register.

9.5.2.2.59 Special FAN Control Mode Extra Vector A, B Temperature Limit of Fan Start Registers (Index=90h, 94h, Default=FFh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Start**

9.5.2.2.60 Special FAN Control Mode Extra Vector A, B Slope Registers (Index=91h, 95h, Default=00h)

For Original Fan Control Mode:

Bit	R/W	Description
7	R/W	**Temperature Input Select 0** Please refer to the description of Special FAN Control Mode Extra Vector A, B △-Temperature Registers for the detail.
6-0	R/W	**Slope PWM Bit[6:0]** Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/℃

For Tachometer Closed-Loop Mode:

Bit	R/W	Description
7	R/W	**Temperature Input Select 0** Please refer to the description of Special FAN Control Mode Extra Vector A, B △-Temperature Registers for the detail.
6-0	R/W	**Slope of Extra A and B RPM** Slope = 8 * Bit[6:0] (RPM/℃)

9.5.2.2.61 Special FAN Control Mode Extra Vector A, B △-Temperature Registers (Index=92h, 96h, Default=00h)

Bit	R/W	Description
7	R/W	**Temperature Input Select 1** For **Temperature Input Select 0**, please refer to bit 7 of Special FAN Control Mode Extra Vector A, B Slope Registers. 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved
6-5	R/W	**Target FAN Select** These bits are to determine the target FAN to be added for extra vector. 00: None 01: FAN1 10: FAN2 11: FAN3
4-0	R/W	**△-Temperature Interval [4:0]**

9.5.2.2.62 PCH/AMDTSI Host Status Register (Index=98h, Default=---00000b)

Bit	R/W	Description
7	R/W	**Data FIFO Pointer Clear** Writing 1 clears Read/Write Data FIFO pointers. 0: No action It always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers cleared Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
6	R/W	**Bus Selection** This bit selects the SMB host protocol. 0: PCH SM-Link 1: AMDTSI
5	R/WC	**Reserved**
4	R/WC	**Transmission Killed**
3	R/WC	**Bus Error** 0: No Error 1: Error
2	R/WC	**Data Valid** Writing 1 clears this bit. In the AMDTSI mode, it reports the valid bit of Data phase. If this bit is set to 0(valid data =0), the data is valid. 0: Data valid 1: Data invalid
1	R/WC	**Finish (FNSH)** Writing 1 clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	**HOST Busy (BUSY)** 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.5.2.2.63 PCH/AMDTSI Host Target Address Register (Index=99h, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Target Address Register (HAddr [7:0])** This register is the Target Address field of the PCH/AMDTSI protocol.

9.5.2.2.64 PCH/AMDTSI Host Command Register (Index=9Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Command Register (HCMD [7:0])** This register is the command field of the protocol. In the AMDTSI mode, it is the Command field. If the host controller is busy, the value of this register cannot be changed or the host will send the wrong command. If the value is out of definition (for example, 03h to FFh for AMDTSI protocol), the host will transfer it to the normal value and no error will be detected by the host controller.

9.5.2.2.65 PCH/AMDTSI Write Data Register (Index=9Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	**Write Data** This is a 16-byte FIFO register.

9.5.2.2.66 PCH/AMDTSI Host Control Register (Index=9Eh, Default=00h)

Bit	R/W	Description
7-6	R/W	**Auto-Start Control (Auto-START)** The host will start the transaction in a regular rate automatically. 00: Disable auto-start 01: 16 Hz 10: 8 Hz 11: 4 Hz
5-4	R/W	**For AMDTSI Temperature Reading Report Register Selection** 00: None 01: Index 29h (TMPIN1) 10: Index 2Ah (TMPIN2) 11: Index 2Bh (TMPIN3) **For SM-Link Max. Temperature of CPU or MCH Reading Report Register Selection** 01: Index 29h 11: Index 2Bh **For SM-Link PCH Temperature Reading Report Register Selection** 00: Index 2Ah, if 9Eh<1>=1. **For MxM Temperature Reading Report Register Selection** 10: Index 2Ah, if 9Eh<1>=1.
3	R/W	**Reserved**
2	R/W	**AMDTSI Clock Selection** 0: 100 kbits/s 1: 400 kbits/s

Bit	R/W	Description
1	R/W	**PCH/MxM Temp Reported to 2Ah** 0: Disable 1: Enable Please refer to 9Eh<bit 5-4> for the detail. **AMDTSI_byte_sel** This bit selects 8/16 bit data in the AMDTSI mode. 0: AMDTSI 8-bit data 1: AMDTSI 16-bit data
0	R/W	**Start (START)** This bit is **write-only**. Writing 0 to it during transaction will issue a "kill process" and bit 4 of 98h register will be set. Writing 1 to it during the "NOT BUSY" state (bit 0 of 98h = 0) will start a transaction. Writing 1 to it during the "BUSY" state (bit 0 of 98h = 1) will not issue any transaction. So, the programmer should check whether the status is "BUSY" before issuing a transaction. 0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.

9.5.2.2.67 PCH/AMDTSI Read Data (1-16) Register (Index=9Fh, Default=--h)

Bit	R/W	Description
7-0	R/W	**Read Data (1-16) [7:0]** This is a 21-byte FIFO register.

9.5.3 Operation

9.5.3.1 Power on Reset and Software Reset

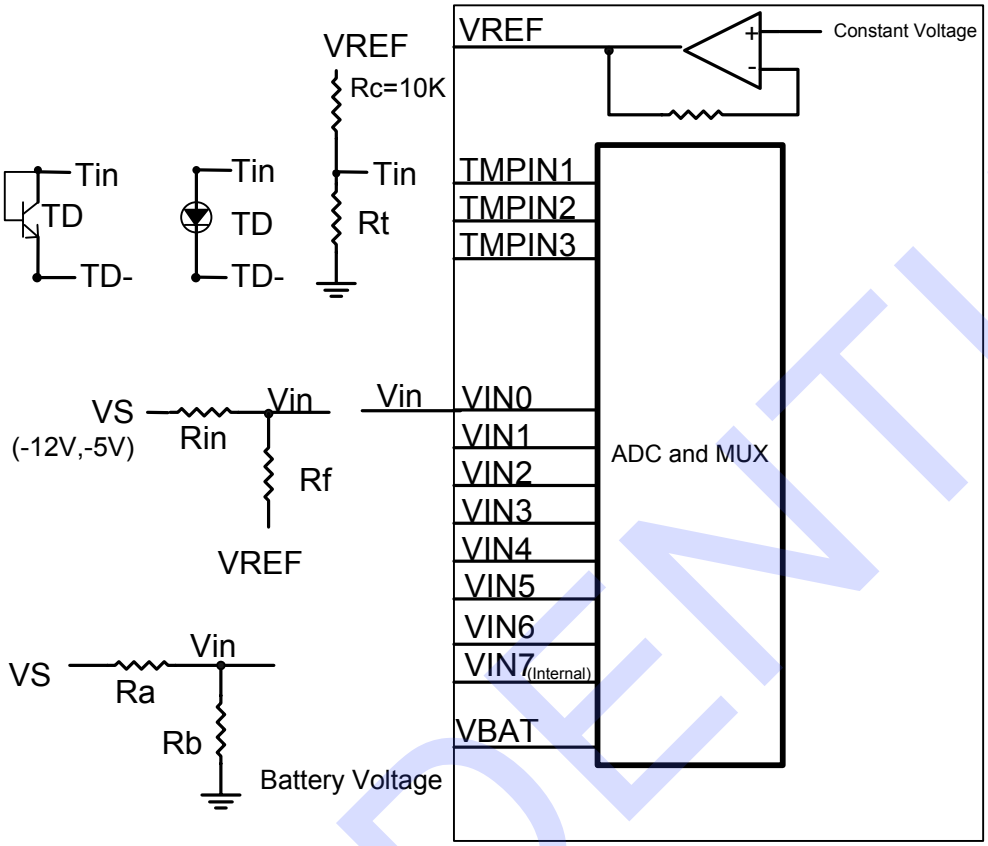
When the system power is first applied, the Environment Controller performs "power on reset" on the registers, making them return to their individual default values during a system hardware reset, and the EC will acquire a monitored value before it goes inactive. The ADC is activated to monitor the VBAT pin and then goes inactive. A software reset through bit 7 of Configuration Register (Index=00h, Default=18h) (refer to page 91) performs the same functions as the hardware reset except the function of the Serial Bus Interface Address register.

9.5.3.2 Starting Conversion

The monitoring function in the EC is activated when bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, this function will be enabled by setting several enabled bits, which are categorized into three groups, positive voltages, temperatures and FAN Tachometer inputs. Before the EC monitoring function is able to be executed then the monitoring process can then be started.

1. Set the limits.
2. Set the interrupt masks.
3. Set the enable bits.

Figure 9-4. Application Example



Note: The resistor should provide approximately 2V at the Analog Inputs.

9.5.3.3 Voltage and Temperature Inputs

The 8-bit ADC has a 12mV LSB with an input range from 0V to 3.072V. The 2.5V supplies of PC applications can be directly connected to the inputs. When the input voltage is greated than 3.072V, it is necessary to divide the input voltage into an acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider, which is connected to VREF (constant voltage, 2.8V), and do not attempt to measure it with the divider connected to the ground. The EC temperature measurement system converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage, an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated below:

Positive Voltage: Vs = Vin X (Ra+Rb) / Rb
Negative Voltage: Vs = (1+Rin/Rf) X Vin – (Rin/Rf) X VREF

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground; nevertheless, the current limiting input resistor is recommended since no dividing circuit is available.

9.5.3.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is essential to achieve accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as closely as possible to the IT8728F. However, the thermistors of the temperature loops should be positioned within the measuring area. In addition, the power supply bypass and the parallel combination of 10μF and 0.1μF bypass capacitors connected between AVCC3 and analog ground also needs to be located as closely as possible to the IT8728F.

Due to the small differential voltage of thermal diode (diode-connected transistor), it is necessary to adhere to the steps below for PCB layout.

- Position the sensor as closely as possible to the EC.
- The sensor ground should be directly shorted to GNDA with excellent noise immunity.
- Keep traces away from any noise sources. (High voltage, fast data bus, fast clock , CRTs …)
- Use trace width of10 mil minimum and provide guard ground (flanking and under).
- Position 0.1μF bypass capacitors as closely as possible to IT8728F.

9.5.3.5 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or 16-bit counter (maximum count=255 or 65535) for one period of the input signals. Counts are based on two pulses per revolution for tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor) ; (Default Divisor = 2)

The maximum input signal range is from 0 to VCC. An additional external circuit is needed to clamp the input voltage and current.

9.5.3.6 Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled by Configuration Register (Index=00h, Default=18h) (refer to page 91). The Interrupt Status Registers will be reset after a read operation. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. It takes EC 1.5 seconds to allow all the EC Registers to be safely updated between completed read operations. When bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume after this bit is cleared.

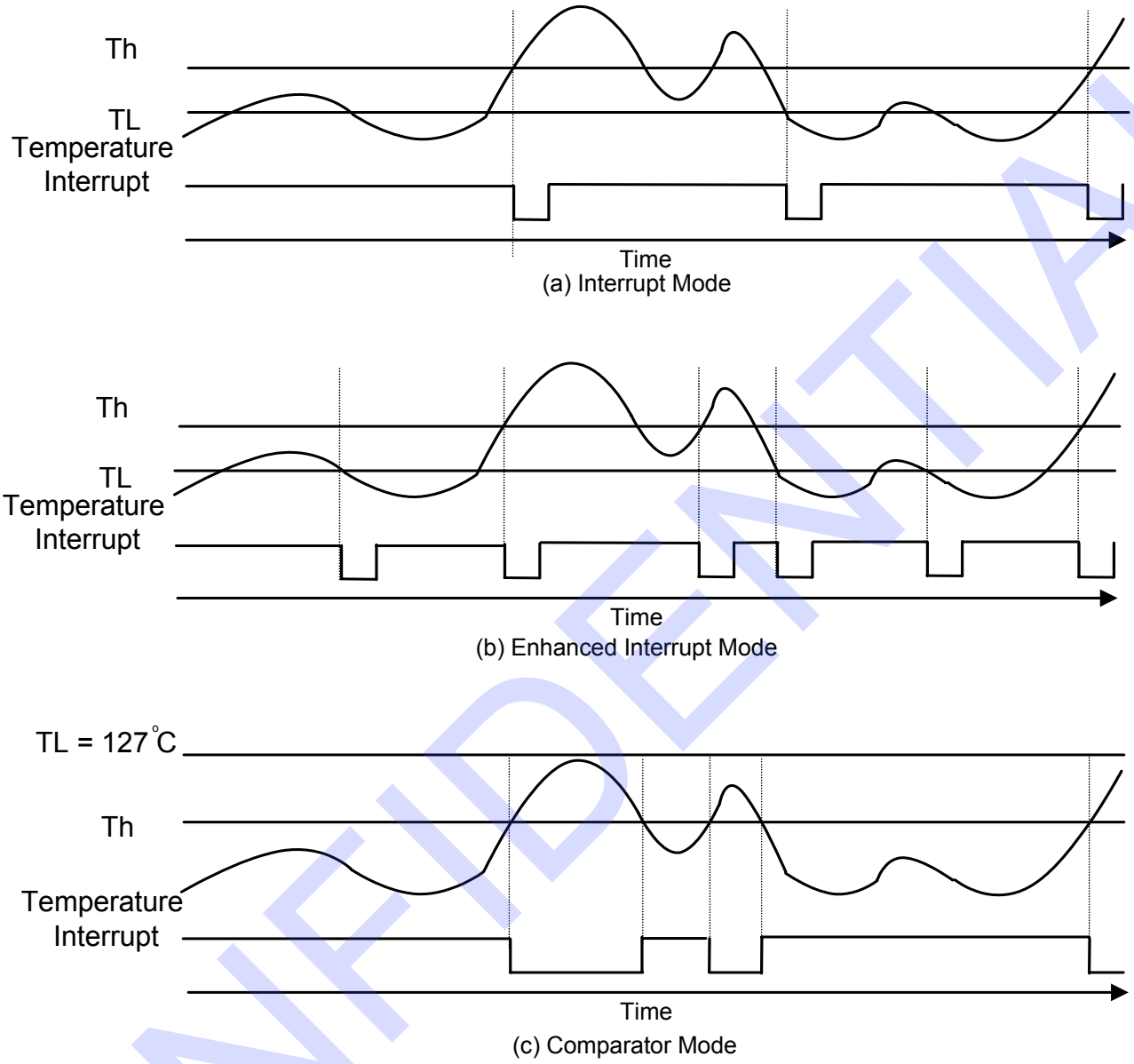
All analog voltage inputs have both high and low Limit Registers to generate interrupts whereas FAN monitoring inputs only have low Limit Register to warn the host. The IT8728F provides three modes dedicated to temperature interrupts in the EC: “Interrupt” mode, “Enhanced Interrupt” mode and “Comparator” mode.

Interrupt Mode
An interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 92). Once an interrupt event occurs by exceeding Th limit, an interrupt will only occur again when the temperature goes below TL limit after being reset. Again, it will set the corresponding status bit to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 92).

Enhanced Interrupt Mode
When the enhanced interrupt mode is enabled (bit 3, 6 and 7 of Fan Tachometer Control Register (Index=0Ch, Default=00h) for TMPIN1, 2, and 3 respectively) (refer to page 94), an interrupt will be generated when the temperature is higher than the high limit or lower than the low limit.

Comparator Mode
This mode is entered when the TL limit register is set to 127°C. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 92), but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

Figure 9-5. Temperature Interrupt Response Diagram



9.5.3.7 FAN Controller FAN_CTL's ON-OFF and SmartGuardian Modes

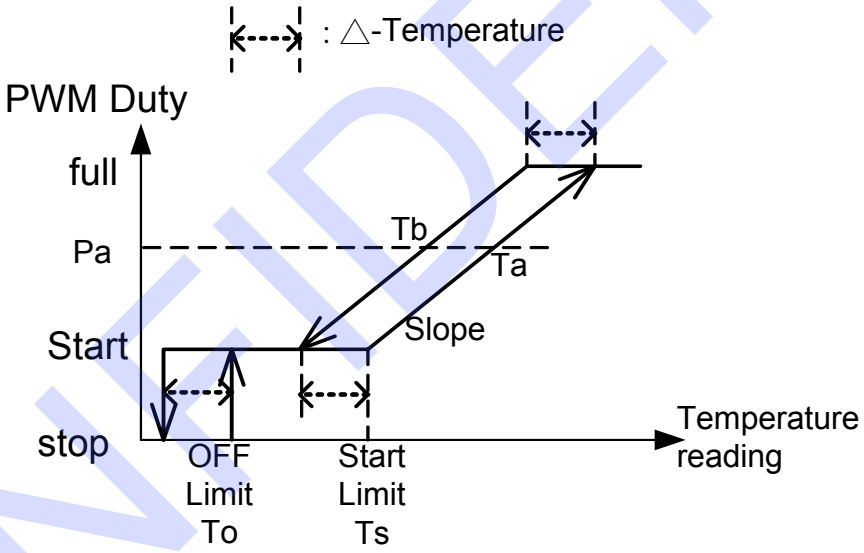
The IT8728F provides an advanced FAN Controller. Two modes, ON_OFF and SmartGuardian, are provided for each controller. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application circuits, the FAN's voltage values can be varied easily.

In the SmartGuardian Mode, there are two operational choices, software control or automatic control.

While under software control, the PWM value is subject to the changes in the values of bit 6-0 of FAN_CTL 1-3 PWM Control Registers (Index=15h, 16h, 17h). With the application circuits, FAN_CTL can generate 256 steps of voltage. So, the FAN_CTL 1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speeds or other voltage control cooling device can be varied in 256 steps.

While under automatic mode, the PWM value is subject to the temperature inputs by linear changes. When the temperature exceeds a start limit, FAN_CTL spins in a start PWM value (Index 73h, 6Bh, 63h). When the temperature reading is between the Start limit and the full limit (=Ts+(256- Start PWM)/Slope), the PWM value changes depending on the temperature reading if the reading exceeds the right boundary. If the temperature increases X ℃, the PWM value will increase X * K. K (Slope) is a constant value with 4 bits for the integer and 3 bits for the decimal, and is determined by bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode Start PWM register and bit 5-0 of FAN_CTL 3-1 SmartGuardian Automatic mode control registers. However, if the reading doesn't exceed the right boundary, the PWM value will keep the original value. For example, if PWM is currently at a value of Pa, it will not change if Tb < the temperature reading < Ta. If the new reading (Tnew) > Ta, the new PWM value will be Start PWM + K * (Tnew – Ts). If the new reading < Tb, there are two decreasing modes. If bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode △-Temperature is 0, the new PWM value will be Start PWM + K * ((Tnew+Ta)/2 – Ts). If the bit is 1, the new PWM value will be Start PWM + K * (Tnew – Ts). When the temperature is lower than the start limit but larger than the OFF limit (Index 70h, 68h, 60h), FAN_CTL will not stop, but keep in the start PWM value until the temperature is lower than the OFF limit.

Figure 9-6. SmartGuardian Automatic Mode



9.5.3.8 External Thermal Sensor Programming Procedure

Figure 9-7. PECI Programming Procedure

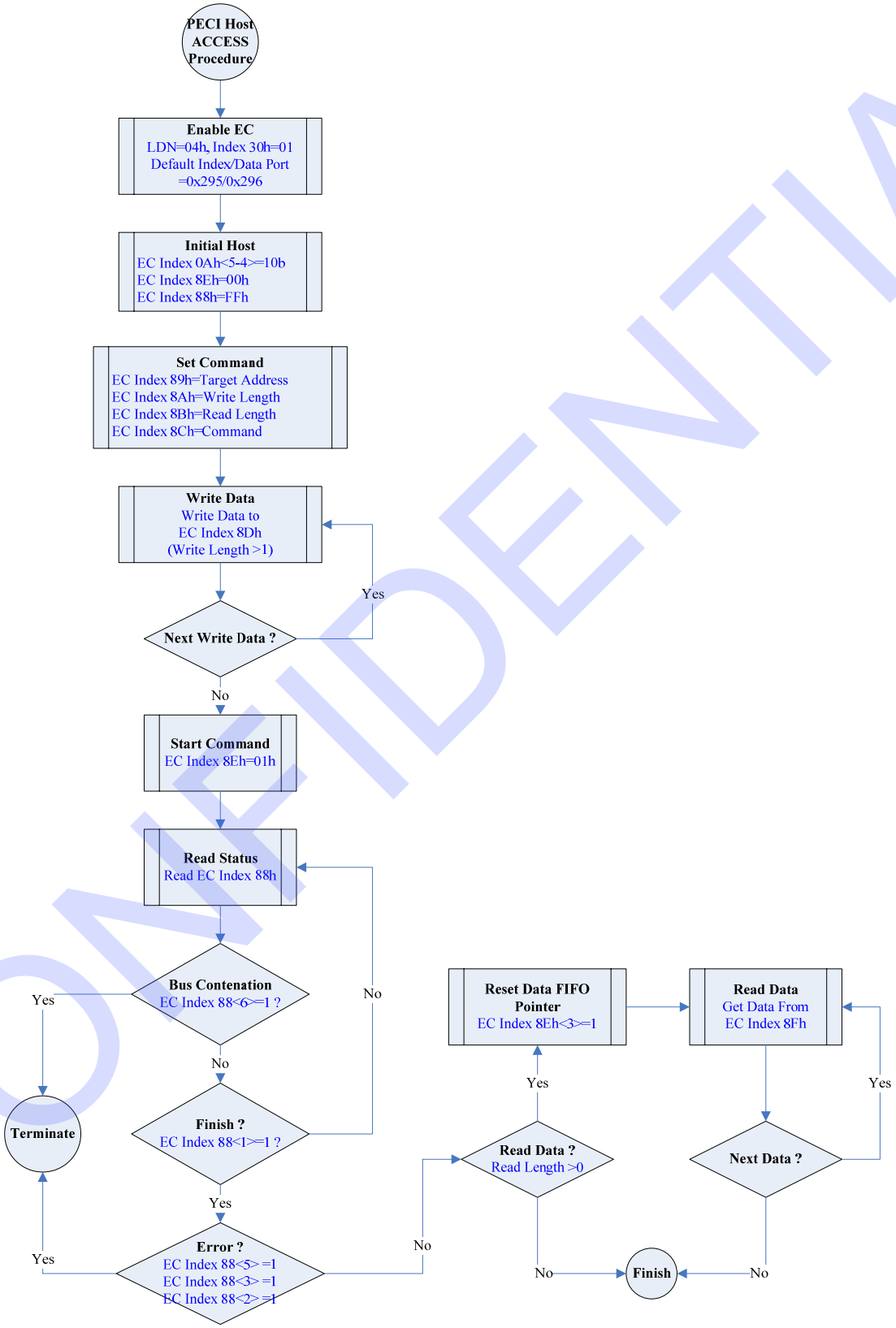


Figure 9-8. SST Host Programming Procedure

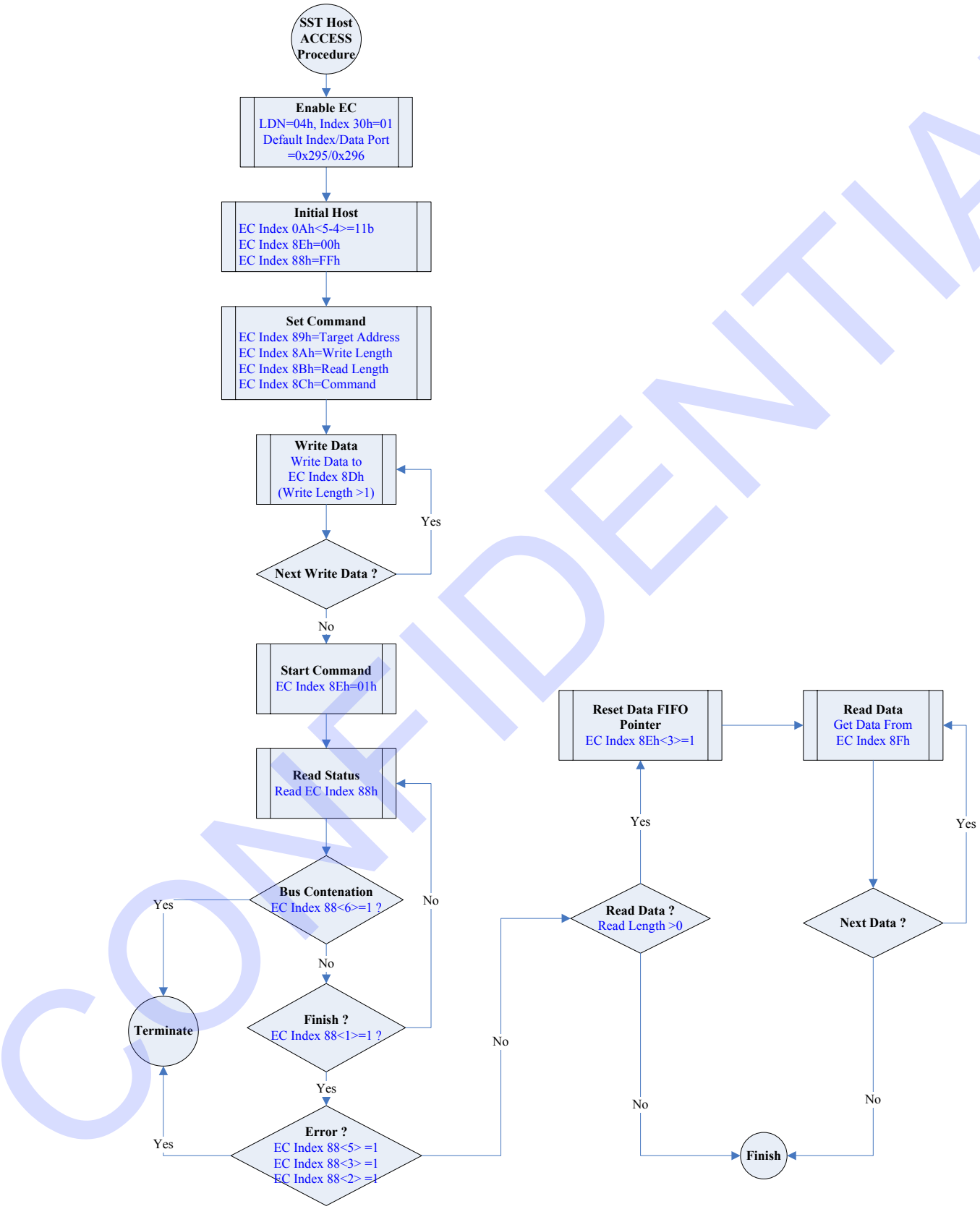


Figure 9-9. SST Slave Programming Procedure

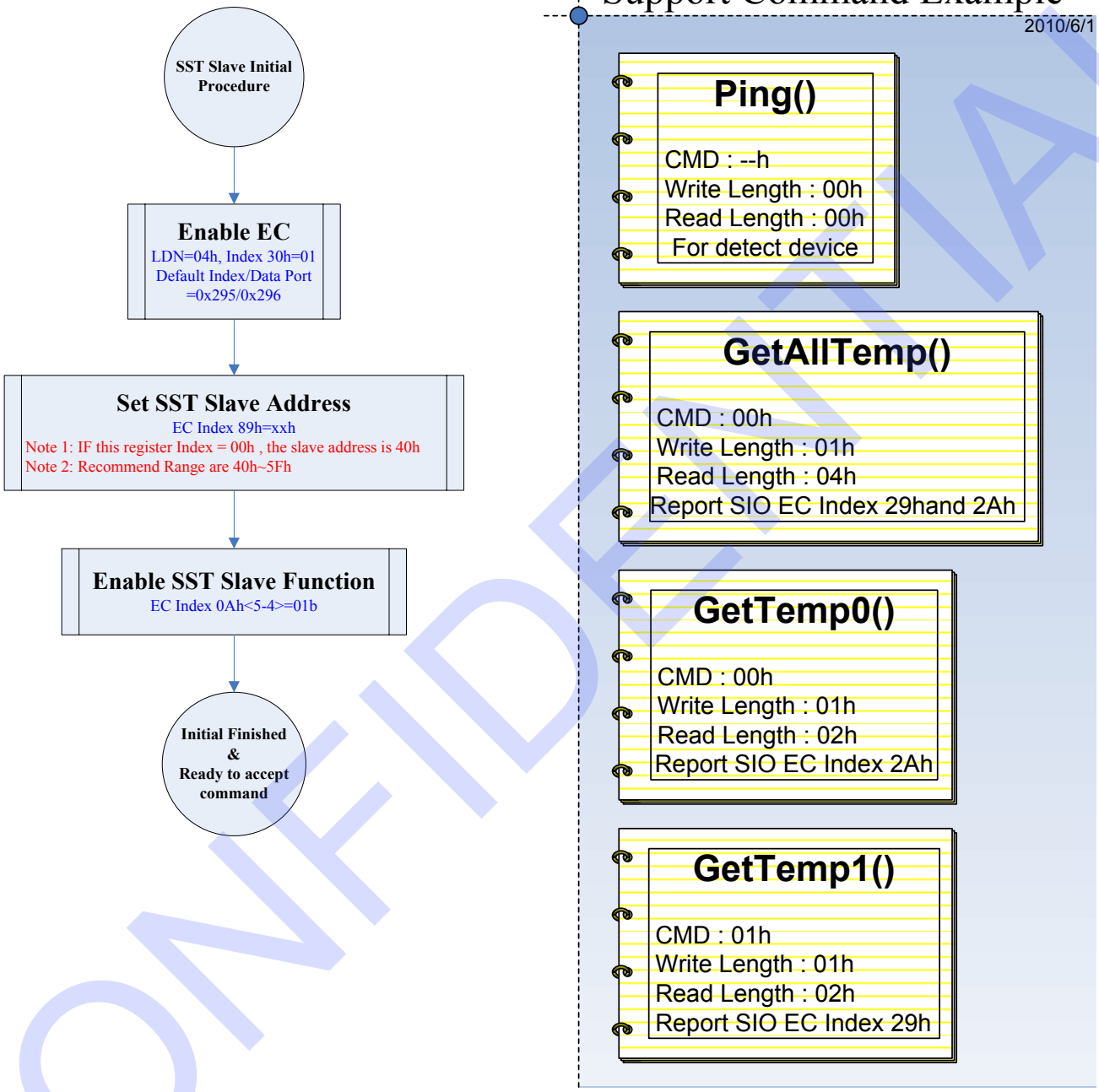


Figure 9-10. SMBUS Host Programming Procedure

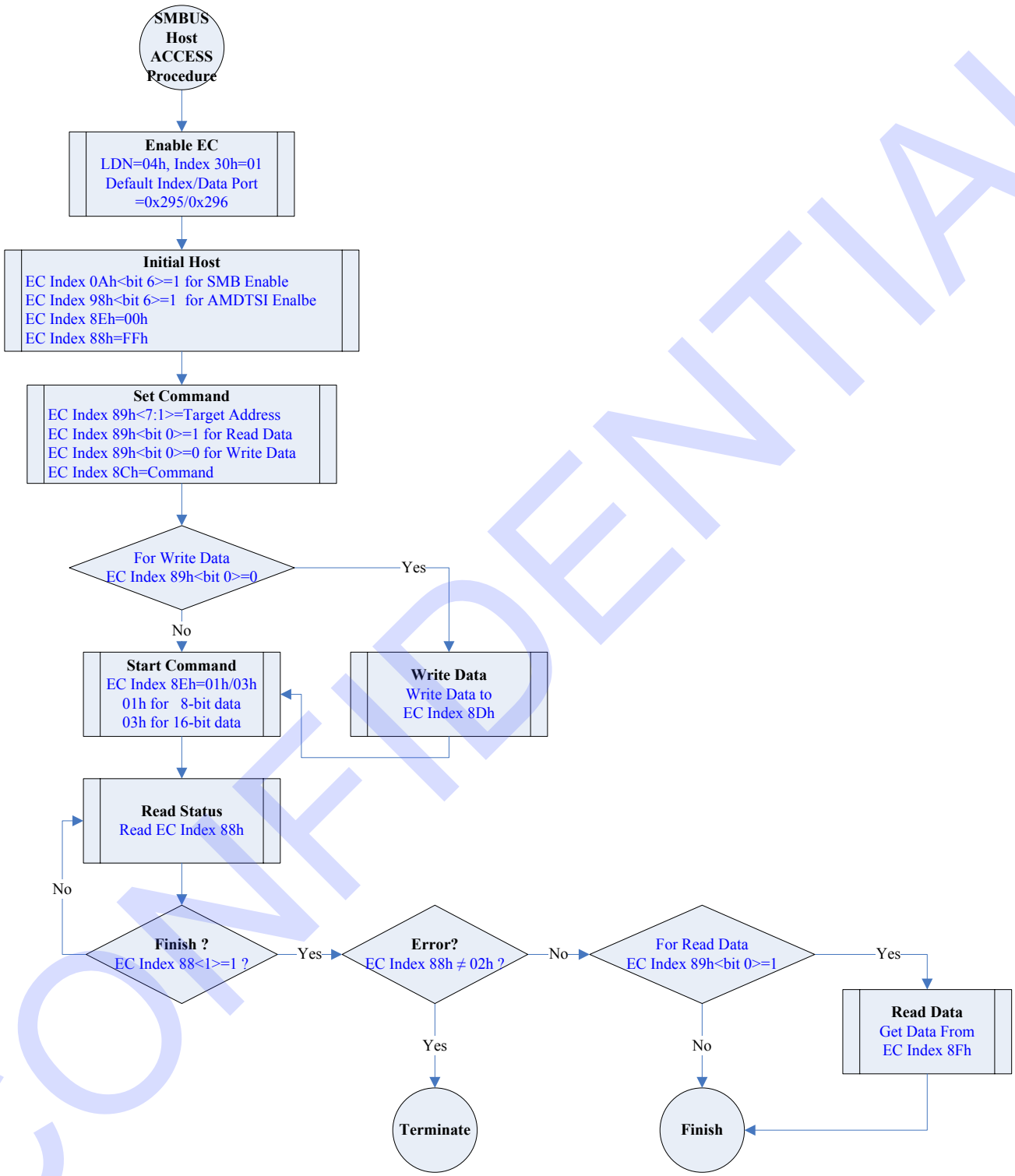


Figure 9-11. AMDTSI Host Programming Procedure

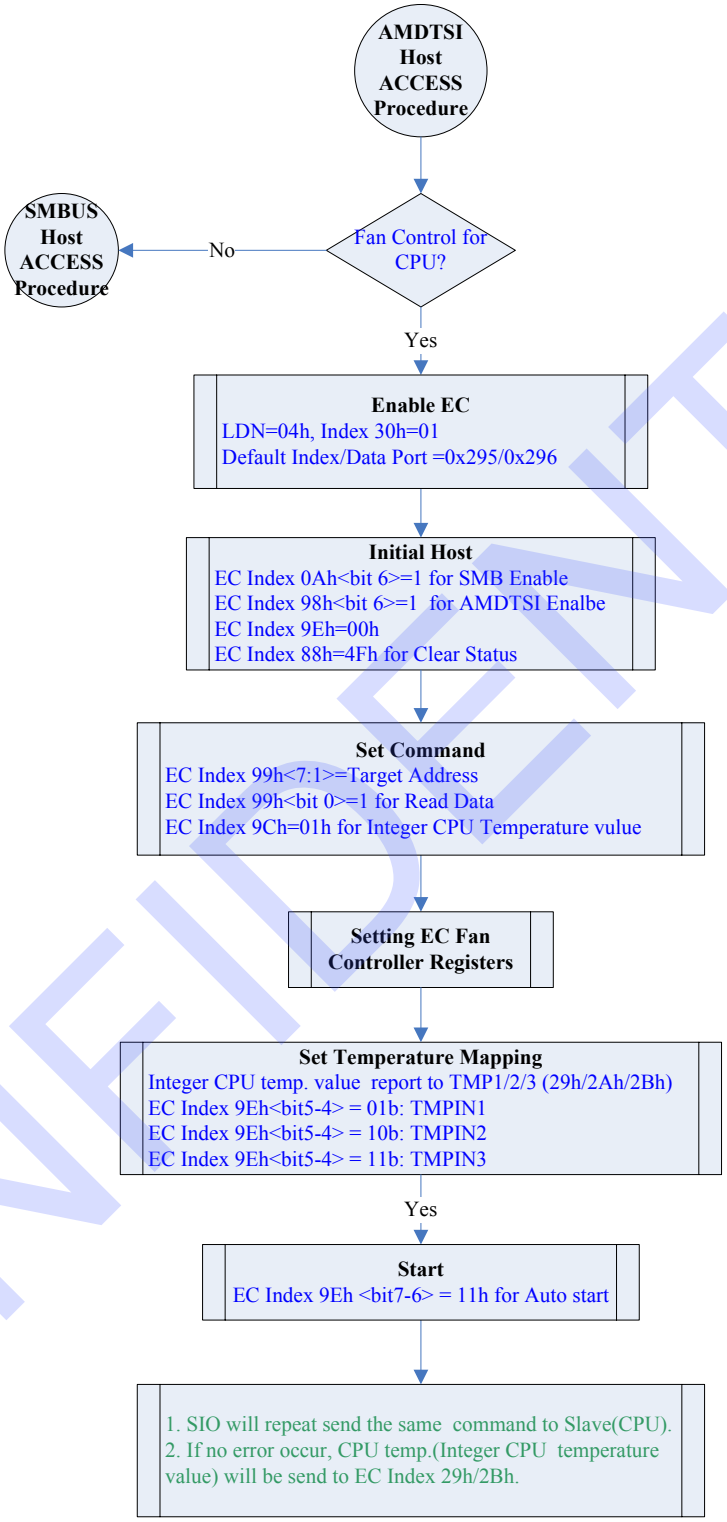
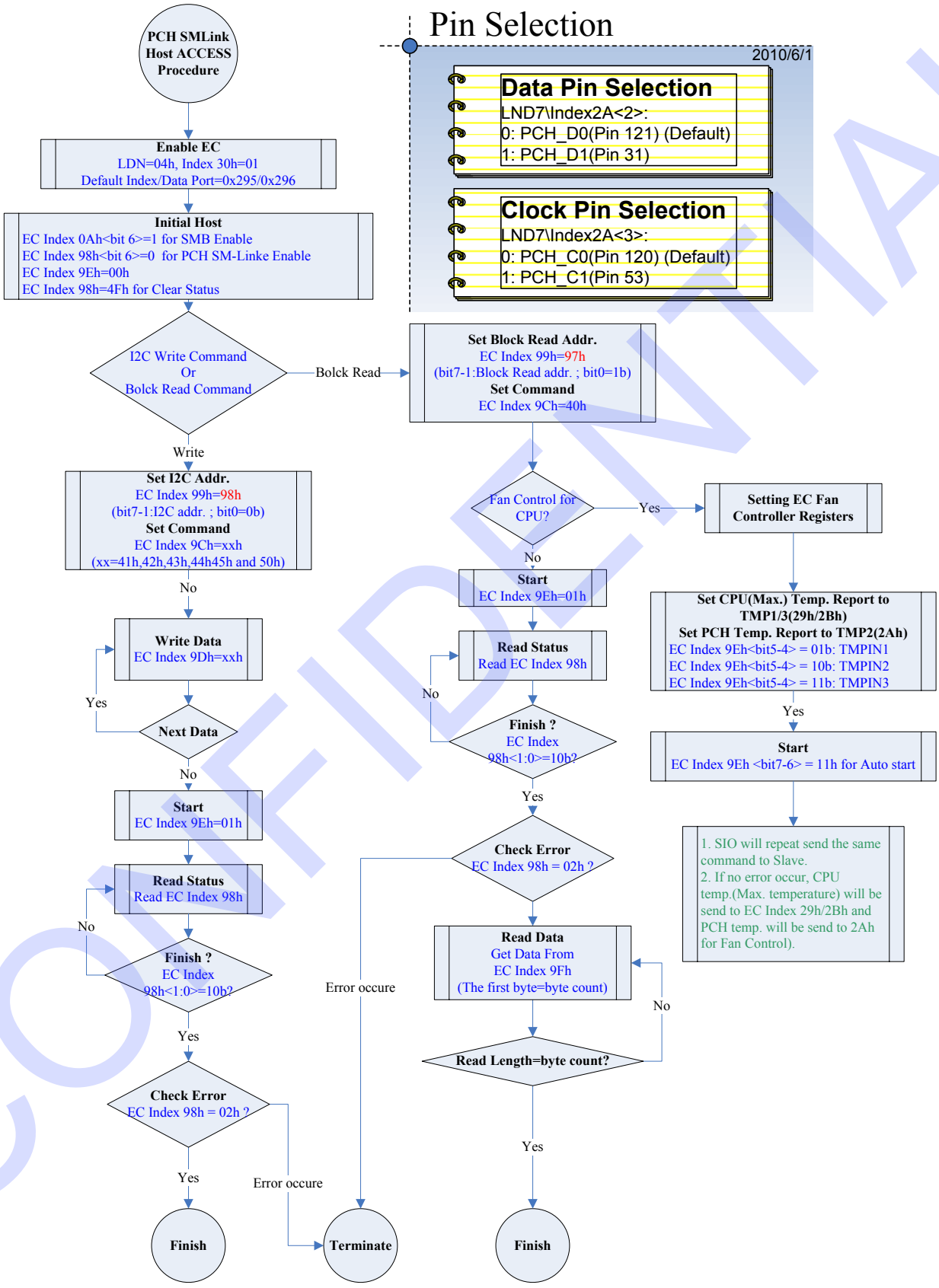


Figure 9-12. PCH SM-Link Programming Procedure



9.6 Floppy Disk Controller (FDC)

9.6.1 Overview

The Floppy Disk Controller (FDC) provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in the PC/AT mode and supports the 3-mode type drive. Additionally, the FDC is software compatible with the 82077. The controller manages data transfer using a set of data transfer and control commands, which are processed in three phases, Command, Execution, and Result, but not all of them will be utilized.

The FDC can be configured by software and a set of configuration registers. The **Status, Data and Control Registers** facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors of the data or operation of the FDC/FDD.

9.6.2 Reset

The IT8728F device implements both software and hardware reset options for the FDC. Either option will reset the FDC, terminating all operations and making the FDC enter an idle state. A reset during a write to the disk will disorder the data and the corresponding CRC.

9.6.2.1 Software Reset (DOR Reset and DSR Reset)

When the reset bit in **Digital Output Register (DOR, FDC Base Address + 02h)** or **Data Rate Select Register (DSR, FDC Base Address + 04h)** is set, all registers of the FDC core will be cleared. A reset performed by setting the reset bit in the DOR has a higher priority over that in the DSR. In addition, to exit the reset state, the DSR bit will be self-cleared when the host clears the DOR bit.

9.6.2.2 Hardware Reset (LRESET# Pin)

When the FDC receives an LRESET# signal, all registers of the FDC core will be cleared, except those programmed by the SPECIFY command. To exit the reset state, the host must clear the DOR bit.

9.6.3 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is to separate the encoded clock from data pulses.

9.6.4 Write Precompensation

Write precompensation is a method to adjust the effects of bit shifting on data as it is written to the disk. It is harder for the data separator to read data that have been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions.

Write precompensation can be selected by bit 4-2 of **Data Rate Select Register (DSR, FDC Base Address + 04h)**.

9.6.5 Data Rate Selection

Selecting one of the four possible data rates for the floppy disk can be achieved by setting bit 1-0 of **Data Rate Select Register (DSR, FDC Base Address + 04h)**. The data rate is determined by the last value written to either DCR or the DSR. After the data rate is set, the data separator clock will be scaled appropriately.

9.6.6 Status, Data and Control Registers

9.6.6.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register, which controls drive selection as well as motor, software reset, and DMA enable. The I/O interface reset may be used anytime to clear DOR's contents.

Bit	Symbol	Description
7-6	-	**Reserved**
5	MOTB EN	**Drive B Motor Enable** 0: Disable 1: Enable
4	MOTA EN	**Drive A Motor Enable** 0: Disable 1: Enable
3	DMAEN	**Disk Interrupt and DMA Enable** 0: Disable (DRQx, DACKx#, TC and INTx) 1: Enable
2	RESET#	**FDC Function Reset** 0: Function reset 1: Function reset cleared This reset has no impact on DSR, DCR or DOR.
1	-	**Reserved**
0	DVSEL	**Drive Selection** 0: Drive A selected 1: Drive B selected

9.6.6.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register compatible with 82077 software. The contents of this register are not used internally for the device.

Bit	Symbol	Description
7-2	-	**Reserved**
1-0	TP_SEL [1:0]	**Tape Drive Selection** TP_SEL[1:0]: Drive selected 00: None 01: 1 10: 2 11: 3

9.6.6.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register, which indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from **Data Register (FIFO, FDC Base Address + 05h)**, except when it is in the DMA mode.

Bit	Symbol	Description
7	RQM	**Request for Master** 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and can receive data from the host.
6	DIO	**Data I/O Direction** This bit indicates the direction of data transfer once an RQM has been set. 0: Write 1: Read
5	NDM	**Non-DMA Mode** 0: DMA mode selected 1: Non-DMA mode selected This mode is selected via the SPECIFY command during **Execution Phase**.
4	CB	**Diskette Control Busy** This bit indicates whether a command is in progress (FDD busy) or not. 0: A command has been executed and the end of **Result Phase** has been reached. 1: A command is being executed.
3-2	-	**Reserved**
1	DBB	**Drive B Busy** This bit indicates whether Drive B is in SEEK command operation. 0: Not busy 1: Busy
0	DAB	**Drive A Busy** This bit indicates whether Drive A is in the SEEK command operation. 0: Not busy 1: Busy

9.6.6.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register, which determines the data rate, write precompensation selection, power-down mode, and software reset. The data rate of the FDC is determined by the last value written to either DSR or DCR. The DSR is unaffected by a software reset and can be set to "02h" by a hardware reset. The "02h" represents the default precompensation, and 250 Kbps indicates the data transfer rate.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>S/W RESET</td><td>Software Reset
This bit is active high and has the same function as that of RESET# of DOR, except that it is self-cleared.</td></tr>
<tr><td>6</td><td>POWER DOWN</td><td>Power Down
When "1" is written to this bit, FDC will enter the manually low-power mode. The clocks of FDC and data separator circuits will be turned off until software reset, Data Register or Main Status Register is accessed.</td></tr>
<tr><td>5</td><td>-</td><td>Reserved</td></tr>
<tr><td>4-2</td><td>PRE-COMP 2-0</td><td>Precompensation Select
These three bits are to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default of the starting track number, which can be changed by the CONFIGURE command for precompensation.
<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>
Default Precompensation Delay
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1 Mbps</td><td>41.7 ns</td></tr>
<tr><td>500 Kbps</td><td>125.0 ns</td></tr>
<tr><td>300 Kbps</td><td>125.0 ns</td></tr>
<tr><td>250 Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>DRATE1-0</td><td>Data Rate Select
<table>
<tr><th>Bit 1-0</th><th>Data Transfer Rate</th></tr>
<tr><td>00</td><td>500 Kbps</td></tr>
<tr><td>01</td><td>300 Kbps</td></tr>
<tr><td>10</td><td>250 Kbps (Default)</td></tr>
<tr><td>11</td><td>1 Mbps</td></tr>
</table></td></tr>
</table>

9.6.6.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register, which transfers command information, diskette drive status, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer the information or status to the data bus at a time.

Bit	Symbol	Description
7-0	-	**Data** Command information, diskette drive status, and result phase status data.

9.6.6.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register, which shares this address with the Diskette Control Register (DCR).

Bit	Symbol	Description
7	DSKCHG	**Diskette Change** This bit indicates the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	**Reserved**

9.6.6.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register, which shares this address with the Digital Input Register (DIR) and controls the data transfer rate for the FDC.

Bit	Symbol	Description
7-2	-	**Reserved** Always 0
1-0	DRATE1-0	**Data Rate Select** **Bit 1-0** — **Data Transfer Rate** 00 — 500 Kbps 01 — 300 Kbps 10 — 250 Kbps 11 — 1 Mbps

9.6.7 Controller Phases

The FDC is to process data transfer and control commands in three phases, Command, Execution and Result, not all of which will be utilized.

9.6.7.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. Refer to **Data Transfer Command** and **Control Commands** sections for details of various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.6.7.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfer occurs between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in the DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.6.7.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.6.7.4 Result Phase Status Registers

For commands containing a Result phase, these **read only** registers indicate the status of the latest executed command.

Table 9-3. Status Register 0 (ST0)

Bit	Symbol	Description
7-6	IC	**Interrupt Code** 00: The execution of the command has been completed successfully. 01: The execution of the command is activated but fails to be completed successfully. 10: It means an invalid command. 11: The execution of the command is not completed successfully due to a polling error.
5	SE	**Seek End** The FDC executes a SEEK or RE-CALIBRATE command.
4	EC	**Equipment Check** The TRK0# pin is not set after a RE-CALIBRATE command is issued.
3	NU	**Not Used**
2	H	**Head Address** The current head address
1	DSB	**Drive B Select**
0	DSA	**Drive A Select**

Table 9-4. Status Register 1 (ST1)

Bit	Symbol	Description
7	EN	**End of Cylinder** This bit indicates the FDC attempts to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	NU	**Not Used**
5	DE	**Data Error** A CRC error occurs in either the ID field or the data field of a sector.
4	OR	**Overrun/Underrun** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	NU	**Not Used**

Bit	Symbol	Description
2	ND	**No Data** No data are available for the FDC when any of the following conditions occurs: • The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are being executed. • While a READ ID command is being executed, an error occurs upon reading the ID field. • While a READ A TRACK command is being executed, the FDC cannot find the starting sector.
1	NW	**Not Writeable** It is set when WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	**Missing Address Mark** This flag bit is set when either of the following conditions is met: • The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track. • The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin.

Table 9-5. Status Register 2 (ST2)

Bit	Symbol	Description
7	NU	**Not Used**
6	CM	**Control Mark** This flag bit is set when either of the following conditions is met: • The FDC finds a Deleted Data Address Mark during a READ DATA command. • The FDC finds a Data Address Mark during a READ DELETED DATA command.
5	DD	**Data Error in Data Field** This flag bit is set when a CRC error is found in the data field.
4	WC	**Wrong Cylinder** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	**Scan Equal Hit** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	**Scan Not Satisfied** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	**Bad Cylinder** This flag bit is set when the track address equals to “FFh” and is different from the track address in the FDC.
0	MD	**Missing Data Address Mark** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-6. Status Register 3 (ST3)

Bit	Symbol	Description
7	FT	**Fault** This bit indicates the current status of the Fault signal from the FDD.
6	WP	**Write Protect** This bit indicates the current status of the Write Protect signal from the FDD.
5	RDY	**Ready** This bit indicates the current status of the Ready signal from the FDD.
4	TK0	**Track 0** This bit indicates the current status of the Track 0 signal from the FDD.
3	TS	**Two Side** This bit indicates the current status of the Two Side signal from the FDD.
2	HD	**Head Address** This bit indicates the current status of the Head Address signal to the FDD.
1-0	US1, US0	**Unit Select** This bit indicates the current status of the Unit Select signal to the FDD.

9.6.8 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte containing the op-code, and a series of additional bytes containing the required set of parameters and results. For the description of the common set of parameter byte symbols, please refer to the following table. The FDC commands may be executed whenever it is in the Command phase and will check whether the first byte is a valid command or not. If yes, it will proceed. If not, an interrupt will be issued.

Table 9-7. Command Set Symbol

Symbol	Description
C	**Cylinder Number** The current/selected cylinder (track) number, 0-255.
D	**Data** The data pattern to be written into a sector.
DC3-DC0	**Drive Configuration Bit 3-0** Designate which drives are the perpendicular drives on the PERPENDICULAR MODE command.
DIR	**Direction Control** Head Step Direction Control of Read/Write. 0: Step out 1: Step in
DR0, DR1	**Disk Drive Selection** The selected drive number, 0 or 1.
DTL	**Data Length** When N is defined as 00h, DTL designates the number of data bytes to be read out or written into the Sector. When N is not 00h, DTL is undefined.
DFIFO	**Disable FIFO** 0: Enable 1: Disable (Default)
EC	**Enable Count** If EC=1, DTL of VERIFY command will be SC.
EIS	**Enable Implied Seek** If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	**End of Track** This is the final sector number on a cylinder. During a READ or WRITE operation, the FDC

Symbol	Description
	stops data transfer after the sector number is equal to EOT.
GAP2	**Gap 2 Length** By PERPENDICULAR MODE command, this parameter changes the length format of Gap 2.
GPL	**Gap Length** During a FORMAT command, it determines the length of Gap 3.
H	**Head Address** The Head number, 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	**Head** The selected Head number, 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	**Head Load Time** The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	**Head Unload Time** The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK	If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.
MFM	**FM or MFM Mode** If MFM is low, FM mode (single density) is selected. If MFM is high, MFM mode (double density) is selected.
MT	**Multi-Track** If MT is high, a Multi-Track operation will be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation in the last sector on side 0.
N	**Number** The number of data bytes written into a sector, where: 00: 128 bytes (PC standard) 01: 256 bytes 02: 512 bytes … 07: 16 Kbytes
NCN	**New Cylinder Number** A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	**Non-DMA Mode** When ND is high, the FDC operates in the Non-DMA Mode.
OW	**Overwrite** If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	**Present Cylinder Number** This is the cylinder number at the completion of a SENSE INTERRUPT STATUS command, indicating the present head position.
POLLD	**Polling Disable** If POLLD=1, the internal polling routine is disabled.
PRETRK	**Precompensation Starting Track Number** Programmable from track 0-255.
R	**Record** The sector number to be read or written.
RCN	**Relative Cylinder Number** To determine the relative cylinder offset from the present cylinder used by the RELATIVE SEEK command.
SC	**Number of Sector Per Cylinder**
SK	**Skip**

Symbol	Description
	If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Otherwise, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	**Step Rate Time** This is the stepping rate for the FDD (1 to 16 ms in 1 ms increments) and it is applied to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	**Status 0** **Status 1** **Status 2** **Status 3** ST0-3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by A_0 = 0). ST0-3 may be **read only** after a command has been executed and contain information associated with that particular command.
STP	If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-8. Command Set Summary

READ DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ A TRACK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

FORMAT A TRACK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution	W	C								Input Sector Parameters per-sector FDC formats an entire cylinder
	W	H								
	W	R								
	W	N								
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

SCAN EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

VERIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ ID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information during execution phase
	R	H								
	R	R								
	R	N								

CONFIGURE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	1	DIR	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	R	0	DIS	DFIFO	POLLD	FIFOTHR				
	R	PRETRK								

LOCK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

VERSION									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each SEEK operation
	R	PCN								

SENSE DRIVE STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Result	R	ST3								Status information about FDD

SPECIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

PERPENDICULAR MODE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into the standby state)
Result	R	ST0								ST0 = 80h

9.6.9 Data Transfer Command

All data transfer commands utilize bytes with the same parameter (except for FORMAT A TRACK command) and return data bytes with the same result. The only difference between them is the five bits (bit 0-bit 4) of the first byte.

9.6.9.1 READ DATA Command

The READ DATA command contains nine command bytes that make the FDC enter the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. After the data from the given sector are read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector are read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC will stop sending data but continue reading data from the current sector and check the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:
Sector Size = $2^{(7+N\ value)}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, set the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If it occurs to a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operation, the FDC can also perform Multi-Track Read operation. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-9 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-9. Effects of MT and N Bit

MT	N	Maximum Data Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X16 =16384	16 on side 1

9.6.9.2 READ DELETED DATA Command

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.9.3 READ A TRACK Command

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowable under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark is found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

9.6.9.4 WRITE DATA Command

The WRITE DATA command contains nine command bytes that make the FDC enter the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data fields with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in ST0 to 01 and the DE bit in ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.6.9.5 WRITE DELETED DATA Command

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.9.6 FORMAT A TRACK Command

The FORMAT A TRACK command is to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) required to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.6.9.7 SCAN Command

The SCAN command allows the data read from the disk to be compared with the data sent from the system. Followings are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The execution of SCAN command will not be terminated until the scan condition has been met, EOT has been reached, or TC is asserted. Read errors on the disk have the same error condition as that for the READ DATA command. If the SK bit is set, sectors with Deleted Data Address Marks are ignored. If all sectors' read is skipped, the command terminates with D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 9-10. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.6.9.8 VERIFY Command

The VERIFY command is to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data are transferred to the host. This command is designed for post-format or post write verification. Data are read from the disk as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data are transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value is equal to the final sector to be checked.

Table 9-11. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

9.6.10 Control Commands

The control commands do not transfer any data and . Instead, these commands are used to monitor and manage the data transfer instead. Three of them, READ ID, RE-CALIBRATE and SEEK, will generate an interrupt after data transfer is completedcompletion. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

9.6.10.1 READ ID Command

T The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark beforeby the time the second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.6.10.2 CONFIGURE Command

The CONFIGURE command determines some specific operation modes of the controller and does not need to be issued if the default values of the controller meet the system requirements.

EIS: Enable Implied Seek. A SEEK operation is performed before a READ, WRITE, SCAN, or VERIFY command.
0: Disable (Default)
1: Enable

DFIFO: Disable FIFO.
0: Enable
1: Disable (Default)

POLLD: Disable polling of drives.
0: Enable (Default) When enabled, a single interrupt is generated after a reset.
1: Disable

FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 byte to 16 bytes). The default is 1 byte.

PRETRK: The Precompensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). The default is track 0.

9.6.10.3 RE-CALIBRATE Command

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, SE [and EC bits] of the ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 to high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and the drives attached.

9.6.10.4 Seek Command

The SEEK command controls the FDC read/write head movement from one track to the other. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head if required. The direction of movement is determined by the followings:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses.
PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses.
PCN = NCN — Terminate the command by setting ST0 SE bit to 1.

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.6.10.5 RELATIVE SEEK Command

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is to determine whether to step in or out. RCN (Relative Cylinder Number) is to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other commands except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.6.10.6 DUMPREG Command

The DUMPREG command is designed for system run-time diagnostics, application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of the parameter set in other commands.

9.6.10.7 LOCK Command

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters of DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after software reset.

9.6.10.8 VERSION Command

The VERSION command is to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.6.10.9 SENSE INTERRUPT STATUS Command

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of ST0, as shown in Table 9-12 below.
It is necessary to generate an interrupt under any of the following conditions:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (Without Result phase)
- When a data transfer is required during Execution phase in the non-DMA mode

Table 9-12. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling
1	00	Normal termination of SEEK or RE-CALIBRATE command
1	01	Abnormal termination of SEEK or RE-CALIBRATE command

9.6.10.10 SENSE DRIVE STATUS Command

The SENSE DRIVE STATUS command is to acquire drive status information and there is no Execution phase for this command.

9.6.10.11 SPECIFY Command

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in the following three tables respectively. The FDC is operated in the DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-13. HUT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
-	-	-	-	-
E	112	224	373	448
F	120	240	400	480

Table 9-14. SRT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
-	-	-	-	-
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-15. HLT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
-	-	-	-	-
7E	126	252	420	504
7F	127	254	423	508

9.6.10.12 PERPENDICULAR MODE Command

The PERPENDICULAR MODE command is to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes of unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operate in the "Extra High Density" mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used and not set to 00, the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to the Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 9-16. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-17. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional	22 bytes	0 bytes
	Perpendicular	22 bytes	19 bytes
1 Mbps	Conventional	22 bytes	0 bytes
	Perpendicular	41 bytes	38 bytes

9.6.10.13 INVALID Command

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set Main Status Register (MSR, FDC Base Address + 04h) bit 7 (RQM) and bit 6 (DIO) to 1 (refer to page 121) and terminate the command without issuing an interrupt.

9.6.11 DMA Transfer

DMA transfer is enabled by the SPECIFY command and initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycle.

9.6.12 Low Power Mode

When writing a "1" to bit 6 of the DSR, the controller will enter the low-power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit will be gated. The FDC can be resumed from the low-power state in two ways. One is a software reset via the DOR or DSR, and the other is a read or write to either the Data Register or Main Status Register. The latter is preferred since all internal register values are retained.

9.7 Serial Port (UART)

The IT8728F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can be programmed from 115.2K baud down to 50 baud as well. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-18. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.7.1 Data Register

The TBR and RBR individually hold five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. Bit 0 of any word is first received and transmitted.

9.7.1.1 Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

9.7.1.2 Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before data transmission.

9.7.2 Control Register

9.7.2.1 Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is to enable or disable four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Bit	Default	Description
7-4	-	**Reserved**
3	0	**Enable Modem Status Interrupt** Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt** Set this bit high to enable the receiver line status interrupt, which happens when overrun, parity, framing or break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt** Set this bit high to enable the transmitter holding register empty interrupt.
0	0	**Enable Received Data Available Interrupt** Set this bit high to enable the received data available interrupt and time-out interrupt in the FIFO mode.

9.7.2.2 Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine the interrupt priority and its source. The four existing interrupts are listed below in priority order.

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the interrupt type is stored in the IIR which is accessed by the host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the host. Any new interrupts will not be acknowledged until the host access is completed. Please refer to the following table for the detail.

Table 9-19. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Function			
Bit 3	Bit 2	Bit 1	Bit 0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last four character times and there is at least one character in it during this period.	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not Defined

IIR(7), IIR(6): Set when FCR(0) = 1.
IIR(5), IIR(4): Always logic 0.
IIR(3): In the non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
IIR(2), IIR(1): Used to identify the highest priority interrupt pending.
IR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

9.7.2.3 FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to not only enable and clear the FIFO but also set the RCVR FIFO trigger level.

Bit	Default	Description
7-6	-	**Receiver Trigger Level Selection** These bits are to set the trigger level for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	This bit does not affect Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	**Transmitter FIFO Reset** This self-cleared bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1".
1	0	**Receiver FIFO Reset** Setting this self-cleared bit to a logic "1" will clear all contents of the RCVR FIFO and resets its related counter to "0" (except the shift register).
0	0	**FIFO Enable** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT whereas disabled and cleared respectively when this bit is cleared to low. This bit must be a logic "1" if data are written to the other bits of the FCR, or they will not be properly programmed. When this register is switched to the non-FIFO mode, all of its contents will be cleared.

Table 9-20. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

9.7.2.4 Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during initialization to generate a desired baud rate.

9.7.2.5 Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG, which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The number of DLL or DLM is in 16-bit format, providing the divisor ranging from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-21. Baud Rate Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

9.7.2.6 Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

9.7.2.7 Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line.

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** This bit must be set high to access the Divisor Latches of the baud rate generator during READ or WRITE operation whereas set low to access Data Register (refer to page 145) or Interrupt Identification Register (IIR) (Read only, Address offset=2) (refer to page 146).
6	0	**Set Break** This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, which will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	**Stick Parity** When this bit and LCR(3) are high at the same time, the parity bit is transmitted and then detected by a receiver in an opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Selection** When the parity is enabled (LCR(3) = 1), 0: Odd parity 1: Even parity
3	0	**Parity Enable** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bit** This bit specifies the number of stop bits in each serial character, as summarized in Table 9-22. Stop Bit Number Encoding.
1-0	00	**Word Length Select [1:0]** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-22. Stop Bit Number Encoding

LCR (2)	Word Length	No. of Stop Bit
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

9.7.2.8 Modem Control Register (MCR) (Read/Write, Address offset=4)

This register controls the interface by the modem or data set (or device emulating a modem).

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loopback** This bit provides a loopback feature for diagnostic test of the serial channel when set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high then the transmitted data are immediately received, allowing the processor to verify the transmitted and received data path of the serial channel.
3	0	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	**OUT1** This bit does not have an output pin and can only be read or written by CPU.
1	0	**Request to Send (RTS)** This bit controls the Request to Send (RTS#), which is in an inverse logic state with that of MCR(1).
0	0	**Data Terminal Ready (DTR)** This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with that of the MCR(0).

9.7.3 Status Registers

9.7.3.1 Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides the status indication and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Bit	Default	Description
7	0	**Error in Receiver FIFO** In the 16450 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.
6	1	**Transmitter Empty** This **read only** bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0" and has the same function as that in the FIFO mode.
5	1	**Transmitter Holding Register Empty (THRE)** This **read only** bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to the XMIT FIFO.
4	0	**Line Break** The Line Break (LB) Interrupt status bit indicates that the last character received is a break character, which is invalid but complete. It includes parity and stop bits. This situation occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in IIR, with bit 2 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) previously enabled(refer to page 146).

Bit	Default	Description
3	0	**Framing Error (FE)** A logic 1 indicates that the stop bit in the received character is not valid. It will be reset low when CPU reads the contents of the LSR.
2	0	**Parity Error (PE)** A logic 1 indicates that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever LSR is read by CPU.
1	0	**Overrun Error (OE)** A logic 1 indicates that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when LSR is read by the CPU.
0	0	**Data Ready** A logic 1 indicates a character has been received by RBR. A logic 0 indicates all the data in RBR or RCVR FIFO have been read.

9.7.3.2 Modem Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits, MSR(4) - MSR(7), can provide the state change information when the modem control input changes the state. It is reset low when the host reads the MSR.

Bit	Default	Description
7	0	**Data Carrier Detect(DCD)** This bit indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator(RI)** This bit indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready(DSR)** This bit indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# of MCR.
4	0	**Clear to Send(CTS)** This bit indicates the complement of CTS# input. When the serial channel is in the Loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# of MCR.
3	0	**Delta Data Carrier Detect(DDCD)** This bit indicates that the DCD# input state has been changed since being read by the host last time.
2	0	**Trailing Edge Ring Indicator(TERI)** This bit indicates that the RI input state to the serial channel has been changed from low to high since being read by the host last time. The change in a logic “1” does not activate the TERI.
1	0	**Delta Data Set Ready(DDSR)** A logic "1" indicates that the DSR# input state to the serial channel has been changed since being read by the host last time.
0	0	**Delta Clear to Send(DCTS)** This bit indicates the CTS# input to the chip has changed the state since MSR was read last time.

9.7.4 Reset

The reset of the IT8728F should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the internal clock counters of transmitter and receiver.

Table 9-23. Reset Control of Register and Pinout Signal

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT1, SOUT2	Reset	High
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.7.5 Programming

Each serial channel of the IT8728F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though these control registers can be written in any given order, IER should be the last register written because it controls whether the interrupt is enabled or not. After the port is programmed, these registers still can be updated whenever the port does not transfer data.

9.7.6 Software Reset

This approach allows the serial port to return to a completely known state without a system reset. It is achieved by writing the required data to LCR, DLL, DLM and MCR. LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.7.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.7.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 148) and bit 0 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 146) high, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The receive data available interrupt will be issued only when the FIFO has reached its programmed trigger level and cleared as soon as the FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from RCVR FIFO.

For the RCVR FIFO time-out interrupt, it will occur under the following conditions by enabling the RCVR FIFO and receiver interrupts:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in FIFO whenever the interval between the most recently received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 148) and bit 1 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 146) high, the XMIT FIFO and transmitter interrupts are enabled. The XMIT interrupt occurs under the following conditions:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed for one character time minus the last stop bit time whenever the following condition occurs:

   THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication will be delayed for one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts have the same priority as the received data available interrupt. The XMIT FIFO empty has the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via LSR described below:

LSR(7): RCVR FIFO error indication
LSR(6): XMIT FIFO and Shift register empty
LSR(5): The XMIT FIFO empty indication
LSR(4) - LSR(1): Specify that errors have occurred. The character error status is handled in the same way as that in the interrupt mode. The IIR is not affected since IER(2)=0.
LSR(0): High whenever RCVR FIFO contains at least one byte.
No trigger level is reached or time-out condition indicated in FIFO Polled Mode.

9.8 Parallel Port

The IT8728F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). For enabling/disabling, changing the base address of the parallel port, and operation mode selection, please refer to section 8.7 configuration registers on page 59 for the detail.

Table 9-24. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	11	STB#	WRITE#	NStrobe
2-9	12-19	PD0 - 7	PD0 - 7	PD0 - 7
10	6	ACK#	INTR	nAck
11	5	BUSY	WAIT#	Busy PeriphAck(2)
12	4	PE	(NU) (1)	PError nAckReverse(2)
13	3	SLCT	(NU) (1)	Select
14	10	AFD#	DSTB#	nAutoFd HostAck(2)
15	9	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	8	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	7	SLIN#	ASTB#	nSelectIn

Note 1: NU: Not used
Note 2: Fast mode
Note 3: For more information, please refer to the IEEE 1284 standard.

9.8.1 SPP and EPP Mode

Table 9-25. Address Map and Bit Map for SPP and EPP Mode

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port 3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

9.8.1.1 Data Port Register (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by bit 5 of the logic state of Control Port Register (Base Address 1 + 02h), which forwards the direction when the bit is low (0) whereas reverses the direction when the bit is high (1).

9.8.1.2 Status Port Register (Base Address 1 + 01h)

This is a **read only** register. Writing data to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7: BUSY#
Inverse of printer BUSY signal; a logic "0" means that the printer is busy and cannot accept another character whereas a logic "1" means that it is ready to accept the next character.
Bit 6: ACK#
Printer acknowledge; a logic "0" means that the printer has received a character and is ready to accept another whereas a logic "1" means that it is still processing the last character.
Bit 5: PE
Paper end; a logic "1" indicates the paper end.
Bit 4: SLCT
Printer selected; a logic "1" means that the printer is on line.
Bit 3: ERR#
Printer error signal; a logic "0" means an error has been detected.
Bits 2-1: Reserved
These bits are always "1" at read.
Bit 0: TMOUT
This bit is valid only in the EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurs whereas a logic “1” means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic “1” to it. When the chip is selected as the non-EPP mode (SPP or ECP), this bit is always a logic "1" at read.

9.8.1.3 Control Port Register (Base Address 1 + 02h)

This is a **read/write** register and the port provides all output signals to control the printer.
Bit 7-6: Reserved
These two bits are always "1" at read.
Bit 5: PDDIR
Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus whereas "1" to input from PD bus.
Bit 4: IRQE
Interrupt request enable. Setting this bit "1" enables the interrupt request from the parallel port to the host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3: SLIN
Inverse of SLIN# pin; setting this bit to "1" selects the printer.
Bit 2: INIT
Initiate printer; setting this bit to "0" initializes the printer.
Bit 1: AFD
Inverse of the AFD# pin; setting this bit to "1" causes the printer to automatically advance one line after each line is printed.
Bit 0: STB
Inverse of the STB# pin; this pin controls the data strobe signal to the printer.

9.8.1.4 EPP Address Port Register (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the host writes data to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP ADDRESS WRITE cycle. When the host reads data from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP ADDRESS READ cycle.

9.8.1.5 EPP Data Port 0-3 Register (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the host writes data to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP DATA WRITE cycle. When the host reads data from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP DATA READ cycle.

9.8.2 EPP Mode Operation

When the parallel port of the IT8728F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by Control Port Register (Base Address 1 + 02h) (refer to page 156). The direction of the data port is controlled by bit 5 of Control Port Register (Base Address 1 + 02h). There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8728F will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle will be aborted and a logic "1" will be read from bit 0 of Status Port Register (Base Address 1 + 01h) (refer to page 156). The host must write 0 to bit 0, 1, 3 of Control Port Register (Base Address 1 + 02h) before any EPP READ/WRITE cycle (EPP spec.). Pin STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

9.8.2.1 EPP ADDRESS WRITE

1. The host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.8.2.2 EPP ADDRESS READ

1. The host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.8.2.3 EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04h - 07h). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.8.2.4 EPP DATA READ

1. The host reads a byte from the EPP DATA Port (Base address +04h - 07h). The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.8.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports the DMA or ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports hardware run-length encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8728F does not support hardware RLE compression. For the detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-26. Bit Map of ECP Register

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

9.8.3.1 ECP Register Definition

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000h	R/W	000-001	Data Register
ecpAFifo	Base 1 +000h	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001h	R/W	All	Status Register
dcr	Base 1 +002h	R/W	All	Control Register
cFifo	Base 2 +000h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000h	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000h	R/W	110	Test FIFO
cnfgA	Base 2 +000h	R	111	Configuration Register A
cnfgB	Base 2 +001h	R	111	Configuration Register B
ecr	Base 2 +002h	R/W	All	Extended Control Register

Note 1: Base address 1 depends on Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h) and Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h) (refer to page 59 and 59).

Note 2: Base address 2 depends on the Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h) and Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h) (refer to page 59 and 59).

9.8.3.2 ECP Mode Description

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: For the mode selection, please refer to ECP Register Definition on page 159 for the detail.

9.8.3.3 ECP Pin Description

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device
PD0-PD7	I/O	Address or data or RLE data
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the host
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe) whereas for determining whether a command or data information is present on PD0-PD7 in the reverse direction.
Perror (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus
Select	I	Printer On-Line Indication
nAutoFd (HostAck)	O	This signal is used for handshaking between the nAck and the host in the reverse direction. A peripheral data byte is requested when it is asserted. This signal is to determine whether a command or data information is present on PD0-PD7 in the forward direction.
nFault (nPeriphRequest)	I	For the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while entering the ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to make the PD bus in the reverse direction. The peripheral is permitted to drive the PD bus when nInit is low and nSelectIn high in the ECP mode.
NSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

9.8.3.4 Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a reset. The contents of the LPC data fields are latched by the Data Register then sent without being inverted to PD0-PD7 in **write** operation whereas the contents of data ports are read and sent to the host in **read** operation.

9.8.3.5 ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data bytes written to this port are placed in FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends these data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

9.8.3.6 Device Status Register (dsr) (Base 1 +01h, Mode All)

Bit 2-0 of this register are not implemented. The states of these bits remain high in **read** operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

9.8.3.7 Device Control Register (dcr) (Base 1+02h, Mode All)

There is no function porivided by bit 7-6 of this register, which are r**ead only** and set high in **read** operation. Contents of bit 5-0 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.
dcr(5): Except in mode 000 and 010, setting this bit low means that the PD bus is in output operation whereas setting it high means that it is in input operation. This bit will be forced to low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.
dcr(3): This bit is inverted and output to SelectIn.
dcr(2): This bit is output to nInit without inversion.
dcr(1): This bit is inverted and output to nAutoFd.
dcr(0): This bit is inverted and output to nStrobe.

9.8.3.8 Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

9.8.3.9 ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The host can receive these bytes by performing **read** operations or DMA transfer from this FIFO.

9.8.3.10 Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfer to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Operating READ from an empty tFifo causes the last data byte to return.

9.8.3.11 Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

9.8.3.12 Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

cnfgB(7): A logic “0” read indicates that the chip does not support hardware RLE compression.
cnfgB(6): Reserved.
cnfgB(5)-cnfgB(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)-cnfgB(0): A value 000 read indicates that the DMA channel is set to 8-bit DMA.

9.8.3.13 Extended Control Register (ecr) (Base 2+02h, Mode All)

This is an ECP function control register.

ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-27. Mode and Description of Extended Control Register (ECR)

ECR	Mode and Description
000	**Standard Parallel Port Mode** The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	**PS/2 Parallel Port Mode** It is similar to the SPP mode, except that the dcr(5) is **read/write**. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	**Parallel Port Data FIFO Mode** This mode is similar to the 000 mode, except that the host writes or DMA transfers the data bytes to FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	**ECP Parallel Port Mode** In the forward direction, bytes in the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	**Reserved; undefined**
110	**Test Mode** In this mode, FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	**Configuration Mode** In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode
- 1: Disable the interrupt generated on the asserting edge of the nFault input.
- 0: Enable the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE
- 1: Enable DMA. DMA is started when serviceIntr (ecr(2)) is 0.
- 0: Disable DMA unconditionally.

ecr(2): ServiceIntr, READ/WRITE
- 1: Disable DMA and all service interrupts.
- 0: Enable the service interrupts. This bit will be set to “1” by hardware when one of the three service interrupts occurs.

Writing “1” to this bit will not generate an interrupt.

Case 1: dmaEn=1
During DMA, this bit will be set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0
This bit is set to 1 (a service interrupt generated) whenever there is writeIntrThreshold or more bytes space free in FIFO.

Case 3: dmaEn=0, dcr(5)=1
This bit is set to 1 (a service interrupt generated) whenever there is readIntrThreshold or more valid bytes to be read from FIFO.

ecr(1): full, **read only**
- 1: FIFO is full and cannot accept another byte.
- 0: FIFO has at least one free data byte space.

ecr(0): empty, **read only**
1: FIFO is empty.
0: FIFO contains at least one data byte.

9.8.3.14 Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting the mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

For mode 000 and 001, they may be immediately switched. To change the direction, the mode must be set to 001 first.

In the extended forward mode, FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In the ECP reverse mode, all data must be read from FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking when the mode is changed during a data transfer. In such a condition, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

9.8.3.15 Software Operation (ECP)

Before the ECP operation can be started, it is necessary for the host to switch the mode to 000 first in order to negotiate with the parallel port. During this process, the host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfer is PWord-wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change the direction, the host has to switch the mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches the mode to 001. If the direction is set to 1, the hardware performs the handshaking for each ECP data byte read, and then tries to fill FIFO. At this time, PWords may be read from the ecpDFifo while retaining data. It is also possible to perform the ECP transfer by handshaking with individual bytes under programmed control in mode 001 or 000 even though this is a comparatively time-consuming approach.

9.8.3.16 Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets the direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents of FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

9.8.3.17 Interrupt

It is necessary to generate an interrupt when any of the following states is reached.

5. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.
6. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.
7. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.
8. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
9. ackIntEn = 1. In current implementation of using existing parallel ports, the generated interrupt may be either edge or level trigger type.

9.8.3.18 Interrupt-driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

For any PC LPC bus implementation adjusted to expedite DMA or I/O transfer, it is necessary to ensure that the bandwidth on ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

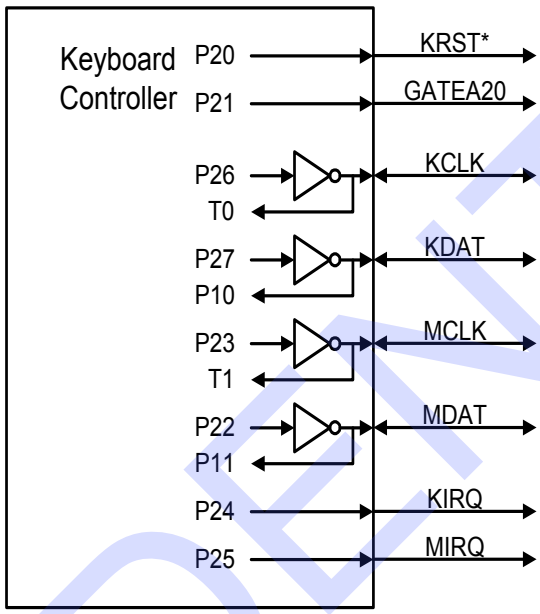
9.8.3.19 Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.9 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter the power-down mode by executing two types of power-down instructions.

Figure 9-13. Keyboard and Mouse Interface



9.9.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The following table shows how the interface decodes the control signals.

Table 9-28. Data Register READ/WRITE Controls

Host Address [Note]	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (Set F1)

Note: These are the default values of LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.
WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.
READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.

WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

9.9.2 Data Registers and Status Register

The keyboard controller provides two data registers, one is DBIN for data input, and the other is DBOUT for data output. Both are 8-bit wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 9-29. Status Register below. The bit 0 OBF is set to "1" when the microcontroller writes data into DBOUT, and is cleared when the system initiates DATA READ operation. The bit 1 IBF is set to "1" when the system initiates WRITE operation, and is cleared when the microcontroller executes an "IN A, DBB" instruction. The F0 and F1 flags can be set or reset when the microcontroller executes clear and complement flag instructions. F1 also holds the system WRITE information when the system performs WRITE operation.

Table 9-29. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.9.3 Keyboard and Mouse Interface

KCLK is a keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin. Its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin. Its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software-controlled or user defined outputs. External pull-ups may be required for these pins.

9.9.4 KIRQ and MIRQ

KIRQ is the interrupt request for the keyboard (Default IRQ1), and MIRQ is the interrupt request for the mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

9.10 Consumer Remote Control (TV Remote) IR (CIR)

9.10.1 Overview

CIR is used in the consumer remote control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisors and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

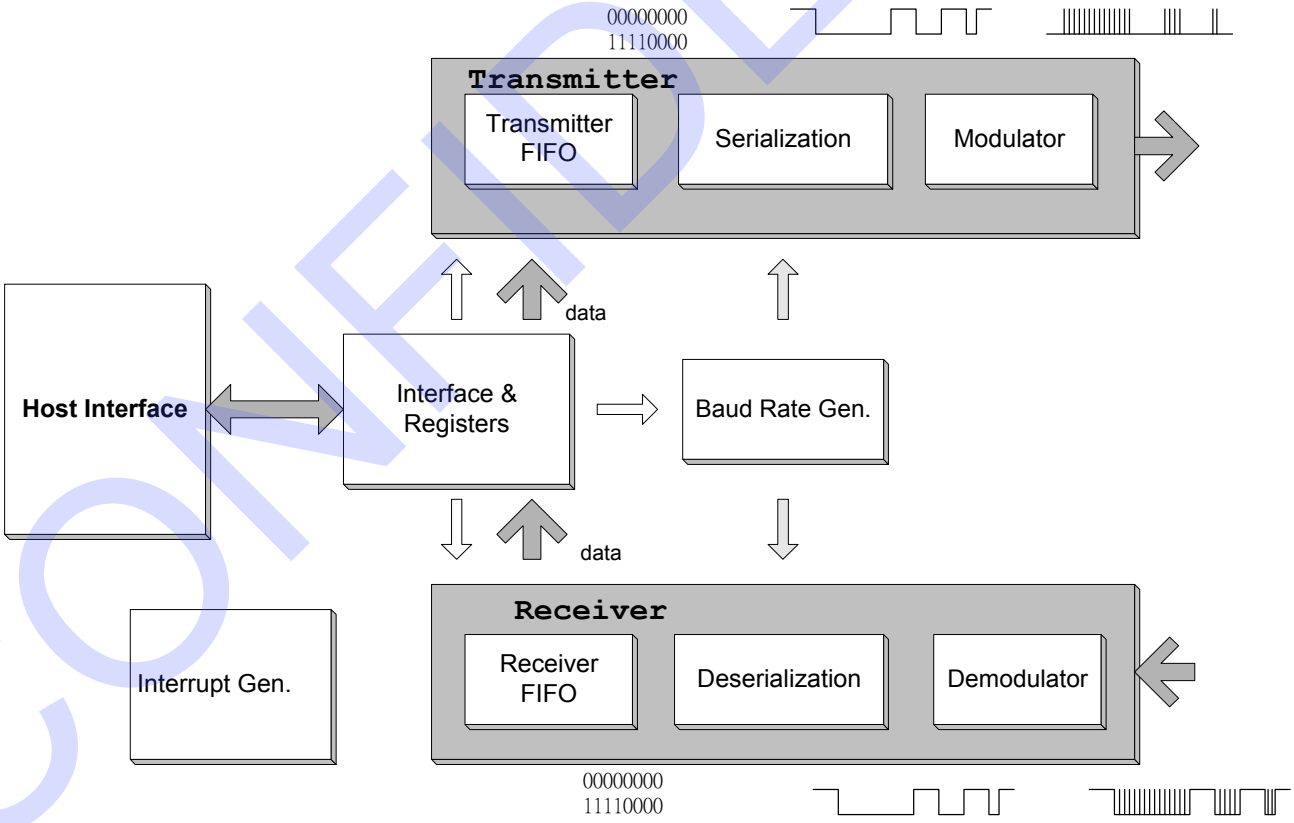
9.10.2 Features

- Supports 30 kHz - 57 kHz (low frequency) or 400 kHz - 500 kHz (high frequency) carrier transmission
- Baud rate up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral function
- 32-byte FIFO for data transmission or data reception

9.10.3 Block Diagram

CIR consists of two parts, transmitter and receiver. Regarding the transmitter part, it is responsible for transmitting data to FIFO, processing FIFO data by serialization and modulation and sending out data through the LED device. As for the receiver part, it is responsible for receiving data, processing data by demodulation and deserialization and storing data in the Receiver FIFO.

Figure 9-14. CIR Block Diagram



9.10.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with the carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can be started, code byte write operation must be performed to the Transmitter FIFO DR. Bit TXRLE of TCR1 needs to be set to “1” before the data in run-length decode can be written into the Transmitter FIFO. Setting TXENDF of TCR1 will enable the data transmission deferral, and avoid the Transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers, BDLR and BDHR. When the two bits, HCFS and CFQ[4:0], are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bit TXMPM[1:0] and TXMPW[2:0] specify the pulse number in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic “0” can activate the Transmitter LED in the format of a series of modulating pulses.

9.10.5 Receive Operation

The Receiver function will be enabled if bit RXEN of RCR is set to “1”. Either demodulated or modulated RX# signal is loaded into Receiver FIFO, and bit RXEND of RCR determines whether the demodulation logic should be used or not. It determines the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequency by programming bit HCFS and CFQ[4:0]. Set RDWOS to “0” to synchronize. Bit RXACT of RCR is set to “1” when the serial data or the selected carrier is incoming, and the sampled data will then be kept in Receiver FIFO. Write “1” to bit RXACT to stop the Receiver operation whereas “0” to bit RXEN to disable it.

9.10.6 Register Description and Address

Table 9-30. CIR Register

Register Name	R/W	Address	Default
CIR Data Register (DR)	R/W	Base + 0h	FFh
CIR Interrupt Enable Register (IER)	R/W	Base + 1h	00h
CIR Receiver Control Register (RCR)	R/W	Base + 2h	01h
CIR Transmitter Control Register 1 (TCR1)	R/W	Base + 3h	00h
CIR Transmitter Control Register 2 (TCR2)	R/W	Base + 4h	5Ch
CIR Transmitter Status Register (TSR)	R	Base + 5h	00h
CIR Receiver Status Register (RSR)	R	Base + 6h	00h
CIR Baud Rate Divisor Low Byte Register (BDLR)	R/W	Base + 5h	00h
CIR Baud Rate Divisor High Byte Register (BDHR)	R/W	Base + 6h	00h
CIR Interrupt Identification Register (IIR)	R/W	Base + 7h	01h

9.10.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through it.

Address: Base Address + 0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**CIR Data Register (DR[7:0])** Writing data to this register causes data to be written to Transmitter FIFO. Reading data from this register causes data to be received from Receiver FIFO.

9.10.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is to enable the CIR interrupt request.

Address: Base Address + 1h

Bit	R/W	Default	Description
7	R/W	0b	**Transmitter Data Output Select (TX_sel)** This bit is to select transmitter data output. 0: CIRTX1 (Default) 1: CIRTX2
6	R/W	0b	**Receiver Data Input Select (RX_sel)** This bit is to select receiver data input. 0: CIRRX1 (Default) 1: CIRRX2
5	R/W	0b	**Reset** The function of this bit is software reset. Writing “1” to this bit resets register DR, IER, TCR1, BDLR, BDHR and IIR and then it will be self-cleared to the initial value.
4	R/W	0b	**Baud Rate Register Enable (BR)** This bit is to control whether the baud rate register can enable read/write function or not. 1: Enable 0: Disable
3	R/W	0b	**Interrupt Enable Control (IEC)** This bit is to control whether the interrupt function can be enabled or not. 1: Enable 0: Disable
2	R/W	0b	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is to control Receiver FIFO Overrun Interrupt request. 1: Enable 0: Disable
1	R/W	0b	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in FIFO exceed the FIFO threshold level. 1: Enable 0: Disable
0	R/W	0b	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in FIFO are less than the FIFO threshold Level. 1: Enable 0: Disable

9.10.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is to control the CIR Receiver.

Address: Base Address + 2h

Bit	R/W	Default	Description
7	R/W	0b	**Receiver Data without Sync. (RDWOS)** This bit is to control the sync. logic for received data. Set this bit to “1” to obtain the received data without sync. logic. Set this bit to “0” to obtain the received data with sync. logic.
6	R/W	0b	**High-Speed Carrier Frequency Select (HCFS)** This bit is to select the carrier frequency between the high-speed and low-speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
5	R/W	0b	**Receiver Enable (RXEN)** This bit is to enable the Receiver function. Receiver Enable and RXACT will be activated if the selected carrier frequency is received. 1: Enable 0: Disable
4	R/W	0b	**Receiver Demodulation Enable (RXEND)** This bit is to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to “1” to enable it. 1: Enable 0: Disable
3	R/W	0b	**Receiver Active (RXACT)** This bit is to control the Receiver operation. This bit is set to “0” when the Receiver is inactive. This bit will be set to “1” when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with the correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a “1” to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001b	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are to set the tolerance of the Receiver. For the detailed demodulation carrier frequency, please refer to Table 9-32. Receiver Demodulation Low Frequency (HCFS = 0) and Table 9-33. Receiver Demodulation High Frequency (HCFS = 1) on page 174 and 175.

9.10.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base Address + 3h

Bit	R/W	Default	Description
7	R/W	0b	**FIFO Clear (FIFOCLR)** Writing a "1" to this bit clears FIFO. This bit is then self-cleared to "0".
6	R/W	0b	**Internal Loopback Enable (ILE)** This bit is to execute internal loopback for test and must be "0" in normal operation. 1: Enable 0: Disable
5-4	R/W	0b	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO threshold level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in the internal loopback mode (ILE = 1). **16-Byte Mode** / **32-Byte Mode** 00: 1 / 1 (Default) 01: 3 / 7 10: 7 / 17 11: 13 / 25
3	R/W	0b	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bit 6-0. 1: Enable 0: Disable
2	R/W	0b	**Transmitter Deferral (TXENDF)** This bit is to avoid Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be kept until the transmitter time-out condition occurs, or FIFO reaches full.
1-0	R/W	0b	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are to define the Transmitter modulation pulse mode. **TXMPM[1:0] Modulation Pulse Mode** C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit period. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6_pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved.

9.10.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is to determine the carrier frequency.

Address: Base Address + 4h

Bit	R/W	Default	Description
7-3	R/W	01011b	**Carrier Frequency (CFQ[4:0])** These five bits are to determine the modulation carrier frequency. Please refer to the following table.
2-0	R/W	100b	**Transmitter Modulation Pulse Width (TXMPW[2:0])** These three bits are to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the setting of the carrier frequency and the selection of Transmitter Modulation pulse width.

TXMPW[2:0]	HCFS = 0	HCFS = 1
000	Reserved	Reserved
001	Reserved	Reserved
010	6 μs	0.7 μs
011	7 μs	0.8 μs
100	**8.7 μs**	**0.9 μs (Default)**
101	10.6 μs	1.0 μs
110	13.3 μs	1.16 μs
111	Reserved	Reserved

Table 9-31. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (default)**	**480 kHz (default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-32. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.2.15	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.2.15	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-33. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.10.6.6 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base Address + 5h

Bit	R/W	Default	Description
7-6	R	-	**Reserved**
5-0	R	000000b	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in the Transmitter FIFO.

9.10.6.7 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base Address + 6h

Bit	R/W	Default	Description
7	R	0b	**Receiver FIFO Time-out (RXFTO)** This bit will be set to "1" when a Receiver FIFO time-out condition occurs. Followings are the conditions required for the occurrence of Receiver FIFO time-out: 1. At least one byte of data are queued in the Receiver FIFO for more than 64 ms. 2. The Receiver has been inactive (RXACT=0) for more than 64 ms.
6	-	-	**Reserved**
5-0	R	000000b	**Receiver FIFO Byte Count (RXFBC)** Return the number of bytes left in Receiver FIFO.

9.10.6.8 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is to program the CIR Baud Rate clock.

Address: Base Address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BDLR[7:0])** These bits, for dividing the Baud Rate clock, are the low byte of the register.

9.10.6.9 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BDHR[7:0])** These bits, for dividing the Baud Rate clock, are the high byte of the register.

Baud rate divisor = 115200 / baud rate
Ex1: 2400 bps → 115200 /2400 = 48 → 48(d) = 0030(h) → BDHR = 00h, BDLR = 30h
Ex2: bit width = 0.565 ms (1770 bps (115200 / 1770 = 65(d) = 0041(h) (BDHR = 00(h), BDLR = 41(h)

9.10.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit register, is to identify the pending interrupt.

Address: Base address + 7h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-1	R	00b	**Interrupt Identification** These two bits are to identify the source of the pending interrupt. **IIR[1:0] Interrupt Source** 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	**Interrupt Pending** This bit will be set to “1” while an interrupt is pending.

10. DC Electrical Characteristics

Operating Conditions

3VSB/SYS_3VSB/AVCC3 .....3.3V ± 0.15V

VBAT..... 2.3V to 3.0V

Operation Temperature (Topt).....0°C to +70°C

Absolute Maximum Ratings*

Applied Voltage..... -0.3V to 3.6V

Input Voltage (Vi)..... -0.3V to VCC3 + 0.3V

Output Voltage (Vo)..... -0.3V to VCC3 + 0.3V

Operation Temperature (Topt).....0°C to +70°C

Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics(VCC3=3.3V±5%, Ta=0°C~70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DO8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
DOD8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
DIO8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0			10	µA
I_{IH}	High Input Leakage	V_{IN} = VCC3			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0			10	µA
I_{IH}	High Input Leakage	V_{IN} = VCC3			-10	µA
I_{OZ}	3-state Leakage				20	µA

DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DIO16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0			10	µA
I_{IH}	High Input Leakage	V_{IN} = VCC3			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0			10	µA
I_{IH}	High Input Leakage	V_{IN} = VCC3			-10	µA
I_{OZ}	3-state Leakage				20	µA
DO24L Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
DIO24 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0			10	µA
I_{IH}	High Input Leakage	V_{IN} = VCC3			-10	µA
I_{OZ}	3-state Leakage				20	µA
DI Type Buffer						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
V_{IH}	High Input Voltage(clock)		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0				µA
I_{IH}	High Input Leakage	V_{IN} = VCC3				µA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AI Type Buffer for AMD CPU power sequence function						
V_{trig}	Trigger point for VCORE(1.1V)	VREF=2.8V	-	1.0	-	V
V_{hyst}	Hysteresis for VCORE(1.1V)		-	100	-	mV
V_{trig}	Trigger point for VDIMM_STR	VREF=2.8V	-	1.35V	-	V
V_{hyst}	Hysteresis for VDIMM_STR		-	130	-	mV
V_{trig}	Trigger point for VLDT_12	VREF=2.8V	-	1.0	-	V
V_{hyst}	Hysteresis for VLDT_12		-	100	-	mV

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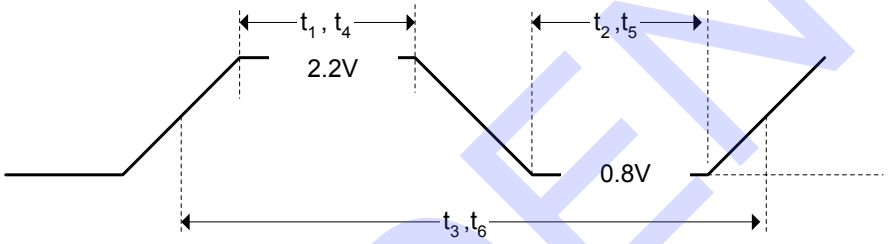
11. AC Characteristics

11.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz [1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz [1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz [1]	40			nsec

Not tested. Guaranteed by design.

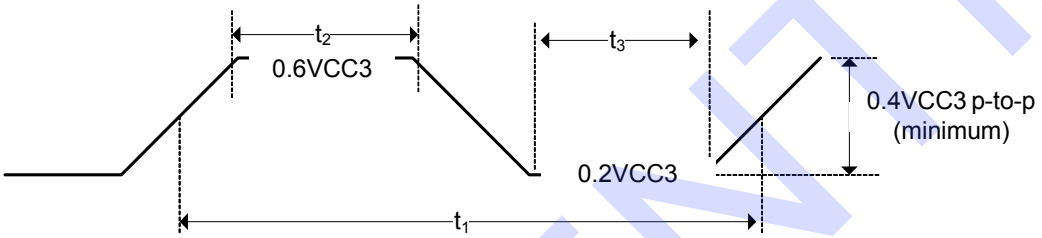
Figure 11-1. Clock Input Timings



11.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			µsec

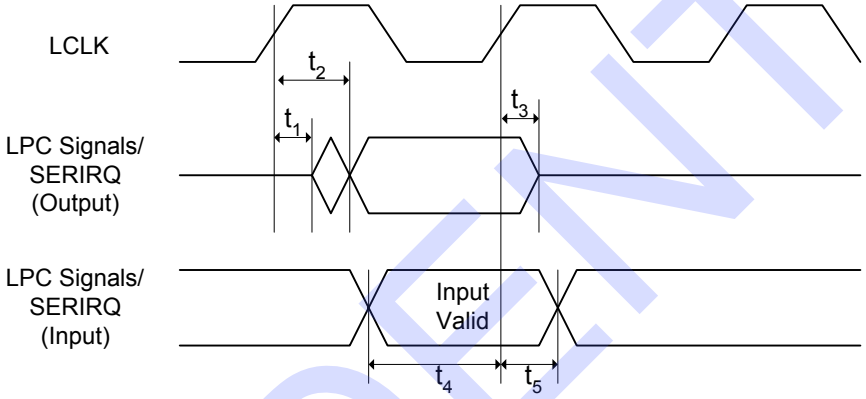
Figure 11-2. LCLK (PCICLK) and LRESET Timings



11.3 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			13	nsec
t_3	Active to Float Delay			20	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

Figure 11-3. LPC and SERIRQ Timings

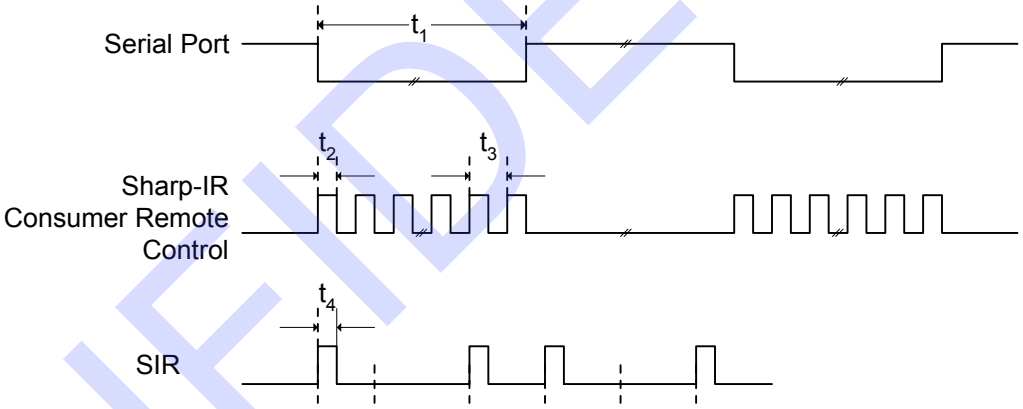


11.4 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in Serial Port and ASKIR	Transmitter	t_{BTN} – 25 Note1	t_{BTN} + 25	nsec
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	nsec
t_2	Modulation Signal Pulse Width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation Signal Period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	2000X(23/24)	2000X(25/24)	nsec
t_4	SIR Signal Pulse Width	Transmitter, Variable	(3/16) x t_{BTN} – 25	(3/16) x t_{BTN} + 25	nsec
		Transmitter, Fixed	1.48	1.78	µsec
		Receiver	1		µsec

Note 1: t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Divisor registers.

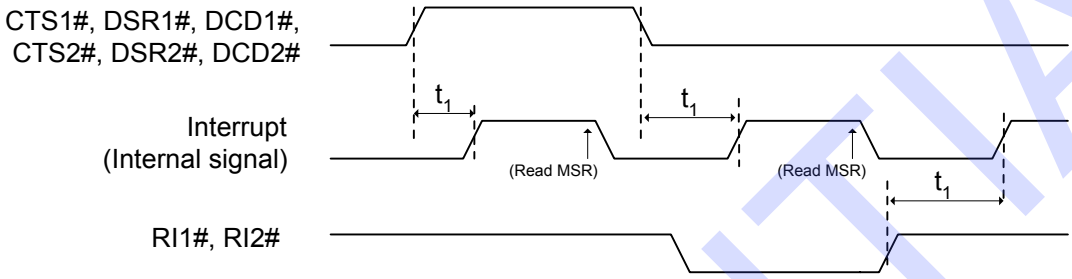
Figure 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings



11.5 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

Figure 11-5. Modem Control Timings



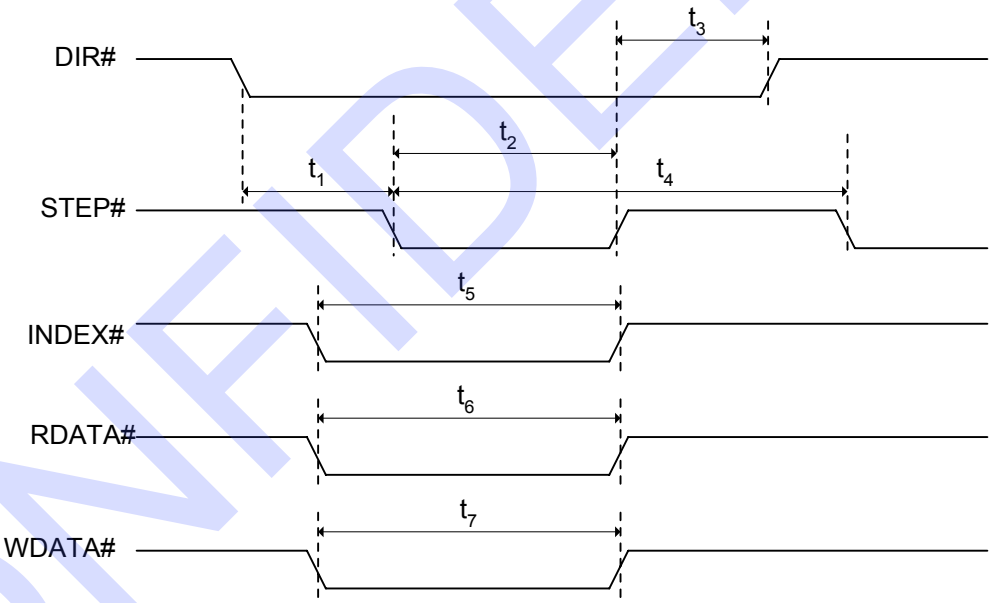
11.6 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} Note1		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} Note2		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. t_{mclk} =8M/ 4M/ 2.4M/ 2M for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.

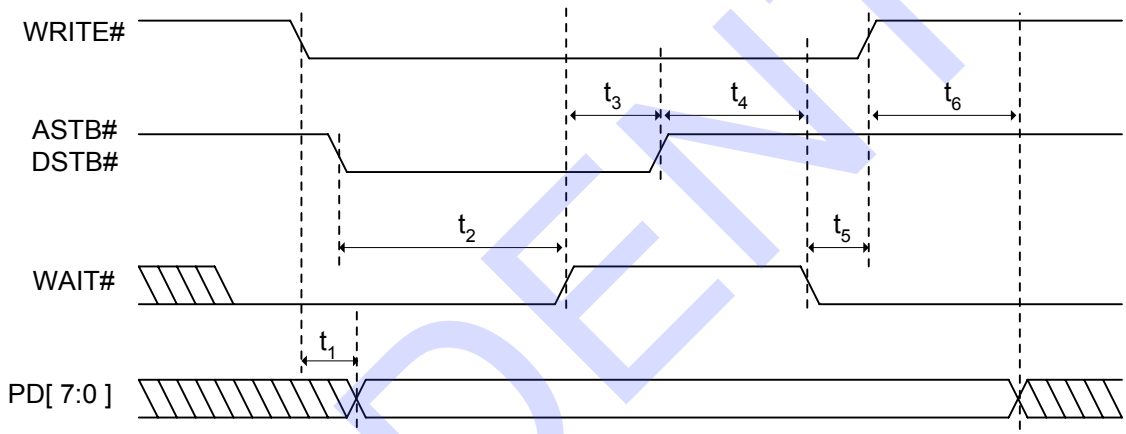
Figure 11-6. Floppy Disk Drive Timings



11.7 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec

Figure 11-7. EPP Address or Data Write Cycle Timings

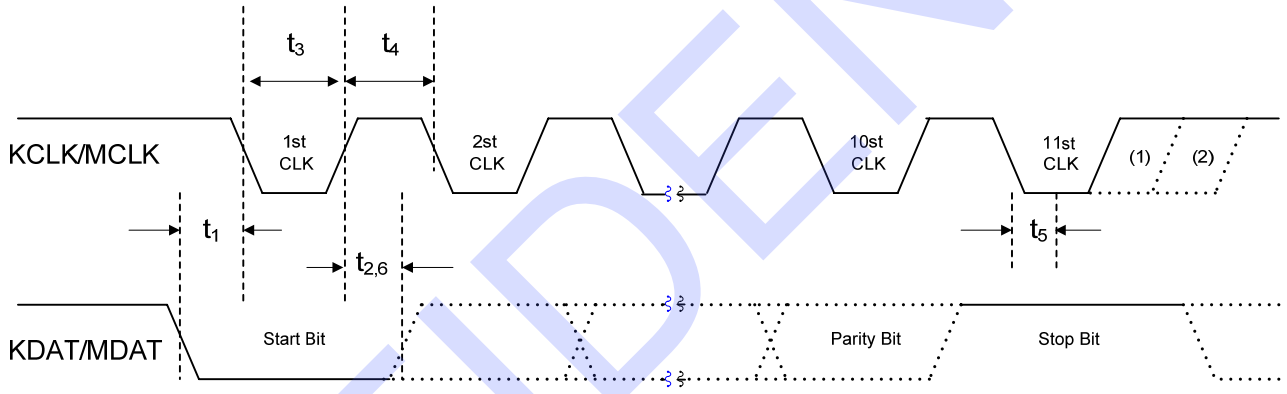


11.8 Keyboard/Mouse Receive/Send Data Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Time form DATA transition to falling edge of CLK (Receive)	5		25	µsec
t_2	Time form rising edge of CLK to DATA transition (Receive)	5		T4-5	µsec
t_3	Duration of CLK inactive (Receive/Send)	30		50	µsec
t_4	Duration of CLK active (Receive/Send)	30		50	µsec
t_5	Time to keyboard inhibit after clock 11 to ensure the keyboard device does not start another transmission (Receive)	>0	50		µsec
t_6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

Note: (1) The system can hold the 'clock' signal inactive to inhibit the next transmission.
(2) The system raises the 'clock' line to allow the next transmission.

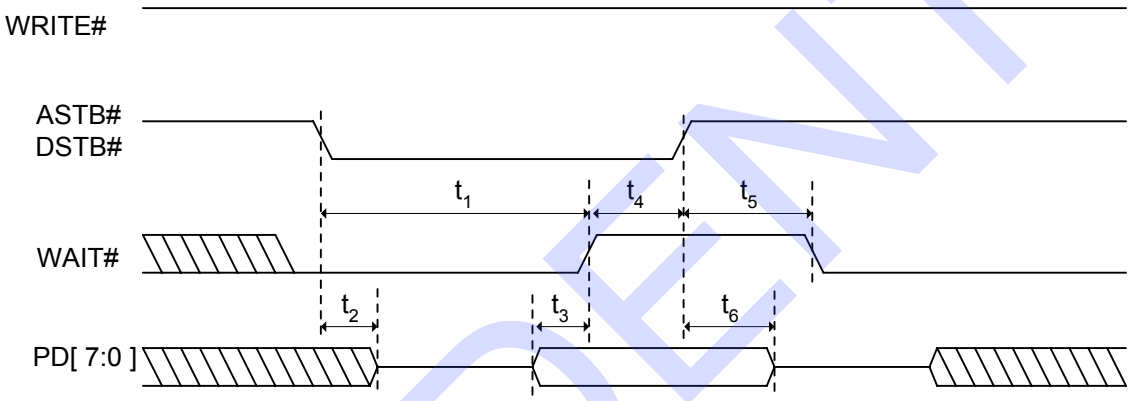
Figure 11-8. Keyboard/Mouse Receive/Send Data Timings



11.9 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

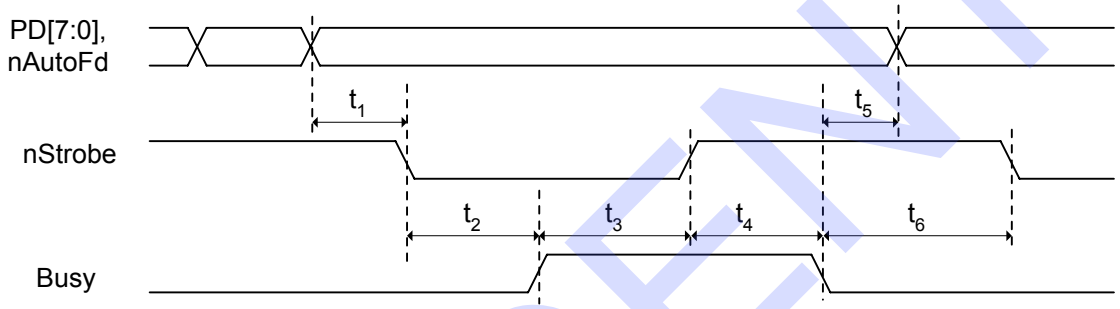
Figure 11-9. EPP Address or Data Read Cycle Timings



11.10 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

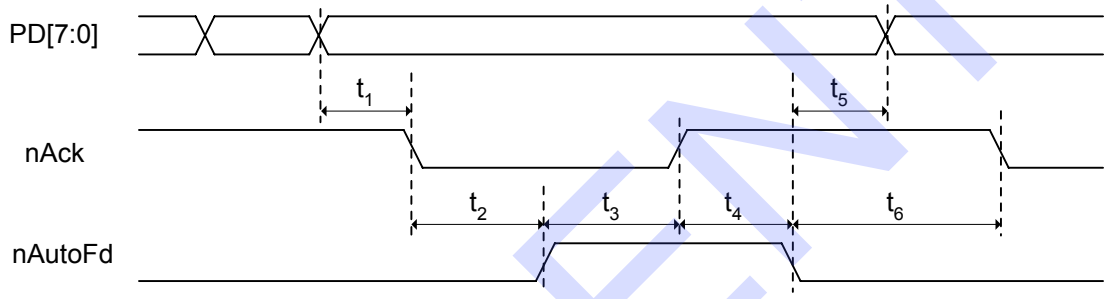
Figure 11-10. ECP Parallel Port Forward Timings



11.11 ECP Parallel Port Backward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

Figure 11-11. ECP Parallel Port Backward Timings



11.12 RSMRST# and ACPI Power Control Signal Timings

Symbol	Parameter	Typ.	Unit
t_1	RSMRST# de-actives delay from 3VSB=3V	75	msec
$t_{2*Note1}$	PWRGD3 active delay from 0.8 * AVCC3	Reference: Section 11.13	msec
t_3	Overlap of PSON# and 3VSBSW#	10	msec
t_4	Delay time of 3VSBSW# falling edge to PWRGD3 falling edge	<1	msec
t_5	Delay time of 3VSBSW# rising edge to PWRGD3 rising edge	1 Note:2A<Bit 0>=0 (Default)	usec
$t_{5'}$		135 Note:2A<Bit 0>=1	msec

Figure 11-12. RSMRST# Timings

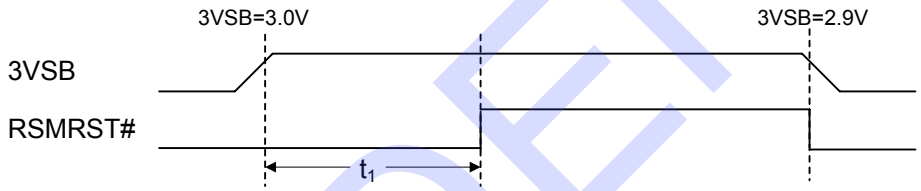


Figure 11-13. PWRGD3 Timings

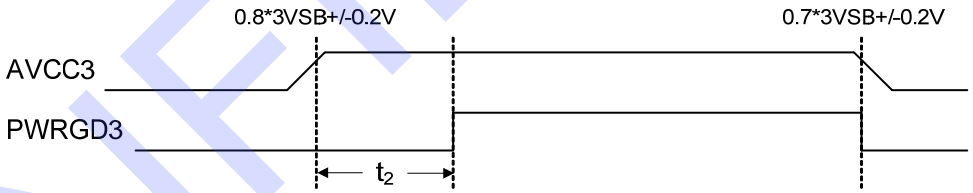
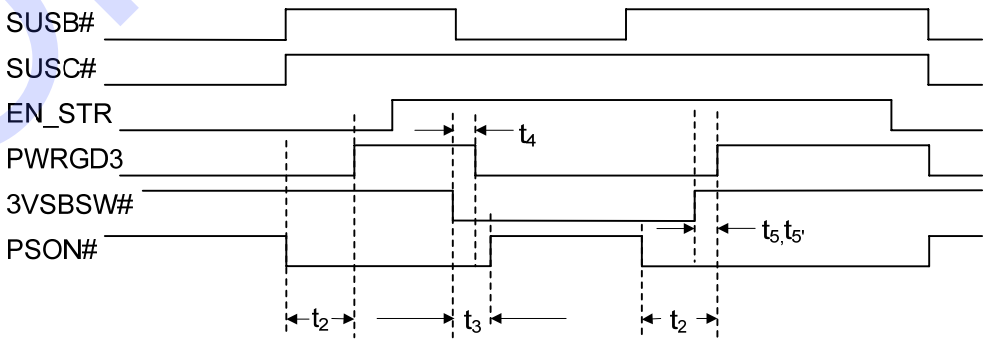


Figure 11-14. ACPI Power Signal Timings



11.13 PWRGD1, PWRGD2, PWRGD3 Signal Timings

Symbol	Parameter	Min.	Typ.	Max.
t_6	Delay time of (3V/5V/12V reach 80% detected AND SUSB#) to internal_GD.		<1ms	
t_7	Delay time of internal_GD to PWRGD1 rising edge	30ms	33ms	36ms
t_8	Delay time of internal_GD to PWRGD2 rising edge	50ms	55ms	60ms
t_9	Delay time of internal_GD to PWRGD3 rising edge	150ms	165ms	180ms
t_{10}	Delay time of SUSB# falling edge to PWRGD falling edge		< 1ms.	

Figure 11-15. PWRGD1/2/3 Signal Condition

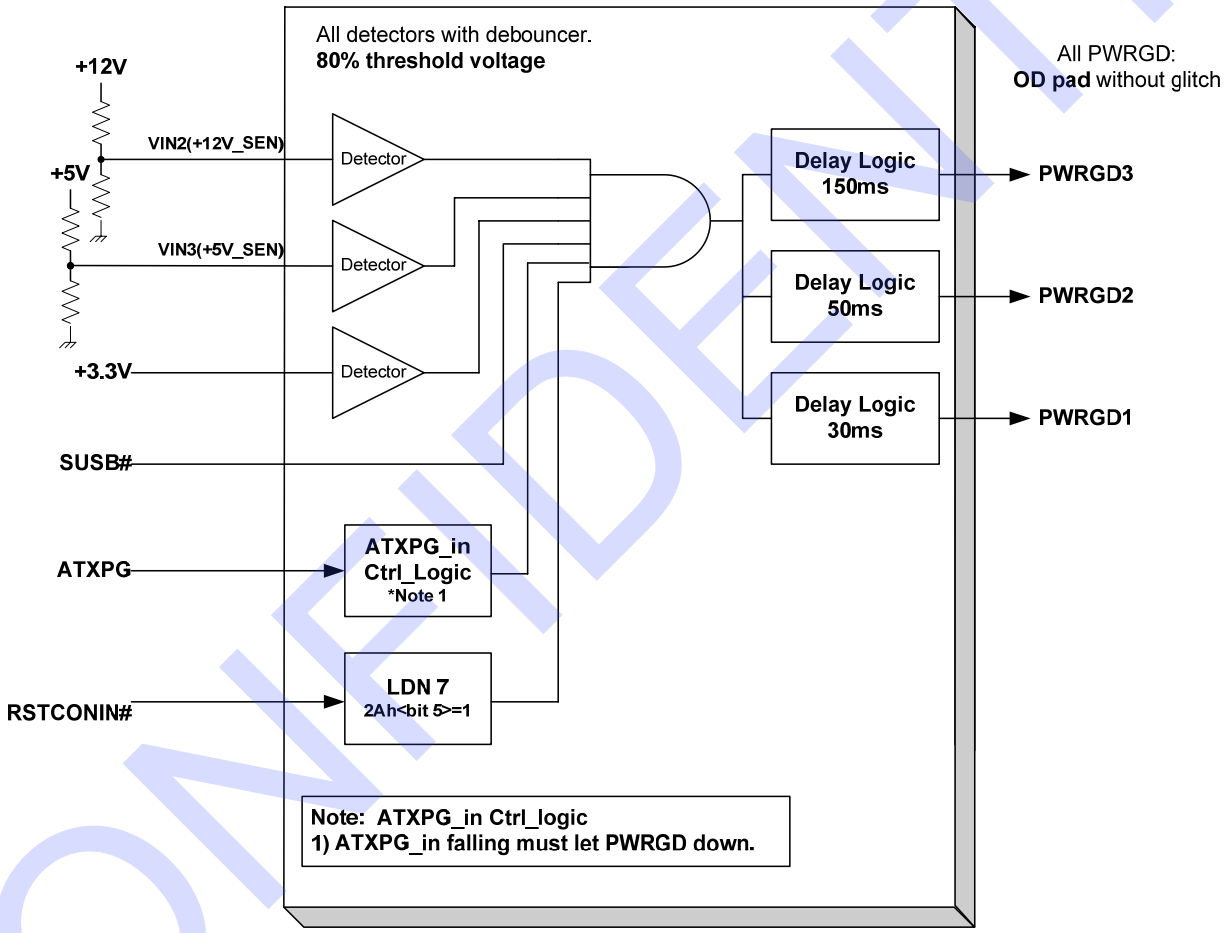
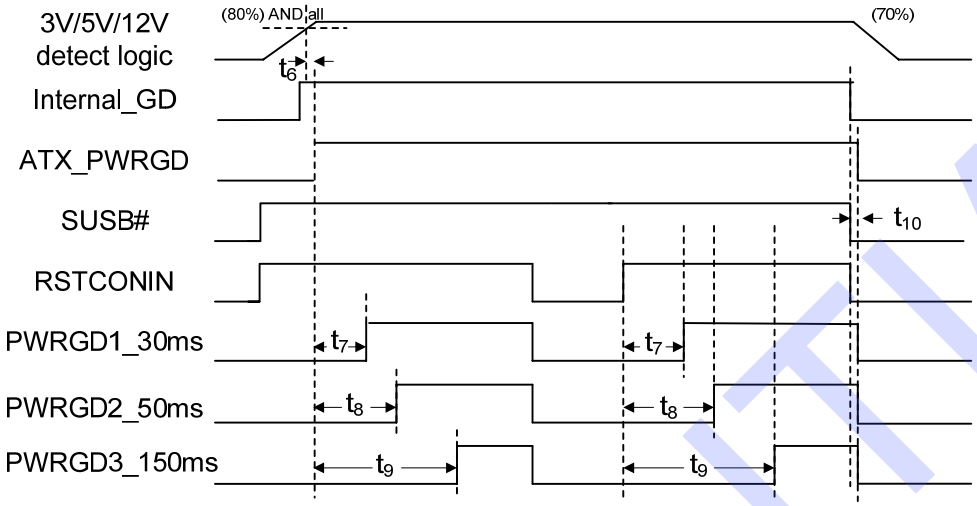
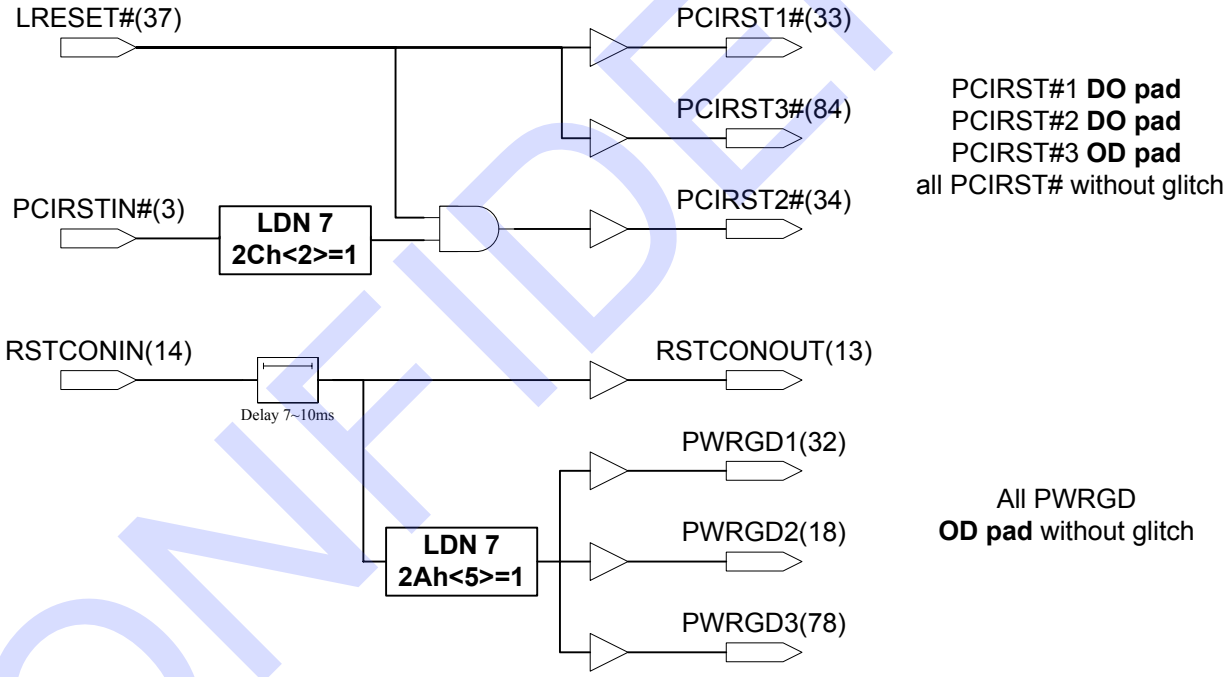


Figure 11-16. PWRGD1/2/3 Signal Timings



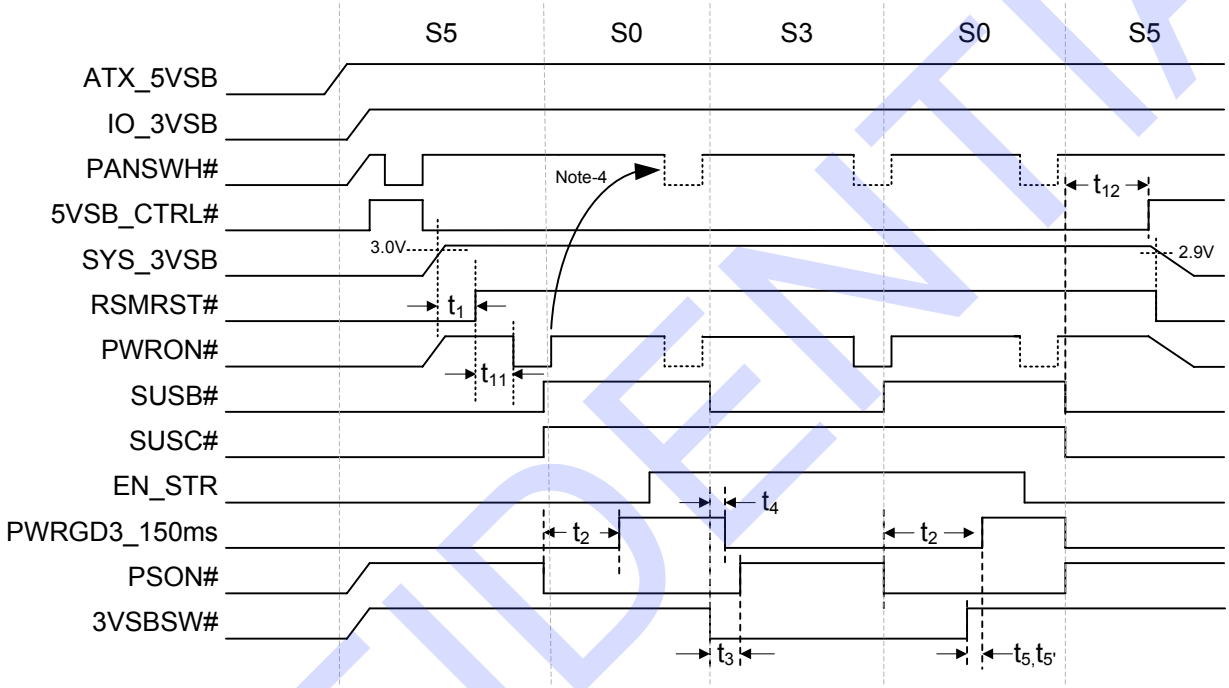
11.14 PCIRST#1, PCIRST#2 and PCIRST#3 Signal Timings



11.15 Energy-using Product (EuP) Power Control Signal Timings

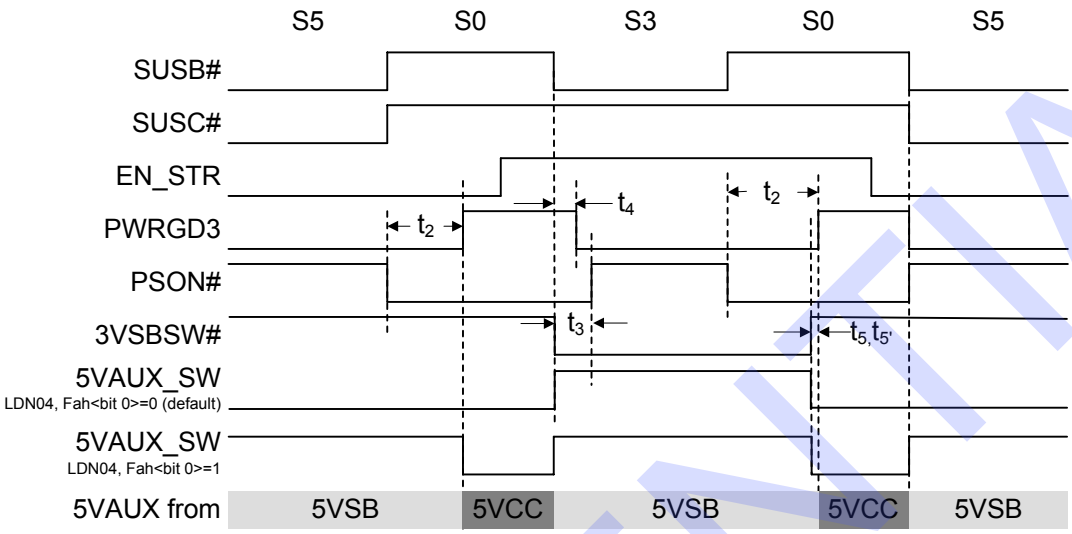
Symbol	Parameter	Min.	Typ.	Max.
t_{11}	Delay time of RSMRST# rising to first PWRON# pulse.	-	200ms	-
t_{12}	Delay time of AVCC3 falling edge to 5VSB_CTRL# rising edge.	-	4.6s	-

Figure 11-17. EuP Function Signal Timings



11.16 5VAUX_SW Power Control Signal Timings

Figure 11-18. 5VAUX_SW Signal Timings



11.17 AMD K8 Power Sequence

Figure 11-19. AMD K8 Power Sequence Timings

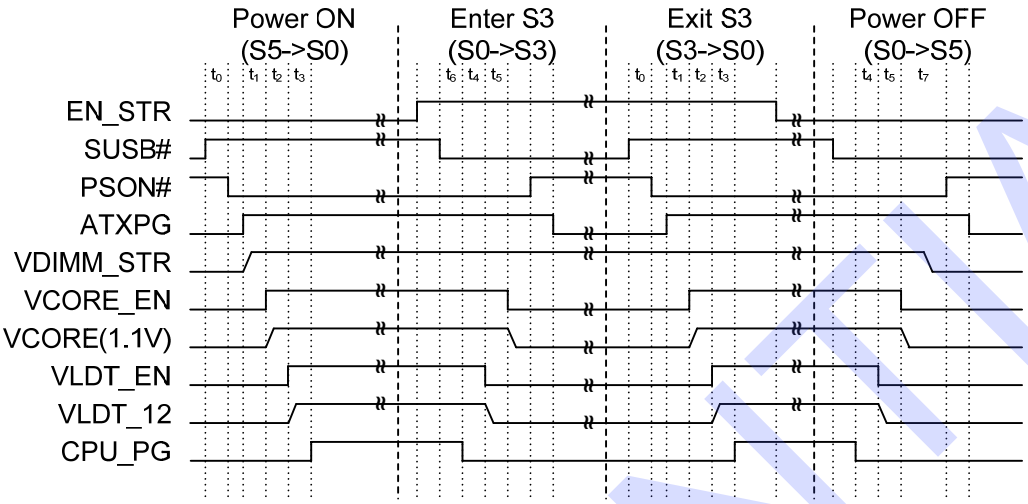


Table 11-1. Power Sequence AC Timing Parameter

Symbol	Typ.	Description
t_0	1.5ms	The rising edge of SUSB# to the assertion of PSON#.
t_1	2ms + t_vdimm_gd	Both ATXPG & VDIMM_STR ready to the rising edge of VCORE_EN. The t_vdimm_gd is the rise time of the VDIMM_STR voltage from 0V to 1.35V.
t_2	50us + t_vcore_gd	The rising edge of VCORE_EN to the rising edge of VLDT_EN. The t_vcore_gd is the rise time of the VCORE(1.1V) voltage from 0V to 1.0V.
t_3	2ms + t_vldt_gd	The rising edge of VLDT_EN to the rising of CPU_PG. The t_vldt_gd is the rise time of the VLDT voltage from 0V to 1.0V.
t_4	50us	The de-assertion of CPU_PG to the de-assertion of VLDT_EN.
t_5	10ms	The de-assertion of VLDT_EN to the de-assertion of VCORE_EN.
t_6	1.5ms	The falling edge of SUSB# to the de-assertion of CPU_PG.
t_7	210ms	The falling edge of VCORE(1.1V) to the rising edge of PSON#

11.18 DSW Timings

Figure 11-20. DPWORK Timings

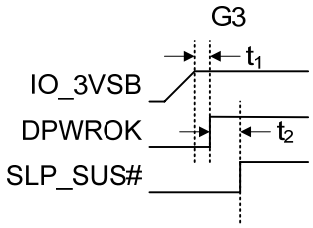


Figure 11-21. DSW Timings

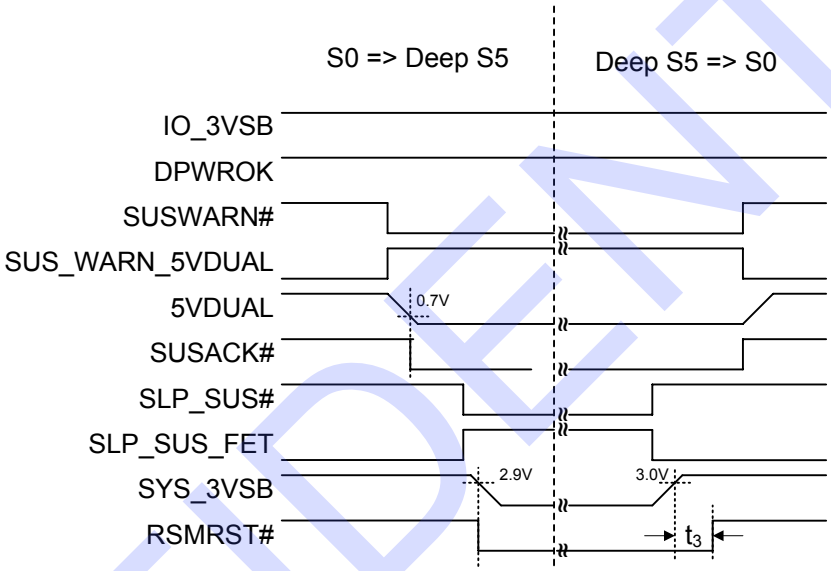


Table 11-2. DSW Timings Parameter

Symbol	Typ.	Description
t_1	26ms	The rising edge of IO_3VSB to rising edge of DPWORK
t_2	by SB	The rising edge of IO_3VSB to rising edge of SLP_SUS#
t_3	75ms	SYS_3VSB voltage over 3.0V to the rising edge of RSMRST#

11.19 UVP/OVP Timings

Table 11-3. UVP/OVP Timings Parameter

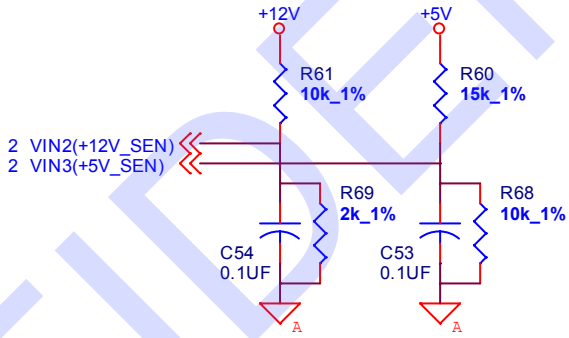
Symbol	Typ.	Description
t_2	LND4\F9h<4-3> 00: 0.5s 01: 1s (default) 10: 2s 11: 4s	PSON# Pull-up Time for Notice Mode

Table 11-4. UVP/OVP Detecting Voltage Threshold

Detected PIN	+12V_SEN(VIN2)		+5V_SEN(VIN3)		+3.3V_SEN(AVCC3)	
UVP/OVP	OVP	UVP	OVP	UVP	OVP	UVP
Threshold	2.40±0.05V	1.49±0.05V	2.40±0.05V	1.45±0.05V	3.90±0.1V	2.40±0.1V

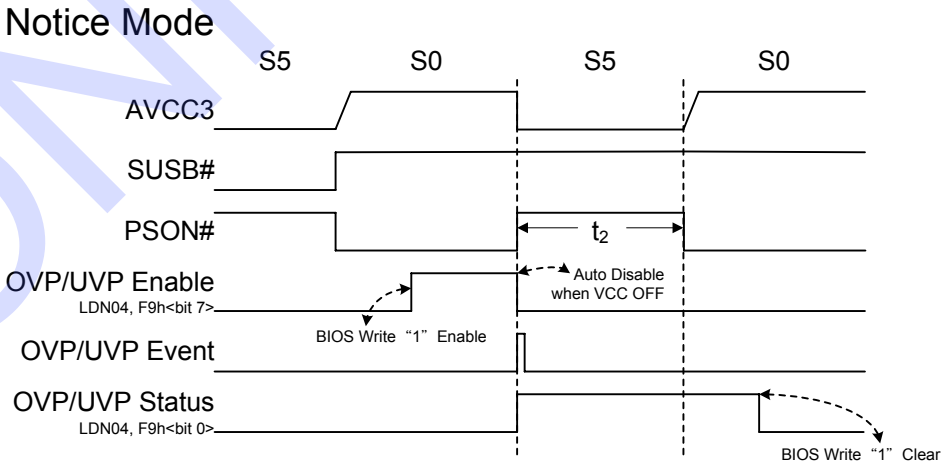
Note: The UVP / OVP voltage range is determined by Figure 11-22. UVP/OVP Application. Changing the resistance value will result in the change of the UVP / OVP voltage range. It is recommended to use the resistance value shown in Figure 11-22. UVP/OVP Application.

Figure 11-22. UVP/OVP Application



11.19.1 Notice Mode

Figure 11-23. UVP/OVP Force Mode Timings



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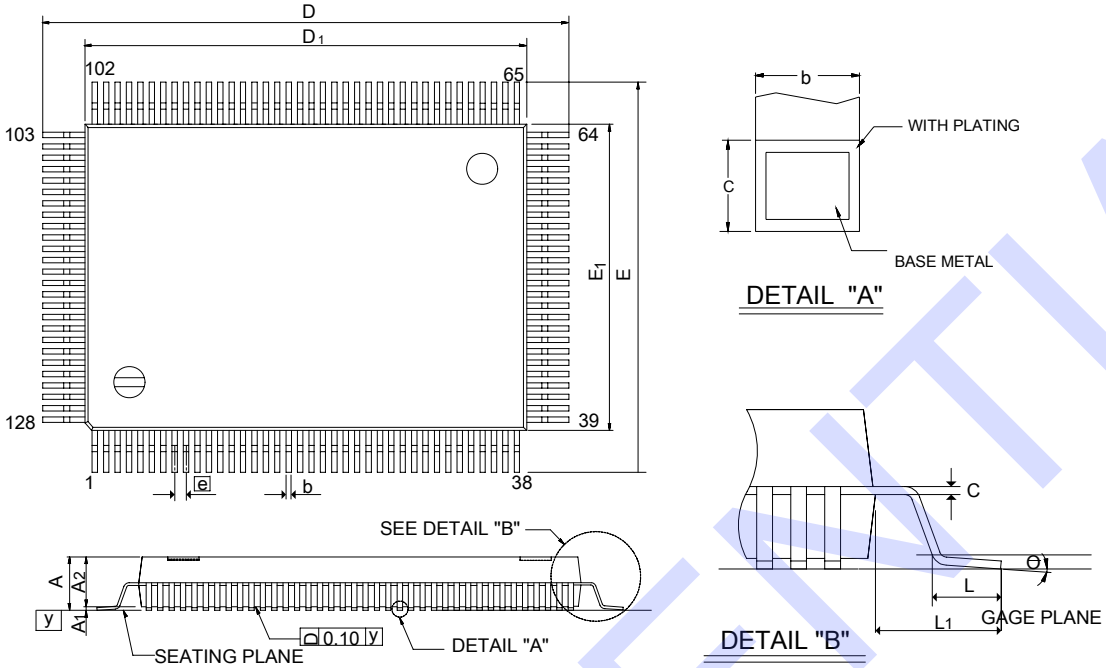
12. Package Information

QFP 128 Outline Dimensions **unit: inches/mm**



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.2.15	-	-
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.2.12	0.2.17
c	0.004	-	0.008	0.09	-	0.2.10
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter

DI-QFP128(14*20)v2

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13. Ordering Information

Part No.	Package
IT8728F	QFP 128

All components provided are RoHS-compliant (100% Green Available).

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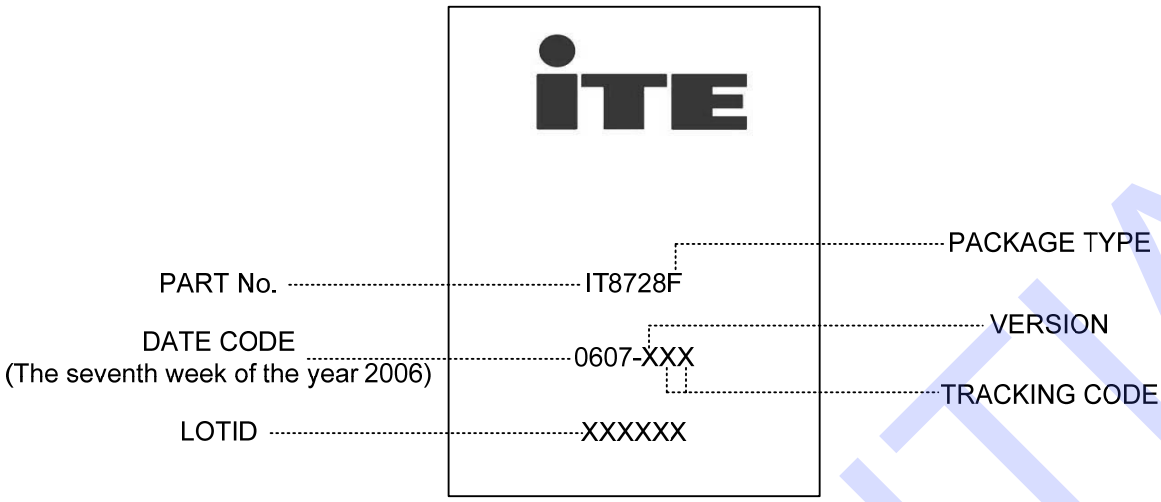
14. Top Marking Information



*PACKAGE TYPE :

E:	LQFP
F:	QFP
FN:	QFN
R:	SSOP

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.
Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.