AMBA AHB SLAVE CIRCUIT

- split transfer implemented

TEAM 7:

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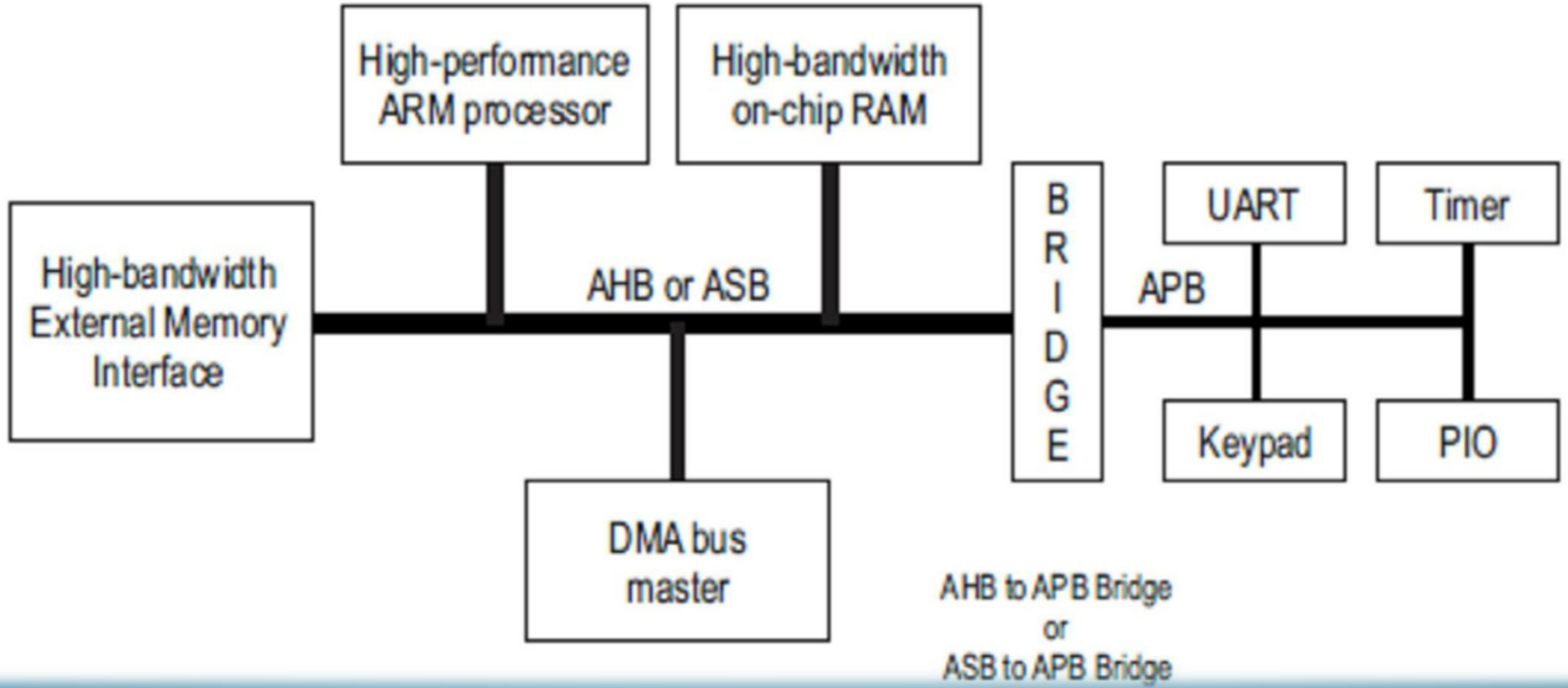
AMBA(Advanced microcontroller bus architecture)

- On-chip bus in system on-a-chip devices (SOC)
  - SOC: integrated circuit(**IC**) that integrates all components of a computer or other electronic system into a single chip.
- Introduced by ARM Ltd in 1996
- Widely used on applications processors used in modern portable mobile devices.
- AMBA buses:
  1. ASB(Advanced System Bus)
  2. APB(Advanced Peripheral Bus)
  3. ATB(Advanced Trace Bus)
  4. AHB(Advanced High-performance Bus)

AMBA AHB

- Implements features for high performance and high frequency systems:

1. Burst transfers
2. Split transactions
3. Pipelined Operation
4. Single-clock edge operation
5. Non-tristate implementation
6. Single-cycle bus master handover
7. Wider data bus configurations (64/128 bits)
8. Multiple master multiple slave handling capability

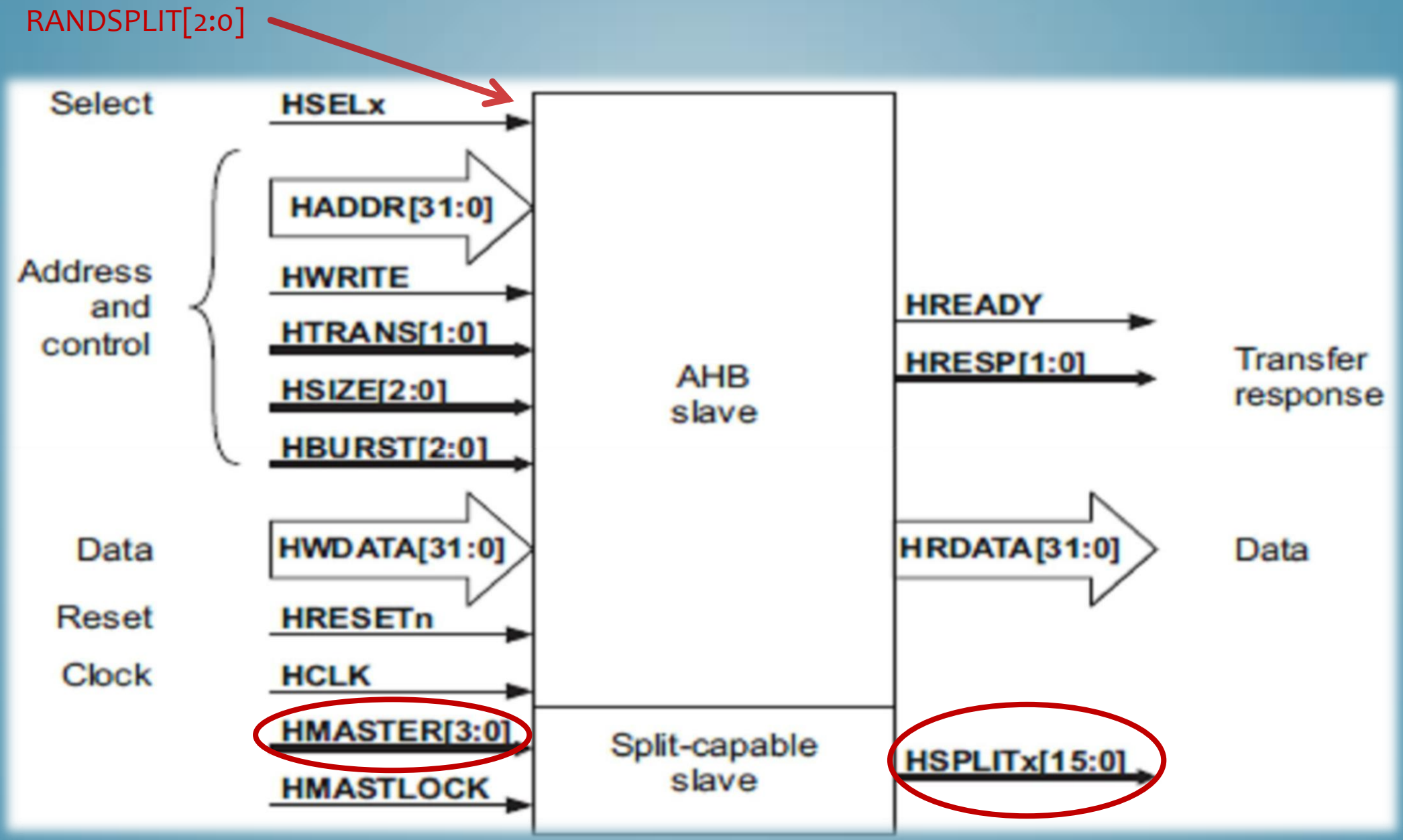

High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth External Memory Interface
AHB or ASB
B R I D G E
APB
UART
Timer
Keypad
PIO
DMA bus master
AHB to APB Bridge
or
ASB to APB Bridge

AHB COMPONENTS

- *Master*
- *Slave*
- *Arbiter*

  Arbiter determines which request will be served first, from a total of asynchronous requests that arrive.

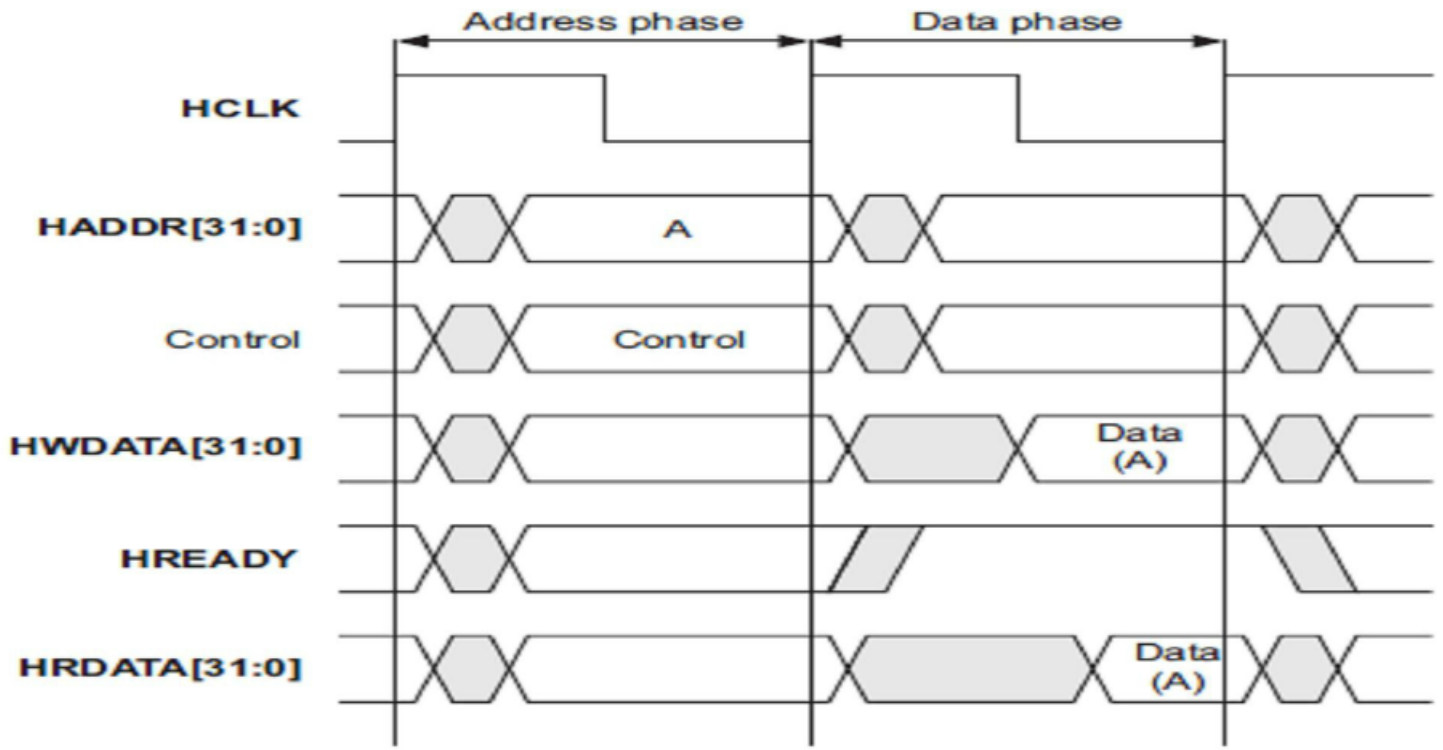
- *Decoder*



RANDSPLIT[2:0]: First bit indicates whether or not split will be used, and the rest 2 bits the wait states.

Single Read/Write

- Master Drives Address & Control signals after rising edge of HCLK.
- Slave Samples the Address & Control information on the next rising edge of the HCLK.
- Then slave drives the appropriate response.
- This is sampled by master on the third rising edge of the clock.



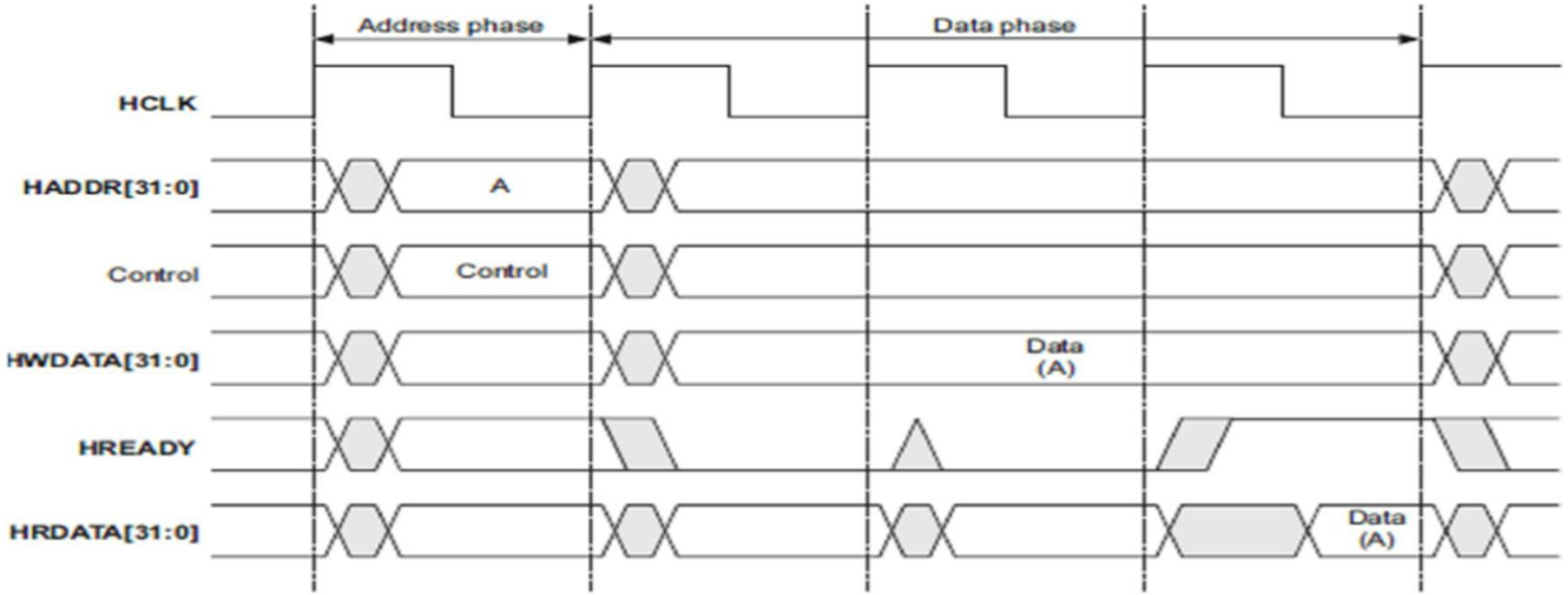
SPLIT IMPLEMENTATION:

- In the current implementation, split usage will be defined by the first bit of RANDSPLIT[2:0]. (If 1 -> enable split)

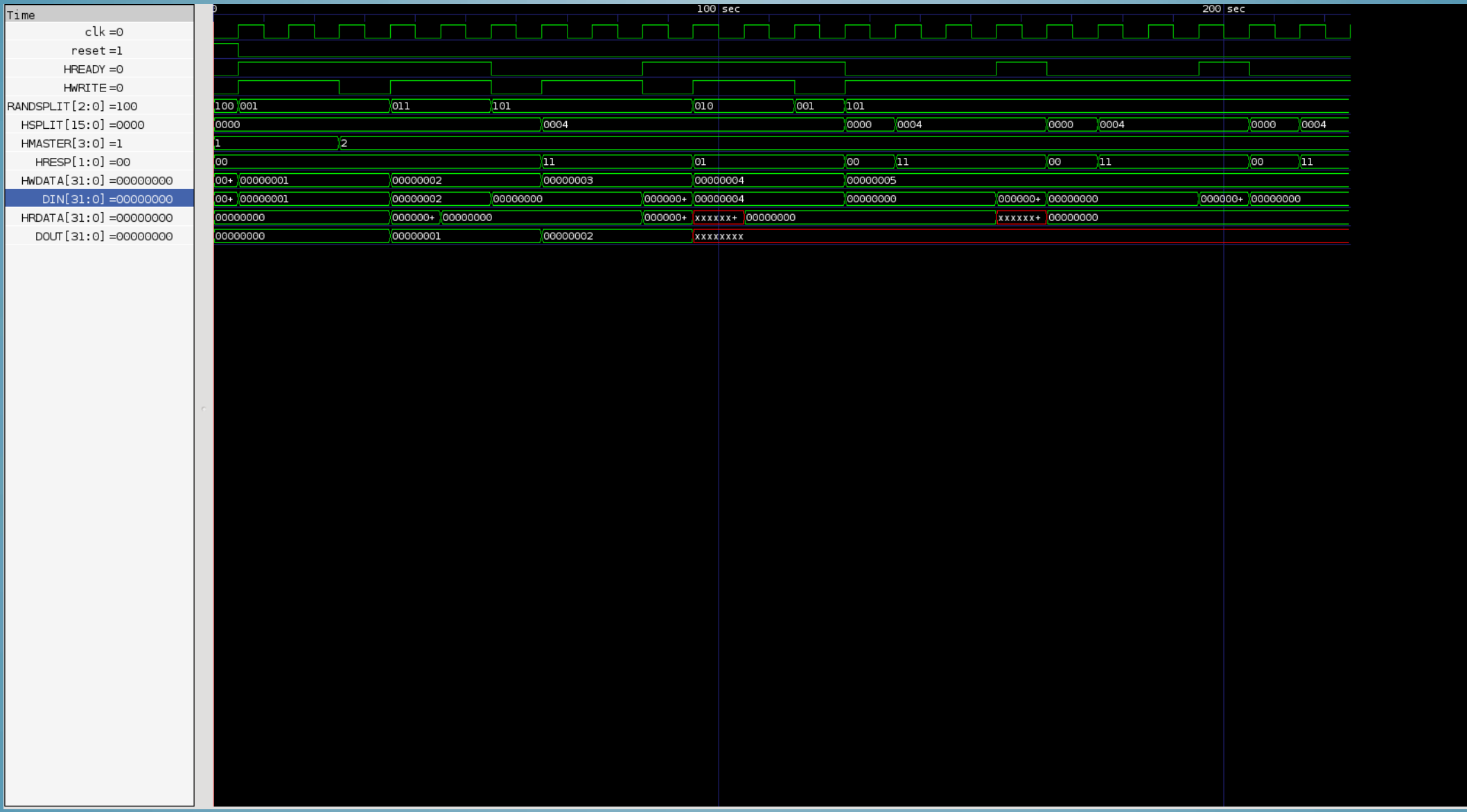
- When split is enabled, in order to free the bus, HREADY is driven low until the current transaction is finished. HRESP is also changed to value 11 (SPLIT answer).

Transfer with wait states

- For Write Operations bus master will hold the data stable throughout the extended cycles.
- For read transfers the slave does not have to provide valid data untill the transfer is about to complete

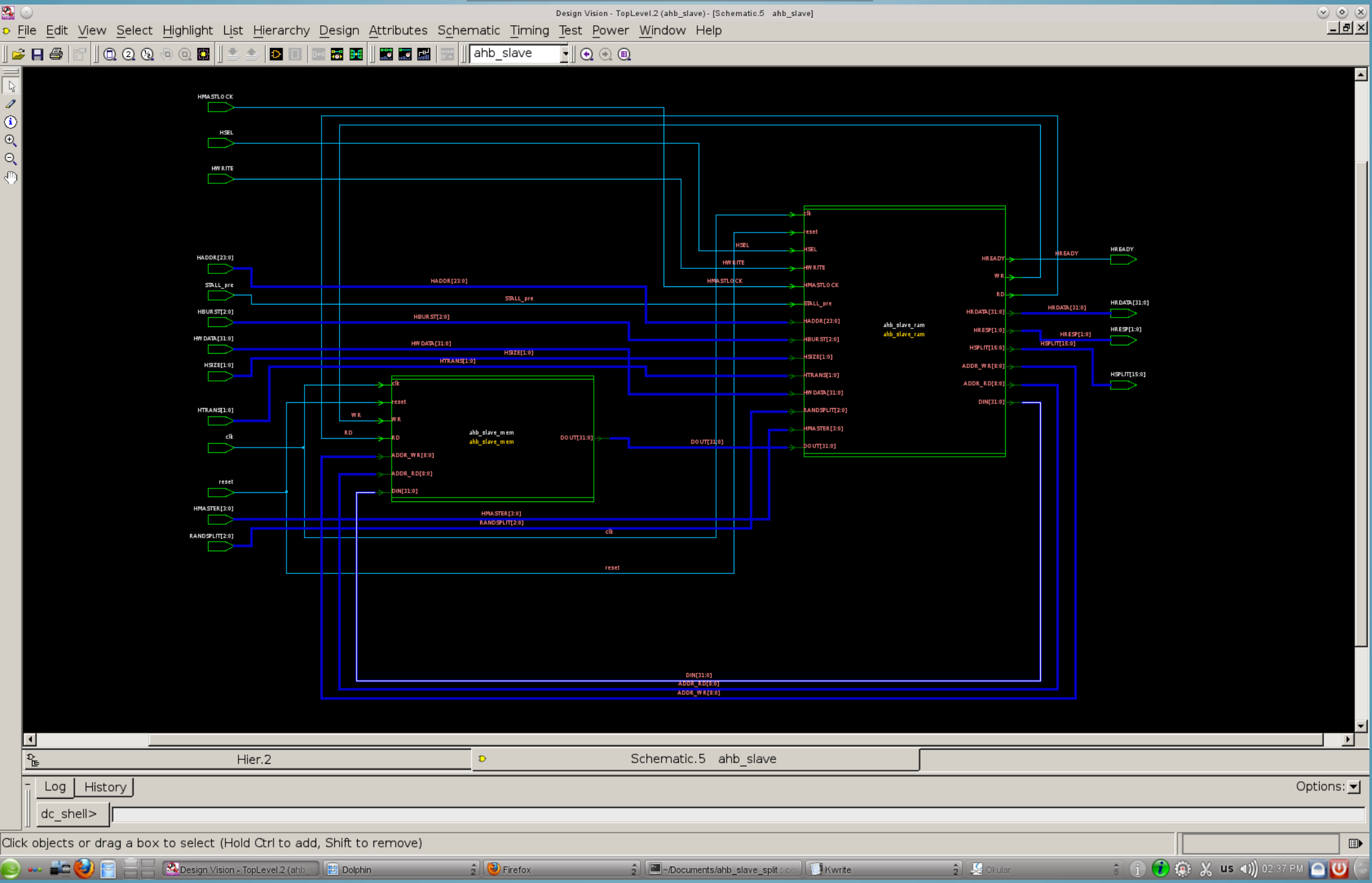


WAVEFORM:



- VCD file: Testsplit.vcd

SYNOPSYS DC RUN:



SYNOPSYS DC RESULTS:

- Clean compilation.
- Best clk period: 4ns.
- Total slack = 0.01ns.
- Complete timing report -> timing.rep
- Complete power report -> power.rep
- Complete cell report -> cell.rep
- Output netlist -> netlist.v

CADENCE ENCOUNTER:

- Had problem loading the design after working on it and save it.
- Save file -> ahb_slave.enc