21VL611 – CMOS DIGITAL INTEGRATED CIRCUITS

TERM WORK PROJECT

ON

OPTIMIZATION OF LEAKAGE POWER DISSIPATION IN CMOS INVERTER USING SELF BIASED AND W/L SCALING TECHNIQUES

By

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Abstract

With the advancement of wireless technology, minimizing power dissipation in VLSI circuits, especially CMOS inverters, has become a priority. CMOS inverters are fundamental in digital circuits and significantly impact power efficiency. This project explores techniques to reduce leakage power in CMOS inverters through self-biasing, W/L scaling, and stacking, using LTSpice simulations for evaluation. The baseline analysis of a conventional CMOS inverter showed leakage power around 50 pW for both NMOS and PMOS, with short-circuit power at 4.16 mW. The substrate-biased CMOS inverter, where body terminals are connected to positive and negative voltages, reduced leakage power to 21.93 pW (NMOS) and 30.04 pW (PMOS) and short-circuit power to 4.11 mW, though it introduced a small delay. A third approach, the stacking-biased CMOS inverter, split the NMOS and PMOS transistors, reducing leakage power significantly to 3.92 pW (NMOS) and 575.43 fW (PMOS), with short-circuit power reduced to 60.7 µW. However, this approach caused a higher delay due to increased circuit resistance and slower switching times.

This study reveals a key trade-off: as power dissipation decreases, delay tends to increase. The delay is influenced by factors like increased threshold voltage and reduced simultaneous conduction. This work contributes to understanding power-delay optimization in CMOS design, providing guidance for developing energy-efficient digital circuits in applications requiring low power and balanced performance. The findings support future advances in low-power VLSI design, aligning with sustainable technology goals.

1. INTRODUCTION

The ongoing growth of wireless technologies, which need a finite supply of power, has increased the demand for low power VLSI circuits. In modern digital circuits, power dissipation is becoming a significant problem. Therefore, the primary goal of VLSI designers is to minimise power consumption.In fact the inverter serves as the foundation of all digital designs. developing more complex CMOS structures after its function and features are thoroughly understood. A major challenge in the creation of high performance integrated circuits is the generation, distribution, and dissipation of power. In paper [1] Author presents a number of low power and high speed integrated circuit design strategies such as substrate biasing. This techniques is used for reducing device power consumption without compromising speed of the device.The development of semiconductor technology is mostly constrained by power consumption. In order to create power reduction approaches at the circuit architecture. It is essential to identify the causes of power consumption. With the help of LTSpice Simulation, we are identifying how much leakage power and how much short circuit power is flowing through the Inverter and putting the technique to reduce these power dissipations.

2. LTSPICE ANALYSIS

In this section, we are going to implement 4 variants of CMOS Inverters to compare the power dissipation with respect to each circuit.

2.1 CONVENTIONAL CMOS INVERTER

In Conventional CMOS INVERTER, NMOS transistor's body is always connected to ground, while PMOS transistor's body is always connected to power supply V_{DD} as shown in below figure.

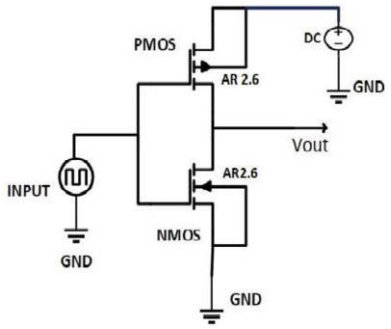

Fig 2.1.1 CONVENTIONAL CMOS INVERTER

We have implemented the above circuit in LTSpice Simulator which is shown below.

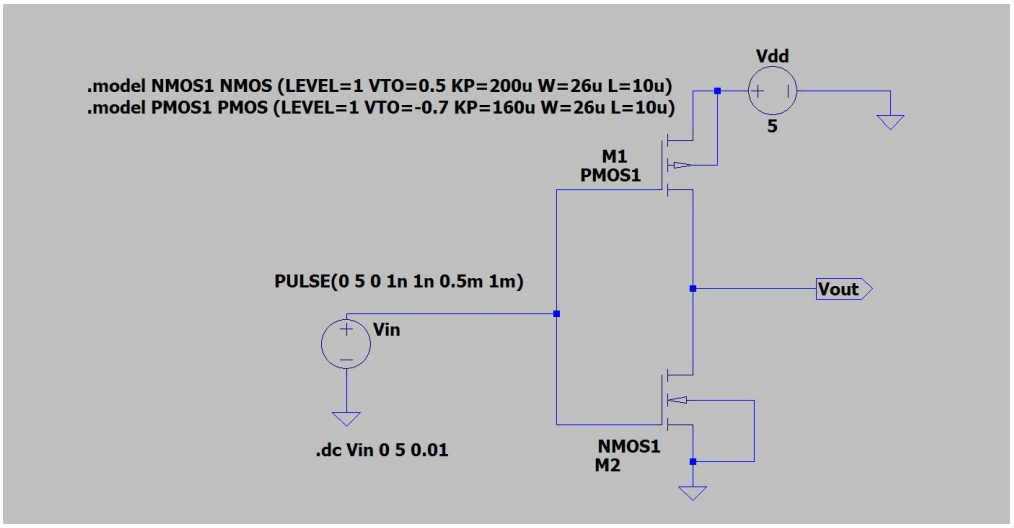

Fig 2.1.2 CMOS INVERTER USING LTSPICE

In LTSpice, we have defined MOS parameters like aspect ratio (W/L), process transconductance parameter of both PMOS and NMOS(Kn') and threshold voltage of PMOS and NMOS (VT0).

We have given input Square pulse of duty cycle 50%, period of 1ms whose transient response is shown below.

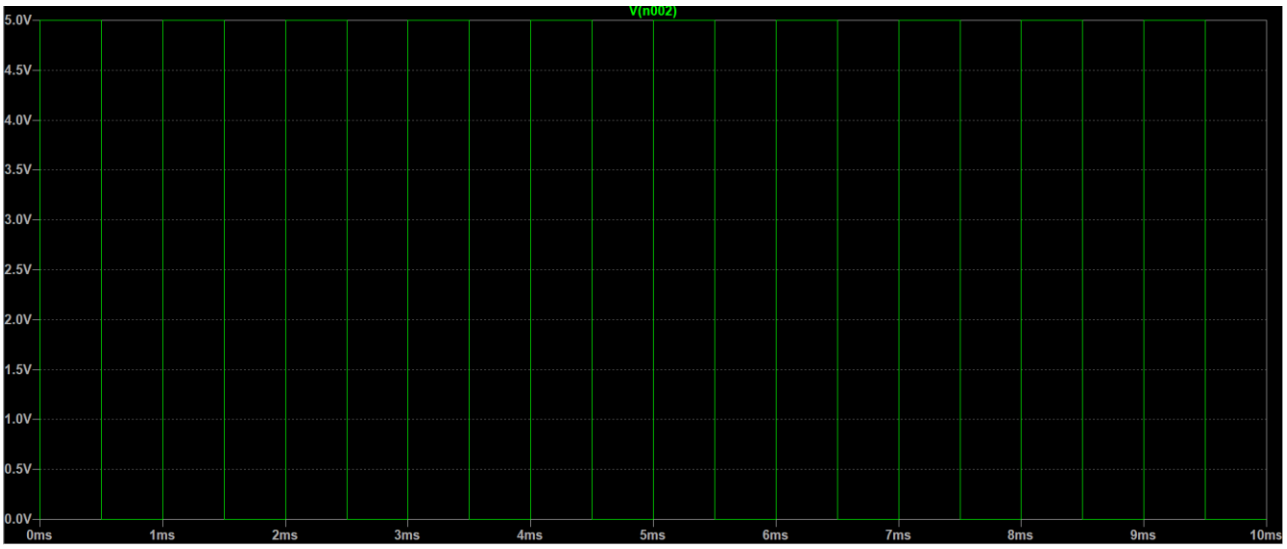

Fig 2.1.3 Input to the CMOS INVERTER

Output DC Response of the Conventional CMOS INVERTER is shown below which shows both Input and Output of the circuit.

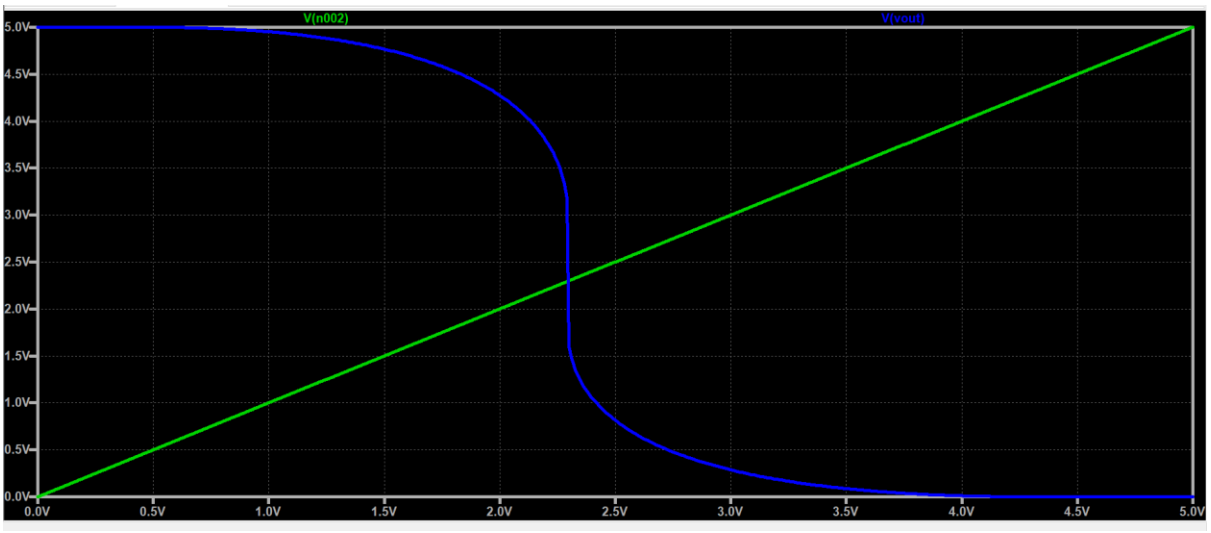

Fig 2.1.4 DC Response of the CMOS INVERTER

CMOS conventional Power consumption is shown below.

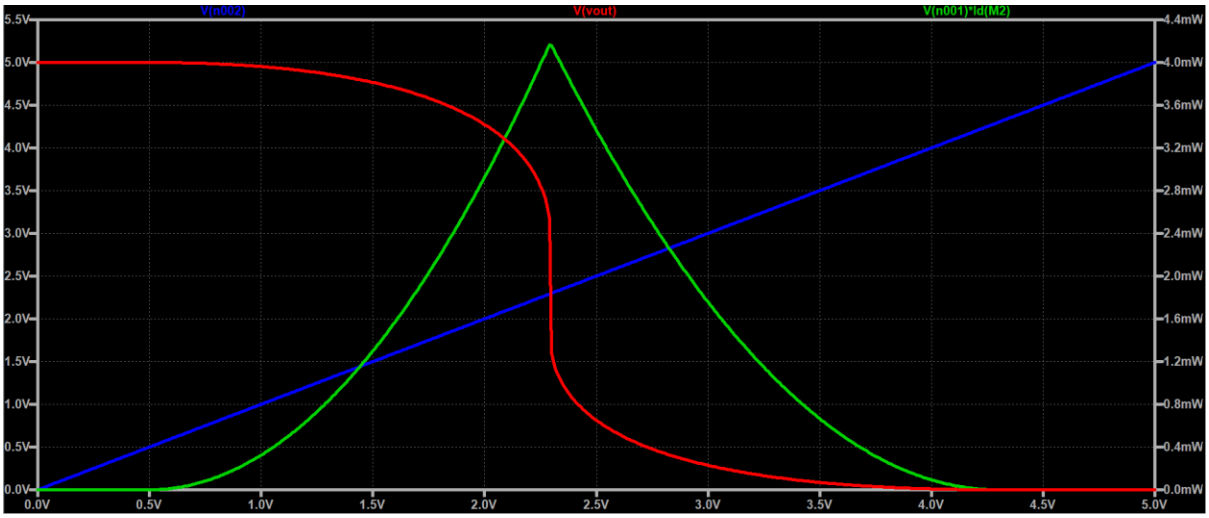

Fig 2.1.5 CONVENTIONAL CMOS INVERTER POWER CONSUMPTION

Green colour line indicates power consumption of Conventional CMOS Inverter.

According to this graph, **leakage power by NMOS is 50.04pw** , **leakage power by PMOS is 50.05pw** and **short circuit power is 4.16mW.** We are seeing leakage power through NMOS when input voltage 0 is applied and leakage power through PMOS when input voltage 5V is applied to inverter. Short circuit power dissipation occurs when both the transistors are conducting. Peak of the graph is 4.6mW.

For calculating delay of the circuit, we are increasing rise time and fall time of the input to see the delay properly. Input and output transient response for that is shown below.

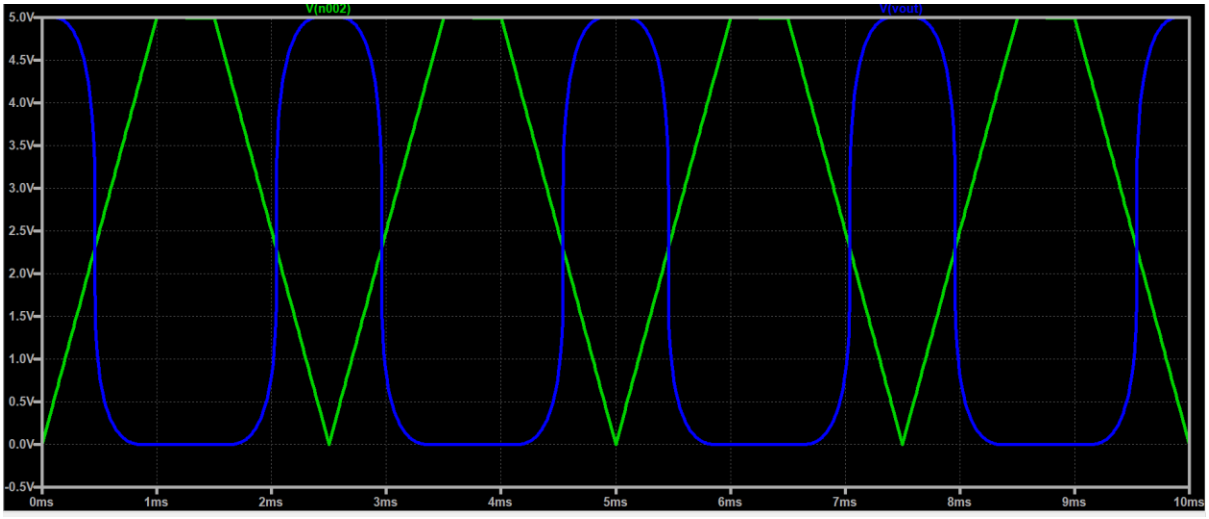

Fig 2.1.6 CONVENTIONAL CMOS INVERTER INPUT AND OUTPUT RESPONSE WITH INCREASE IN DELAY TIME

Average Delay of the Conventional CMOS INVERTER is $(T_{PHL}+ T_{PLH})$ / 2.

= (43.691972µs+ 49.153468µs)/2 =2557.072641 µs/2 =**46.42 µs**

2.2 SUBSTRATE BAISED CMOS INVERTER

In a CMOS inverter for varying the threshold voltage of PMOS and NMOS, the body terminals of PMOS and NMOS are connected to the positive and negative voltages, respectively as shown in below figure.

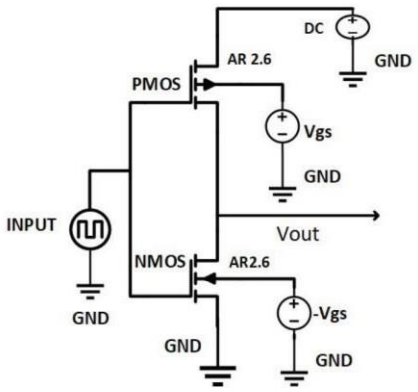

Fig 2.2.1 SUBSTRATE BIASED CMOS INVERTER

The same above circuit is simulated in LTSPICE which is shown below

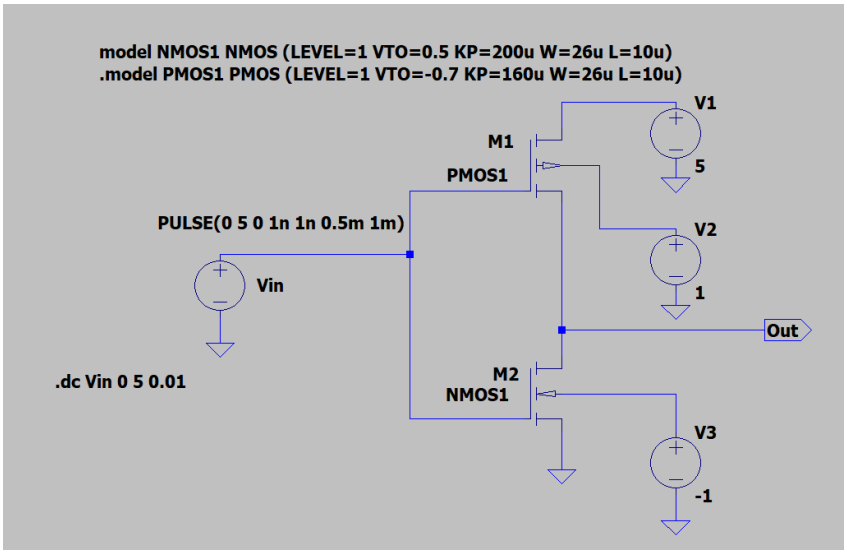

Fig 2.2.2 LTSPICE CIRCUIT OF SUBSTRATE BIASED CMOS INVERTER

Output for the circuit is shown below

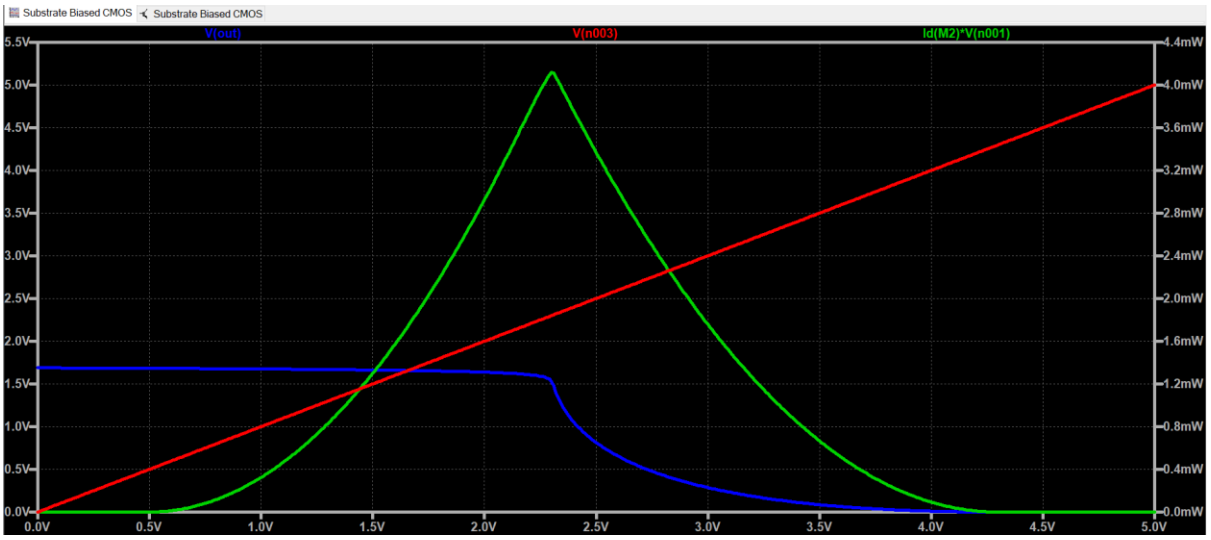

Fig 2.2.3 OUTPUT RESPONSE OF THE SUBSTRATE BAISED CMOS INVERTER

From the above circuit, green colour indicates power consumption by the substrate biased CMOS Inverter. According to this graph, **leakage power by NMOS is 21.93pW**, **leakage power by PMOS is 30.04pW**and **short circuit power is 4.11mW.** We are seeing leakage power through NMOS when input voltage 0 is applied and leakage power through PMOS when input voltage 5V is applied to inverter. Short circuit power dissipation occurs when both the transistors are conducting. Peak of the graph is **4.11mW.**

For calculating delay of the circuit, we are increasing rise time and fall time of the input to see the delay properly. Input and output transient response for that is shown below.

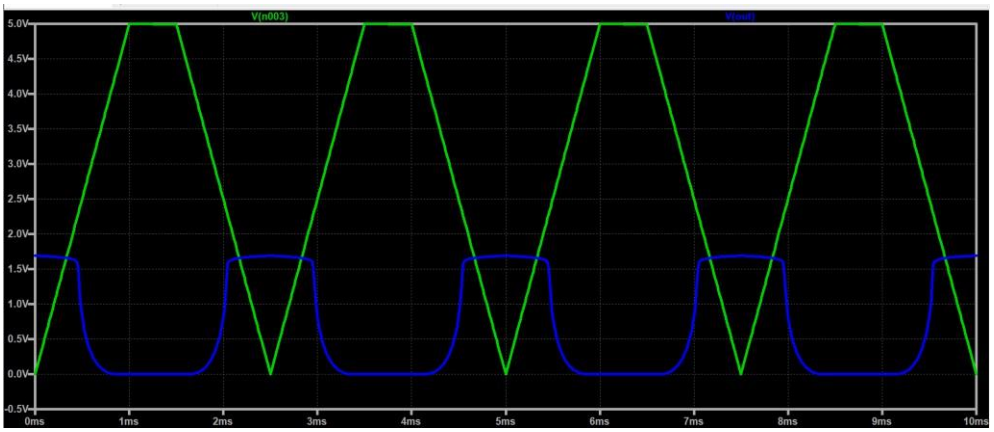

Fig 2.2.4 SUSTRATE BIASED CMOS INVERTER INPUT AND OUTPUT RESPONSE WITH INCREASE IN DELAY TIME

Average Delay of the Substrate Biased CMOS INVERTER is $(T_{PHL}+ T_{PLH})$ / 2.

= (92.84544µs+92.84544µs)/2 = **92.84 µs**

2.3 STACKING BAISED CMOS INVERTER

In this Inverter, PMOS and NMOS re splitted into two halves for reducing leakage power.

In the first phase we are giving parameter values same as were given in previous circuits, to see whether power is getting reduced or not. In the second phase, we are going to change aspect ratios to reduce power dissipation further.

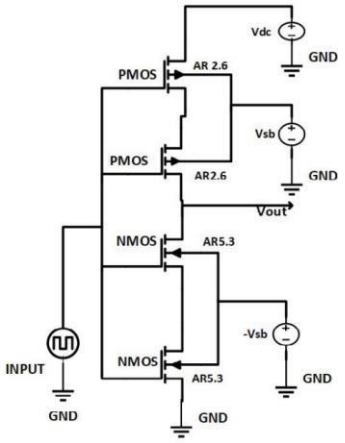

Fig 2.3.1 STACKING BIASED CMOS INVERTER CIRCUIT

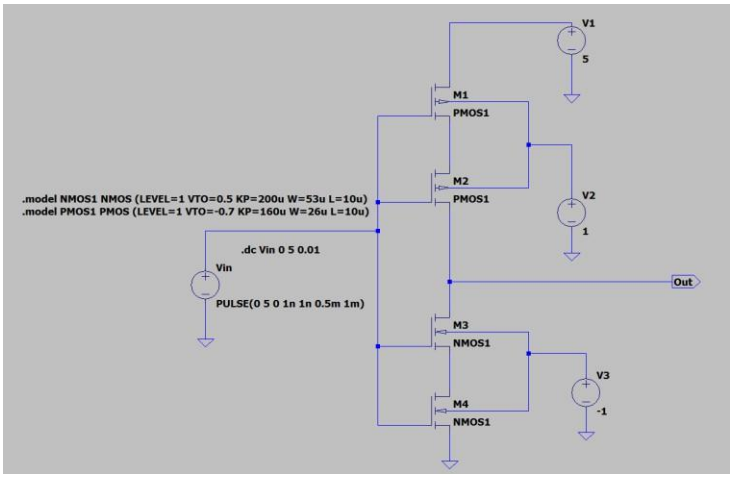

Fig 2.3.2 STACKING BIASED CMOS INVERTER CIRCUIT USING LTSPICE.

Response of the above circuit , is shown below.

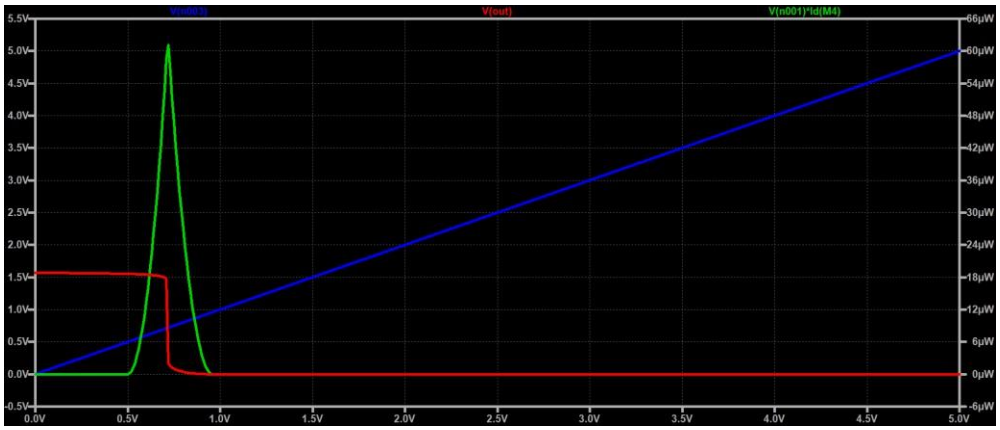

Fig 2.3.3 RESPONSE OF THE STACKING BIASED CMOS INVERTER

From the above circuit, green colour indicates power consumption by the substrate biased CMOS Inverter. According to this graph, **leakage power by NMOS is 3.92pW**, **leakage power by PMOS is 575.43fW**and **short circuit power is 60.7uW.** We are seeing leakage power through NMOS when input voltage 0 is applied and leakage power through PMOS when input voltage 5V is applied to inverter. Short circuit power dissipation occurs when both the transistors are conducting. Peak of the graph is **60.7uW.**

For calculating delay of the circuit, we are increasing rise time and fall time of the input to see the delay properly. Input and output transient response for that is shown below.

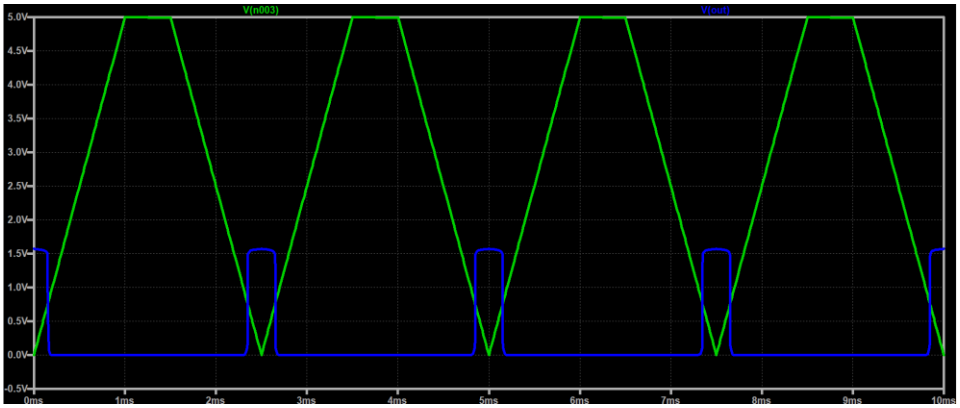

Fig 2.3.4 STACKING BIASED CMOS INVERTER INPUT AND OUTPUT RESPONSE WITH INCREASE IN DELAY TIME

Average Delay of the Stacking Biased CMOS INVERTER is $(T_{PHL}+ T_{PLH}) / 2$.

= (349.53577µs+338.61278µs)/2 = **344 µs**

3. COMPARISON BETWEEN THREE CIRCUITS

In this section , we are going to see leakage power and short circuit power values of Conventional CMOS Inverter, Substrate Biased CMOS Inverter and Stacking Biased CMOS Inverter also corresponding average delays. This comparison is shown in the form of a table.

Power Dissipation and Average Delay	**Conventional CMOS Inverter**	**Substrate Biased CMOS Inverter**	**Stacking Biased CMOS Inverter**
Leakage Power (PMOS)	**50.05 pW**	**30.04 pW**	**575.43 fW**
Leakage Power (NMOS)	**50.04 pW**	**21.93 pW**	**3.92 pW**
Short Circuit Power	**4.16 mW**	**4.11 mW**	**60.7 uW**
Average Delay	**46.42 µs**	**92.84 µs**	**344 µs**

TABLE 3.1 COMPARING BETWEEN THREE CIRCUITS

From the table, we can infer that as power dissipation goes on decreasing , delay is increasing. This is because of four reasons:

- **Threshold Voltage Increase:** Substrate biasing and stacking raise threshold voltage, reducing leakage but slowing switching, increasing delay.
- **Reduced Leakage, Slower Switching:** Lower leakage from raised threshold voltage or stacked transistors results in slower switching speeds.
- **Power vs. Speed Trade-off:** Lower power dissipation increases circuit resistance, slowing charging/discharging and raising delay.
- **Short-Circuit Power Reduction:** Reduced simultaneous conduction decreases short-circuit power, but prolongs transition times, adding delay.

4. CONCLUSION

This project shows that we can reduce power loss in CMOS inverters using techniques like self-biasing, Width-to-Length (W/L) scaling, and stacking. Through simulations, we found that these methods lower the power used by CMOS circuits, which is important for making electronics more energy-efficient. Starting with a standard CMOS inverter as a baseline, we saw that power loss could be high. When we applied the substrate-biasing technique, power loss dropped, with only a slight delay in the circuit's speed. Stacking, another method we tested, further reduced power loss, but with a bigger delay because the circuit slowed down due to higher resistance.

Our findings show a clear trade-off: reducing power loss often means the circuit operates a bit slower. This balance between saving energy and keeping good performance helps designers choose the best technique based on specific needs, whether it's prioritizing low power, high speed, or a mix of both. Overall, this study provides useful insights for creating more efficient circuits, helping to advance low-power technology in devices where conserving energy is essential.

REFERENCES:

1. A. Prakash and P. Jain, "Optimization of Leakage Power Dissipation in CMOS Inverter using Self biased and W/L Scaling Techniques," 2023 2nd International Conference on Futuristic Technologies (INCOFT), Belagavi, Karnataka, India, 2023, pp. 1-5, doi: 10.1109/INCOFT60753.2023.10425379. keywords: {Stacking;Voltage;Very large scale integration;CMOS technology;Inverters;Power dissipation;Substrates;CMOS inverter;W/L scaling;Substrate biased;Cadence Virtuoso;Low power integrated circuit},
2. https://www.geeksforgeeks.org/cmos-inverter/
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