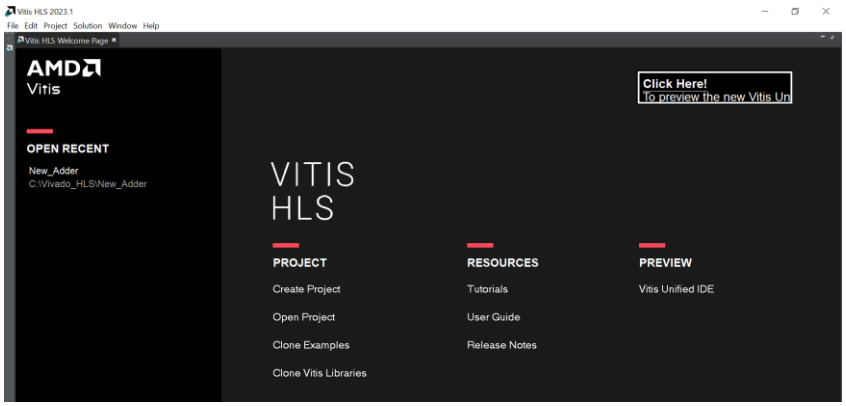
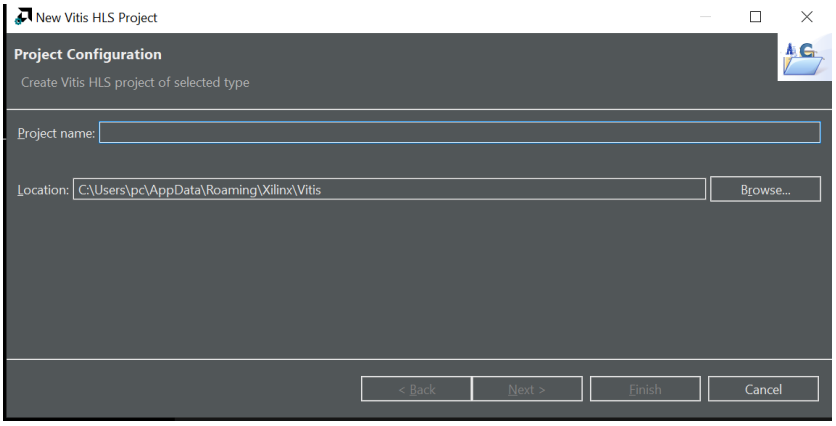
HLS Design Flow

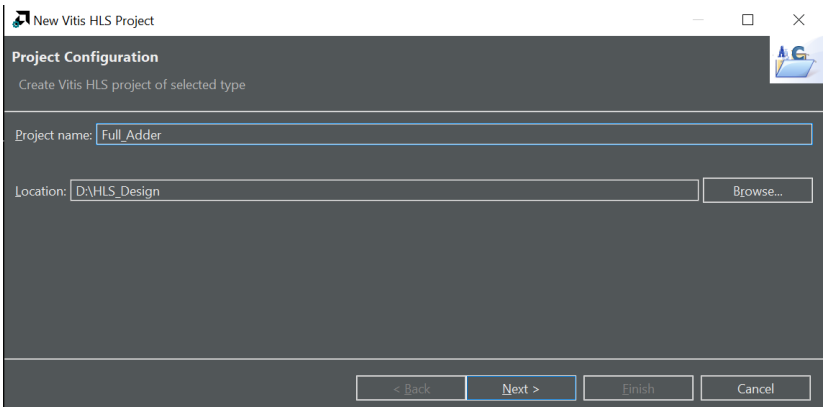
1. Open Vitis / Xilinx HLS



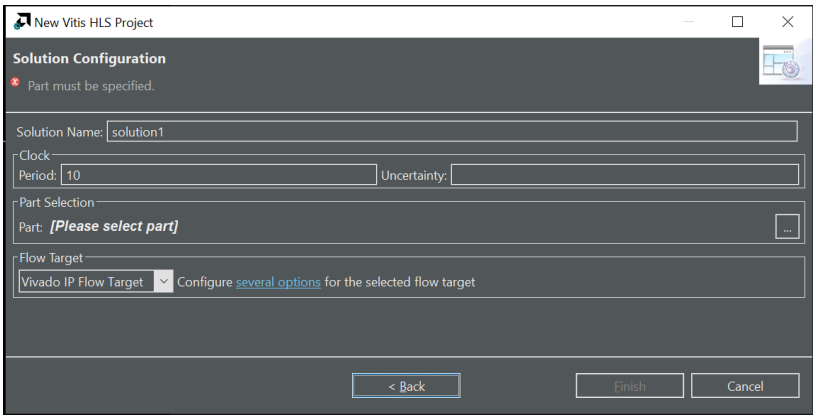
2. Create Project



You can choose your own location. But remember that folder name shouldn't have any spaces. You underscore required. For example I am doing full adder as an example as shown below



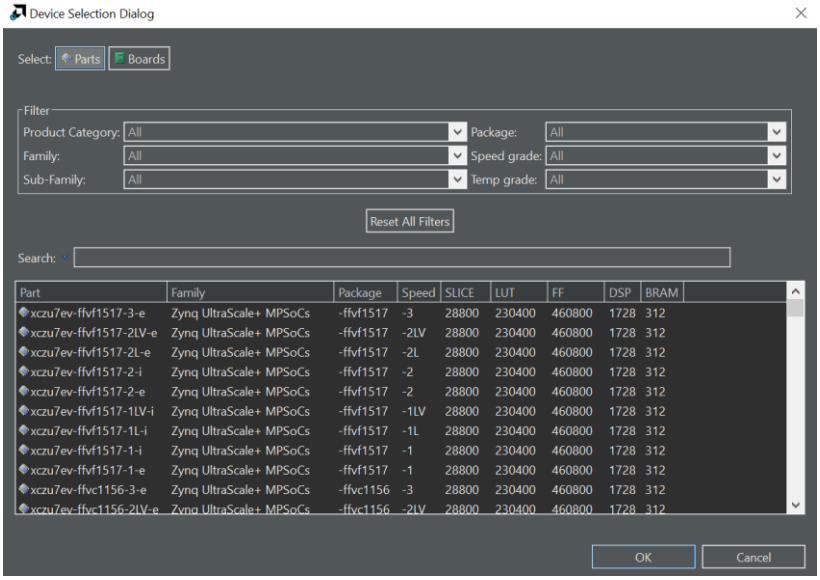
3. Solution Configuration.



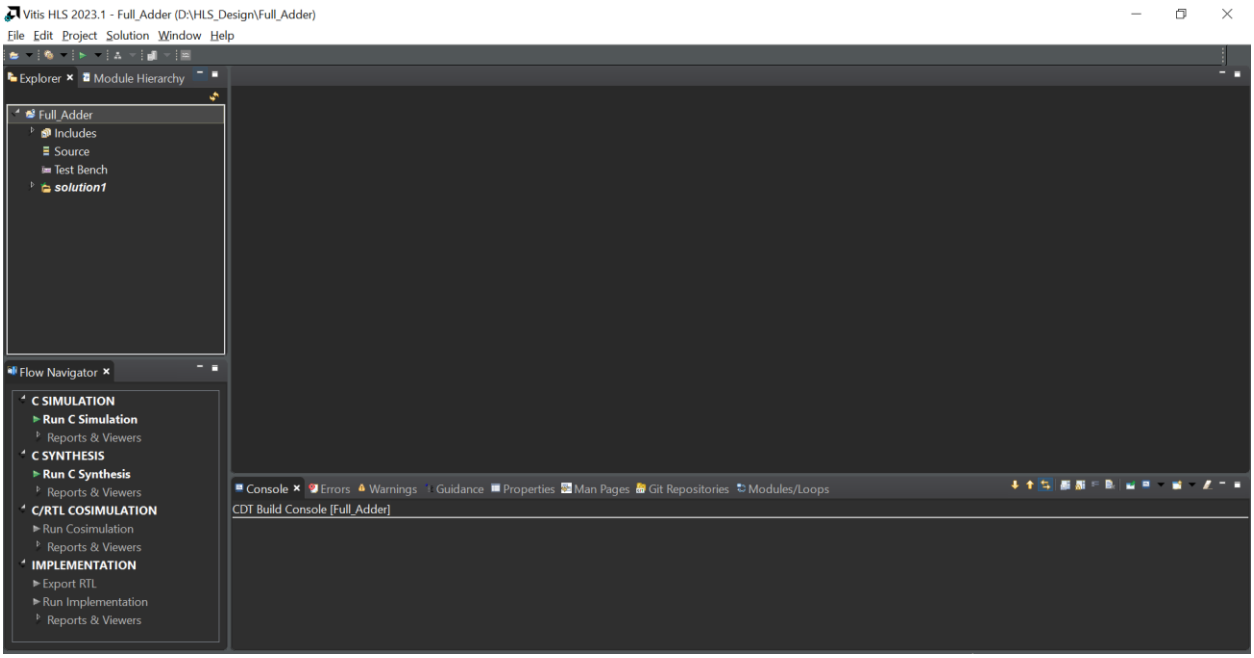
Click on Next button until you see the Solution Configuration. Here in Solution Configuration, you can select your own clock period, and the board on which you want you dump your design.

For selecting board, in part selection section right corner, you will find 3 dots, click on that.

You will get a window as shown below.

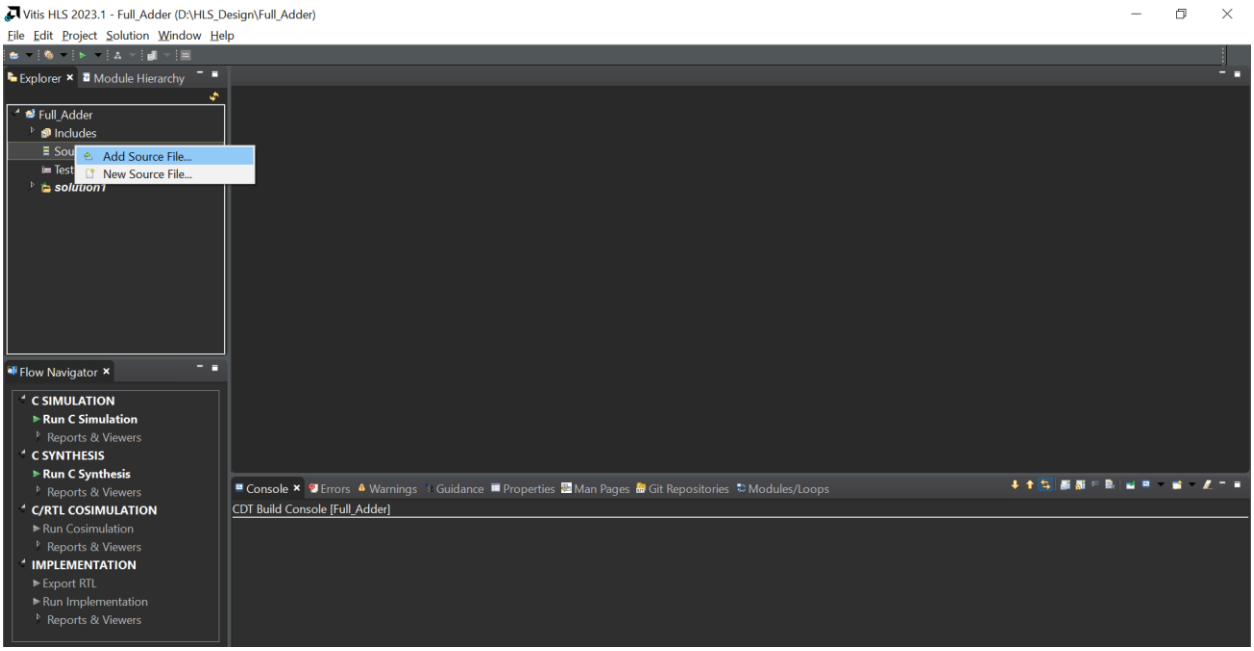


Click on Boards, and select your own board. For example I am selecting Basys3 board. and click finish. You will get main window as shown in below image.

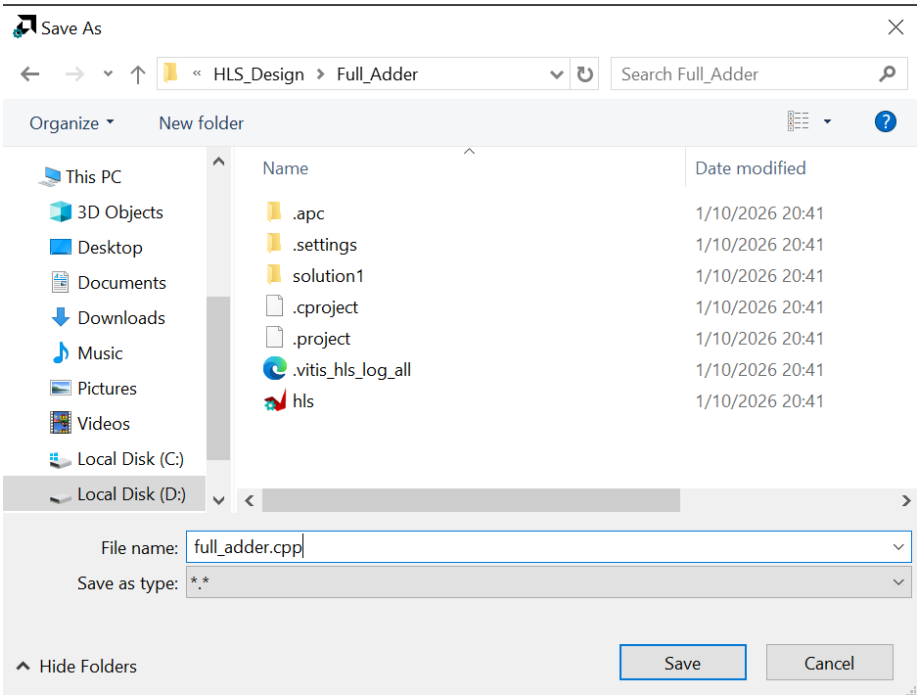


Till here, creating project, setting up target board is done. Next is to write design code and test bench in C++.

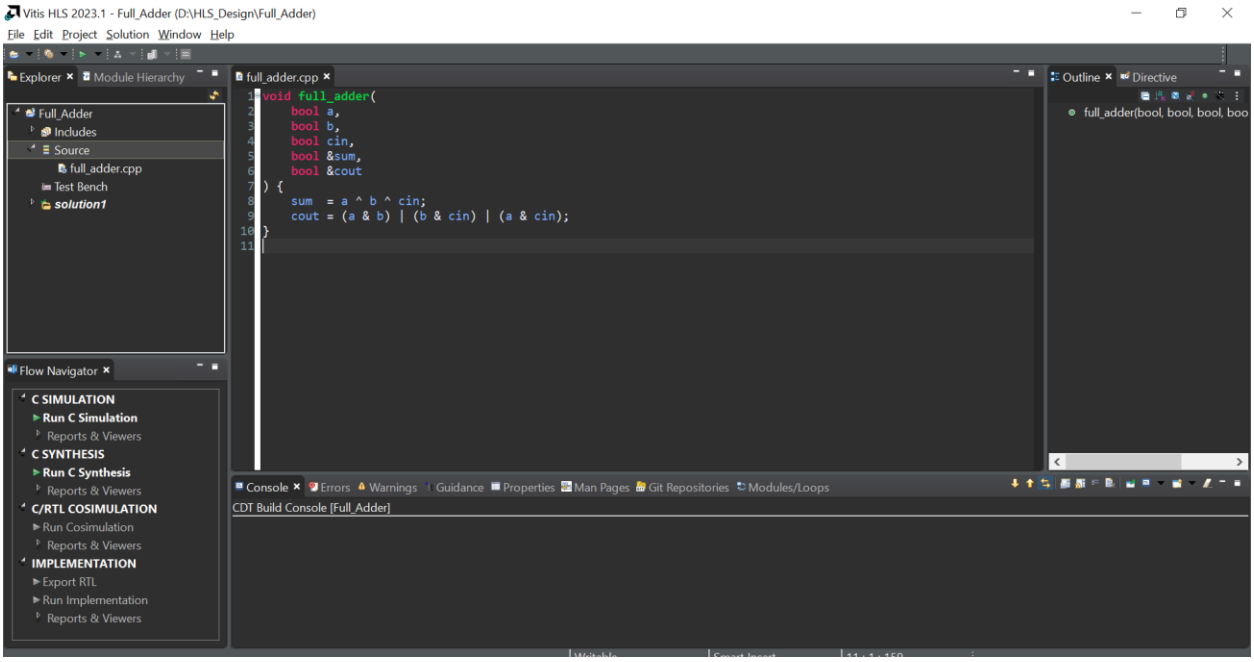
4. Writing Design Code and Test Bench



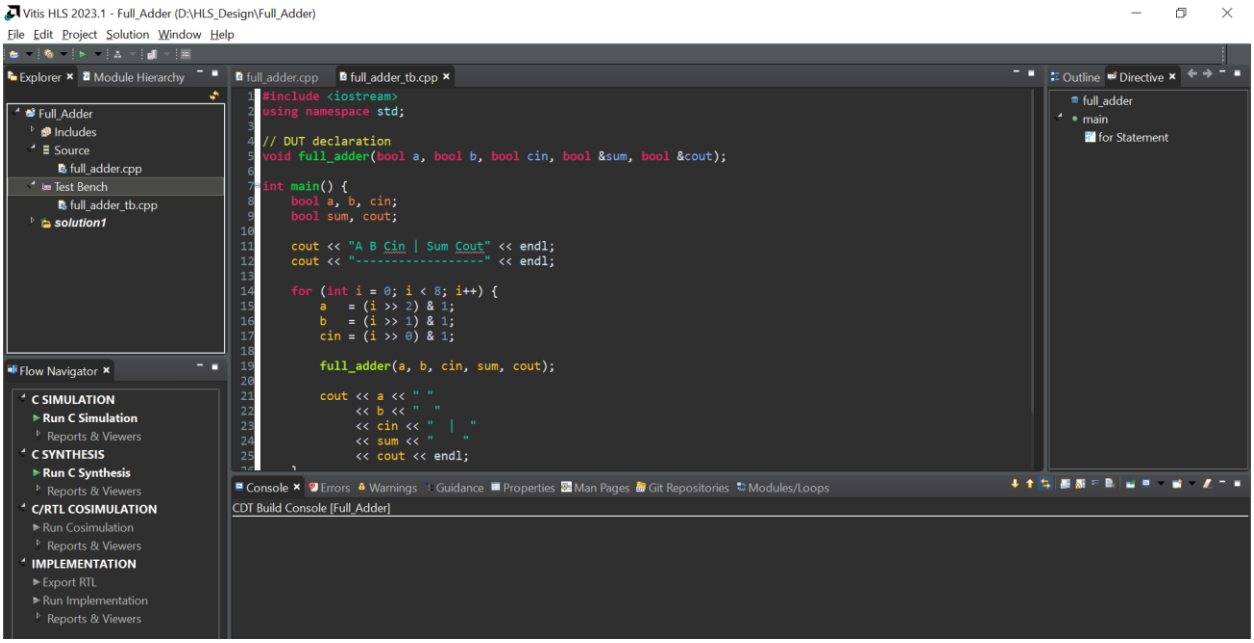
On the left side, you can find your project name, under which you can find sources and test bench. To add source file which means your design file, right click on source. You you are writing code, then select option new source file, save your file with **cpp extension**, and see that file lies inside your project name for safety. For example I am doing full_adder, which I am saving shown below:



Now design file will be created and will open. Now you can write your design code. For example shown below:



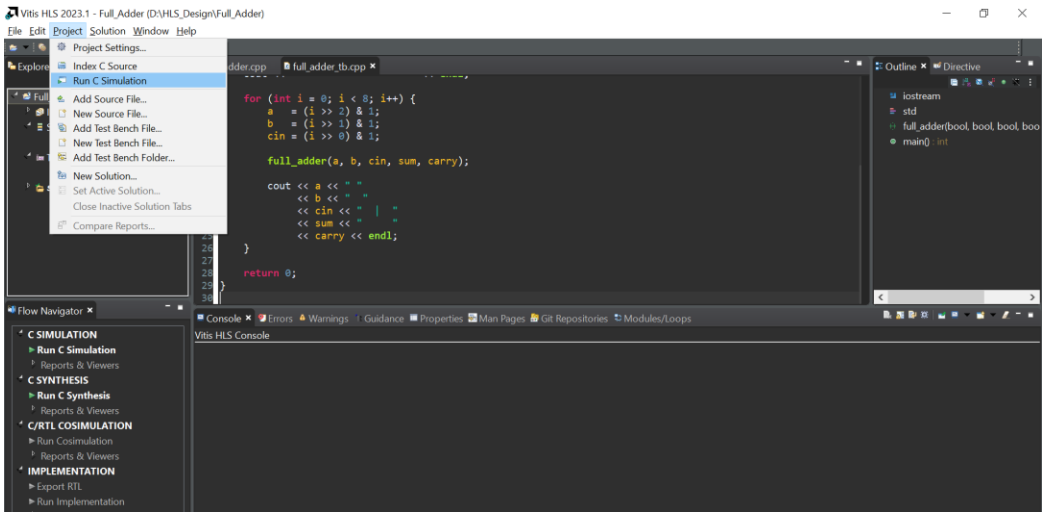
Same I will create test bench file under test bench and save as **full_adder_tb.cpp**



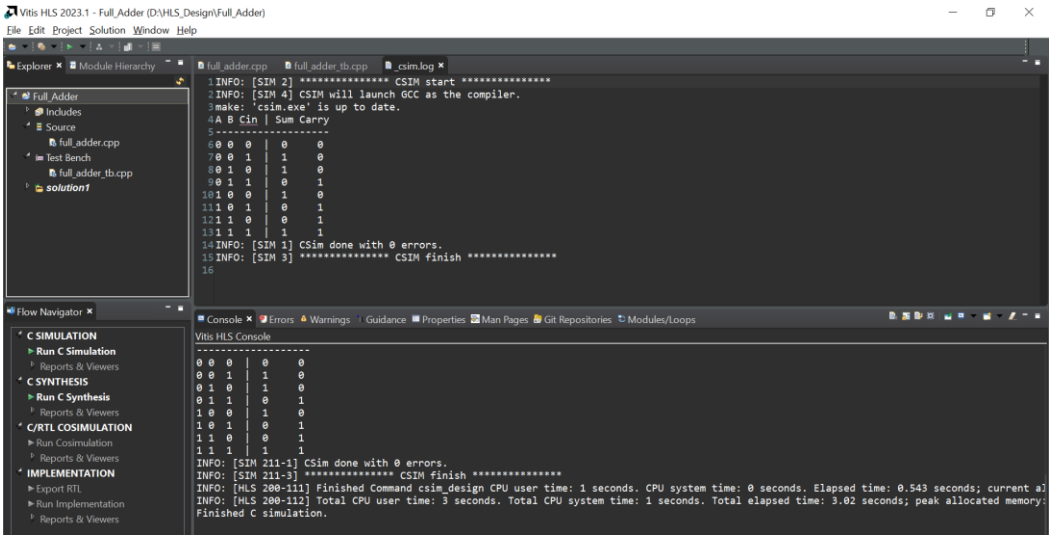
In the above image you can see under source , design code is there and under test bench , test bench

code is there.

5. To Simulate



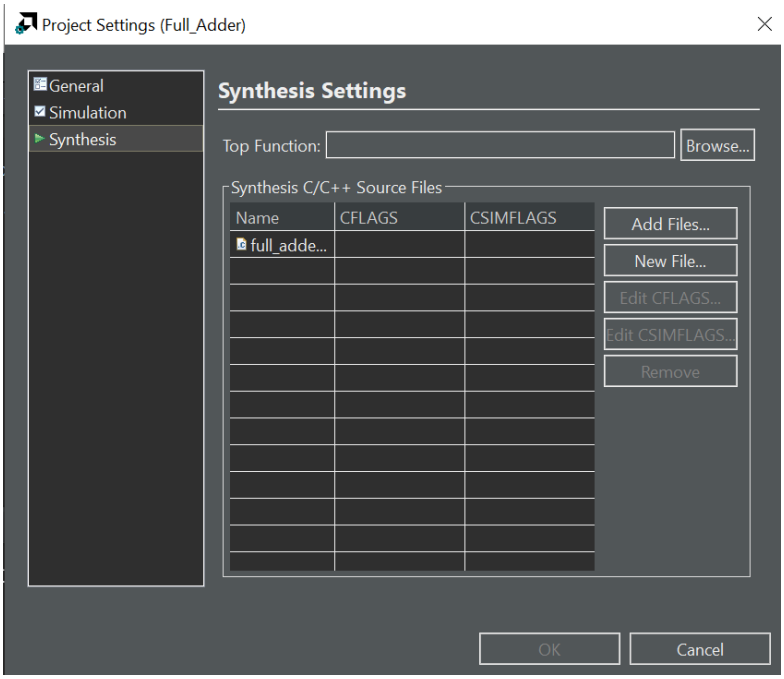
Top you can find Project, under that click on **Run C Simulation and click OK.** Then you will get output. For example output will come as shown below:



Till here, C ++ Design and output verification is done. Next is to Synthesize this C++ Code and get Verilog code, so that we can see waveform in vivado.

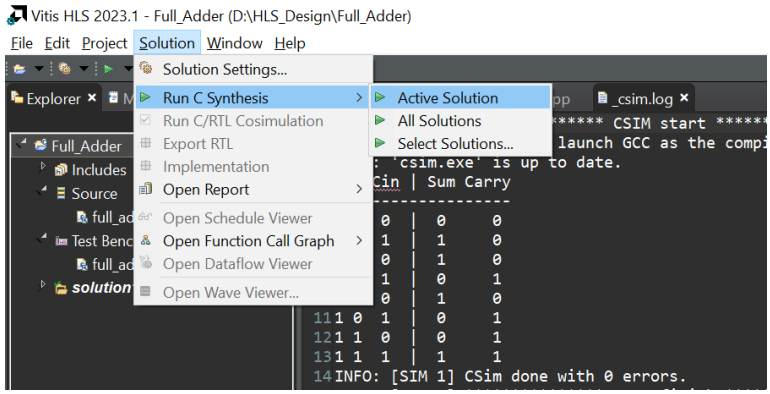
6. To Synthesize

Before, synthesizing code, we need to specify which function we are going to synthesize. For that click on Project -> Project settings -> select option synthesis. You will get below window

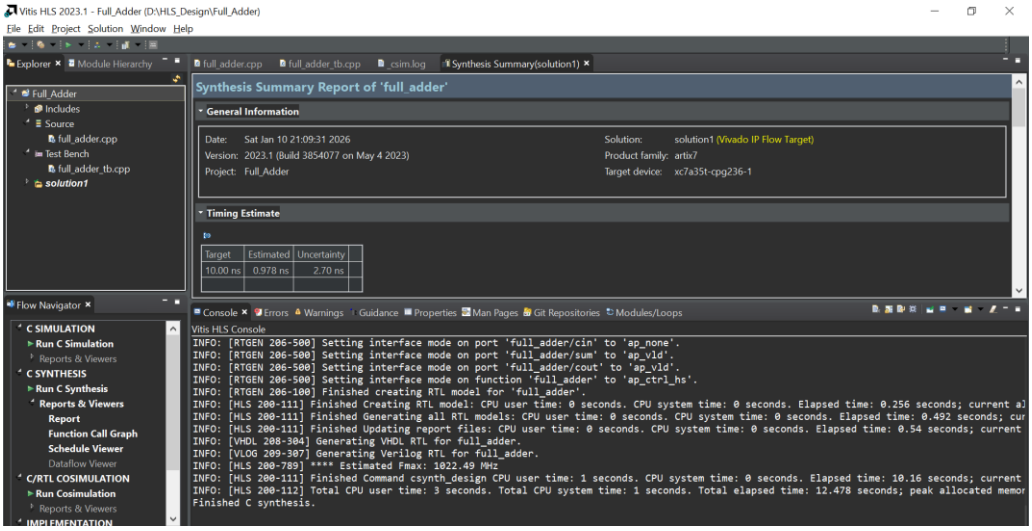


Here, in Top function : type design name and click ok. Now you can synthesize.

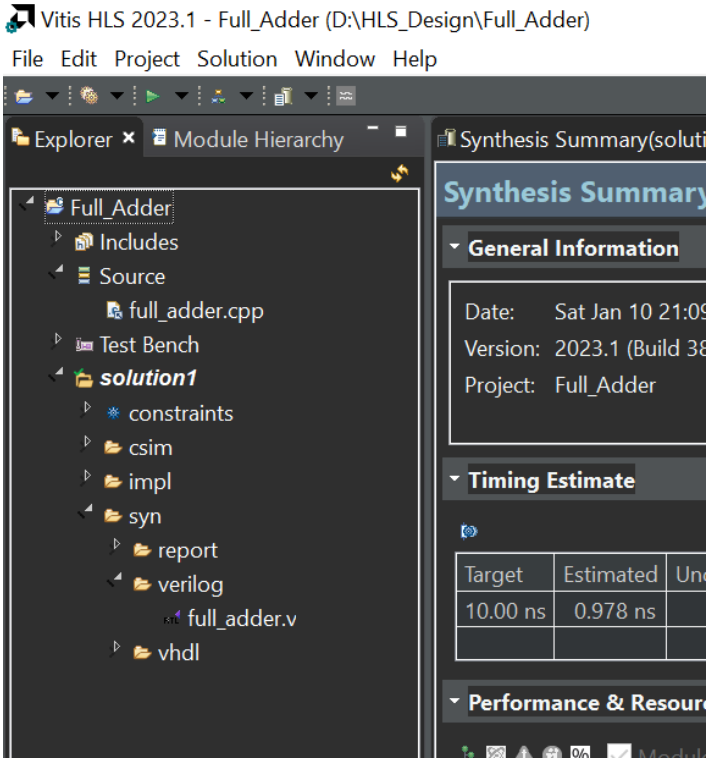
To synthesize click Solution -> Run C Synthesis -> Active Solution as shown in below image and click OK.



You will get summary report as shown in below image.



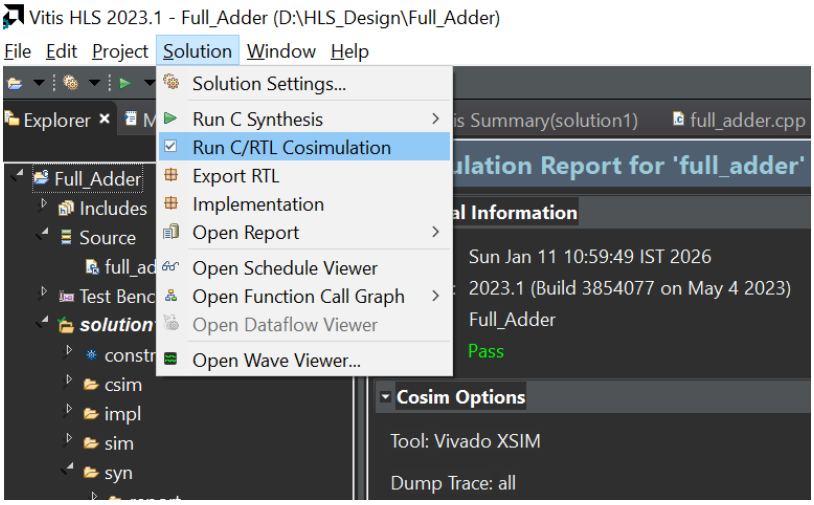
Till here, synthesis is done. You will find .v files in **solution1** folder as shown in below image.



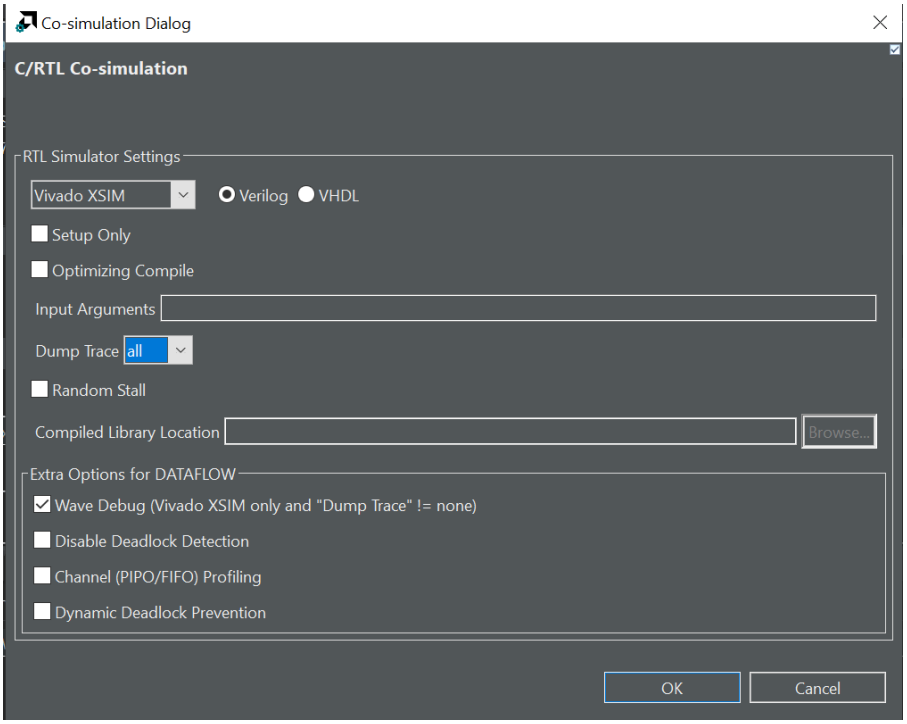
7. To see wave form output

You can see wave form output in Vivado directly by running **Run C / RTL C Simulation.**

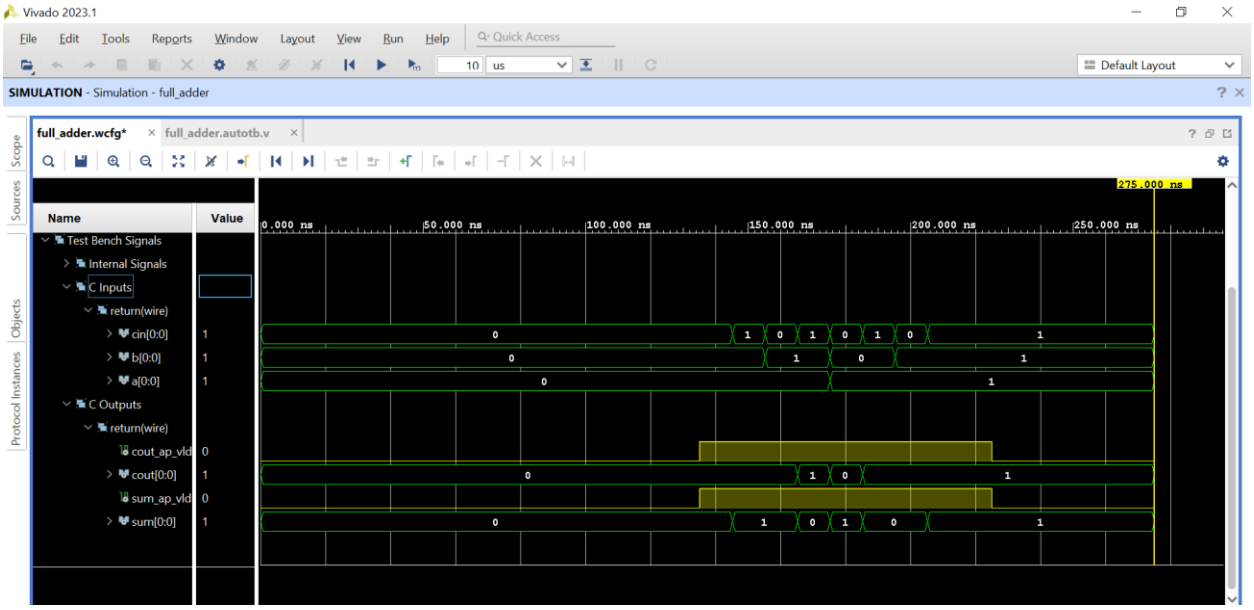
For that select Solution -> Run C / RTL C Simulation as shown in below image



You will get a dialog window as shown below. Select options as shown in image below and click ok.

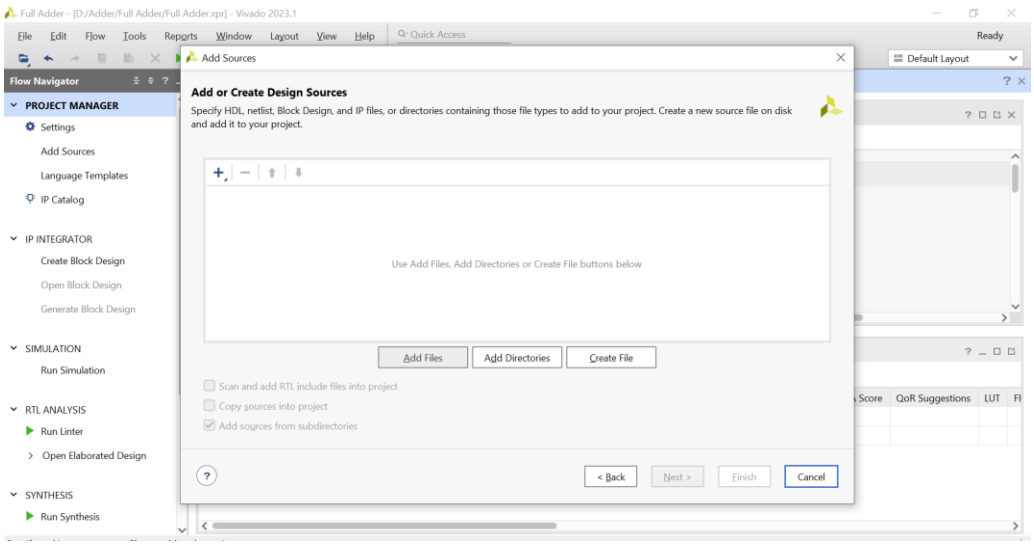


After sometime, Vivado opens and waveform window opens directly as shown in below image.

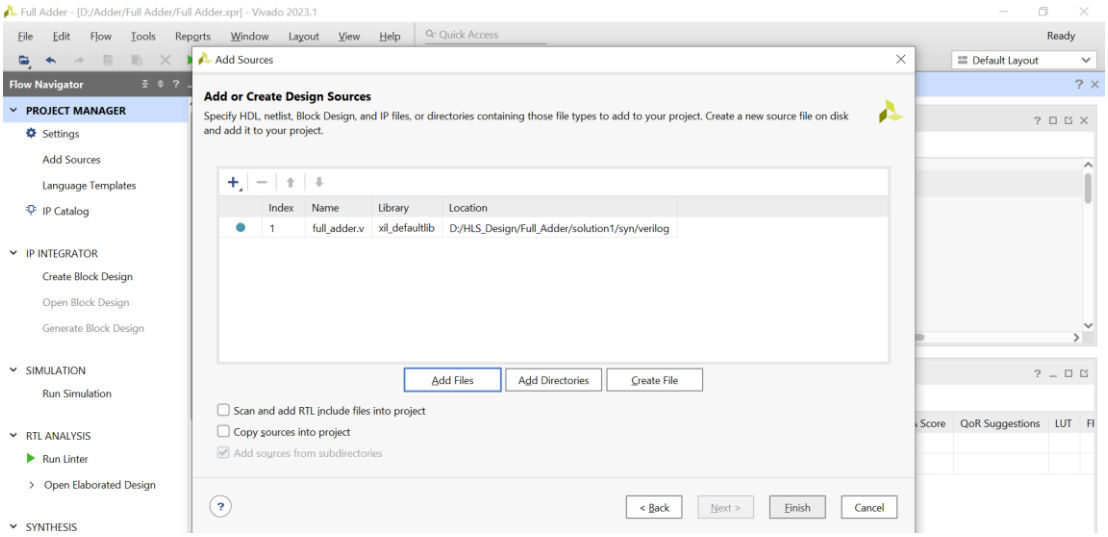


8. To do post implementation

Open Vivado , create project , select same board which you have selected during hls design.



Now add .v file synthesized from hls. Example is shown below.



Click finish. Verilog file is added.

Now you can write test bench and verify output. Then can do post implementation and get outputs required.

To get design codes, and test bench codes, You can find in the below Github link

https://github.com/magantidatta/VLSI/tree/main/HLS%20Design/Full%20Adder%20Design%20Codes