COMP0019 Revision Notes

x86-64.

CPU

Registers

PC

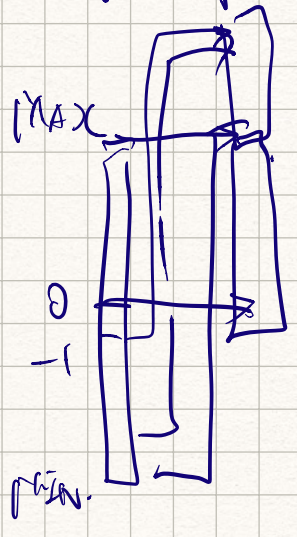
Condition Codes

C Arith.

Shift operations

UB: shift < 0

≥ word size



Signed

Unsigned

$-1 = U_{max}$

Cast signed → unsigned (implicit ())

signed overflow UB!

unsigned overflow defined!

wrap

Dynamic Memory Alloc

malloc() / free().

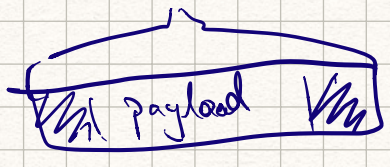
Explicit allocator — malloc free

Implicit allocator.

- new in Java
garbage collector

Allocators are dyned

Intern / Extend Fragmentation.



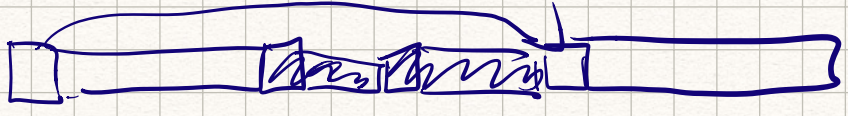
↓

Caused by program
no single free block
is large enough.

Implicit free list.

visit each block.
tag.

Explicit free list.



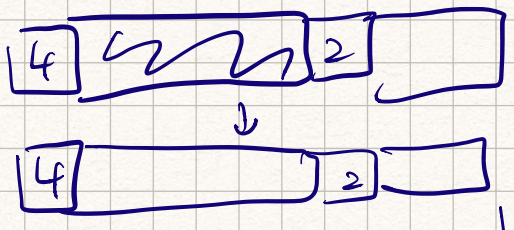
Segregated free-list.

Blocks sorted by size.

Allocating in a Free Block.

Splitting.

Freeing a Block.



False Fragmentation !

Coalesce !

Need Boundary Tags for codescing

Constant time codescing via Boundary Tag.

Boundary Tag.

Allocator Policies.

First fit, next fit, best-fit

Placement.

Segregated free lists can approx. best fit policy.

Splitting policy When do we split?
Intend Fragmentation. toleration ?

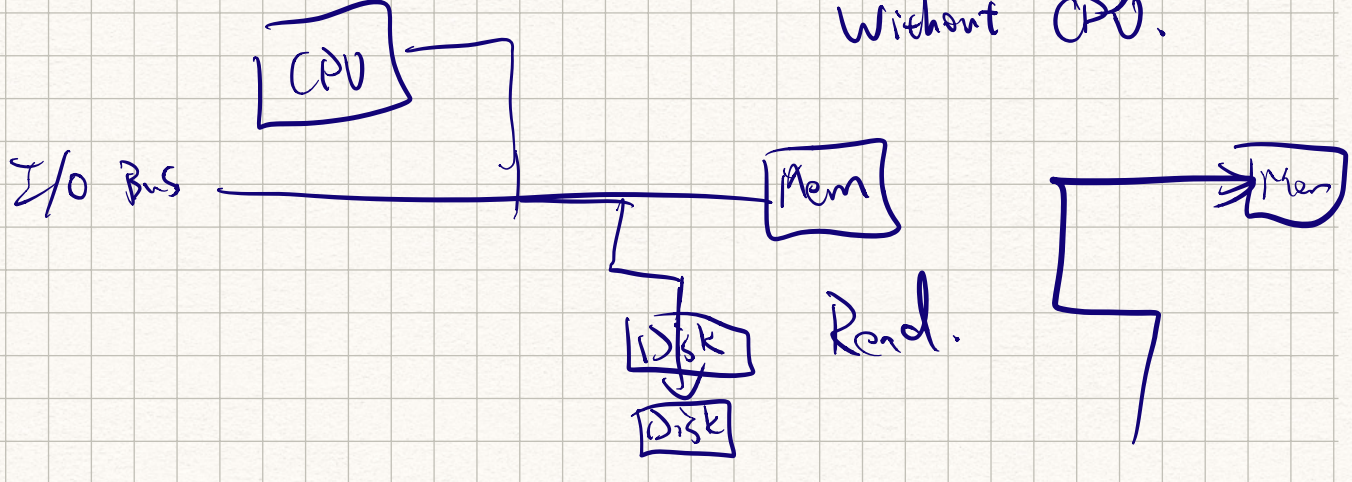
Coalescing policy
Immediately ? — each free()
Deferred ? — perf ↑.

Memory Hierachy
SRAM DRAM. SDRAM
DDR.

SRAM Expensive large. Static
DRAM. cheap. smaller requires refreshing.

Reading a Disk.

Actual Reading Without CPU.



When reading done. notify CPU via interrupt.

SSD vs. Rotating Disks.

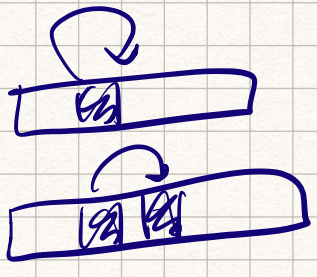
↓

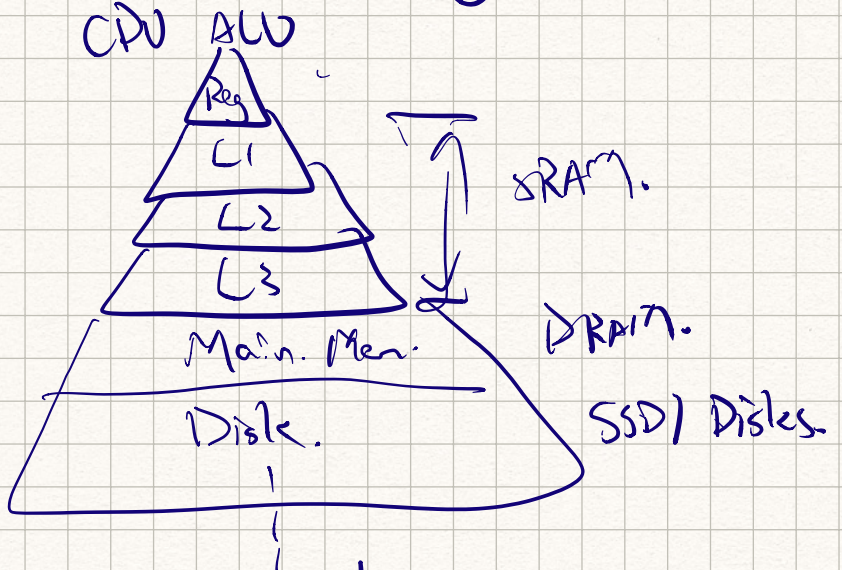
faster, less power, more rugged.

Locality.

Temporal locality.

Spatial locality.





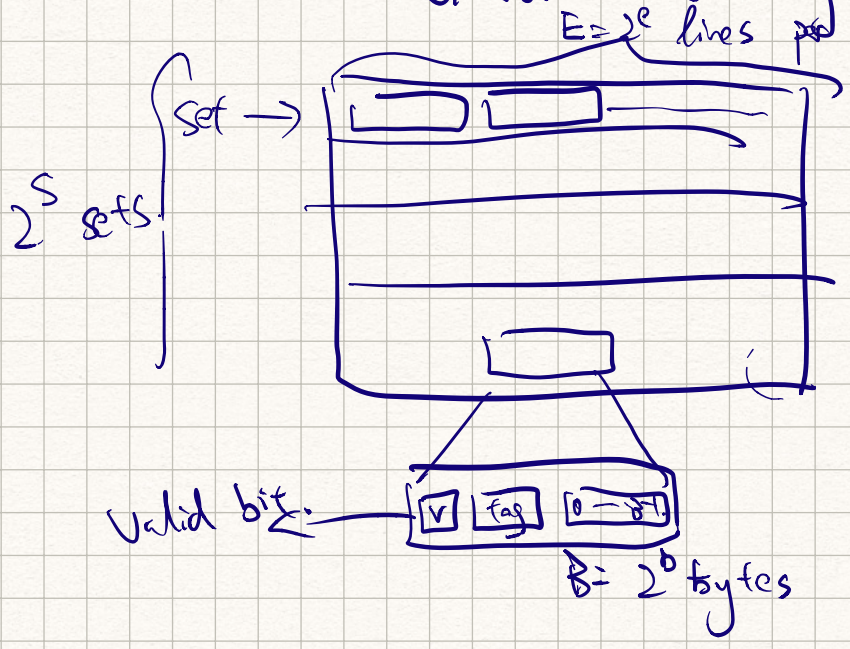
3 Types of Cache misses.

Cold miss (warm up yet) cache empty

Capacity miss. active working blocks > cache size.

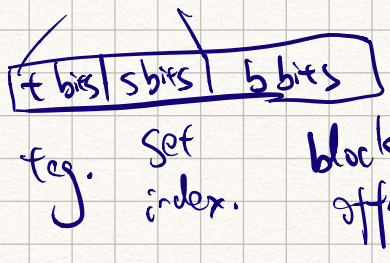
Conflict miss. Cache policy

General Cache Organisation (S, E, B)

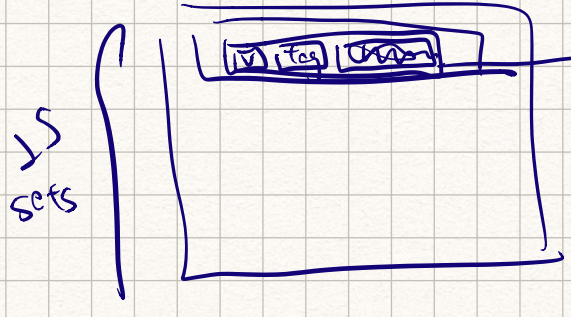


Cache size $2^s \times 2^e \times 2^b$ bytes

Read Cache



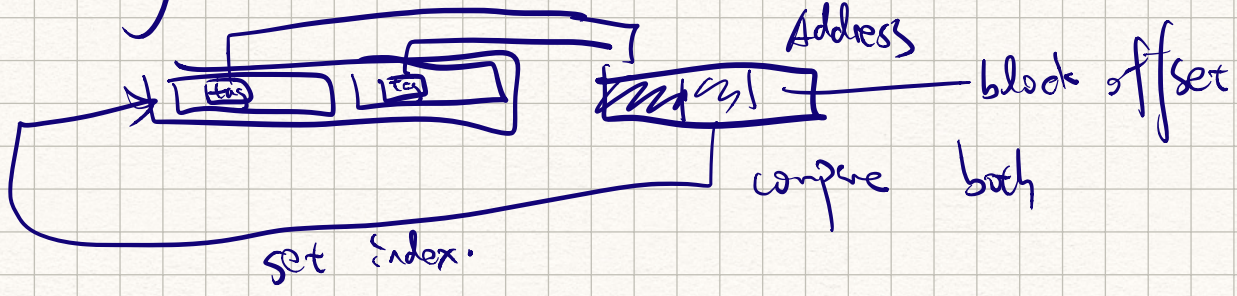
Direct Mapped Cache.



Direct Mapped Cache — fast

— but only one line per set

E-way Set Associative Cache.



If. No match, cache replacement policy

Write.

- write-hit

  write-through - skip cache

  write-back - write to cache
  write to memory later.

- write-miss.

  write-allocate - get into cache,
  and update in cache.

  no-write-allocat - write to memory

Typically, write-back + write-allocate.

Middle-Bits Set Index.

avoid conflicts.

$b = 6 \qquad e = 3$

$t = 47 - 9 = 38$

$C = 32 \times 1024 = 2^{15} \qquad S = 6$

$S = 64$

97% hits $\quad 1 \times 0.97 + 0.03 \times 100$

≈ 4 cycles

99%

$1 \times 0.99 + 0.01 \times 100$

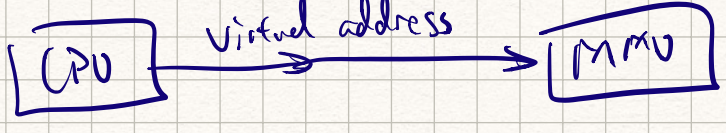
≈ 2 cycles

↓

two tiles better

Process. — Each process has the illusion of whole address space

Context switching — switch address space registers



DRAM Cache.

10x slower than SRAM

but! Disk 10000x slower than DRAM

Typically: fully assoc.

large block size.

large mapping funct.

sophisticated expensive replacement policy

write-back.

Page Table.

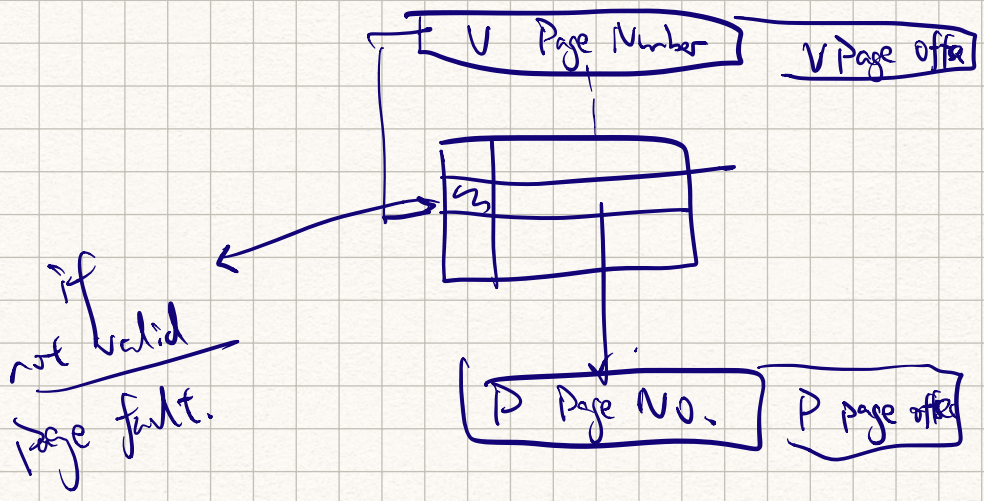
maps virtual pages to physical ones

page hit: page in DRAM

fault: not in

Page fault → an exception handler evicts a victim page.

Address Translation.



CPU asks MMU of a VA.

MMU fetches page table — PT Entry Address →

MMU. figure out Physical Address. ← PT Entry

Mem sends data to CPU — PA → Mem.

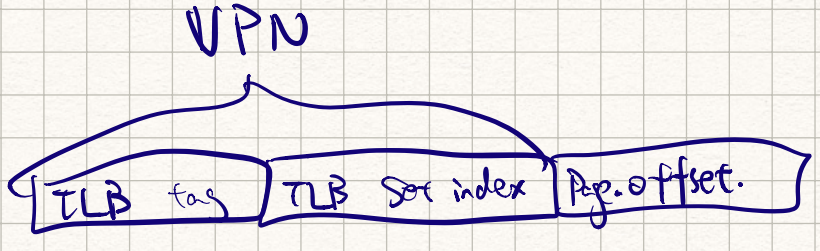
Data

if not valid, page fault handler.

Swaps victim page / new page.

in memory / disk.

Translation Lookaside Buffer TLB



TLB hit eliminates memory access for PTE.

TLB misses are rare. — locality!

Multi-level page table.

Level 1 Page table:

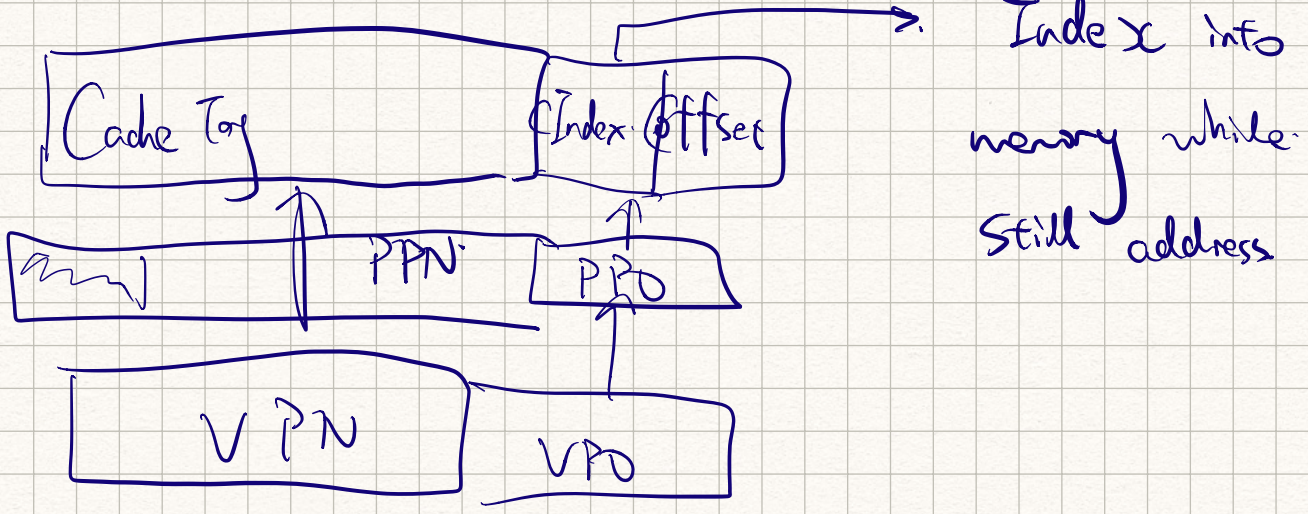
each PTE points a table.

But not always exist

Level Page table.

each PTE points to a pag.

Speed up access



Index into memory while still address

Memory mapping. : areas can be backed by regular file. (from a file)

Anonymous file. (new file)

first fault → demand-zero page.

full zero page!

once written to, (dirtied)
it's like any page

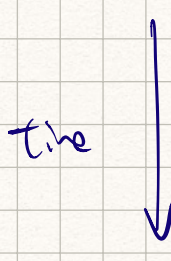
Share page.

Private Copy on Write (CoW)

User-level mmap.

maps file to address start.
with offset. preferably

Process / Exception Control flow



- Jumps / branches
- call return.

Insufficient! Data comes from disk / network.

Inst. ≠ 0?

Ctrl C ?

Exceptions

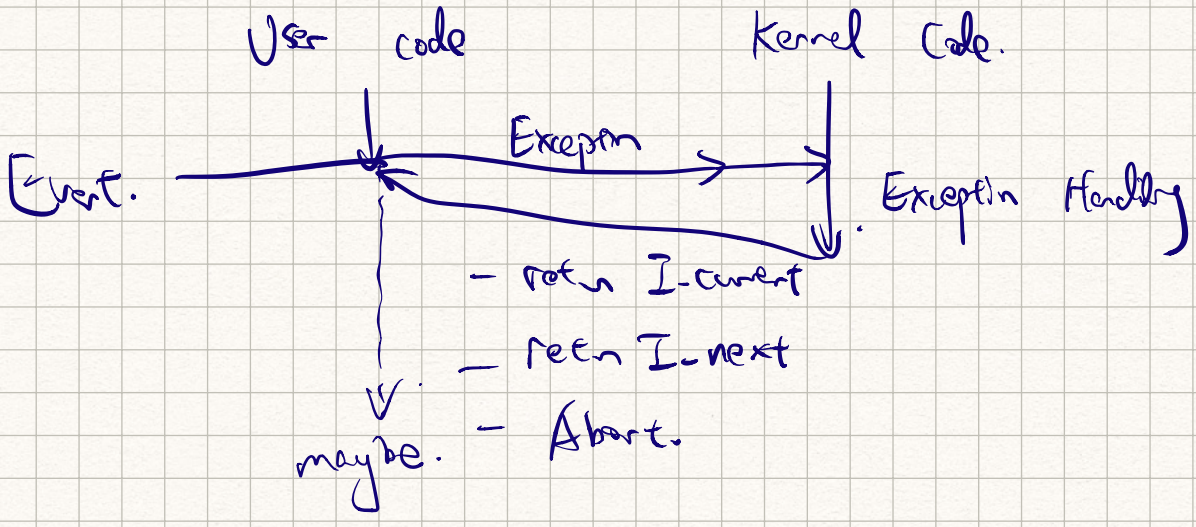
Low-level mechanisms.

- Exceptions. hw + OS.
- Context switch OS timer

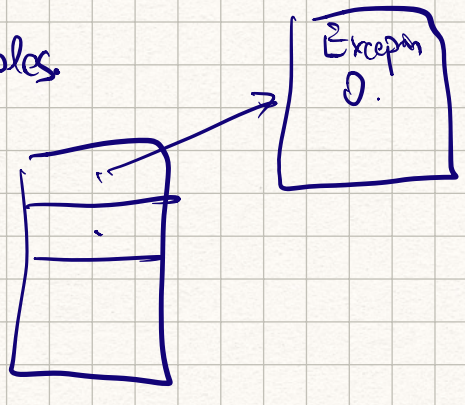
- Signals OS.
- Nonlocal jmps C runtime lib

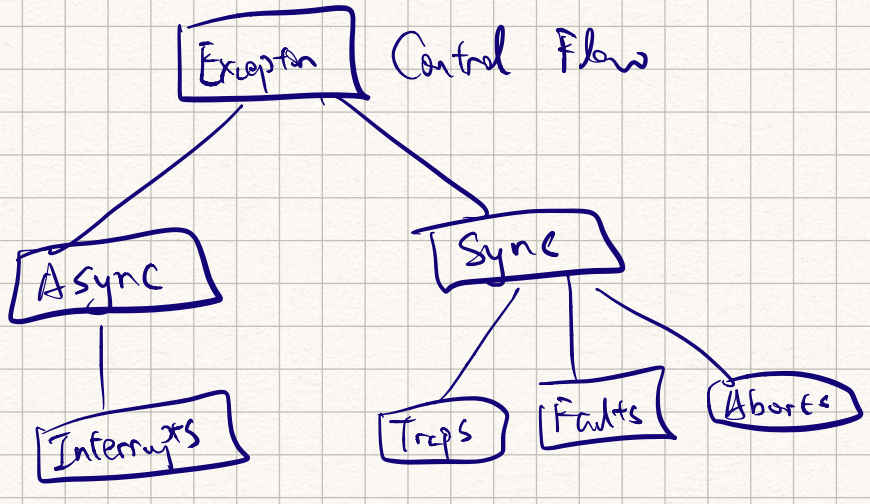
Exception

Control to OS kernel in response to an event.



Exception Tables.





Async Interrupts.

Events external to processor.

Timer Interrupt.

every few ms. external chip triggers a interrupt.

I/O Interrupt

Ctrl + C.

packet arrived

data arrived

Sync Exceptions.

— Traps ie. breakpoint. / specid inst.

intentional.

returns control to next inst.

— Faults. possibly recoverable..

page faults, floating point exceptions

Either re-execute

or. abort.

— Aborts illegal instruction

parity error data corruption.

ABORTS!

System Calls :

each syscall has an ID.

0 read.

:

59 execve

opening a file.

open(filename, options)

↓

invokes a syscall.

%rax is a syscall number.

%rdi - - - args.

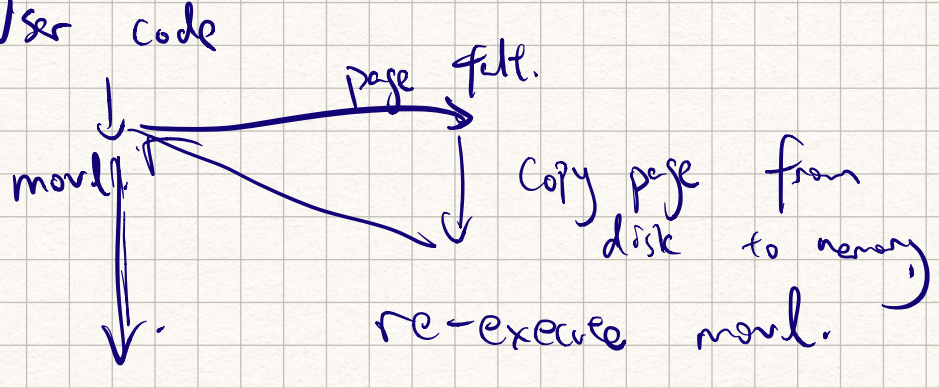
return in %rax.

Almost like a function call.

But! Executed in Kernel

with (higher) privileges

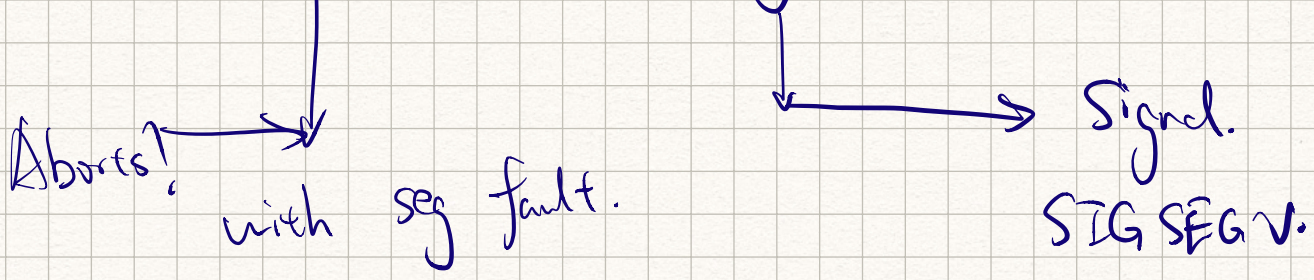
Fault : Page fault.



Fault if write to invalid address.

Kernel

↓ detect invalid address


Aborts!
with seg fault.
Signal.
SIGSEGV.