芯片设计自动化与智能优化
VLSI CAD Spring 2021
Assignment 1 – Logic Synthesis

1. (Programming) Tautology checking: given a circuit, check whether it is tautology using binary decision diagram.
    - Input format: cube list
    - Output format: output 1 or 0 to the screen if tautology or not.
    - Use benchmarks along with the assignment.

2. (Programming) Check two circuits implementing the same Boolean function using a SAT solver.
    - Input format: BLIF
    - Output format: output 1 or 0 to the screen if two circuits implement the same Boolean function
    - Use benchmarks along with the assignment.
    - Hint: 1) ABC/Yosys can read BLIF and output CNF format; 2) MiniSAT is a good SAT solver.

3. (Programming) Technology mapping with standard cell library {INV, NAND2, NOR2, AOI21, AOI22}.
    - Input format: BLIF
    - Output format: BLIF; summarize the number of gates and logic depth in your report.
    - EPFL Benchmarks.

4. (Writing) Write down the pseudo-code of your algorithms and analyze the time and space complexity in Problems 1-3.

Turn in your code, README, and report. Recommend to use CMake building system. Please make your code readable and your report concise (<= 2 pages). Extra pages will be ignored.

Extra requirements:
1. Compress your files (in .zip, .tar). Name it with "hw1_your-student-id.*". The directory tree of your files is supposed to look like:

```
- hw1_your-student-id
---- README (.md, .txt)
---- CMakeLists.txt
---- src/                          (your source code)
---- hw1_your-student-id.pdf  (your report)
```

2. Make sure your code can generate executable files with cmake & make. Name the executables with ‘tautology’, ‘equivalence’ and ‘techmap’. All executables are supposed to take file path as argument.