ECEN 220
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Lab 11 – LC3 Datapath
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Datapath Verilog file (10pt)

```
module Datapath(
            input reset,
            input clk,
   output [15:0] IR,
   output N,
   output Z,
   output P,
   input [1:0] aluControl,
   input [2:0] SR1,
   input [2:0] SR2,
   input [2:0] DR,
   input [1:0] selPC,
   input [1:0] selEAB2,
   input enaALU,
   input regWE,
   input enaMARM,
   input selMAR,
   input selEAB1,
   input enaPC,
   input ldPC,
   input ldIR,
   input ldMAR,
   input ldMDR,
   input selMDR,
   input memWE,
   input enaMDR,
   input flagWE
   );
            wire[15:0] Ra, Rb, aluOut, eabOut, PC, Buss, MARMuxOut, mdrOut;

            ts_driver ts_dr0( MARMuxOut, Buss, enaMARM );
            ts_driver ts_dr1( PC, Buss, enaPC );
            ts_driver ts_dr2( mdrOut, Buss, enaMDR );
            ts_driver ts_dr3( aluOut, Buss, enaALU );


ALU alu0(Ra, Rb, IR[5:0], aluControl, aluOut);
EAB eab(eabOut, IR[10:0], Ra, PC, selEAB1, selEAB2);
IR ir(IR, clk, ldIR, reset, Buss);
MARMux marmux(MARMuxOut, IR[7:0], eabOut, selMAR);
Memory mem0(mdrOut, Buss, clk, reset, ldMAR, ldMDR, selMDR, memWE);
```

```
 NZP znp(N, Z, P, clk, flagWE, reset, Buss);
 PC pc(Buss, clk, reset, ldPC, eabOut, selPC, PC);
 RegFile reg0(Ra, Rb, Buss, clk, regWE, reset, DR, SR1, SR2);

endmodule
```

Master TCL file (2pt)

```
source wave.tcl

isim force add clk 0 -time 0 -value 1 -time 5ns -repeat 10ns
isim force add reset 1 -time 0 -value 0 -time 8ns
run 12ns

source fetch.tcl
source and.tcl

source fetch.tcl
source add.tcl

source fetch.tcl
source not.tcl

source fetch.tcl
source br.tcl

source fetch.tcl
source jsr.tcl

source fetch.tcl
source ld.tcl

source fetch.tcl
source ld1.tcl

source fetch.tcl
source add1.tcl

source fetch.tcl
source st.tcl

source fetch.tcl
source jmp.tcl

source fetch.tcl
source br1.tcl

source fetch.tcl
```

Wave TCL file (2pt)

```
wave add clk
wave add reset
wave add Buss -radix hex

#add signals to view the PC and PC control
wave add selPC
wave add enaPC
wave add ldPC
wave add PC -radix hex

#add signals to view the IR and IR control
wave add ldIR
wave add IR -radix hex

#add signals to view the EAB control
wave add selEAB1
wave add selEAB2
wave add eabOut -radix hex

#add signals to view the MARMux control
wave add selMAR
wave add enaMARM
wave add MARMuxOut -radix hex

#add signals to view Register File control
wave add DR
wave add SR1
wave add SR2
wave add regWE

#add signals to view the Registers in the Register File
wave add /reg0/r0 -radix hex
wave add /reg0/r1 -radix hex
wave add /reg0/r2 -radix hex
wave add /reg0/r3 -radix hex
wave add /reg0/r4 -radix hex
wave add /reg0/r5 -radix hex
wave add /reg0/r6 -radix hex
wave add /reg0/r7 -radix hex
wave add Ra -radix hex
wave add Rb -radix hex

#add signals to view the ALU control
```

```
wave add aluControl
wave add enaALU
wave add aluOut -radix hex

#view the condition flags
wave add N
wave add Z
wave add P
wave add flagWE

#add signals to view the Memory Registers and the Memory control
wave add ldMAR
wave add /mem0/MARReg -radix hex
wave add ldMDR
wave add enaMDR
wave add selMDR
wave add  mdrOut -radix hex
wave add /mem0/memOut -radix hex
wave add memWE
```

Inactive TCL file (2pt)

```
isim force add enaALU 0
isim force add enaMARM 0
isim force add enaPC 0
isim force add enaMDR 0
isim force add ldIR 0
isim force add ldPC 0
isim force add ldMAR 0
isim force add ldMDR 0
isim force add regWE 0
isim force add memWE 0
isim force add flagWE 0
```

Fetch TCL file (2pt)

```
source inactive.tcl

#fetch0
isim force add enaPC 1
isim force add ldMAR 1
run 10ns
source inactive.tcl

#fetch1
isim force add ldPC 1
isim force add selPC 00
isim force add ldMDR 1
isim force add selMDR 1
```

```
run 10ns
source inactive.tcl

#fetch2
isim force add ldIR 1
isim force add enaMDR 1
run 10ns
source inactive.tcl
```

All instruction TCL files (12pt)

```
#add0
isim force add aluControl 01
isim force add SR1 000
isim force add DR 001
isim force add enaALU 1
isim force add regWE 1
isim force add flagWE 1

run 10ns
```

```
#add1
isim force add aluControl 01
isim force add SR1 010
isim force add SR2 001
isim force add DR 110
isim force add enaALU 1
isim force add regWE 1
isim force add flagWE 1

run 10ns
```

```
#and0
isim force add aluControl 01
isim force add SR1 000
isim force add DR 000
isim force add enaALU 1
isim force add regWE 1
isim force add flagWE 1

run 10ns
```

```
#br0
isim force add selPC 01
```

```
isim force add selEAB1 0
isim force add selEAB2 10
isim force add ldPC 1

run 10ns
```

```
#br1
isim force add selPC 01
isim force add selEAB1 0
isim force add selEAB2 10
isim force add ldPC 1

run 10ns
```

```
#jmp
isim force add SR1 111
isim force add selPC 01
isim force add selEAB1 1
isim force add selEAB2 00
isim force add ldPC 1

run 10ns
```

```
#jsr0
isim force add DR 111
isim force add regWE 1
isim force add enaPC 1

run 10ns
#jsr
source inactive.tcl
isim force add selEAB1 0
isim force add selPC 01
isim force add selEAB2 11
isim force add ldPC 1

run 10ns
```

```
#ld0
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1
```

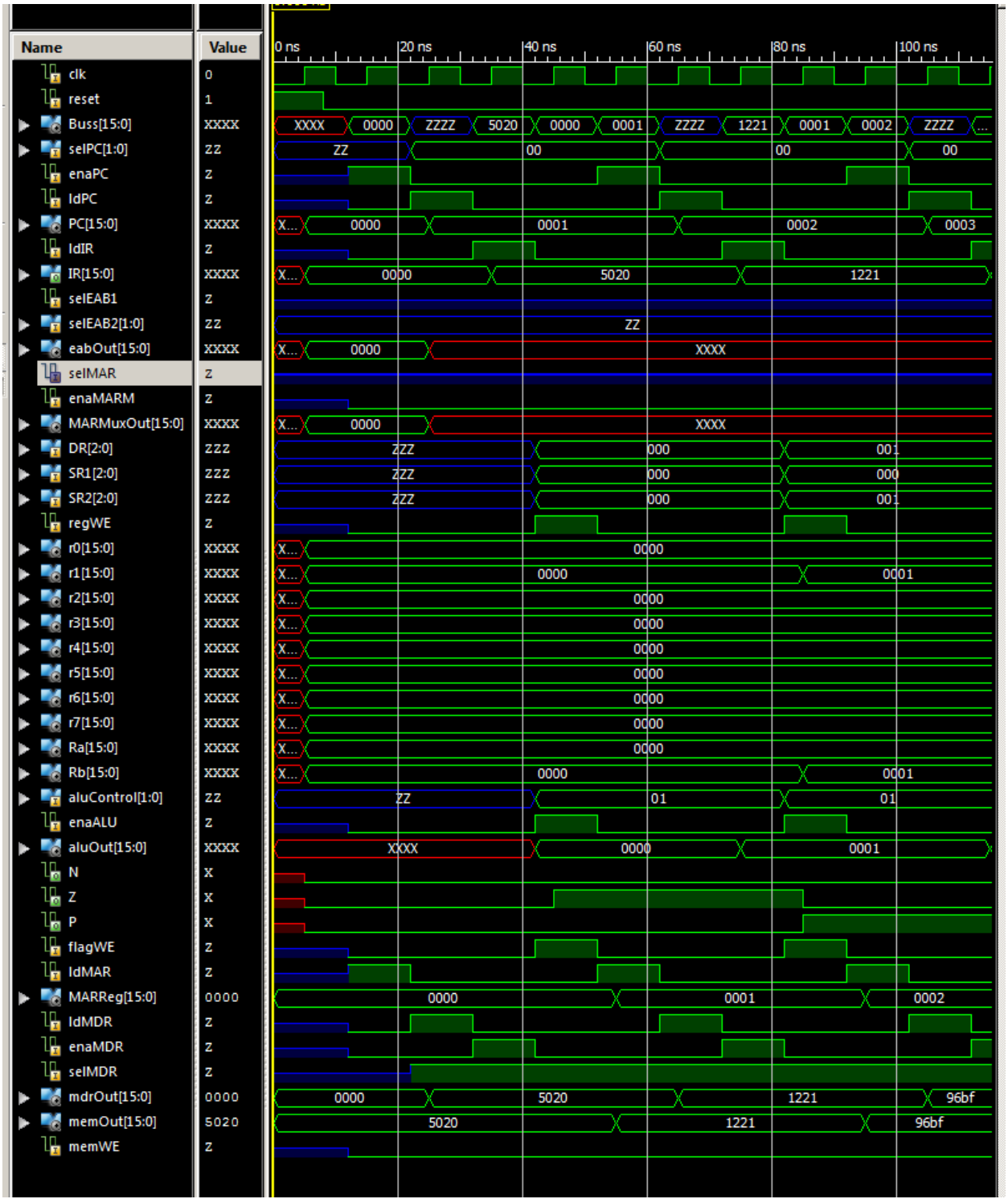
```
isim force add selMAR 0

run 10ns

#ld1
source inactive.tcl
isim force add ldMDR 1
isim force add selMDR 1

run 10ns

#ld2
source inactive.tcl
isim force add DR 010
isim force add regWE 1
isim force add flagWE 1
isim force add enaMDR 1

run 10ns
```

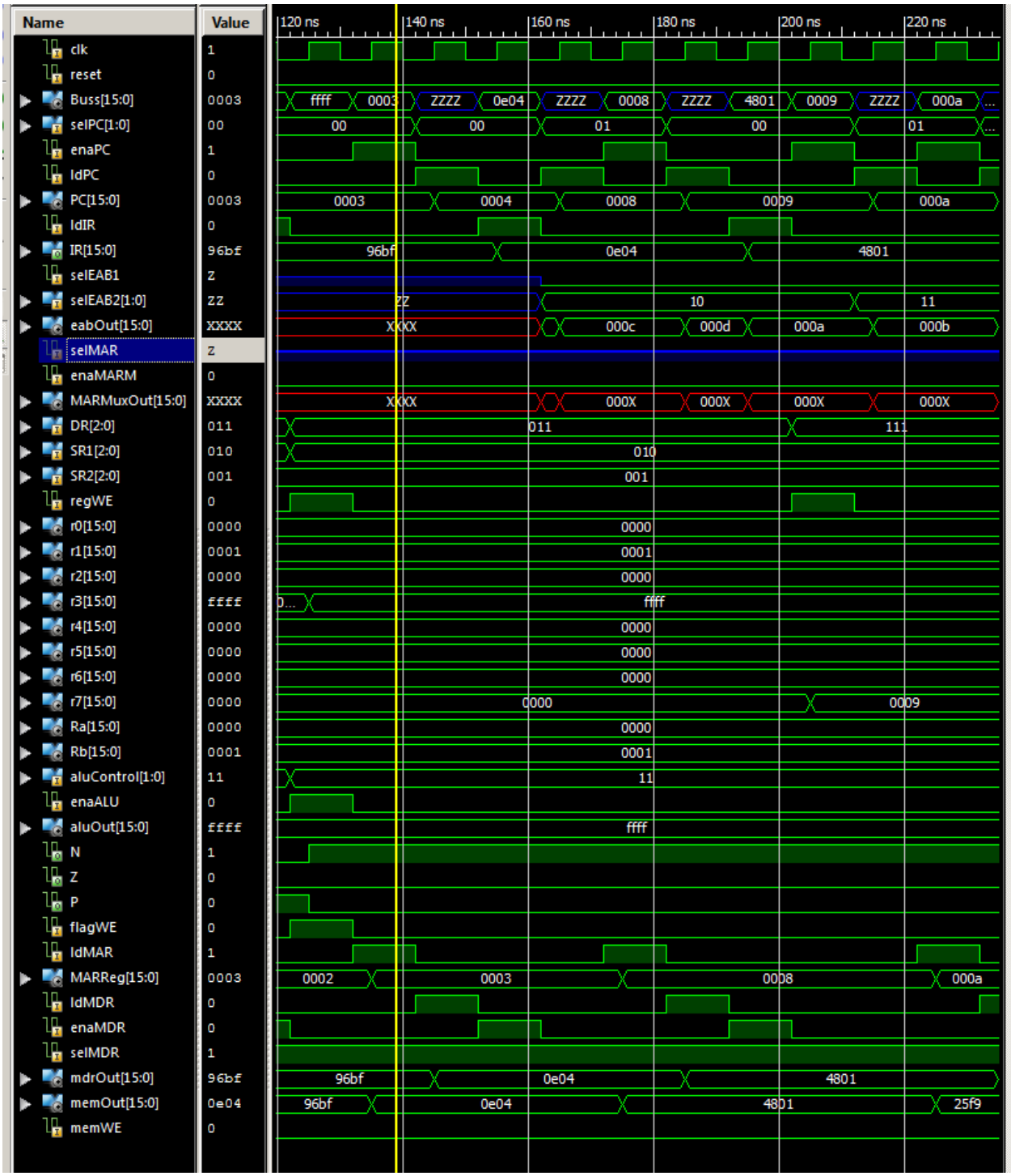
```
#ld0
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1
isim force add selMAR 0

run 10ns

#ld1
source inactive.tcl
isim force add ldMDR 1
isim force add selMDR 1

run 10ns

#ld2
source inactive.tcl
isim force add DR 001
isim force add regWE 1
isim force add flagWE 1
isim force add enaMDR 1

run 10ns
```

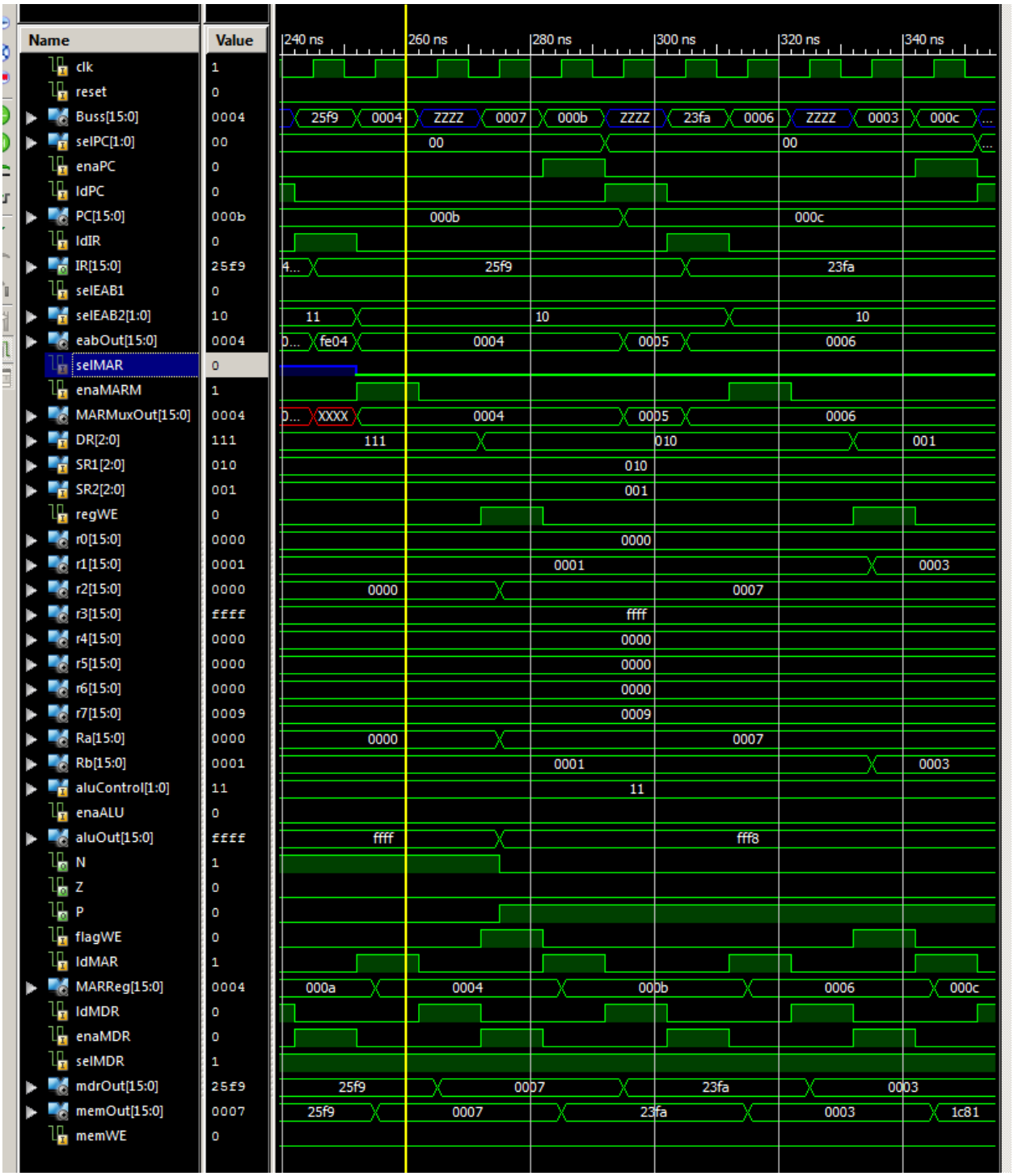
```
#not
isim force add aluControl 11
isim force add DR 011
isim force add SR1 010
isim force add enaALU 1
isim force add regWE 1
isim force add flagWE 1

run 10ns
```

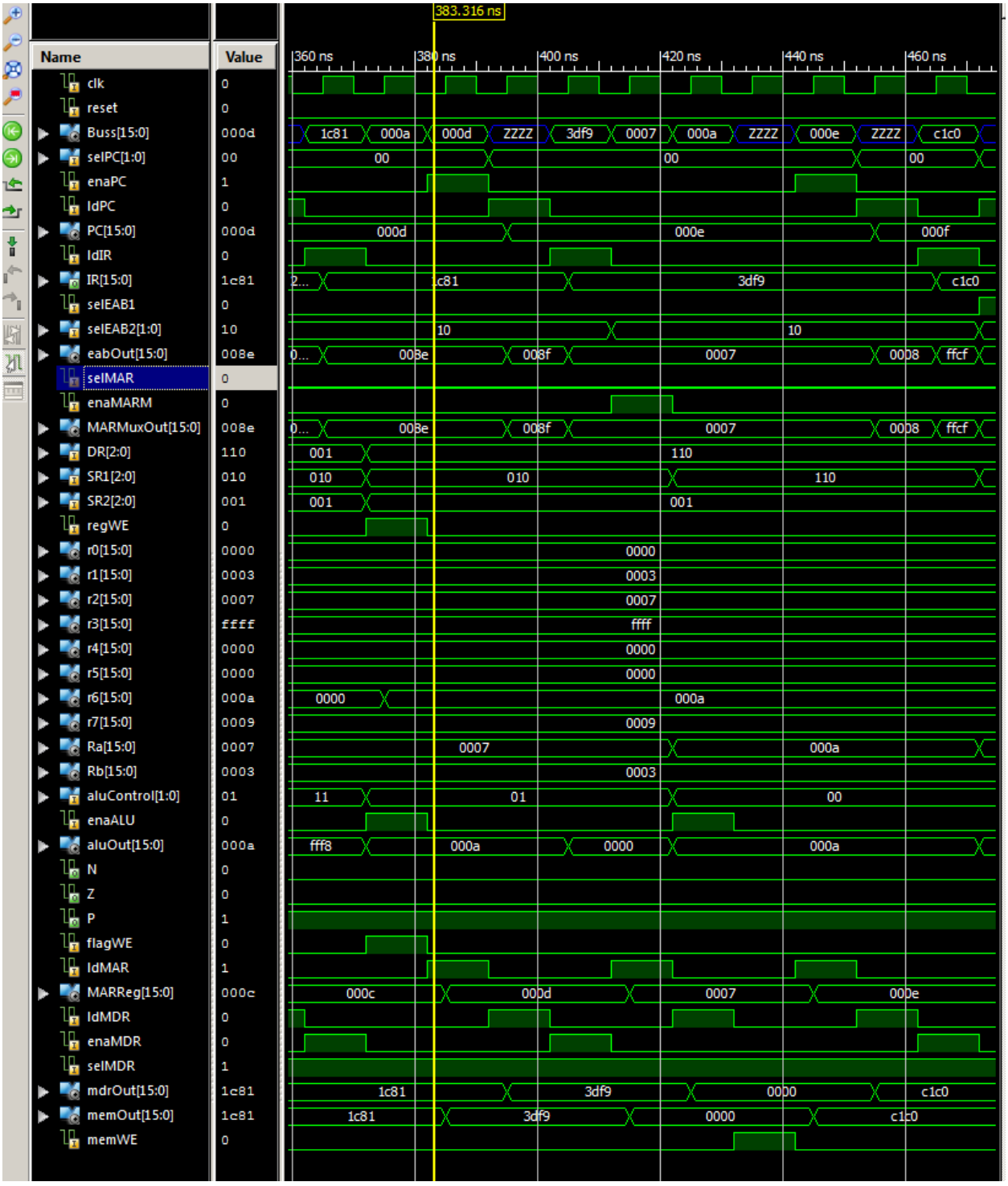
```
#st0
isim force add selEAB1 0
isim force add selEAB2 10
isim force add enaMARM 1
isim force add ldMAR 1

run 10ns

#st1
source inactive.tcl
isim force add aluControl 00
isim force add SR1 110
isim force add enaALU 1
isim force add ldMDR 1

run 10ns

#st2
source inactive.tcl
isim force add memWE 1

run 10ns
```

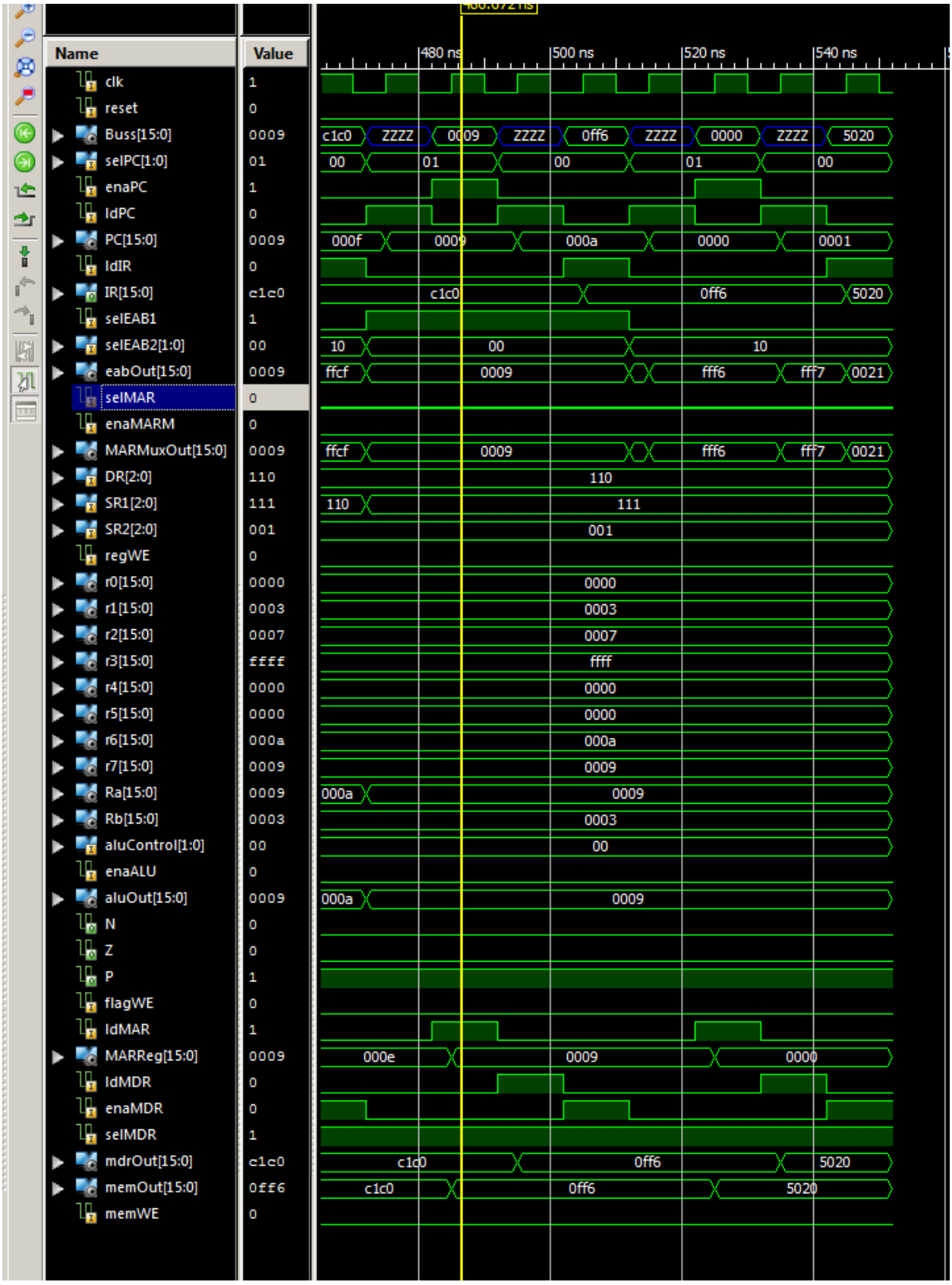
Full Simulation waveform (10pt)


Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
clk 0
reset 1
Buss[15:0] xxxx
selPC[1:0] zz
enaPC z
ldPC z
PC[15:0] xxxx
ldIR z
IR[15:0] xxxx
selEAB1 z
selEAB2[1:0] zz
eabOut[15:0] xxxx
selMAR z
enaMARM z
MARMuxOut[15:0] xxxx
DR[2:0] zzz
SR1[2:0] zzz
SR2[2:0] zzz
regWE z
r0[15:0] xxxx
r1[15:0] xxxx
r2[15:0] xxxx
r3[15:0] xxxx
r4[15:0] xxxx
r5[15:0] xxxx
r6[15:0] xxxx
r7[15:0] xxxx
Ra[15:0] xxxx
Rb[15:0] xxxx
aluControl[1:0] zz
enaALU z
aluOut[15:0] xxxx
N x
Z x
P x
flagWE z
ldMAR z
MARReg[15:0] 0000
ldMDR z
enaMDR z
selMDR z
mdrOut[15:0] 0000
memOut[15:0] 5020
memWE z


Name
Value
clk 1
reset 0
Buss[15:0] 0003
selPC[1:0] 00
enaPC 1
ldPC 0
PC[15:0] 0003
ldIR 0
IR[15:0] 96bf
selEAB1 Z
selEAB2[1:0] ZZ
eabOut[15:0] XXXX
selMAR Z
enaMARM 0
MARMuxOut[15:0] XXXX
DR[2:0] 011
SR1[2:0] 010
SR2[2:0] 001
regWE 0
r0[15:0] 0000
r1[15:0] 0001
r2[15:0] 0000
r3[15:0] ffff
r4[15:0] 0000
r5[15:0] 0000
r6[15:0] 0000
r7[15:0] 0000
Ra[15:0] 0000
Rb[15:0] 0001
aluControl[1:0] 11
enaALU 0
aluOut[15:0] ffff
N 1
Z 0
P 0
flagWE 0
ldMAR 1
MARReg[15:0] 0003
ldMDR 0
enaMDR 0
selMDR 1
mdrOut[15:0] 96bf
memOut[15:0] 0e04
memWE 0
120 ns
140 ns
160 ns
180 ns
200 ns
220 ns


Name
Value
240 ns
260 ns
280 ns
300 ns
320 ns
340 ns
clk 1
reset 0
Buss[15:0] 0004
selPC[1:0] 00
enaPC 0
ldPC 0
PC[15:0] 000b
ldIR 0
IR[15:0] 25f9
selEAB1 0
selEAB2[1:0] 10
eabOut[15:0] 0004
selMAR 0
enaMARM 1
MARMuxOut[15:0] 0004
DR[2:0] 111
SR1[2:0] 010
SR2[2:0] 001
regWE 0
r0[15:0] 0000
r1[15:0] 0001
r2[15:0] 0000
r3[15:0] ffff
r4[15:0] 0000
r5[15:0] 0000
r6[15:0] 0000
r7[15:0] 0009
Ra[15:0] 0000
Rb[15:0] 0001
aluControl[1:0] 11
enaALU 0
aluOut[15:0] ffff
N 1
Z 0
P 0
flagWE 0
ldMAR 1
MARReg[15:0] 0004
ldMDR 0
enaMDR 0
selMDR 1
mdrOut[15:0] 25f9
memOut[15:0] 0007
memWE 0
25f9 0004 ZZZZ 0007 000b ZZZZ 23fa 0006 ZZZZ 0003 000c
00 00
000b 000c
25f9 23fa
11 10 10
fe04 0004 0005 0006
XXXX 0004 0005 0006
111 010 001
010
001
0000
0001 0003
0000 0007
ffff
0000
0000
0000
0009
0000 0007
0001 0003
11
ffff fff8
000a 0004 000b 0006 000c
25f9 0007 23fa 0003
25f9 0007 23fa 0003 1c81


383.316 ns
360 ns
380 ns
400 ns
420 ns
440 ns
460 ns
Name
Value
clk 0
reset 0
Buss[15:0] 000d
selPC[1:0] 00
enaPC 1
ldPC 0
PC[15:0] 000d
ldIR 0
IR[15:0] 1c81
selEAB1 0
selEAB2[1:0] 10
eabOut[15:0] 008e
selMAR 0
enaMARM 0
MARMuxOut[15:0] 008e
DR[2:0] 110
SR1[2:0] 010
SR2[2:0] 001
regWE 0
r0[15:0] 0000
r1[15:0] 0003
r2[15:0] 0007
r3[15:0] ffff
r4[15:0] 0000
r5[15:0] 0000
r6[15:0] 000a
r7[15:0] 0009
Ra[15:0] 0007
Rb[15:0] 0003
aluControl[1:0] 01
enaALU 0
aluOut[15:0] 000a
N 0
Z 0
P 1
flagWE 0
ldMAR 1
MARReg[15:0] 000c
ldMDR 0
enaMDR 0
selMDR 1
mdrOut[15:0] 1c81
memOut[15:0] 1c81
memWE 0


Name
Value
480 ns
500 ns
520 ns
540 ns
clk 1
reset 0
Buss[15:0] 0009 c1c0 ZZZZ 0009 ZZZZ 0ff6 ZZZZ 0000 ZZZZ 5020
selPC[1:0] 01 00 01 00 01 00
enaPC 1
ldPC 0
PC[15:0] 0009 000f 0009 000a 0000 0001
ldIR 0
IR[15:0] c1c0 c1c0 0ff6 5020
selEAB1 1
selEAB2[1:0] 00 10 00 10
eabOut[15:0] 0009 ffcf 0009 fff6 fff7 0021
selMAR 0
enaMARM 0
MARMuxOut[15:0] 0009 ffcf 0009 fff6 fff7 0021
DR[2:0] 110 110
SR1[2:0] 111 110 111
SR2[2:0] 001 001
regWE 0
r0[15:0] 0000 0000
r1[15:0] 0003 0003
r2[15:0] 0007 0007
r3[15:0] ffff ffff
r4[15:0] 0000 0000
r5[15:0] 0000 0000
r6[15:0] 000a 000a
r7[15:0] 0009 0009
Ra[15:0] 0009 000a 0009
Rb[15:0] 0003 0003
aluControl[1:0] 00 00
enaALU 0
aluOut[15:0] 0009 000a 0009
N 0
Z 0
P 1
flagWE 0
ldMAR 1
MARReg[15:0] 0009 000e 0009 0000
ldMDR 0
enaMDR 0
selMDR 1
mdrOut[15:0] c1c0 c1c0 0ff6 5020
memOut[15:0] 0ff6 c1c0 0ff6 5020
memWE 0

Anomalies

This lab took so long. It took a while to figure out how to use ts_driver in my datapath module. Also when I was making tcl files for the instructions, not resetting the enable signals gave us problems. Thank you TAs !!