ECEN 220

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Lab 11 – LC3 Datapath

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**Datapath Verilog file (10pt)**

|  |
| --- |
| module Datapath(  input reset,  input clk,  output [15:0] IR,  output N,  output Z,  output P,  input [1:0] aluControl,  input [2:0] SR1,  input [2:0] SR2,  input [2:0] DR,  input [1:0] selPC,  input [1:0] selEAB2,  input enaALU,  input regWE,  input enaMARM,  input selMAR,  input selEAB1,  input enaPC,  input ldPC,  input ldIR,  input ldMAR,  input ldMDR,  input selMDR,  input memWE,  input enaMDR,  input flagWE  );  wire[15:0] Ra, Rb, aluOut, eabOut, PC, Buss, MARMuxOut, mdrOut;    ts\_driver ts\_dr0( MARMuxOut, Buss, enaMARM );  ts\_driver ts\_dr1( PC, Buss, enaPC );  ts\_driver ts\_dr2( mdrOut, Buss, enaMDR );  ts\_driver ts\_dr3( aluOut, Buss, enaALU );    ALU alu0(Ra, Rb, IR[5:0], aluControl, aluOut);  EAB eab(eabOut, IR[10:0], Ra, PC, selEAB1, selEAB2);  IR ir(IR, clk, ldIR, reset, Buss);  MARMux marmux(MARMuxOut, IR[7:0], eabOut, selMAR);  Memory mem0(mdrOut, Buss, clk, reset, ldMAR, ldMDR, selMDR, memWE);  NZP znp(N, Z, P, clk, flagWE, reset, Buss);  PC pc(Buss, clk, reset, ldPC, eabOut, selPC, PC);  RegFile reg0(Ra, Rb, Buss, clk, regWE, reset, DR, SR1, SR2);  endmodule |

**Master TCL file (2pt)**

|  |
| --- |
| source wave.tcl  isim force add clk 0 -time 0 -value 1 -time 5ns -repeat 10ns  isim force add reset 1 -time 0 -value 0 -time 8ns  run 12ns  source fetch.tcl  source and.tcl  source fetch.tcl  source add.tcl  source fetch.tcl  source not.tcl  source fetch.tcl  source br.tcl  source fetch.tcl  source jsr.tcl  source fetch.tcl  source ld.tcl  source fetch.tcl  source ld1.tcl  source fetch.tcl  source add1.tcl  source fetch.tcl  source st.tcl  source fetch.tcl  source jmp.tcl  source fetch.tcl  source br1.tcl  source fetch.tcl |

**Wave TCL file (2pt)**

|  |
| --- |
| wave add clk  wave add reset  wave add Buss -radix hex  #add signals to view the PC and PC control  wave add selPC  wave add enaPC  wave add ldPC  wave add PC -radix hex    #add signals to view the IR and IR control  wave add ldIR  wave add IR -radix hex    #add signals to view the EAB control  wave add selEAB1  wave add selEAB2  wave add eabOut -radix hex    #add signals to view the MARMux control  wave add selMAR  wave add enaMARM  wave add MARMuxOut -radix hex  #add signals to view Register File control  wave add DR  wave add SR1  wave add SR2  wave add regWE  #add signals to view the Registers in the Register File  wave add /reg0/r0 -radix hex  wave add /reg0/r1 -radix hex  wave add /reg0/r2 -radix hex  wave add /reg0/r3 -radix hex  wave add /reg0/r4 -radix hex  wave add /reg0/r5 -radix hex  wave add /reg0/r6 -radix hex  wave add /reg0/r7 -radix hex  wave add Ra -radix hex  wave add Rb -radix hex  #add signals to view the ALU control  wave add aluControl  wave add enaALU  wave add aluOut -radix hex  #view the condition flags  wave add N  wave add Z  wave add P  wave add flagWE    #add signals to view the Memory Registers and the Memory control  wave add ldMAR  wave add /mem0/MARReg -radix hex  wave add ldMDR  wave add enaMDR  wave add selMDR  wave add mdrOut -radix hex  wave add /mem0/memOut -radix hex  wave add memWE |

**Inactive TCL file (2pt)**

|  |
| --- |
| isim force add enaALU 0  isim force add enaMARM 0  isim force add enaPC 0  isim force add enaMDR 0  isim force add ldIR 0  isim force add ldPC 0  isim force add ldMAR 0  isim force add ldMDR 0  isim force add regWE 0  isim force add memWE 0  isim force add flagWE 0 |

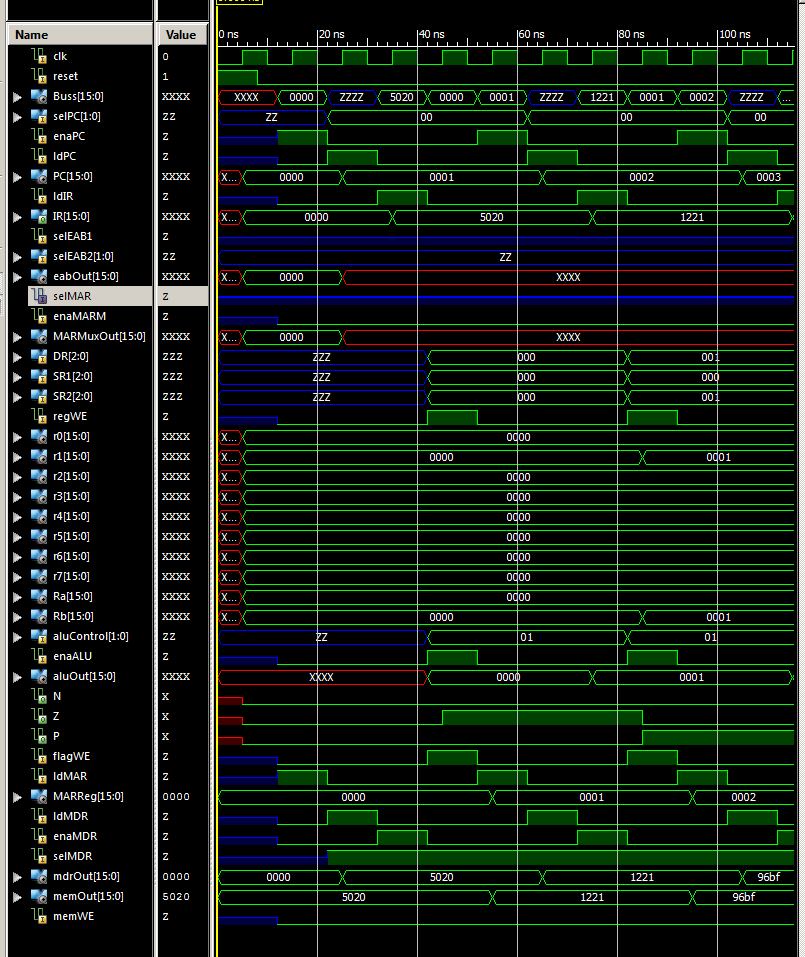
**Fetch TCL file (2pt)**

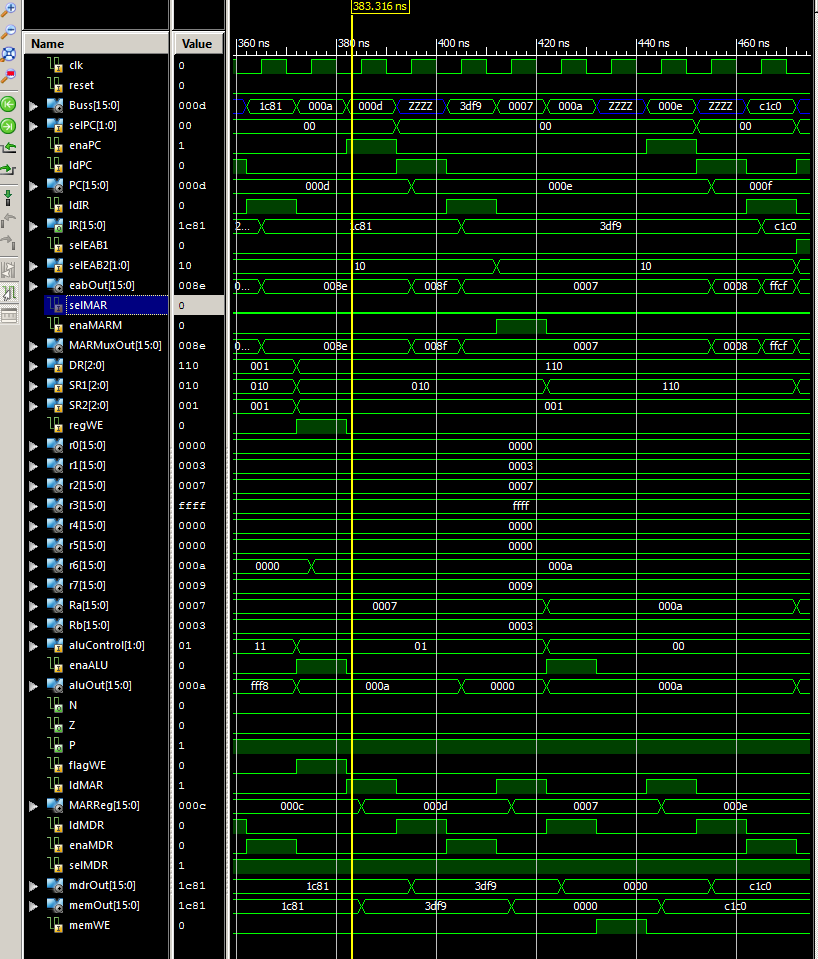
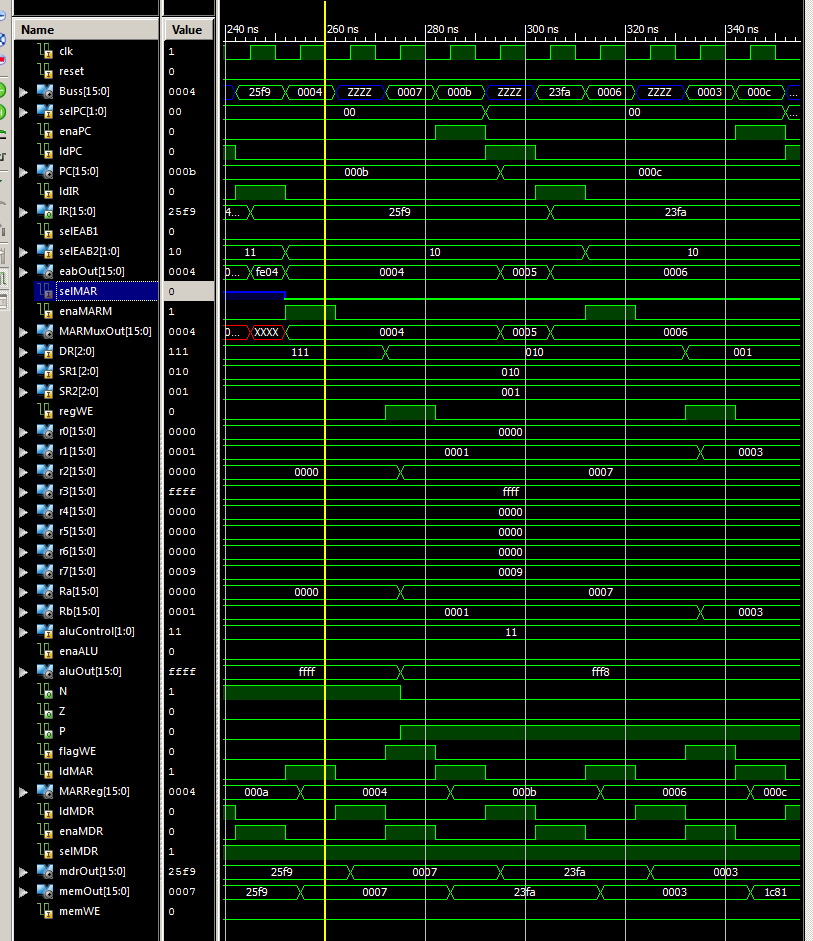
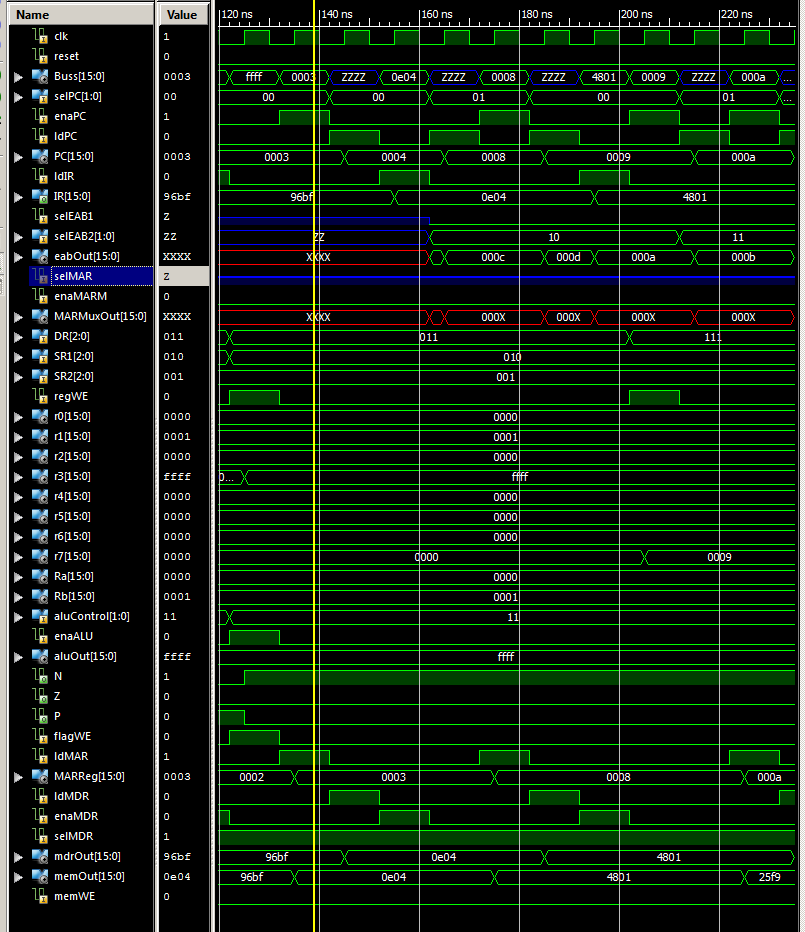
|  |
| --- |
| source inactive.tcl  #fetch0  isim force add enaPC 1  isim force add ldMAR 1  run 10ns  source inactive.tcl  #fetch1  isim force add ldPC 1  isim force add selPC 00  isim force add ldMDR 1  isim force add selMDR 1  run 10ns  source inactive.tcl  #fetch2  isim force add ldIR 1  isim force add enaMDR 1  run 10ns  source inactive.tcl |

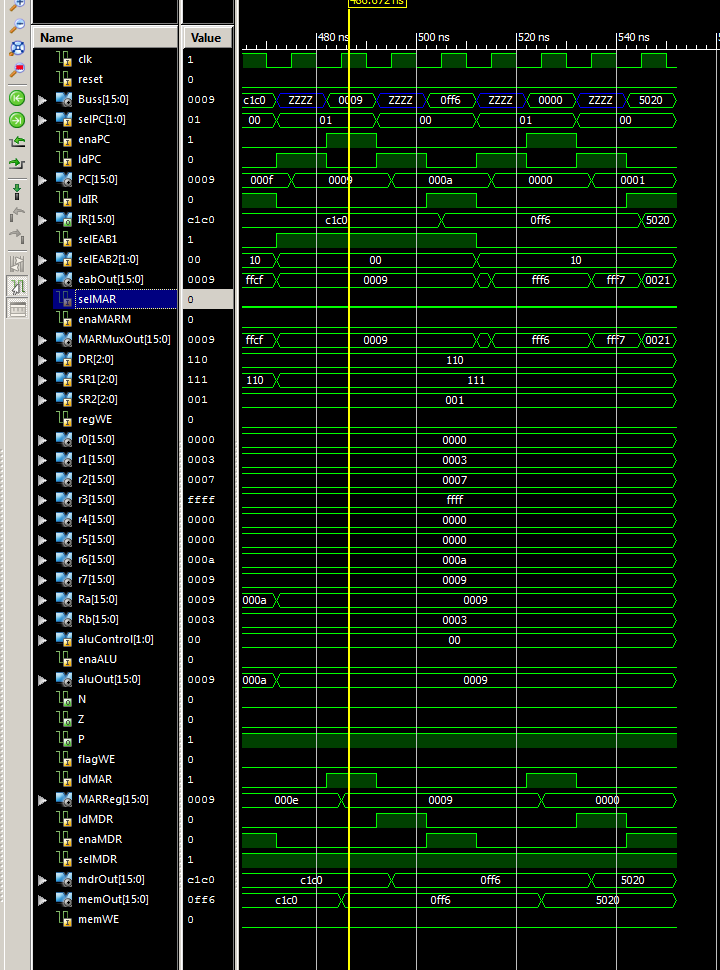
**All instruction TCL files (12pt)**

|  |
| --- |
| #add0  isim force add aluControl 01  isim force add SR1 000  isim force add DR 001  isim force add enaALU 1  isim force add regWE 1  isim force add flagWE 1  run 10ns  #add1  isim force add aluControl 01  isim force add SR1 010  isim force add SR2 001  isim force add DR 110  isim force add enaALU 1  isim force add regWE 1  isim force add flagWE 1  run 10ns  #and0  isim force add aluControl 01  isim force add SR1 000  isim force add DR 000  isim force add enaALU 1  isim force add regWE 1  isim force add flagWE 1  run 10ns  #br0  isim force add selPC 01  isim force add selEAB1 0  isim force add selEAB2 10  isim force add ldPC 1  run 10ns  #br1  isim force add selPC 01  isim force add selEAB1 0  isim force add selEAB2 10  isim force add ldPC 1  run 10ns  #jmp  isim force add SR1 111  isim force add selPC 01  isim force add selEAB1 1  isim force add selEAB2 00  isim force add ldPC 1  run 10ns  #jsr0  isim force add DR 111  isim force add regWE 1  isim force add enaPC 1  run 10ns  #jsr  source inactive.tcl  isim force add selEAB1 0  isim force add selPC 01  isim force add selEAB2 11  isim force add ldPC 1  run 10ns  #ld0  isim force add selEAB1 0  isim force add selEAB2 10  isim force add enaMARM 1  isim force add ldMAR 1  isim force add selMAR 0  run 10ns  #ld1  source inactive.tcl  isim force add ldMDR 1  isim force add selMDR 1  run 10ns  #ld2  source inactive.tcl  isim force add DR 010  isim force add regWE 1  isim force add flagWE 1  isim force add enaMDR 1  run 10ns  #ld0  isim force add selEAB1 0  isim force add selEAB2 10  isim force add enaMARM 1  isim force add ldMAR 1  isim force add selMAR 0  run 10ns  #ld1  source inactive.tcl  isim force add ldMDR 1  isim force add selMDR 1  run 10ns  #ld2  source inactive.tcl  isim force add DR 001  isim force add regWE 1  isim force add flagWE 1  isim force add enaMDR 1  run 10ns  #not  isim force add aluControl 11  isim force add DR 011  isim force add SR1 010  isim force add enaALU 1  isim force add regWE 1  isim force add flagWE 1  run 10ns  #st0  isim force add selEAB1 0  isim force add selEAB2 10  isim force add enaMARM 1  isim force add ldMAR 1  run 10ns  #st1  source inactive.tcl  isim force add aluControl 00  isim force add SR1 110  isim force add enaALU 1  isim force add ldMDR 1  run 10ns  #st2  source inactive.tcl  isim force add memWE 1  run 10ns |

**Full Simulation waveform (10pt)**







**Anomalies**

This lab took so long. It took a while to figure out how to use ts\_driver in my datapath module. Also when I was making tcl files for the instructions, not resetting the enable signals gave us problems. Thank you TAs !!