**Jae Lee**

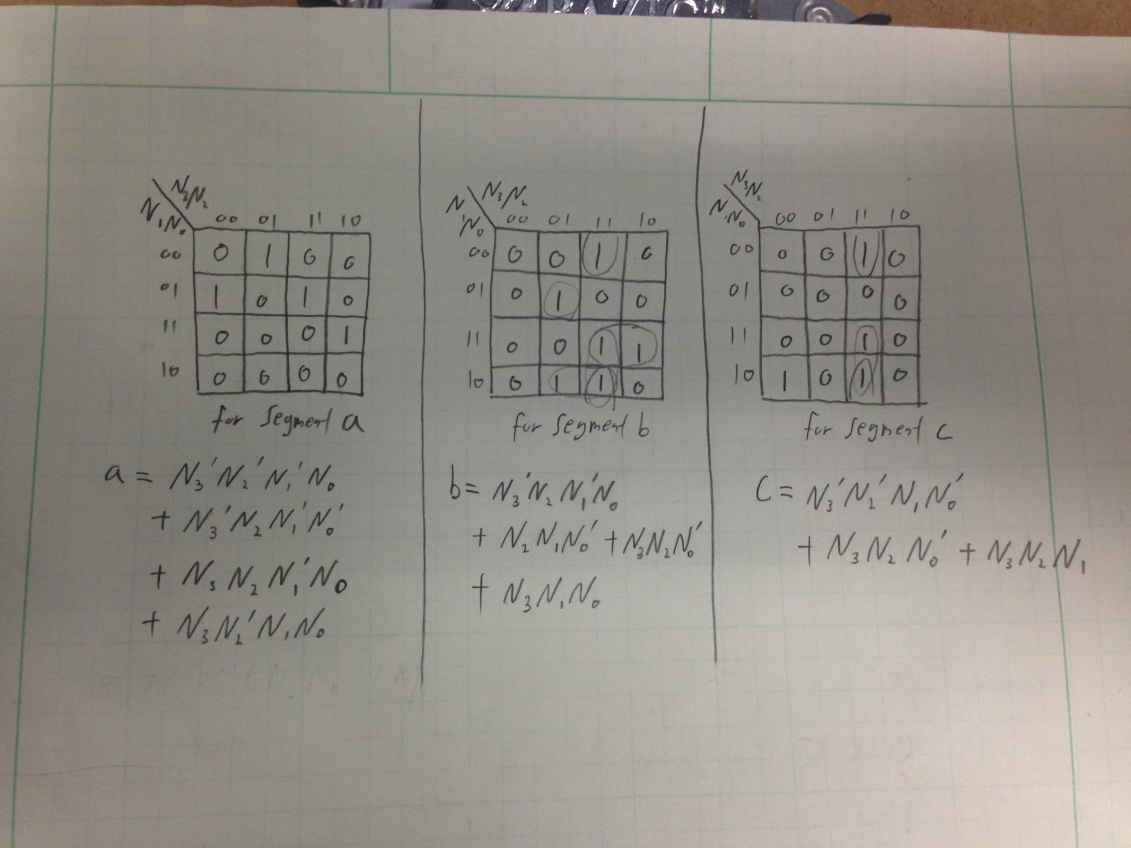
**ECEN 220**

**Lab #4**

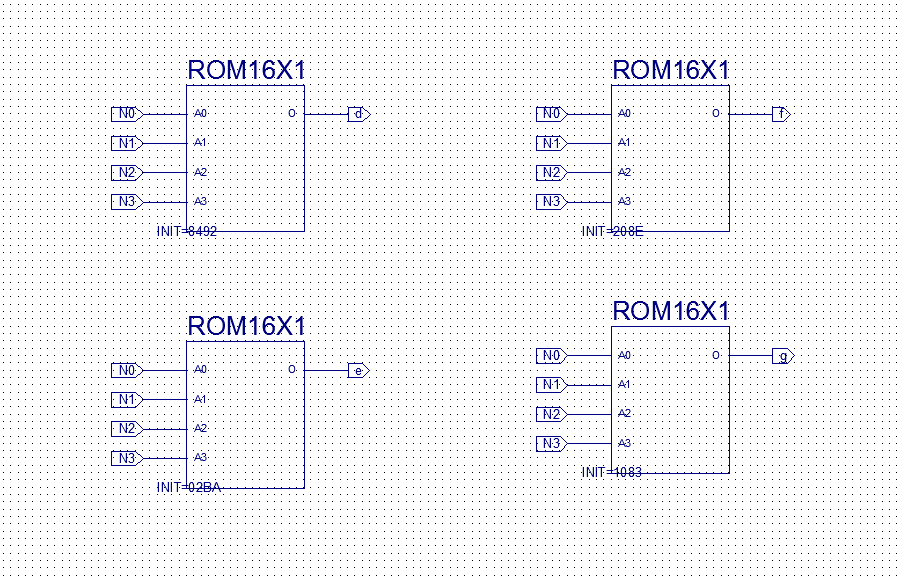
**10/01/2013**

**Truth table for seven segment decorder**

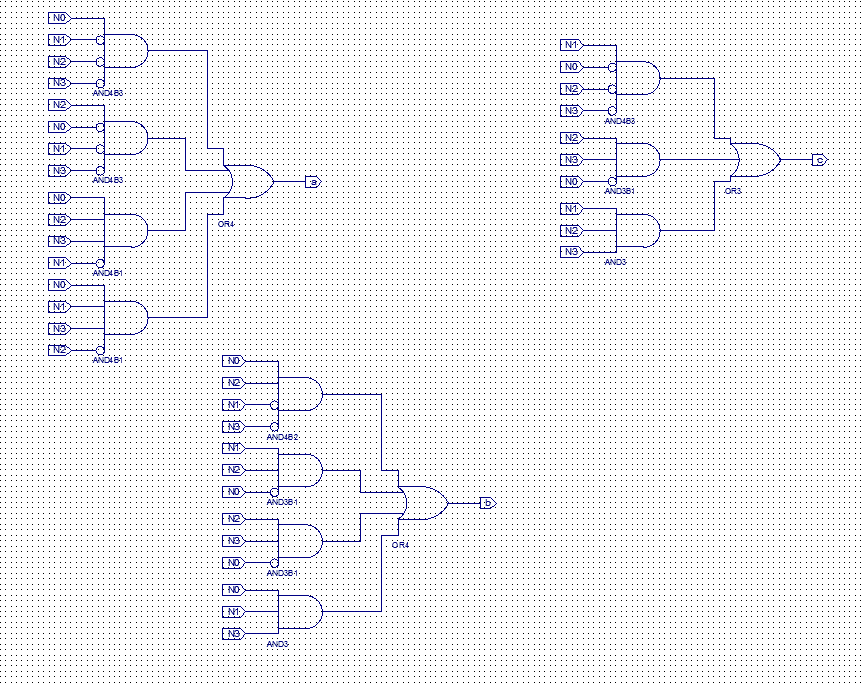
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input(High-asserted) | | | | Output(Low-asserted) | | | | | | | LED |
| N3 | N2 | N1 | N0 | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 6 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 9 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | A |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | b |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | C |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | d |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | E |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | F |

**3 segment equations simplified using K-maps**

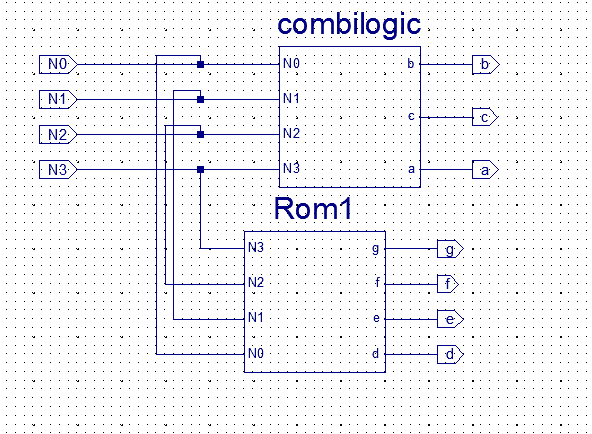
**ROM schematic**



**Combinational Logic Schematic**



**Seven Segment Decorder Schematic**



**TCL files**

wave add / -radix hex

isim force add N0 0 -time 0 -value 1 -time 10ns -repeat 20ns

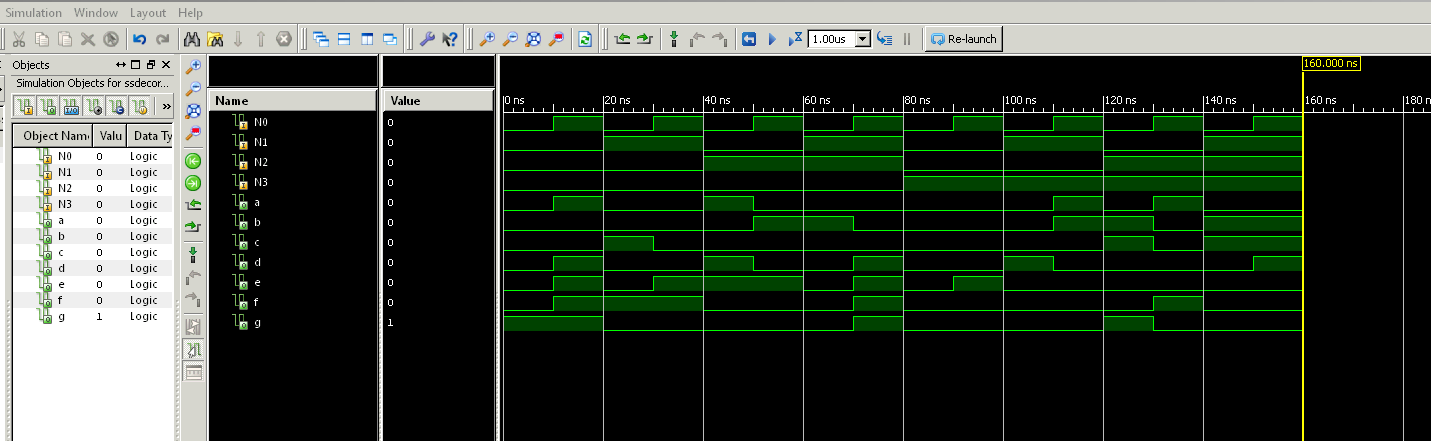
isim force add N1 0 -time 0 -value 1 -time 20ns -repeat 40ns

isim force add N2 0 -time 0 -value 1 -time 40ns -repeat 80ns

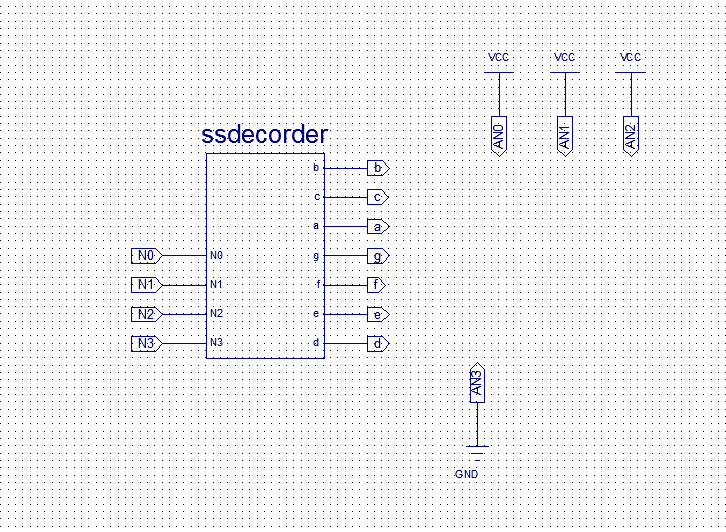
isim force add N3 0 -time 0 -value 1 -time 80ns -repeat 160ns

run 160ns

**Simulation waveforms**



**Test bench schematic**



**Test bench UCF file**

## Switches

#NET "sw<0>" LOC = "G18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW0

#NET "sw<1>" LOC = "H18"; # Bank = 1, Pin name = IP/VREF\_1, Type = VREF, Sch name = SW1

#NET "sw<2>" LOC = "K18"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW2

#NET "sw<3>" LOC = "K17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW3

NET N0 LOC = "L14"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW4

NET N1 LOC = "L13"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW5

NET N2 LOC = "N17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW6

NET N3 LOC = "R17"; # Bank = 1, Pin name = IP, Type = INPUT, Sch name = SW7

## 7 segment display

NET a LOC = "L18"; # Bank = 1, Pin name = IO\_L10P\_1, Type = I/O, Sch name = CA

NET b LOC = "F18"; # Bank = 1, Pin name = IO\_L19P\_1, Type = I/O, Sch name = CB

NET c LOC = "D17"; # Bank = 1, Pin name = IO\_L23P\_1/HDC, Type = DUAL, Sch name = CC

NET d LOC = "D16"; # Bank = 1, Pin name = IO\_L23N\_1/LDC0, Type = DUAL, Sch name = CD

NET e LOC = "G14"; # Bank = 1, Pin name = IO\_L20P\_1, Type = I/O, Sch name = CE

NET f LOC = "J17"; # Bank = 1, Pin name = IO\_L13P\_1/A6/RHCLK4/IRDY1, Type = RHCLK/DUAL, Sch name = CF

NET g LOC = "H14"; # Bank = 1, Pin name = IO\_L17P\_1, Type = I/O, Sch name = CG

#NET "dp" LOC = "C17"; # Bank = 1, Pin name = IO\_L24N\_1/LDC2, Type = DUAL, Sch name = DP

NET AN0 LOC = "F17"; # Bank = 1, Pin name = IO\_L19N\_1, Type = I/O, Sch name = AN0

NET AN1 LOC = "H17"; # Bank = 1, Pin name = IO\_L16N\_1/A0, Type = DUAL, Sch name = AN1

NET AN2 LOC = "C18"; # Bank = 1, Pin name = IO\_L24P\_1/LDC1, Type = DUAL, Sch name = AN2

NET AN3 LOC = "F15"; # Bank = 1, Pin name = IO\_L21P\_1, Type = I/O, Sch name = AN3

**Anomalies**

This lab was harder than all the labs so far. I encountered many errors when I was trying to overwrite symbols. Somehow Xilinx didn’t overwrite. So I had to create a new source file and do the same thing. For TCL file, I accidently included the capital W for waveform command which caused an error.