Jae Lee

ECEN 220

Lab #6 – Oscilloscope / Logic Analyzer

10/15/2013

**Toggle Circuit Verilog Code**

|  |
| --- |
| module Toggle(Qout, Clkout, Gclk, Clr);  input Gclk, Clr;  output Clkout, Qout;    wire temp1;    FF ff1(Qout, Gclk, Clr, temp1);    not(temp1, Qout);  buf(Clkout, Gclk);    endmodule |

**Toggle Circuit Screen Capture**

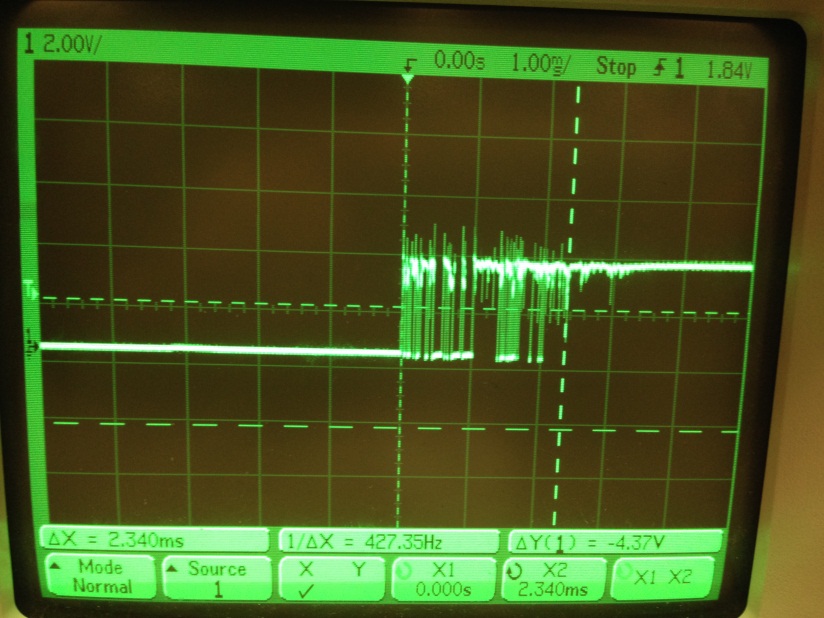
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Time between two rises = 3ns

**Toggle Circuit Question and answer**

Analog signal doesn’t have infinitely sharp slope. So If we zoom in enough, we should be able to see a steady rise of the signal.

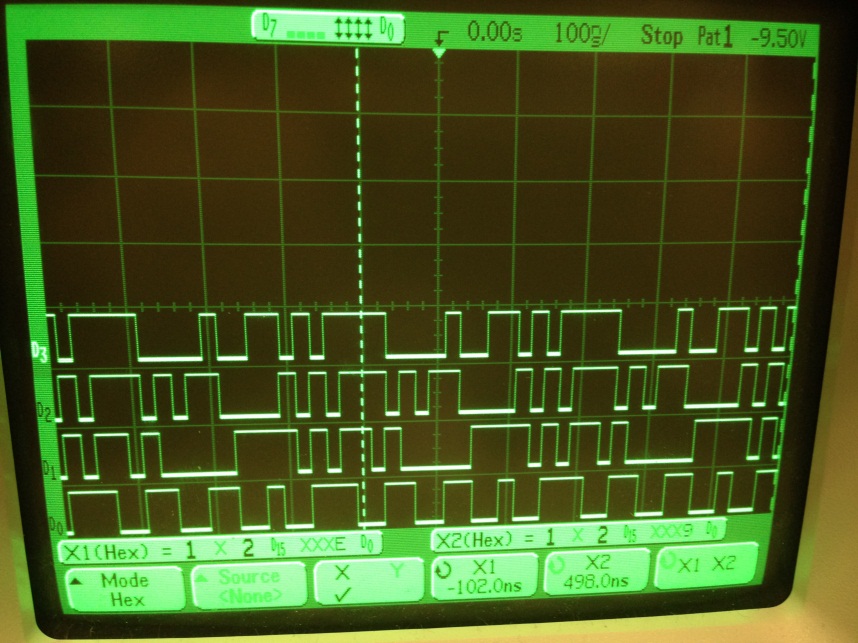
**Bounce Circuit Screen capture**

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**Bounce Circuit Setting time**

2.340ms

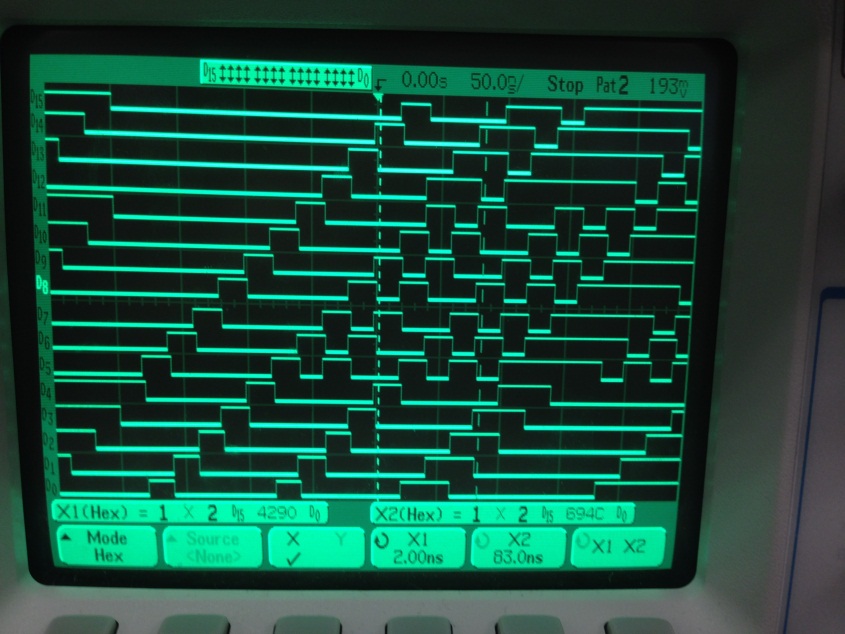
**4-bit Shifter Screen capture**

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**4-bit shifter pattern of values**

7, 9, F, E, C, 3, 5, 0, 4, D, 1, 2, A, B, 6, 8 repeated.

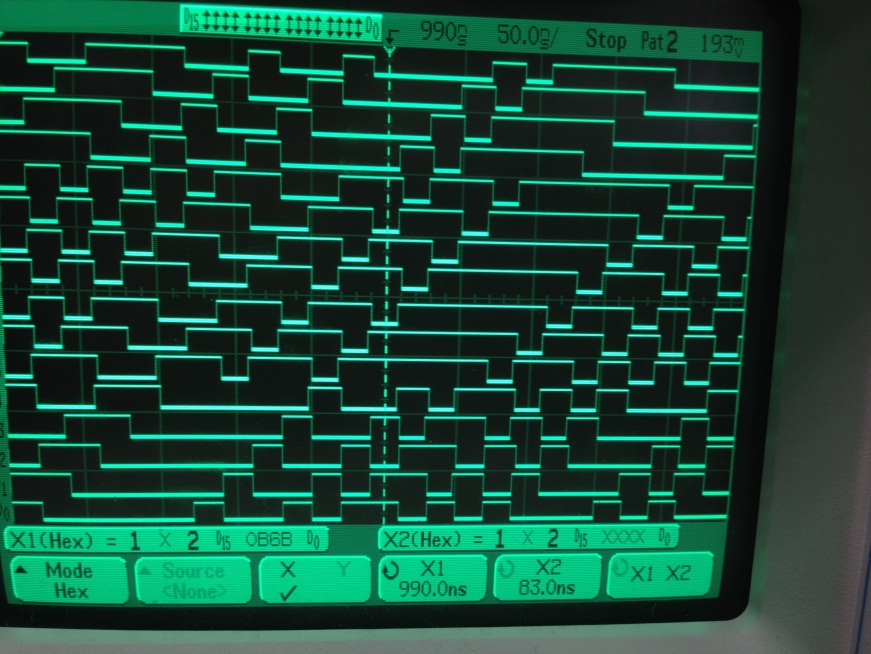
**16-bit Shifter Screen Capture(4290 Hex)**



**16-bit Shifter Pattern of Values(4290 Hex)**

4290, 8521, 1A43, 34A6, 694C, D2B8, B570, 7AE0, F5E0, FBC1 and so on

**16-bit Shifter Screen Capture(990ns after triggered pattern)**

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**16-bit Shifter Value(990ns after triggered patter)**

OB6B, 16F6, 2DED, 5BFA, B7D5, 7FAA and so on

**16-bit Shifter Screen Capture(16.38us after triggered pattern)**

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**16-bit Shifter Value(16.38us after triggered pattern)**

4290, 8521, 1A43, 34A6, 694C and so on

**16-bit Shifter total number of values in repeating pattern**

16.38us / .02us = 819

**Anomalies**

Oscilloscope sometimes combined signals together. I had to distribute manually. Also, I couldn’t get 0x4290 starting point at first because scope 1 and 2 were set to not X.